Enhanced Linearity in FD-SOI CMOS Body-Input Analog Circuits – Application to Voltage-Controlled Ring Oscillators and Frequency-based $\Sigma\Delta$ ADCs

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***Abstract*—This paper investigates the use of the body terminal of MOS transistors to improve the linearity of some key circuits used to implement analog and mixed-signal circuits integrated in Fully Depleted Silicon on Insulator (FD-SOI) CMOS. This technology allows to increase the body factor with respect to conventional (bulk) CMOS processes. This effect is analyzed in basic analog building blocks – such as switches, simple-stage transconductors and Voltage-Controlled Ring Oscillators (VCROs). Approximated expressions are derived for the non-linear characteristics and harmonic distortion of some of these circuits. As an application, transistor-level simulations of two VCRO-based $\Sigma\Delta$ modulators designed in a 28-nm FD-SOI CMOS technology are shown in order to demonstrate the benefits of the presented techniques.**

***Index Terms*—Body effect, fully-depleted silicon-on-insulator, bulk-input analog circuits, voltage-controlled ring oscillators, sigma-delta modulators, analog-to-digital converters.**

I. Introduction

ONE of the direct consequences of technology downscaling towards the nanoscale has been the *redefinition* of the Metal-Oxide-Semiconductor (MOS) transistor, in terms of the materials used for its fabrication as well as the structure of the device itself. Among other alternatives, two types of Fully Depleted (FD) devices are being used by semiconductor industry in 28-nm technology processes and beyond, namely: Fin-FET and FD Silicon-On-Insulator (FD-SOI). The latter has been postulated as one of the key technologies in those applications requiring ultra-low-power consumption – such as biomedical devices, wireless sensor networks, and Internet-of-Things (IoT) – thanks to its better performance in terms of transconductance efficiency, reduced impact of passive parasitic circuit elements, as well as improved noise isolation [1].

One of the best features of FD-SOI technology for analog design is its enhanced body effect, i.e. the dependency of the threshold voltage, V_{th}, on the bulk biasing, as compared to standard (bulk) CMOS processes. Based on this effect and the physical structure of FD-SOI, the value of V_{th} can be tuned by using the body terminal of MOS transistors as control voltage, what can be exploited to enhance the performance of analog, mixed-signal and Radio-Frequency (RF) Integrated Circuits (ICs) [2]–[6]. Among other benefits, the tuning of V_{th} allows analog circuits to operate with reduced supply voltages, even within the order of a few hundreds of mV [1]. This requirement is becoming more and more necessary due to the limited dynamic range imposed by the reduction of supply voltages with technology downscaling below 1V. This fact precludes the use of conventional Operational Transconductance Amplifiers (OTAs) to implement the active elements of basic analog building blocks such as filters and Analog-to-Digital Converters (ADCs) [7].

Indeed, one of the trends to implement ADCs in deep nanometer nodes – either based on Sigma-Delta Modulation ($\Sigma\Delta$M) or SAR – is based on the use of Voltage-Controlled Ring Oscillators (VCROs) as basic building blocks. Although the first VCRO-based $\Sigma\Delta$ ADCs were based on replacing the conventional amplitude-based quantizers by time-based quantizers built with VCROs, these circuits have been also used to implement other basic building blocks of $\Sigma\Delta$ ADCs, SAR and hybrid SAR-$\Sigma\Delta$M ADCs [8]–[21]. However, in spite of the potential advantages of VCROs to design mostly-digital ADCs, the performance of these kinds of converters is degraded by the nonlinearity caused by the voltage-to-frequency (V-to-F) transformation carried out by VCRO circuits. In order to address this limitation, several strategies have been proposed, which include among others, the use of calibration [15], phase detection [16] or the so-called Gated switched-Ring Oscillators (GROs) [9], [14], [19]. In the majority of cases, reported linearization techniques imply an increased circuit complexity, thus loosing some of the benefits of VCROs as a digital-based alternative to analog signal processing [22].

In this scenario, this paper explores the use of FD-SOI CMOS technology to design body-input analog circuits with improved linearity as compared to their bulk CMOS counterparts. Based on the authors' previous work [23], the main objective of this article is to investigate how the enhanced threshold-voltage modulation (body effect) presented in FD-SOI technologies can be exploited to get a more linear performance in basic analog building blocks – such as OTAs, CMOS

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switches and voltage-controlled oscillators – and show their potential application to design analog circuits and systems. This improved linear performance can be achieved thanks to the higher linear relationship obtained between the threshold voltage and the bulk (body) voltage of FD-SOI MOS transistors. As an application, the presented techniques are shown for the linearization of VCROs implemented with current-starved inverter cells. A theoretical study of the V-to-F characteristic is carried out, which is verified by transistor-level simulations in a 28-nm FD-SOI CMOS technology. In order to show the potential benefits of the presented approach, transistor-level simulations of a 1st-order and a 2nd-order VCRO-based $\Sigma\Delta$Ms are shown that demonstrate an improvement in the effective Dynamic Range (DR) thanks to its linearity enhancement with respect to conventional approaches.

The rest of this paper is organized as follows. Section II gives some background on FD-SOI and compares its main features with respect to bulk CMOS process, paying attention to the body effect and enhanced V_{th} tuning. Section III analyzes the linearity of some basic analog circuits, such as simple OTAs and CMOS switches. Section IV and Section V apply the presented approach to increase the linearity of VCROs and frequency-based $\Sigma\Delta$ ADCs. Finally, conclusions are drawn in Section VI.

II. Background on FD-SOI CMOS

Fig. 1 shows a conceptual cross-section view of MOS transistors in 28-nm FD-SOI CMOS technology considered in this work as case study. As stated in [1], FD-SOI MOS devices behave as dual-gate transistors, having a front-side gate like in bulk CMOS technologies, and a back-side gate – denoted in Fig. 1 as V_{bn} and V_{bp} for the nMOS and pMOS transistors, respectively. It is well known that the body effect in CMOS can be expressed (for a nMOS transistor) as:

$$V_{\text{th}} = V_{\text{th0}} + \gamma \cdot (\sqrt{|2\phi_F - V_{\text{bs}}|} - \sqrt{|2\phi_F|}) \qquad (1)$$

where V_{th} denotes the threshold voltage; V_{th0} is the threshold voltage when there is no body effect, i.e. the bulk-source voltage, V_{bs}, is zero; γ is the body-effect parameter, and ϕ_F is the Fermi potential.

A. Enhanced Body Effect of FD-SOI CMOS

The back-gate terminal of MOS devices in Fig. 1 allows to implement a more efficient body biasing of V_{th} than in bulk CMOS, thanks to the wider voltage ranges (in the order of 3V) allowed by the parasitic zener diodes between N-well to substrate (in pMOS) and P-well to N-well (in nMOS) [1]. This allows to increase the body factor in MOS transistors while keeping a linear relationship between V_{th} and $(V_{\text{bn}}, V_{\text{bp}})$ as compared to the root square dependency of (1). This effect is shown in Fig. 2, which represents the variation of V_{th} with respect to V_{bn} and V_{bp} in a 28-nm FD-SOI CMOS process for different transistor sizes. The simulation data in Fig. 2 fit well with a linear function–also depicted in Fig. 2– given by:

$$V_{\text{thn}} = V_{\text{thn0}} - r_n \cdot V_{\text{bn}} \qquad (2)$$

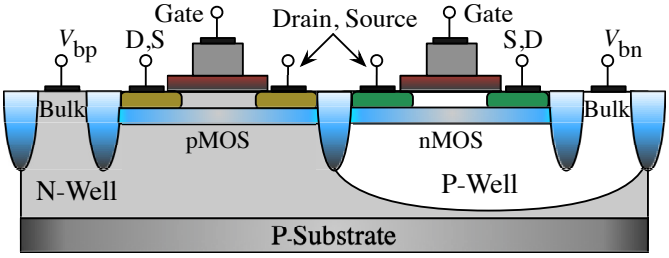

Fig. 1. Physical cross-section view of MOS transistors in 28-nm FD-SOI [1].

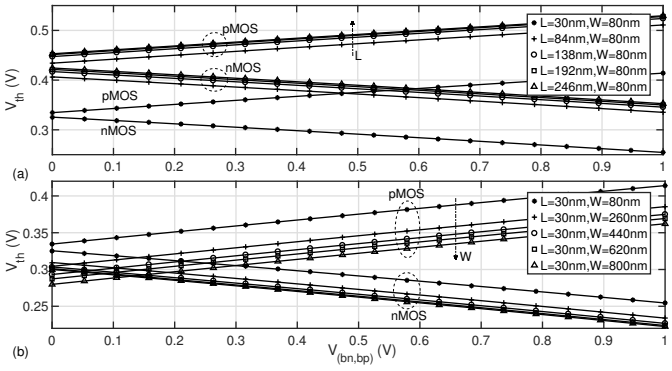

Fig. 2. Variation of V_{th} with respect to V_{bn} and V_{bp} in 28-nm FD-SOI CMOS for different values of: (a) the transistor channel length (L) with minimum width ($W = 80$nm) and (b) width (W) with minimum length ($L = 30$nm).

$$|V_{\text{thp}}| = |V_{\text{thp0}}| + r_p \cdot V_{\text{bp}} \qquad (3)$$

where V_{thn0} and V_{thp0} stand for the zero-bias threshold voltages of nMOS and pMOS, respectively, and r_n and r_p are the corresponding body factors. The values of V_{thn0} and V_{thp0}, are respectively $V_{\text{thn0}} = 326$mV and $V_{\text{thp0}} = 335$mV for minimum-size transistors. The body factors are $r_n \simeq 70$mV/V and $r_p \simeq 80$mV/V for minimum transistor sizes, slightly varying from $r_n \simeq 68.8$mV/V to $r_n \simeq 77.8$mV/V, and $r_p \simeq 76.5$mV/V to $r_p \simeq 82.4$mV/V for the sizes shown in Fig. 2. These body-factor values are higher than typical body factors of bulk CMOS[1], thus allowing to increase the tuning range of V_{th}. Note also from (2) and (3) that the linear coefficients have opposite signs. This feature can be used to compensate for nonlinear dependencies in some body-input analog circuits, such as ring oscillators, thus allowing a better control of (V_{gs}-V_{th}), and consequently of the nonlinear V-to-F characteristic of VCROs as will be discussed later.

B. Main Performance Metrics of FD-SOI CMOS

In addition to the linear performance, the enhanced body factor of FD-SOI process may be advantageous to design analog and mixed-signal circuits in terms of other main performance metrics – such as transconductance efficiency, intrinsic gain and speed. A detailed analysis of all these design metrics –beyond the scope of this paper– can be found in [1],

[1]Note that in bulk CMOS processes, the body effect is not a linear function (see Eq. (1)). Therefore, the body factor is considered in this case as the maximum tuning range of V_{th} with respect to V_{bs}.

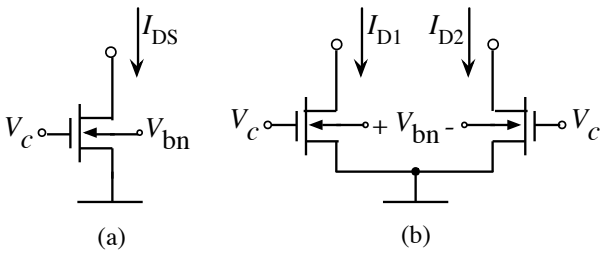

Fig. 3. Basic bulk-input nMOS OTA stages. (a) Single transistor. (b) Differential pair.

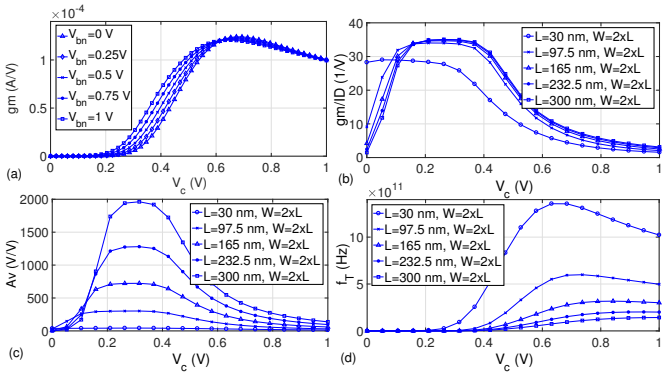

Fig. 4. Illustrating some performance metrics for FD-SOI. (a) g_m vs. V_c for different values of V_{bn}. (b) g_m/I_{DS} vs. V_c. (c) A_v vs. V_c. (d) f_T vs. V_c.

where these metrics are experimentally compared with a 28-nm bulk CMOS process. Instead, some basic expressions and simulations are given to illustrate the influence of V_{th} tuning.

Let us consider the most simple case of a single nMOS transistor configured as a bulk-input OTA – conceptually depicted in Fig. 3(a). For the purposes of this work, let us assume that the transistor is in strong inversion and in saturation region, so that the drain-source current is given by[2]:

$$I_{\text{DS}} = \frac{\beta_n}{2}(V_c - V_{\text{th}})^2 \tag{4}$$

where $\beta_n = \frac{W}{L}\mu_n C_{\text{ox}}$; μ_n is the mobility of electrons; C_{ox} is the gate-oxide capacitance per unit area; and W and L, are respectively the transistor channel width and length of the MOS transistor.

The small-signal transconductance, $g_m \simeq \beta_n(V_c - V_{\text{th}})$, and its derived performance metrics, such as intrinsic voltage gain, $A_v \equiv g_m/g_{ds}$, transconductance efficiency, $gm\text{ID} \simeq g_m/I_{\text{DS}}$, and transit frequency, $f_T \equiv g_m/C_g$, can also benefit from the body biasing [1]. As an illustration, Fig. 4 shows the main simulated performance metrics for different sizing and ranges of V_c and V_{bn}. Note that these metrics can be optimized by properly setting the sizing and values of V_c and V_{bn}.

[2]This simplified first-order model is enough for the analysis presented here without loss of generality. More accurate models (including second-order effects) can be considered, although they will lead to more complex mathematical expressions, without adding significant information to the purposes of this work.

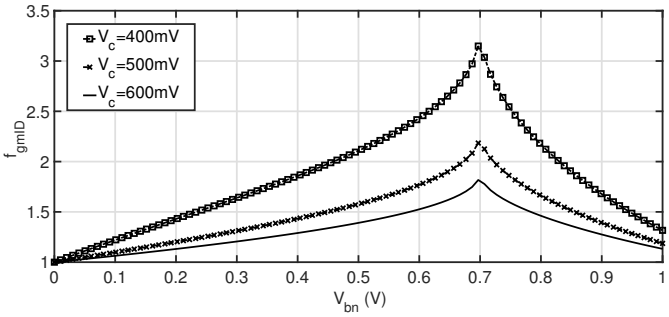

Fig. 5. Ratio between the transconductance efficiency in FDSOI CMOS and bulk CMOS, denoted as f_{gmID}, versus V_{bn}, for different values of V_c.

Moreover, some performance metrics can further benefit from the enhanced body effect provided by FD-SOI process [1]. For instance, the transconductance efficiency, $g_m/I_{\text{DS}} \simeq 2/(V_c - V_{\text{th}})$, can be improved as compared to bulk CMOS, by properly setting V_c and V_{bn}. This can be estimated by computing $gm\text{ID}$ considering two cases: bulk CMOS, i.e. V_{th} as given in (1) and FD-SOI, i.e. V_{th} expressed as in (2). This way, the ratio between the transconductance efficiency in FD-SOI, $gm\text{ID}_{\text{FDSOI}}$, and in bulk CMOS case, $gm\text{ID}_{\text{BULK}}$, can be approximated for an nMOS transistor as follows:

$$\begin{aligned} f_{\text{gmID}} &\equiv \frac{gm\text{ID}_{\text{FDSOI}}}{gm\text{ID}_{\text{BULK}}} = \\ &= \frac{V_c - V_{\text{thn0}} - \gamma \cdot (\sqrt{|2\phi_F - V_{\text{bs}}|} - \sqrt{|2\phi_F|})}{V_c - V_{\text{thn0}} + r_n \cdot V_{\text{bn}}} \end{aligned} \tag{5}$$

This is illustrated in Fig. 5, where f_{gmID} is represented versus V_{bn} for an nMOS transistor with $V_{\text{thn0}} = 326$mV, $r_n = 70$mV/V, $\gamma = 0.4\sqrt{\text{V}}$, $\phi_{\text{F}} = 350$mV and different values of V_c. Note that there is a set of values of V_c and V_{bn} that obtain a better transconductance efficiency than its bulk CMOS counterpart. Indeed, it can be shown that f_{gmID} can be maximized for $V_{\text{bn}} \simeq 2\phi_F$.

A more detailed comparison of main performance metrics of FD-SOI versus bulk CMOS processes can be found in related literature [1]. The main objective of this work is to analyse how the enhanced body effect of FD-SOI CMOS can be exploited to improve the linearity of analog and mixed-signal circuits and systems.

III. Nonlinear Performance of Bulk-Input Basic Analog Circuits: FD-SOI vs. CMOS

Before studying more complex analog circuits, the analysis that follows focuses on some basic analog building blocks – such as single-transistor amplifiers and CMOS switches – as case studies to show how the use of back-gate voltage can be applied to improve the linearity performance of these circuits, and subsequently of the analog and mixed-signal systems based on them: such as oscillators, filters, ADCs, etc. As stated above, other performance metrics – such as electronic noise, finite dc gain, gain-bandwidth, etc. – are beyond the scope of this paper, which mainly focuses on how to get benefit of applying the wider tuning of V_{th} available in FD-SOI CMOS to enhance the linearity of analog and mixed-signal circuits.

A. Bulk-input single-transistor amplifier stages

Let us assume that V_{th} depends on the bulk-source voltage, V_{bn}, i.e. according to the body-effect dependency of a bulk/standard CMOS process given in (1). In this case, it can be shown that, after applying a Taylor Series expansion of (4) as a function of V_{bn}, the drain-source current of an nMOS transistor (Fig. 3(a)) can be expressed as:

$$I_{\text{DS}} \simeq I_{\text{DS0}} + g_{11} \cdot V_{\text{bn}} + g_{12} \cdot (V_{\text{bn}})^2 + g_{13} \cdot (V_{\text{bn}})^3 + ... \quad (6)$$

where

$$\begin{aligned} I_{\text{DS0}} &= \frac{\beta_n}{2}(V_c - V_{\text{th0}})^2,\ g_{11} = \frac{\beta_n \cdot \gamma \cdot (V_c - V_{\text{th0}})}{2 \cdot \sqrt{2\phi_F}} \\ g_{12} &= \frac{\beta_n \cdot \gamma \left[2 \cdot \gamma \cdot \sqrt{\phi_F} + \sqrt{2} \cdot (V_c - V_{\text{th0}})\right]}{32 \cdot (\phi_F)^{3/2}} \\ g_{13} &= \frac{\beta_n \cdot \gamma \left[2 \cdot \gamma \cdot \sqrt{\phi_F} + \sqrt{2} \cdot (V_c - V_{\text{th0}})\right]}{128 \cdot (\phi_F)^{5/2}} \end{aligned} \quad (7)$$

It is clear from (6) that the dependency of I_{DS} on V_{bn} is strongly nonlinear, having multiple nonlinear terms (denoted as g_{1i}), as compared to the quadratic dependency of I_{DS} with respect to the gate-source voltage, V_c. Therefore, from the linearity viewpoint, using the bulk terminal as an input does not provide any advantage with respect to using the gate input terminal. Indeed, the second- and third-order Harmonic Distortion (HD) coefficients can be easily obtained from (7) as [24]:

$$\begin{aligned} \text{HD}_2 &\equiv \frac{g_{12}}{2 \cdot g_{11}} \cdot |V_{\text{bn}}| = \frac{\gamma \cdot \sqrt{2\phi_{\text{F}}} + (V_c - V_{\text{th0}})}{16 \cdot \phi_{\text{F}} \cdot (V_c - V_{\text{th0}})} \cdot |V_{\text{bn}}| \\ \text{HD}_3 &\equiv \frac{g_{13}}{4 \cdot g_{11}} \cdot |V_{\text{bn}}|^2 = \frac{\gamma \cdot \sqrt{2\phi_{\text{F}}} + (V_c - V_{\text{th0}})}{128 \cdot \phi_{\text{F}}^2 \cdot (V_c - V_{\text{th0}})} \cdot |V_{\text{bn}}|^2 \end{aligned} \quad (8)$$

where $|V_{\text{bn}}|$ denotes the amplitude of a sinewave signal applied at the body terminal of the nMOS transistor shown in Fig. 3(a).

Let us consider now that the MOS transistor is implemented in a FD-SOI technology. In this case, there will be a linear body-effect dependency given by (2), which for the nMOS transistor shown in Fig. 3(a), yields to a square-law dependency of the drain-source current given by:

$$I_{\text{DS}_{\text{FDSOI}}} = \frac{\beta_n}{2}(V_c + r_n \cdot V_{\text{bn}} - V_{\text{th0}})^2 \quad (9)$$

In this case, considering a bulk-input differential input pair as that conceptually depicted in Fig. 3(b), the differential drain (output) current can be obtained from (9) as:

$$I_{\text{out}} \equiv I_{\text{D1}} - I_{\text{D2}} = \beta_n \cdot r_n \cdot (V_c - V_{\text{th0}}) \cdot V_{\text{bn}} \quad (10)$$

that means a perfect linear relationship between the output current and the differential input signal applied at the bulk of both transistors[3]. This is illustrated in Fig. 6, where a simulation of the differential output current of Fig. 3(b) is shown for a 28-nm FD-SOI technology. In addition to get a more linear input-output characteristics as compared to a bulk CMOS process, the use of bulk-input FD-SOI OTA stages can use the gate voltage of transistors, V_c, as a gain control voltage – which is varied from 0.35V to 0.65V in Fig. 6. This feature adds some more degrees of freedom to make it easier to program the gain of a given OTA stage in more complex analog subsystems built with these kinds of OTAs.

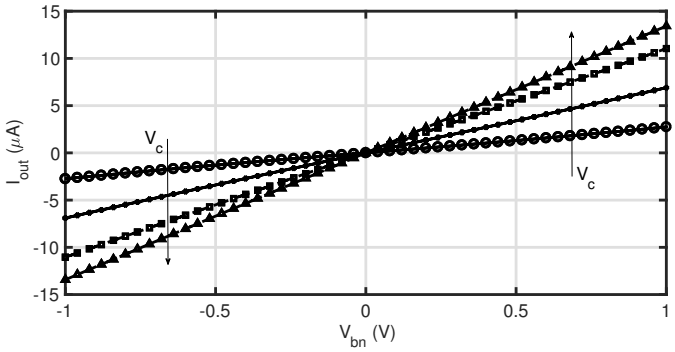

Fig. 6. Simulation of the input-output characteristic of a bulk-input differential pair implemented in a 28-nm FD-SOI CMOS technology, where V_c is used as control voltage, ranging from 0.35V to 0.65V, as highlighted by the arrows.

B. Bulk-terminal controlled CMOS Switches

Switches – usually implemented as CMOS transmission gates like that illustrated in Fig. 7(a)– are also basic building blocks of analog circuits, for instance in Switched-Capacitor (SC) filters and ADCs [25], [26]. Most of these circuits have a sampling and hold (S/H) at the input, which usually limits the linearity of the overall system. Although there might be several circuit/physical effects limiting the nonideal/nonlinear operation of CMOS switches – charge redistribution and clock feedthrough – the discussion presented here focuses on the effect caused by the nonlinear switch-on resistance, since it can be reduced by using the enhanced body effect of FD-SOI as detailed bellow.

Assuming that both nMOS and pMOS transistors in Fig. 7(a) are in ohmic region, it can be shown that the switch-on resistance is approximately given by:

$$R_{\text{on}} \simeq \frac{1}{g_{\text{on}_\text{p}} + g_{\text{on}_\text{n}}} \quad (11)$$

where g_{on_p} and g_{on_n} stand for the switch-on conductances of the nMOS and pMOS transistors, respectively given by:

$$\begin{aligned} g_{\text{on}_\text{n}} &\simeq \beta_{\Omega n} \cdot (V_{dd} - V_{\text{thn}} - v_{\text{in}}) \\ g_{\text{on}_\text{p}} &\simeq \beta_{\Omega p} \cdot (v_{\text{in}} - V_{ss} - |V_{\text{thp}}|) \end{aligned} \quad (12)$$

[3]Similarly to a conventional bulk CMOS technology, this perfect linear relationship can be degraded in practice by second-order effects of MOS transistors–not considered in this work without loss of generality. Moreover, the dependency of I_{DS} and $I_{\text{DS}_{\text{FDSOI}}}$ with respect to V_c is the same in both cases. Therefore, there would not be – *a priori* – any benefits of FD-SOI with respect to bulk CMOS process if a gate-input approach is considered in OTAs.

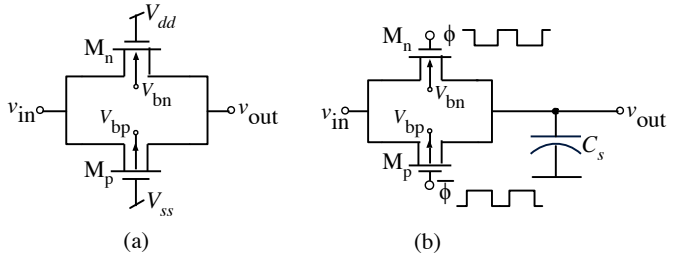

Fig. 7. Bulk-terminal controlled CMOS switches. (a) Switch-on schematic. (b) S/H circuit.

where $\beta_{\Omega(n,p)}$ stands for the β parameter of the (n,p)-MOS transistors in the ohmic region. Note that, as the value of R_{on} is a nonlinear function of the input signal, v_{in}, being transmitted through the switch, then harmonic distortion is generated. Indeed, as discussed in [22], the harmonic distortion caused by this effect is mainly caused by the switches that are directly connected to the input signal given that the voltages at the input/output nodes of the remaining ones remain approximately constant over clock periods, and consequently R_{on} is approximately constant during the sampling phase time. Moreover, the nonlinearity increases with the ratio between the input signal frequency and the sampling frequency. Indeed, it can be shown that, using Volterra series method, the third-order HD due to nonlinear sampling is given by [25]:

$$\text{HD}_3 \simeq \frac{\pi f_{\text{in}} C_s R_{\text{on}}}{2(V_{\text{ON}} - V_T)^2} V_{\text{in}}^2 \tag{13}$$

where V_{in} is the input signal amplitude, C_s is the sampling capacitance, V_{ON} denotes the switch-on voltage (either V_{dd} or $|V_{ss}|$), and V_T is the maximum (worst-case) value of V_{thn} and $|V_{\text{thp}}|$.

However, the influence of the input signal on the switch-on resistance can be reduced if the back-gate terminal voltage of the nMOS and pMOS transistors in the CMOS switch (see Fig. 7(a)) are properly set to compensate for the effect of v_{in}. This can be derived by substituting the V_{th} expressions of (2)-(3) in (12), yielding:

$$\begin{aligned} g_{\text{on}_\text{n}} &\simeq \beta_{\Omega n} \cdot (V_{dd} - V_{\text{thn0}} - v_{\text{in}} + r_n \cdot V_{\text{bn}}) \\ g_{\text{on}_\text{p}} &\simeq \beta_{\Omega p} \cdot (v_{\text{in}} - V_{ss} - |V_{\text{thp0}}| - r_p \cdot V_{\text{bp}}) \end{aligned} \tag{14}$$

It can be inferred from (14) that by using an adaptive circuit mechanism – which can be controlled in some electronic devices by a Digital Signal Processor (DSP)– the effect of v_{in} on the switch-on resistance can be minimized by properly setting the values of V_{bn} and V_{bp}. Indeed, the influence of v_{in} on the switch-on resistance could be theoretically nulled if $V_{\text{bn}} = v_{\text{in}}/r_n$ and $V_{\text{bp}} = v_{\text{in}}/r_p$. However, this is not feasible in practice due to the values of r_n and r_p. Nevertheless, the harmonic distortion caused by the nonlinear switch-on resistance can be attenuated up to some extend by properly tuning V_{bn} and V_{bp}.

In order to illustrate this effect, let us consider a simple S/H circuit like that shown in Fig. 7(b). The distortion generated by the nonlinear sampling can be evaluated through simulations of this circuit as described in [22]. To this end, a sinewave signal

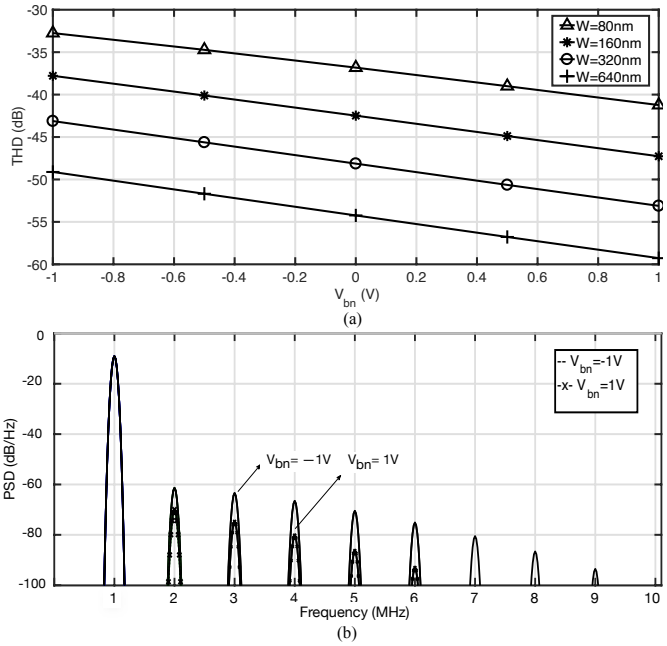

Fig. 8. Effect of bulk voltage on the harmonic distortion of CMOS switches. (a) THD vs. V_{bn} for different CMOS switch sizes. (b) Output spectra for different values of V_{bn} ($W = 640$nm), showing how the power of harmonics decreases with V_{bn}.

with 1-MHz frequency and 0.5-V amplitude is applied at the input and the voltage stored in C_s ($C_s = 1$pF in this example) can be collected at the clock rate to compute the Fast Fourier Transform (FFT) and calculate the Total Harmonic Distortion (THD).

This is illustrated in Fig. 8(a), where the THD caused by the nonlinear switch-on resistance is depicted versus V_{bn} in a 28-nm FD-SOI technology, for different values of the width (W) of Mn and Mp in Fig. 7(a), by assuming the same size in both transistors and a minimum length. Note that THD – dominated by HD_2 in this single-ended circuit example – can be reduced up to 6 dB by the action of V_{bn}. This can be further improved if fully-differential circuits are considered. In this case, THD will be mostly dominated by HD_3. Hence, increasing V_{bn} may lead to a reduction of more than 10dB. This is also illustrated in the output spectra shown in Fig. 8(b), where it can be seen how the power of harmonics due to the nonlinear switch-on resistance, can be reduced by increasing V_{bn}. Moreover, this enhanced linearity feature can be further improved if bulk-control voltages are combined with bootstrapped switches in FD-SOI [27], although the circuit complexity will increase.

IV. Application to VCROs: FD-SOI vs. Bulk CMOS

The simple circuit examples described in previous section show how the use of the bulk terminal of MOS transistors can be used to improve the linearity of basic analog building blocks such as OTAs and switches. Based on this strategy, a similar approach can be followed in order to reduce the nonlinearity of VCROs, which constitute one of the main limiting factors in the so-called time/frequency-based ADCs. To this end, let us analyse first how to apply the proposed technique to improve the linear characteristics of VCROs.

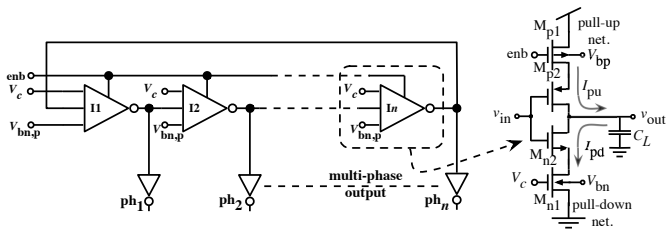

Fig. 9. Single-ended schematic of the multi-phase VCRO/GRO considered in this work.

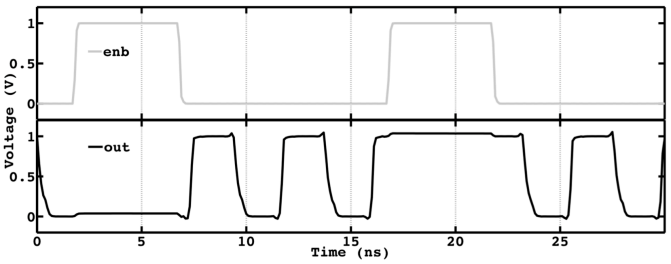

Fig. 10. Transient simulation of a single output phase of the VCRO of Fig. 9. Note that the oscillation is activated as a function of the enable signal, enb.

Fig. 9 shows a conceptual (single-ended) schematic of the VCRO under study. It consists of a pseudo-differential ring oscillator, in which the output of each inverter – denoted as ph_i $(i = 1, 2...n)$– can be taken to generate a multi-phase output signal. Note that the circuit can be configured either as a GRO or as a VCRO, depending on the value of the enable signal –denoted as enb in Fig. 9. Thus, if enb switches between OFF (logic "0") and ON (logic "1") states, this will cause the VCO to oscillate or get frozen as illustrated in Fig. 10. Regardless the VCO is configured as a GRO or not, its operation is governed by different voltage signals: V_c, V_{bn} and V_{bp}. These voltages control the operation of each VCO inverter cell – depicted in Fig. 9. This circuit is a current-starved inverter, in which the current sources – implemented by transistors M_{n1} and M_{p1} – set the current flowing through the inverter – made up of transistors M_{n2} and M_{p2}.

The oscillation frequency, f_{osc}, can be expressed as:

$$f_{\text{osc}} = \frac{1}{2 \cdot m_{\text{ph}} \cdot \tau_d(V_c, V_{\text{bn}}, V_{\text{bp}})} \tag{15}$$

where m_{ph} is the number of inverters, i.e. the number of phases in the VCRO, and τ_d stands for the propagation delay of each inverter-based VCRO cell. This delay depends on the charging/discharging time of the load capacitance, C_L, at the inverter output, which in turns depends on the current flowing through the inverter – controlled by V_c, V_{bn} and V_{bp}. Thus, the overall propagation delay can be expressed as:

$$\tau_d = \tau_{\text{LH}} + \tau_{\text{HL}} \tag{16}$$

where τ_{LH} and τ_{HL} stand respectively for the charging ("Low-High") and discharging ("High-Low") transient times, which will be driven by the pull-up and pull-down networks of the inverter cell (see Fig. 9), such that:

$$\tau_{\text{LH}} \simeq C_L \cdot \frac{\Delta v_{\text{out}_{\text{LH}}}}{I_{\text{pu}}}, \tau_{\text{HL}} \simeq C_L \cdot \frac{\Delta v_{\text{out}_{\text{HL}}}}{I_{\text{pd}}} \tag{17}$$

where I_{pu} and I_{pd} stand for the pull-up and pull-down currents, respectively.

In order to obtain an accurate expression of (16), the transient response should be analyzed in different time intervals, according to the operation region of each transistor of the inverter at each time interval. However, for design purposes, some intuition can be obtained if the analysis is simplified by assuming that all transistors are operating in the saturation region during the transient response. This way, τ_{LH} can be computed as the time for an inverter output to reach a minimum voltage—$\Delta v_{\text{out}_{\text{LH}}} = \Delta v_{\text{out}_{\text{HL}}} = V_{dd}/2$— in order to activate the next cell.

Based on these assumptions, and considering that enb $= 0$V, it can derived from (16) and (17) that:

$$\tau_d \simeq C_L \cdot V_{dd} \left[\frac{1}{\beta_n \cdot (V_c - V_{\text{thn}})^2} + \frac{1}{\beta_p \cdot (V_{dd} - |V_{\text{thp}}|)^2} \right] \tag{18}$$

where V_{dd} is the supply voltage and β_n and β_p stand for the β parameter of transistors M_{n1} and M_{p1}, respectively.

Replacing (18) in (15), it can be shown that:

$$f_{\text{osc}} \simeq \frac{\alpha_{\text{osc}}}{\left[\frac{1}{(V_c - V_{\text{thn}})^2} + \frac{\alpha_\beta}{(V_{dd} - |V_{\text{thp}}|)^2} \right]} \tag{19}$$

where $\alpha_\beta = \beta_n/\beta_p$ and $\alpha_{\text{osc}} = \beta_n/(2 \cdot m_{\text{ph}} \cdot C_L \cdot V_{dd})$.

Note from (19) that, as expected, f_{osc} depends on V_c and $V_{\text{bn,p}}$ through the body effect of $V_{\text{th(n,p)}}$. In order to obtain the V-to-F characteristics that relate f_{osc} with the different control voltages, a Taylor series expansion of (19) as a function of those voltages can be derived. In order to simplify this analysis[4], it will be assumed in (19) that $(V_{dd} - |V_{\text{thp}}|)^2 \gg (V_c - V_{\text{thn}})^2$, yielding to:

$$f_{\text{osc}} \simeq \alpha_{\text{osc}} \cdot (V_c - V_{\text{thn}})^2 \tag{20}$$

where V_{thn} depends on the bulk voltage of M_{n1} as either (1) or (2), giving rise to different performance in terms of linearity.

A. Bulk-Input Controlled VCROs

Let us analyse first the effect of using V_{bn} as control voltage and that V_{thn} depends on V_{bn} according to (1) with $V_{\text{bs}} = V_{\text{bn}}$. Applying a Taylor series expansion of (20), it can be shown that:

$$f_{\text{osc}} \simeq f_q + k_{\text{VCO}_1} \cdot V_{\text{bn}} + k_{21} \cdot V_{\text{bn}}^2 + k_{31} \cdot V_{\text{bn}}^3 + ... \tag{21}$$

[4]Similar conclusions can be derived if the first term in the denominator of (19) is neglected, i.e. if $V_c \gg V_{\text{thn}}$.

where f_q is the quiescent (or running) oscillation frequency, $k_{\mathrm{VCO_1}}$ is the VCRO gain and k_{n1} stands for the n-th order nonlinear terms, respectively given by:

$$\begin{aligned} f_q &= \alpha_{\mathrm{osc}} \cdot (V_c - V_{\mathrm{thn0}})^2 \\ k_{\mathrm{VCO_1}} &= \frac{\alpha_{\mathrm{osc}} \cdot \gamma \cdot (V_c - V_{\mathrm{thn0}})}{\sqrt{2\phi_{\mathrm{F}}}} \\ k_{21} &= \frac{\alpha_{\mathrm{osc}} \cdot \gamma}{8 \cdot \phi_{\mathrm{F}}} \cdot \left[\gamma + \frac{(V_c - V_{\mathrm{thn0}})}{\sqrt{2\phi_{\mathrm{F}}}}\right] \\ k_{31} &= k_{21}/4 \end{aligned} \tag{22}$$

Let us consider that the VCRO cell is implemented using FD-SOI, and hence, V_{thn} depends on V_{bn} according to (2). Proceeding in a similar way, it can be shown that:

$$f_{\mathrm{osc}} \simeq f_q + k_{\mathrm{VCO_2}} \cdot V_{\mathrm{bn}} + k_{22} \cdot V_{\mathrm{bn}}^2 \tag{23}$$

where $k_{\mathrm{VCO_2}} = 2 \cdot \alpha_{\mathrm{osc}} \cdot (V_c - V_{\mathrm{thn0}})$ and $k_{22} = \alpha_{\mathrm{osc}} \cdot r_n^2$.

Note from (23) that only a second-order nonlinearity is obtained in the case of FD-SOI bulk-input controlled VCRO cells, while in the case of conventional bulk processes, higher-order nonlinear terms (3rd-order, 4th-order, etc.) are obtained as shown in (21). This is illustrated in Fig. 11(a), where $f_{\mathrm{osc}}/\alpha_{\mathrm{osc}}$ is represented for $V_c = 0.5$V, $V_{\mathrm{thn0}} = 326$mV, $r_n \simeq 70$mV/V, $\gamma = 0.4\sqrt{\mathrm{V}}$ and $\phi_{\mathrm{F}} = 350$mV. An estimation of the nonlinear error can be computed as [28]:

$$\epsilon_{\mathrm{osc}} = \frac{f_{\mathrm{osc}} - f_{\mathrm{osc\text{-}ideal}}}{f_{\mathrm{osc\text{-}ideal}}} \tag{24}$$

where $f_{\mathrm{osc\text{-}ideal}}$ stands for the ideal (perfectly linear) V-to-F characteristic of the VCRO.

Fig. 11(b) depicts the nonlinear error for both FD-SOI and bulk CMOS, corresponding to the V-to-F characteristics shown in Fig. 11(a). It is clear how the use of FD-SOI technology to apply the bulk terminal as a control voltage of VCROs can reduce the nonlinear error in several orders of magnitude. Moreover, only comparing the expressions of the 2nd-order terms in (21) and (23), it can be shown that k_{22} is lower than k_{21}, and the ratio k_{22}/k_{21} decreases with V_c. This is illustrated in Fig. 12 where k_{22}/k_{21} is represented for $V_c > V_{\mathrm{thn0}}$ for the same MOS parameters used in Fig. 11. This way, V_c and V_{bn} can be combined to reduce the nonlinearity of VCROs within a given frequency tuning range as will be demonstrated later by transistor-level simulations.

B. Gate-Input Controlled VCROs

Let us consider now the most conventional case in which the control voltage of the VCRO cell is the gate voltage of $\mathrm{M_{n1}}$, i.e. V_c, and there is not any body effect, i.e. $V_{\mathrm{bn}} = 0$ and $V_{\mathrm{bp}} = V_{dd}$. In this case, it can be shown from (20) that the oscillation frequency is given by:

$$f_{\mathrm{osc}} \simeq \alpha_{\mathrm{osc}} \cdot V_{\mathrm{thn0}}^2 - 2\alpha_{\mathrm{osc}} \cdot V_{\mathrm{thn0}} \cdot V_c + \alpha_{\mathrm{osc}} \cdot V_c^2 \tag{25}$$

Comparing (23) and (25), it is clear that in both cases, quadratic dependencies on the control voltages are obtained. However, the second-order nonlinear term (k_{22}) in FD-SOI case – eq. (23) – is attenuated by the body factor, which in the 28-nm technology process is $r_n \simeq 70$mV/V, i.e. almost two orders of magnitude lower than the nonlinearity obtained in the case of conventional gate-controlled VCROs – Eq. (25).

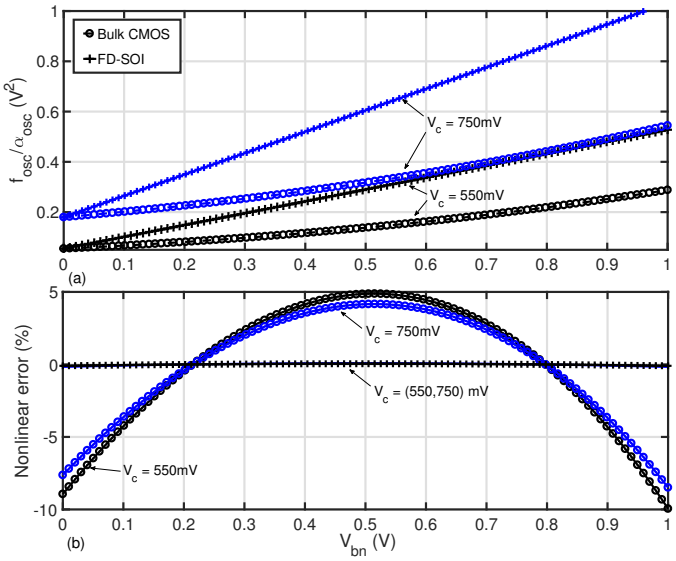

Fig. 11. Bulk-input VCROs: (a) $f_{\mathrm{osc}}/\alpha_{\mathrm{osc}}$ vs. V_{bn}. (b) Nonlinear error (ϵ_{osc}).

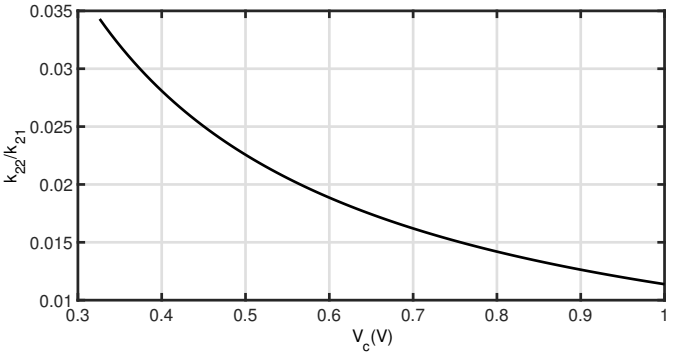

Fig. 12. Comparison of the second-order non-linear term of the V-to-F characteristic in bulk-input VCROs: CMOS (k_{21}) vs. FDSOI (k_{22}).

This is verified by transistor-level simulations as shown in Fig. 13, where the V-to-F characteristic of the VCRO in Fig. 9 is depicted. Note that, as predicted by the above theoretical analysis shown in eqs. (19)-(25) – also illustrated in Fig. 11, the use of bulk-input voltage drastically improves the nonlinear error, at the price of reducing the frequency tuning range with respect to the gate-input case. However, as can be shown in (23), both f_q and k_{VCO} can be tuned also through the gate control voltage, V_c. This feature increases the flexibility and reconfigurability of VCROs in terms of frequency tuning range, thanks to the combined action of both gate- (V_c) and bulk-input (V_{bn}) control voltages, as despited in the simulations shown in Fig. 13. As shown in Fig. 13(a), a wider tuning range can be achieved by using V_c as control voltage, due to its direct effect on f_q. The overall tuning range of f_{osc} is also controlled by V_{bn} through k_{VCO}– see Eq. (21). However, the nonlinear error is much lower if V_{bn} is used as control voltage, as illustrated in the simulated error shown in Fig. 13(b).

The effect of PVT variations and technology parasitics

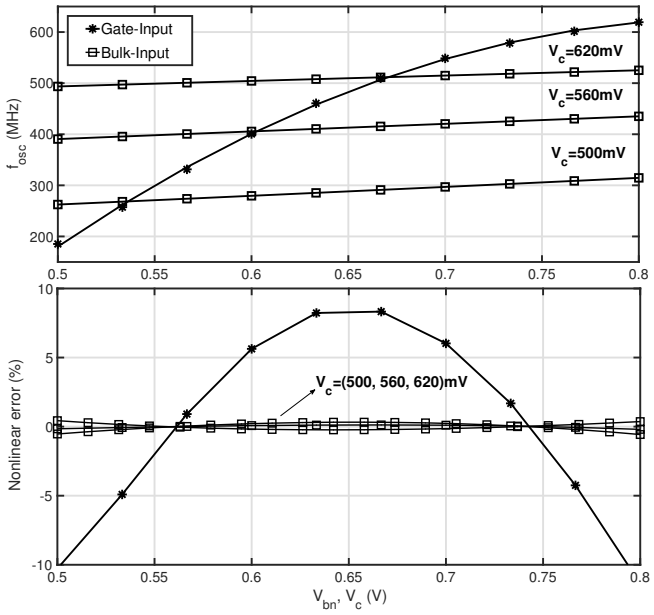

Fig. 13. Transistor-level simulation of the V-to-F characteristic and nonlinear error of a VCRO in 28-nm FD-SOI CMOS: gate-input (V_c) vs. bulk-input ($V_{\rm bn}$).

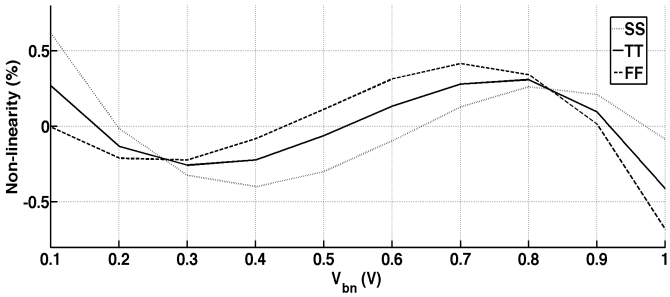

Fig. 14. Effect of technology corners on the nonlinear error of the designed VCRO for $V_c = 510$mV. The notation used for the corners is the following: SS: Slow-Slow, TT: Typical-Typical, FF: Fast-Fast.

have been taken into account in this design example. As an illustration, Fig. 14 shows the impact of the main technology corners of transistor models for $V_{\rm c} = 510$mV. The worst-case nonlinear error is -0.6% – obtained for Fast-Fast (FF) corner when the input signal is close to 1V. Note that this value is still better than that obtained for gate-input VCRO topologies (see Fig. 13(b)). This combined effect of gate-control voltage and bulk-input signals can be exploited to improve the performance of some analog systems which require linear VCROs, such as frequency-based $\Sigma\Delta$ ADCs as described in the next section.

V. Application to VCRO-based $\Sigma\Delta$ ADCs

In the last years, VCROs are being used to build $\Sigma\Delta$ ADCs in order to palliate the reduced dynamic range caused by the technology downscaling in conventional, amplitude-based, quantizers, and $\Sigma\Delta$M loop filters [8]–[19]. For the purposes of the analysis presented in this paper, and without the loss of generality, let us consider as case studies single-loop VCRO-based $\Sigma\Delta$M architectures based on the topologies proposed in [17], [18].

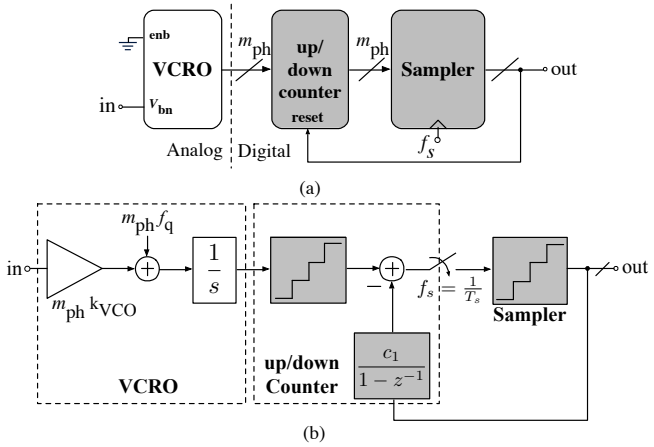

Fig. 15. Bulk-input 1st-order VCRO-based $\Sigma\Delta$M. (a) Block diagram. (b) Equivalent behavioral model. (The system is implemented in practice using a pseudo-differential topology – similar to other VCO-based $\Sigma\Delta$Ms [17], [29]).

A. First-order bulk-input VCRO-based $\Sigma\Delta$ Modulator

Considering this approach, a bulk-input multi-phase VCRO like that shown in Fig. 9 can be used to implement a 1st-order $\Sigma\Delta$M as conceptually depicted in Fig. 15(a). The input signal of the $\Sigma\Delta$M is connected at the back-gate terminal ($V_{\rm bn}$) of the VCRO (see Fig. 9), which implements the front-end integrator of the $\Sigma\Delta$M as shown in the equivalent behavioral model shown in Fig. 15(b) [18]. This VCRO drives a (up/down) counter, which counts the number of transitions of the input signal within a given time period, i.e. sampling time, $T_s = 1/f_s$, with f_s being the sampling frequency. As a result, this block acts as a digital differentiator and as quantizer, generating a digital representation of the input signal plus a phase quantization error [11], [17], as conceptually shown in the model of Fig. 15(b)[5]. The VCRO-based $\Sigma\Delta$M loop is closed by a Flip-Flop (FF) sampling register, which feeds the $\Sigma\Delta$M output back to the VCRO in order to reset its counter, thus avoiding its saturation [17].

In a more practical implementation – as the one used in this example – a pseudo-differential circuit realization is considered, so that the common-mode input frequency of Fig. 15(b) – corresponding to f_q – can be nulled by the action of the differential topology. Thus, assuming a linear model for the quantizer blocks in Fig. 15(b), it can be shown that the Z-domain transform of the modulator output is given by:

$$Y(z) = \frac{k_{\rm VCO}}{f_s} \cdot V_{\rm in}(z) + (1 - z^{-1}) \cdot E_\phi(z) \qquad (26)$$

where $k_{\rm VCO}$ stands for the VCRO gain and E_ϕ denotes the Z-transform of the phase quantization error associated to the VCRO and the sampling process carried out in the FF register. In the circuit design used as a case study, eleven phases ($m_{\rm ph} = 11$) will be used for the VCRO, and $f_{\rm osc}$ can be tuned in a wide range by combining V_c and $V_{\rm bn}$ as shown in Fig. 13(a). A True Single-Phase Clock (TSPC) logic based FF is used to

[5]Note that the quantizer block included to model the behavior of the VCO-based integrator, emulates the effect of phase quantization [11], [17].

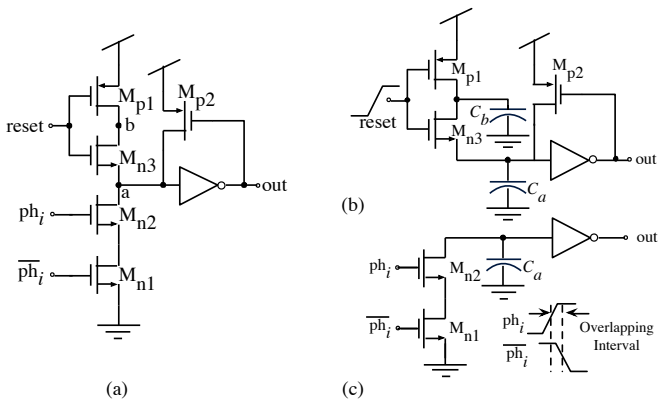

Fig. 16. Proposed TSPC-based up/down counter: (a) Schematic. Equivalent circuit during (b) off-on transition of reset and (c) off-on transition of ph_i.

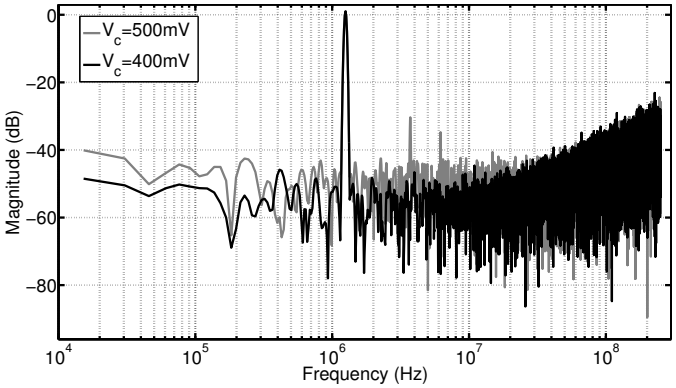

Fig. 17. Output spectra of a bulk-input VCRO-based 1st-order $\Sigma\Delta$M for different values of V_c.

implement the sampling register, since it consumes less power and occupies less area than conventional logic circuits [30].

Fig. 16(a) shows the proposed up/down reset counter circuit for a single VCO phase, ph_i, which is also based on TSPC logic. The counter is made up of a pull-down and a pull-up network. At rising edges of the reset signal, the output will be a "0" logic, whereas at rising edges of ph_i, the output will be a logic "1". Let us consider first the operation of the pull-up network of this circuit, i.e. during the off-on transition of reset signal as shown in Fig. 16(b). When reset signal is "0", the implicit capacitance at node "b" will be charged so that the voltage at this node is V_{dd} and both M_{n3} and M_{p1} will be turned on for a short period of time. During this short period, the current flowing through M_{n3} will charge the capacitance at node "a" so that this node will reach to a maximum value of $V_{dd} - V_{\text{th}}$, leading to a "0" logic at the output of the inverter. The action of M_{n3} is enhanced by the positive feedback implemented by the auxiliary pMOS transistor, M_{p2}, which is placed between the input and output terminals. The opposite situation happens when the pull-down network is active during the off-on transition of ph_i (Fig. 16(c)). In this case, the inverted delayed version of ph_i, denoted as $\overline{\text{ph}_i}$, switches from on to off with a given delay with respect to ph_i. During this delay period, both signals ph_i and $\overline{\text{ph}_i}$ are overlapped, so that both transistors M_{n1} and M_{n2} are on, and hence the current flowing through them discharges the implicit capacitance at node "a", and the counter output is "1".

The VCRO-based $\Sigma\Delta$M of Fig. 15 has been designed in a 28-nm FD-SOI CMOS technology in order to show the benefits of using bulk-input VCROs – rather than gate-input VCROs – on the linearity of frequency-based $\Sigma\Delta$ ADCs. Fig. 17 shows this feature, by depicting two transistor-level simulated output spectra[6] of the 1st-order VCRO-based $\Sigma\Delta$M clocked at $f_s = 500$MHz, with a 1.24-MHz input sinewave signal and two values of V_c, namely: $V_c = 400$mV and $V_c = 500$mV. It can be shown how the latter case yield to a higher harmonic distortion –with HD_3 being in the order of -30dB– while a proper combination of bulk- and gate- control voltages of the VCRO can drastically reduce the harmonic distortion of the modulator.

Note that if an input signal is applied at the gate terminal of the VCRO, i.e. using V_c as the input node of the $\Sigma\Delta$M, a similar noise-shaping performance can be obtained as compared to the bulk-input case. This is illustrated in the output spectra shown in Fig. 18, where the 1st-order VCRO-based $\Sigma\Delta$M is simulated by considering two cases: a gate-input (conventional case) and a bulk-input (proposed approach). In both cases, similar noise-shaping is obtained, and the estimated power consumption is 141.5μW in both cases. However, in the case of the input signal applied at the gate terminal, the maximum input Dynamic Range (DR) corresponds to a peak-to-peak input amplitude of only $V_{\text{in-pp}} = 40$mV, whereas in the bulk-input case, the input DR can be extended up to $V_{\text{in-pp}} = 400$mV, i.e. ten times higher in terms of the input DR of the ADC. Moreover, the input amplitude range of a conventional (gate-input) case can be increased, although the performance of the modulator will be degraded by the nonlinearity. This is illustrated in Fig. 19, where two cases are compared: an input sinewave with $V_{\text{in-pp}} = 100$mV applied at the gate of the VCRO (conventional case), and an input with $V_{\text{in-pp}} = 400$mV applied at the bulk (proposed approach).

The main reason for such a difference in the input range of both cases, gate-input and bulk-input, is due to the wider variation of f_{osc} with respect to V_c and V_{bn} – also illustrated in Fig. 13. Therefore, the frequency range, and consequently the input-voltage range, can be increased if the input signal is applied at the gate of the front-end VCO, at the price of reducing the input amplitude range.

The effect of V_c and V_{bn} on the input DR is better illustrated in Fig. 20, that represents the Signal-to-(Noise+Distortion) Ratio (SNDR) versus the input signal amplitude, by considering a signal bandwidth of BW $= 10$MHz. Note that, although similar values of SNDR are obtained in both gate- and bulk-input cases, in the later case (bulk input), higher values of input amplitudes can be digitized. Thus, the Full-Scale (FS) input amplitude corresponds to 500-mV if the input signal is applied at the body terminal, whereas that FS is reduced

[6]All transistor-level simulations shown in this paper were carried out in Cadence Spectre®, by including electronic noise to accurately estimate the in-band noise power as well as the impact of phase noise in VCROs. Nevertheless, a detailed study on the influence of phase noise is beyond of this paper, which is focused on the nonlinear behavior of VCROs.

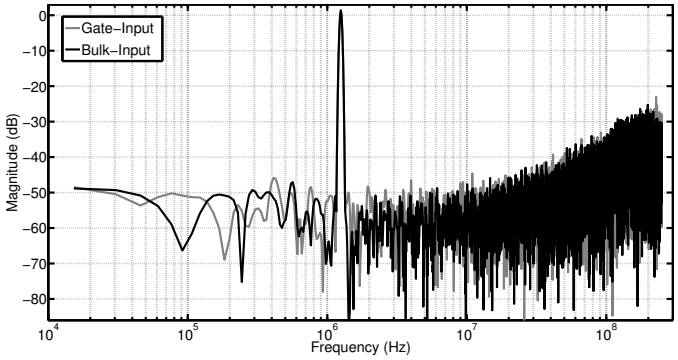

Fig. 18. Output spectra of a 1st-order VCRO-based ΣΔM considering an input 1-MHz sinewave signal in two cases: a bulk-input VCRO with $V_{\text{in-pp}} = 400\text{mV}$ amplitude and a gate-input VCRO with $V_{\text{in-pp}} = 40\text{mV}$.

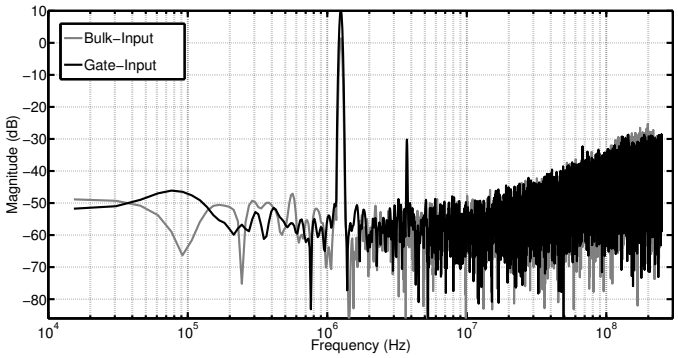

Fig. 19. Output spectra of the 1st-order VCRO-based ΣΔM, considering a bulk-input VCRO with a $V_{\text{in-pp}} = 400\text{mV}$ amplitude and gate-input VCRO with a $V_{\text{in-pp}} = 100\text{mV}$. Note that the magnitude of the FFT is represented in dBV, i.e. not referred to the FS of the modulator, in order to show the differences in the signal amplitude range for the different cases under study.

to 50-mV if the input signal is applied at the gate terminal. However, the input DR obtained in both cases is similar, corresponding to higher input amplitudes in the bulk-case as compared to gate-input case. This feature can be exploited in a practical design by properly combining the action of V_c and V_{bn} as control voltages of the front-end VCRO in ΣΔMs. This way, depending on the input signal amplitude range, either the gate- or the bulk- nodes could be used as the input terminal, while the other is used as an additional control voltage, thus increasing the overall input DR that can be digitized by a given ADC, while keeping the linearity. This is also illustrated in Fig. 20, by showing the effect of varying V_c, while keeping the bulk terminal (V_{bn}) as the input node. This is another potential application of the presented technique, which allows an ADC to adapt the DR to the range of input signals to be digitized.

Following the same approach, a second-order VCRO-based ΣΔM can be implemented as depicted in Fig. 21(a). In this case, the only analog building block is the front-end bulk-input VCRO, while the rest of subcircuits in the ΣΔM can be designed completely in the digital domain. Therefore, the harmonic distortion of the ΣΔM will be mostly dominated by the front-end VCRO – as in the 1st-order ΣΔM. Indeed, the second integrator of the 2nd-order ΣΔM in Fig. 21 can be implemented by using a Digitally-Controlled ring Oscillator (DCO) driven by a counter, as proposed in [17]. The equivalent

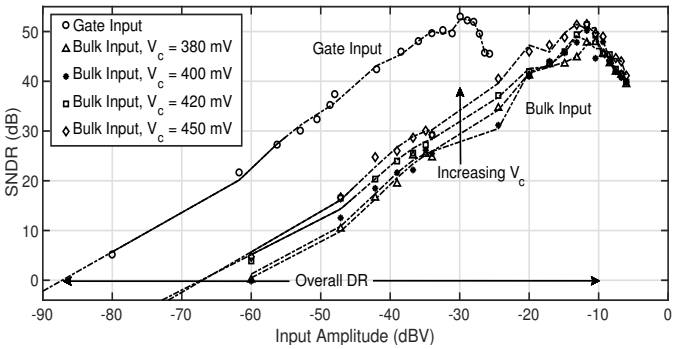

Fig. 20. SNDR vs. input signal of a 1st-order VCO-ΣΔM (BW = 10MHz), considering two cases: input applied at the gate terminal (V_c) and input applied at the bulk terminal (V_{bn}) for different values of V_c.

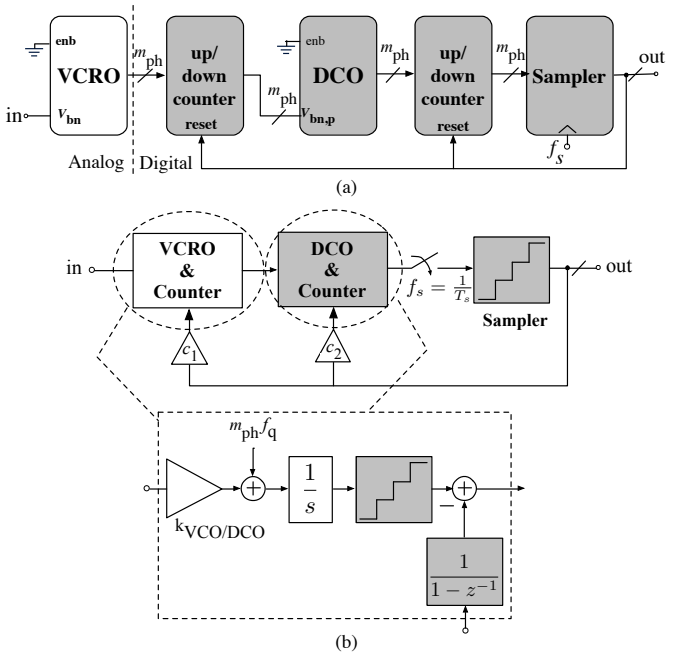

Fig. 21. Bulk-input 2nd-order VCRO-based ΣΔM. (a) Block diagram. (b) Equivalent behavioral model. (The system is implemented in practice using a pseudo-differential topology – not shown here for the sake of simplicity).

system-level model of the 2nd-order VCRO-based ΣΔM is shown in Fig. 21(b). Assuming a linear model for the quantizer blocks and that $c_2 = 2 \cdot c_1/k_{\text{DCO}}$, the analysis of this model yields to an overall Signal Transfer Function (STF) and a Noise Transfer Function (NTF), respectively given by:

$$STF(z) = \frac{k_{\text{VCO}}}{f_s} \cdot z^{-2}, NTF(z) = (1 - z^{-2}) \qquad (27)$$

where $c_1 = 1$ has been assumed. In this case, the phase quantization error of the VCRO, ϕ_1, and the DCO, ϕ_2, are respectively filtered by the following transfer functions:

$$N_{\phi 1} = (1 - z^{-1}) \cdot z^{-1}, N_{\phi 2} = \frac{(1 - z^{-1})^2}{k_{\text{DCO}}} \qquad (28)$$

The modulator in Fig. 21 has been designed in a 28-nm FD-SOI technology in order to validate the use of bulk-input VCROs to improve the linearity in these kinds of ΣΔ ADCs. Fig. 22 shows a transistor-level simulation of the output

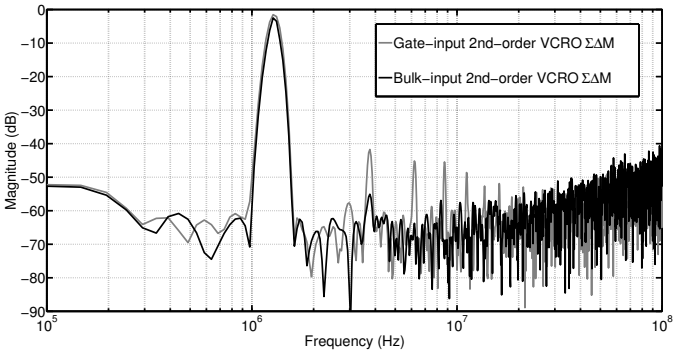

Fig. 22. Output spectra of the 2nd-order VCRO-based $\Sigma\Delta$M clocked at $f_s = 1.6$GHz for both bulk- and gate-input signal.

spectrum of the 2nd-order $\Sigma\Delta$M for $f_s = 1.6$ GHz and a full-scale 1.24-MHz input sinewave[7]. It is shown how the use of bulk-input VCROs allow to drastically improve (up to 3-bit) the THD as compared with conventional VCROs–controlled by the gate voltage, V_c. In this design example, an effective resolution of 10-bit can be achieved for a 10-MHz signal bandwidth, with an estimated power consumption of 230μW in both gate- and bulk- input cases.

VI. Conclusion

The effect of using body (bulk) terminal of MOS transistors as the input signal of analog circuits integrated in FD-DOI CMOS has been analysed in this paper with the objective of improving the linearity performance of some analog and mixed-signal circuits and systems. The analysis of basic building blocks – such as differential pairs, CMOS switches, voltage-controlled ring oscillators – and time-based ADCs, such as VCO-based $\Sigma\Delta$ modulators – reveals that the enhanced tuning of the threshold voltage provided by FD-SOI CMOS, and its linear dependence on the back-gate voltage, results in an improved performance in terms of linearity with respect to conventional (gate-input) circuit techniques. Theoretical analyses carried out in this work are confirmed by transistor-level simulations of several circuits and systems designed in a 28-nm FD-SOI CMOS technology. These results open the doors for using the presented circuit techniques in analog and mixed-signal systems integrated in deep nanometer processes, and very specially in those applications in which linearity is one of the main limiting specifications.

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