Internally compensated LDO regulator based on the Cascoded FVF

J.M. Hinojo[a], C. Luján-Martínez[a], A. Torralba[a] and J.Ramírez-Angulo[b]

[a]*Electronic Engineering Department, University of Seville, Seville 41092, Spain, {jose.hinojo, clara.lujan,torralba}@gie.esi.us.es*
[b]*Klipsch School of Electrical Engineering, New Mexico State University, Las Cruces 88003-0001, USA, jramirez@nmsu.edu*

Abstract

In this paper, an internally compensated low dropout (LDO) voltage regulator based on the Flipped Voltage Follower (FVF) is proposed. By means of capacitive coupling and dynamic biasing, the transient response to both load and line variations is enhanced.. The proposed circuit has been designed and fabricated in a standard 0.5µm CMOS technology. Experimental results show that the proposed circuit features a line and a load regulation of 132.04 µV/V and 153.53 µV/mA, respectively. Moreover, the output voltage spikes are kept under 150 mV for a 2V-to-5V supply variation and for 1mA-to-100mA load variation, both in 1µs.

Keywords: Energy harvesting; Flipped Voltage Follower (FVF); Low Dropout (LDO); Low-power; Low-voltage

1. Introduction

Power management in integrated circuits (ICs) has become a key research area in both, battery powered and energy harvesting applications, as a consequence of the limited amount of available energy. Power management goes beyond turning off a part of the system when it is not required. It is critical in autonomous devices such as those used in wearable electronics and wireless sensor networks, where the source of energy suffers from extremely high variations. In this sense, low dropout (LDO) regulators have shown to be essential blocks as they generate a regulated voltage with low quiescent consumption under large variations of load and input voltage.

A LDO is a linear voltage regulator that operates with a high efficiency thanks to a small input-output voltage difference. An internal compensation of LDOs is usually preferred, as it does not require external capacitors, reducing size and cost. In the last few years, a number of different techniques have been proposed to increase the stability of internally compensated LDOs and to enhance their transient response. Miller compensation results in highly stable LDOs with fast transient response, however, the required area of the Miller capacitor is usually significant in comparison with the total area of the chip. In [1], [2], current amplifier Miller compensation is used, reducing the total compensation capacitance but increasing the power consumption and the complexity of the design. The so-called damping-factor-control (DFC) technique, which was initially proposed to compensate multistage amplifiers driving heavy capacitive loads, has been recently used to compensate a LDO [3], [4]. The DFC block allows controlling the damping factor of the complex pole pairs of the system avoiding the peak of resonance, which is responsible for instability.

On the other hand, different techniques have been proposed in the literature to improve the transient response of LDOs. In [5] and [6], a high slew-rate push-pull output amplifier was used to charge/discharge rapidly the pass transistor gate capacitance resulting in a small settling time under variations of the load current. However, no enhancement is achieved in the transient response for input voltage (V_{IN}) variations.

Another solution uses a fast self-reacting loop that allows rapidly drive the power transistor to regulate the output voltage [7]. In this case, three different paths are added to vary the voltage at the gate of the pass transistor when I_{LOAD} changes. In [8] and [9] the Flipped Voltage Follower (FVF) [10] was identified as core cell for LDO design. The good performances of this cell as a current buffer and its low output impedance make it a highly efficient LDO regulator according to load regulation. However, its response due to input voltage variations is limited by the biasing currents, which are responsible for the charge/discharge of the gate parasitic capacitance of the pass transistor. Thus, there is a trade-off between power consumption and transient response.

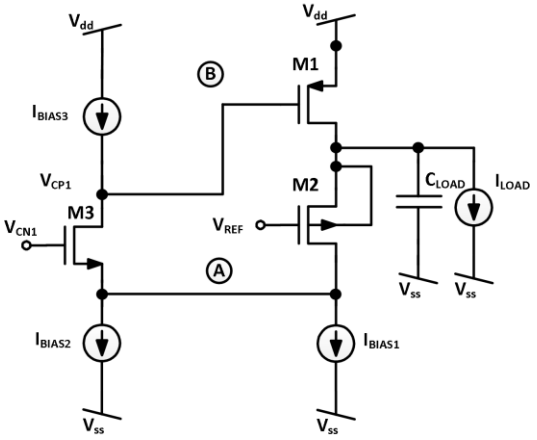


Fig. 1. Structure of the cascoded FVF.

Further work on this structure has been done creating a path that couples the changes variations in the output voltage V_{OUT} to the gate of the pass transistor [12]. This technique can be used to improve both, the line and load transient responses, and can be implemented in a simple way by means of RC coupling.

In this paper, an FVF-based LDO regulator, which uses the cascoded version of the FVF, is proposed which improves line regulation and transient behaviour of existing implementations based on this cell. The proposed regulator uses RC coupling to solve the transient problems of the circuits in [8] and [9] for input voltage variations without a significant increase in the quiescent power consumption. The organization of this paper is as follows: section 2 describes the structure and principle of operation of the proposed structure; section 3 analyses its stability; and in section 4, measurements of the proposed LDO regulator designed in a standard 0.5µm CMOS technology are presented. Finally, some conclusions are drawn in section 5.

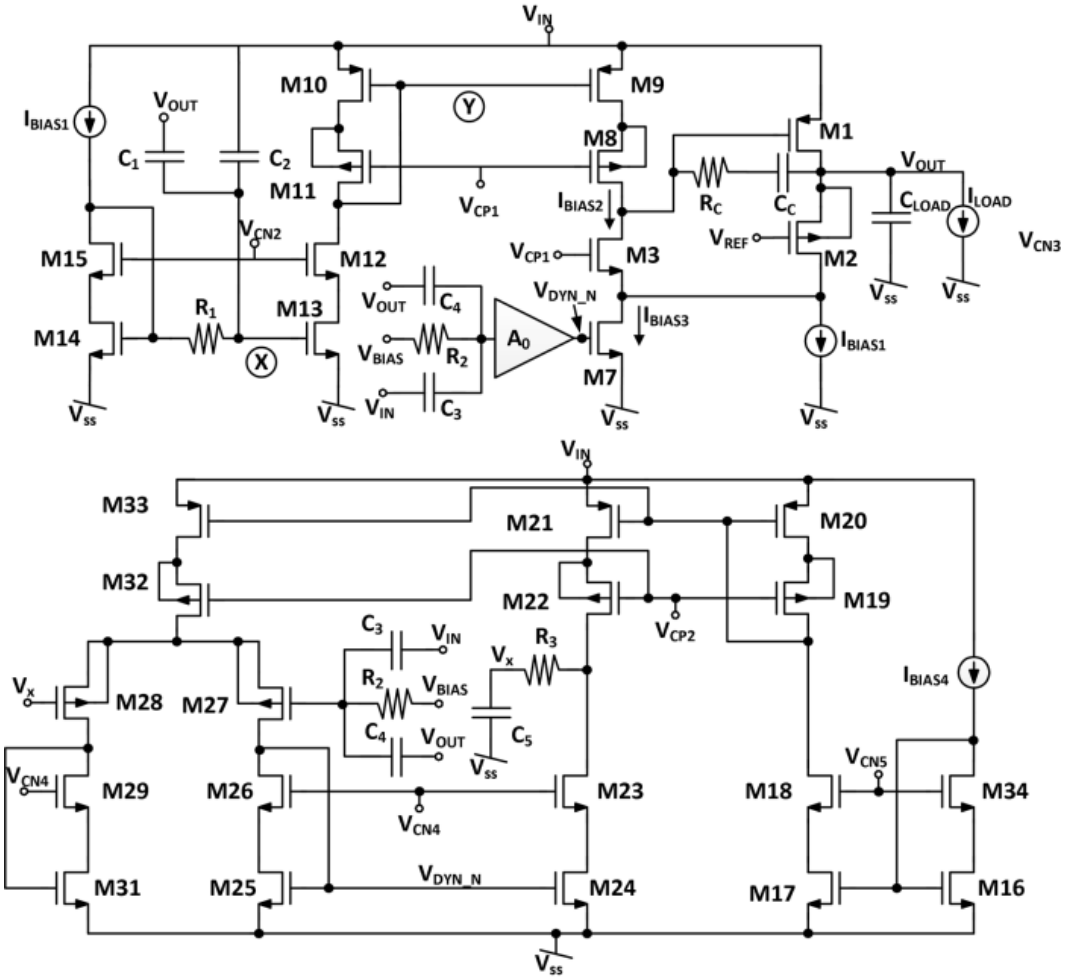


Fig. 2. Structure of the proposed LDO. (a) Core of cirtcuit. (b) Differential amplifier.

2. Structure and principle of operation

The proposed structure is based on the cascoded FVF (Fig. 1), whose core consists of transistors M1-M3. Specifically, M1 is the pass transistor and it is responsible for providing the current to the load (I_{LOAD}). M2 acts as an error amplifier, which compares the output of the LDO with the reference voltage (V_{REF}). Node A tends to follow the variations in V_{OUT} because of the current flowing through transistor M2 is fixed by I_{BIAS1}. As a result, these variations are amplified by the transconductance of the M2 and they are coupled to the node B. In this way, the parasitic capacitor of the pass transistor gate is charged or discharged to cope with changes in I_{LOAD}.

As stated in the introduction, the main disadvantage of the structure in Fig. 1 is its slow transient response. This is limited by biasing currents I_{BIAS2} and I_{BIAS3} which are responsible for charging/discharging the parasitic capacitance at node B. This limitation leads to large output variations. In order to improve the transient response of the circuit, I_{BIAS2} and I_{BIAS3} are replaced by dynamic current sources dependant on the input and output voltages as shown in Fig.2a. For this circuit, if voltage V_{IN} rises, node X instantaneously tends to increase its voltage, producing an increase of the current in M13 and, hence, in I_{BIAS2} which allows a fast charge of the gate parasitic capacitance of M1. In addition, the output voltage is coupled to magnify this effect taking advantage of the instantaneous rise of V_{OUT} with V_{IN}. To obtain a symmetrical response, a similar procedure is done with I_{BIAS3} but this time in addition to the RC coupling an inverting differential amplifier (Fig. 2b) is needed to increase the current in M24 and, thus, in I_{BIAS3} when V_{IN} decreases. This time a fast discharge of the gate parasitic capacitance of M1 is obtained.

The values of C1, C2, R1 and C3, C4, R2 have been calculated in order to maximize gate voltage variations of transistors M13 and M27, respectively. The values of resistors are large enough to establish the correct DC voltages in V_X and in the gate of M27. For these values of resistors, capacitors C1 and C3 are calculated to achieve the appropriate increment of the biasing current (1). In this equation, R represents R1 or R2, ΔV_{GATE} is the gate voltage variation of M13 and M27 required to generate the dynamic biasing currents I_{BIAS1} and I_{BIAS3}. ΔV_{IN} is the variation suffered by the supply voltage at a defined time interval, Δt.

$$C = -\frac{R}{\Delta t}\ln\left[1-\frac{\Delta V_{gate}\cdot\Delta t}{\Delta V_{in}}\right] \tag{1}$$

Note that, in the differential pair, the voltage at of the gate of transistor M27 is compared to a reference V_X which is generated from M21-M24 transistors, avoiding the need for an external reference voltage. C5 and R3 have been calculated to stabilize the reference voltage V_X against fast V_{IN} and/or I_{LOAD} variations.

3. Stability analysis

This section deals with the stability analysis of the proposed LDO. The mayor concern is the stability of the overall control loop for changes in the load, especially for low current loads when the non-dominant poles get closer to the dominant one. The non-dominant pole, which depends on R_{OUT} and C_{LOAD}, approaches the Unity Gain Frequency (UGF) when I_{LOAD} is reduced due the increase of to the equivalent output resistance. Therefore, the phase margin is drastically reduced. Miller compensation with series resistor has been used to achieve a proper phase margin in the whole range of loads (R_C is 1kΩ and C_C is 20 pF). These values represent an effective area of 0.0365 mm^2, which is negligible, compared to the occupied area of M1. An expression for R_C is given in (2). The Miller capacitor is calculated from the requirements of Phase Margin (PM) as seen in expression (3), where GBW stands for Gain-Bandwidth product, and gm_x is the ac transconductance of transistor M_X.

$$R_C \approx \frac{1}{gm_{pass}\Big|_{I_{LOAD}^{\min}}} \tag{2}$$

$$PM \approx 90^{\circ} - \tan^{-1}\left(\frac{GBW}{p_2}\right) + \tan^{-1}\left(\frac{GBW}{z_2}\right) \tag{3}$$

Note that the effect of RC coupling and the differential amplifier can be neglected in this study, as the poles introduced by these elements are located at a very high frequency. Considering these simplifications, the open loop response can be approximated by the expression (4) with poles and zeros given by expressions (5)-(8)

$$H(s) = A_0 \frac{\left(1+\frac{s}{z_1}\right)\left(1+\frac{s}{z_2}\right)}{\left(1+\frac{s}{p_1}\right)\left(1+\frac{s}{p_2}\right)} \tag{4}$$

$$z_1 \approx \frac{gm_1}{C_{gd,1}} \tag{5}$$

$$z_2 \approx \frac{1}{R_C C_C} \tag{6}$$

$$p_1 \approx -\frac{1}{\left[\left(R_{b3} \| \left(r_{o3} + \left(1+gm_3 r_{o3}\right)\right)\right)\left(R_{b2} \| R_{b1} \| \left(r_{o2} + \left(1+gm_2 r_{o2}\right)\right) \cdot r_{o1}\right)\right] \cdot \left[C_{gs1} + C_{gb1} + \left(1+gm_1 r_{o1}\right) \cdot C_{gd1} + C_{db3} + C_{gd3} + C_C\right]} \tag{7}$$

$$p_2 = \frac{1}{\left[r_{o1} \| R_{LOAD} \| \frac{\left[r_{o2} + R_{B1} \| R_{B2} \| \left[\frac{r_{o3} + R_{B3}}{1+g_{m3} r_{o3}}\right]\right]}{1+g_{m2} r_{o2}}\right]\left[C_{LOAD} + C_{gs1} + C_{gb1} + C_{gd1} + C_{db1}\right]} \tag{8}$$

In Fig. 3 post-layout simulations of the open loop response at different load conditions (100 µA, 1 mA, 10 mA, and 100 mA) are shown. In every case the value of load capacitor is 100 pF, which is our worst-case condition. Note that the proposed LDO is stable in the whole range of operation and the achieved loop gain is as high as expected due to the use of cascode current mirrors.

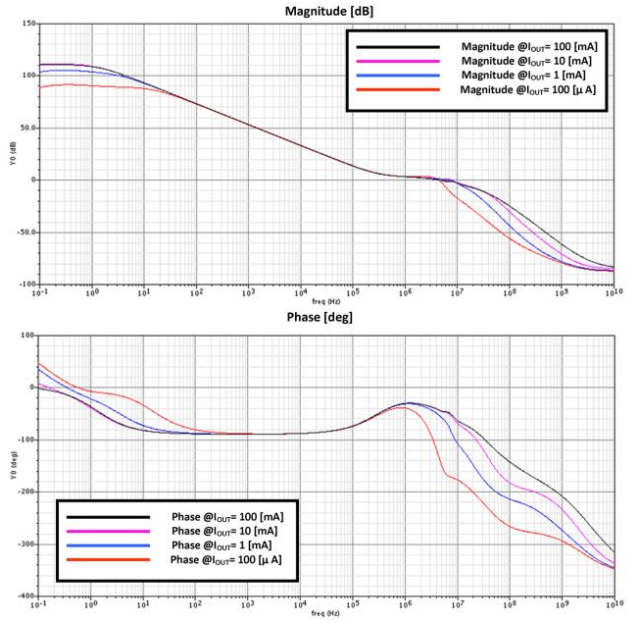


Fig. 3. Simulated loop gain response of the proposed LDO with C_{LOAD}=100pF and I_{LOAD} varying between 0.1 mA and 100 mA.

Table 1 Gain and phase margin for different load conditions

I_{LOAD} (mA)	Gain (dB)	Phase margin (degrees)	I_{LOAD} (mA)	Gain (dB)	Phase margin (degrees)
100	71.44	122.6°	1	99.85	110.3°
10	98.71	131.8°	0.1	88.69	51.32°

4. Measurements

The proposed circuit has been implemented in a standard 0.5 µm CMOS technology using the aspect ratios of the transistors given in Table 2. The micrograph of the LDO is shown in Fig. 4 with a total chip area of 706.95 µm x 1068.15 µm. Note that the area occupied by R_C and C_C is negligible when compared to the pass transistor. The LDO was designed to drive a maximum current load of 100 mA with a variable load capacitance in the range 0-100 pF. Measurements for DC, for transient line and load responses are shown from Fig. 5 to Fig. 7, respectively.

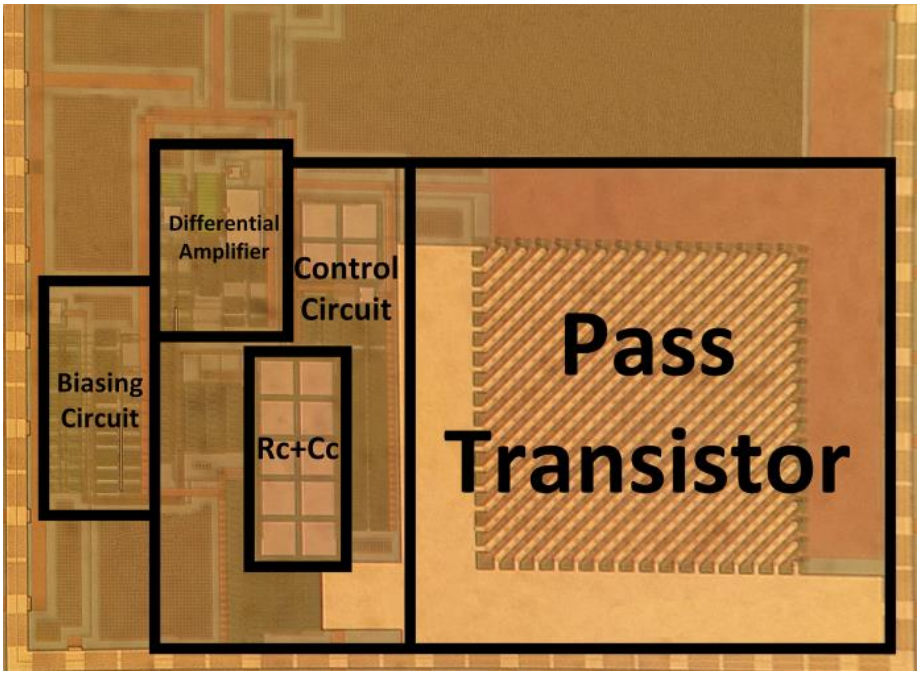


Fig. 4. Microphotograph of the circuit

Table 2. Transistor aspect ratios

Transistor	Size (µm/µm)
M1	25050/0.6
M2	1044.9/0.9
M3	348.3/0.9

In Fig. 5, the measured DC characteristic is shown. The input voltage changes from 0V to the maximum allowed value for the technology and from that value to 0V under I_{LOAD}=100 mA and C_{LOAD}=100 pF conditions. Note that the output voltage remains constant and equal to its nominal value for an input voltage greater than 1.95 V.

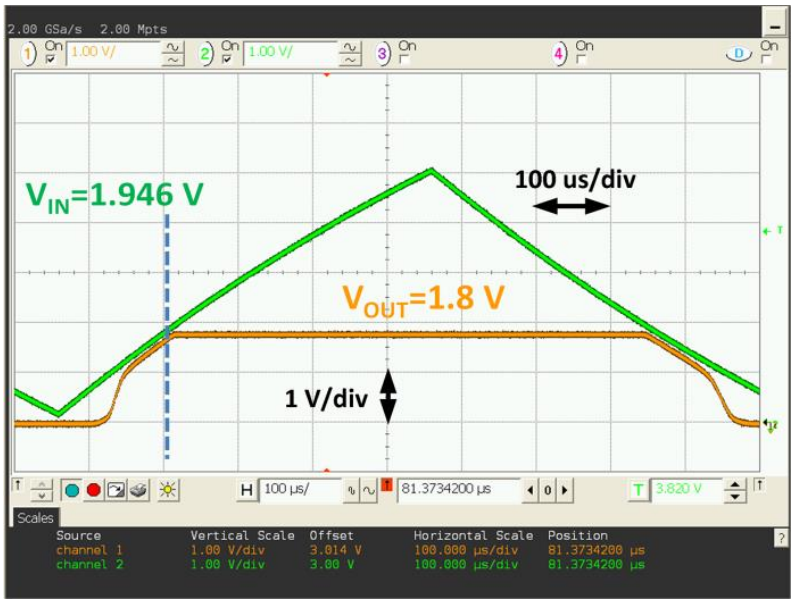
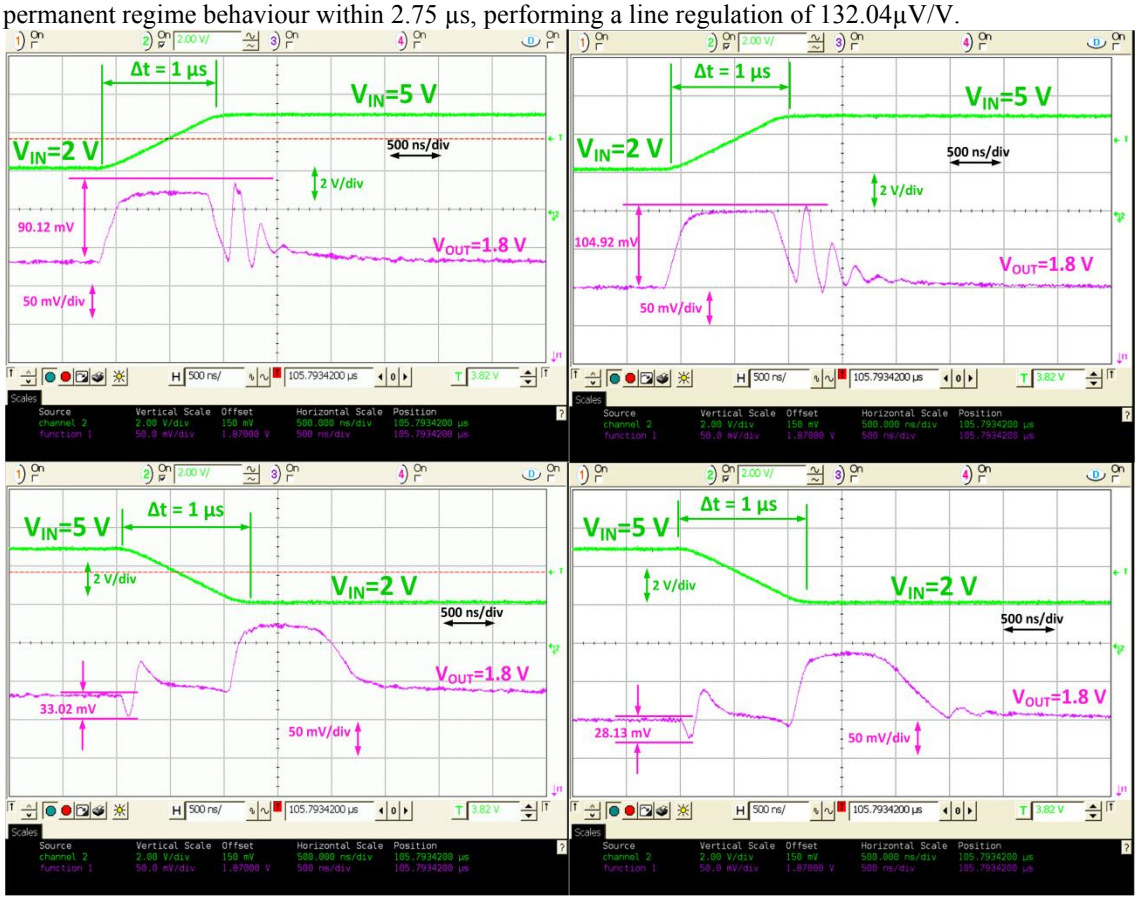


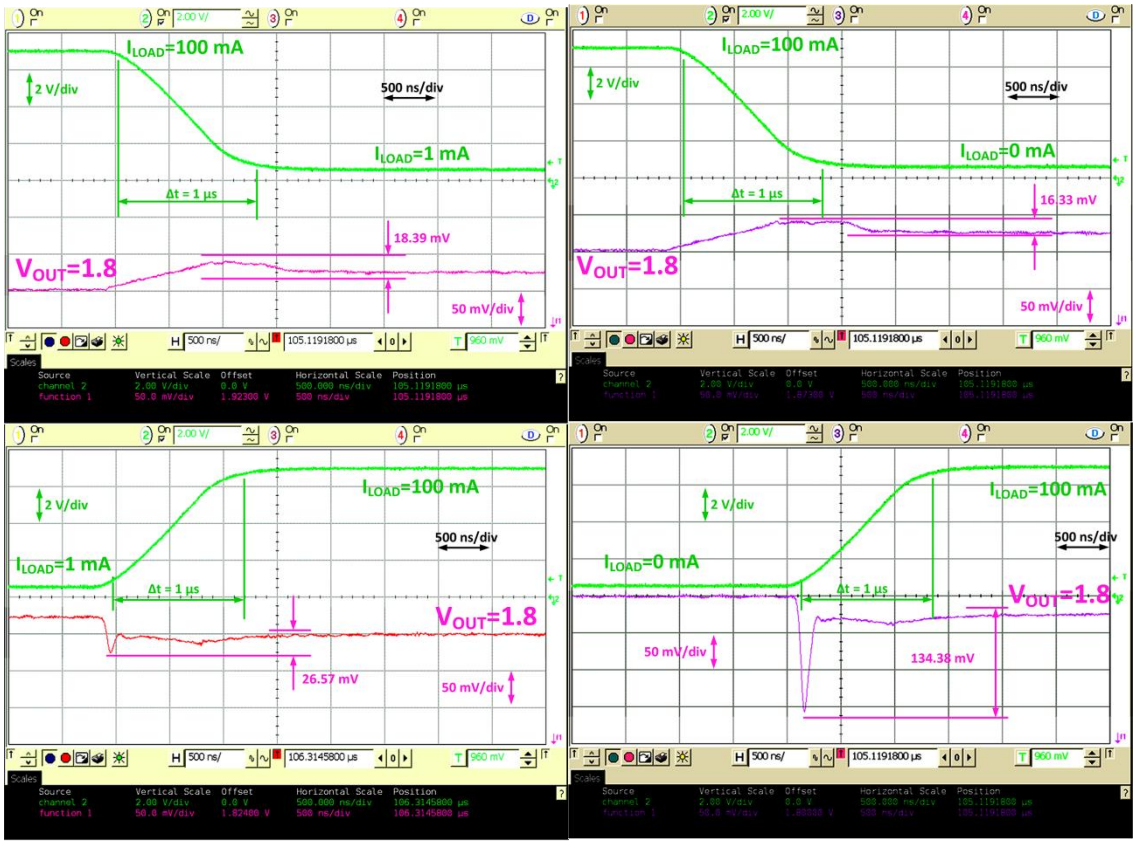
Fig. 5 Measured DC characteristic.

Fig. 6 depicts the line transient response for I_{LOAD}=1 mA and I_{LOAD}=100 mA with C_{LOAD}=100 pF varying V_{IN} from 2 V to 5 V and vice versa. In both cases, the rise and fall times for V_{IN} are 1 µs. Measurements shows a maximum overshoot of 104.92 mV and undershoot of -33.02 mV achieving permanent regime behaviour within 2.75 µs, performing a line regulation of 132.04µV/V.



(a) (b)

Fig. 6. Measured line transient response with C_{LOAD}=100 pF and V_{IN} varying between 2 V and 5 V. (a) I_{LOAD}=1 mA. (b) I_{LOAD}=100 mA.



(a) (b)

Fig. 7. Measured load transient response with CLOAD=100 pF (a) 100 mA to 1 mA.(b) 100 mA to 0 mA

On the other hand, load transient response tests (Fig. 7) have been performed for an equivalent load capacitance of 100 pF and for load current variations from 1 mA to 100 mA, 100 mA to 1 mA, 0 to 100 mA and 100 mA to 0 with a rise and fall time of 1µs in both cases. The proposed circuit performs a maximum undershoot of -134.38 mV and overshoot of 16.63 mV within 2.5 µs, performing a load regulation of 4.06 µV/mA. Any discrepancy between this value and the one depicted in Fig. 7 is due to the parasitic resistance of the output path and wire bonding which is around 190 mΩ in our packaging.

From previous results, it can be demonstrated that the proposed architecture solves the problems of the large overshoots and undershoots for changes in V_{IN} providing good line and load regulation.

Table 3. Summary of performance

Parameter	Proposed LDO
V_{DD} [V]	2-5
V_{OUT} [V]	1.8
Dropout [V]	0.2
I_{LOAD} [mA]	100 mA
$I_{QUIESCENT}$ [µA]	78.21
Efficiency at $I_{LOAD,max}$	90.0%
C_{LOAD} [pF]	0-100
Area [mm2]	0.7
ΔV_{OUT} by varying V_{IN} (*)	
• Maximum [mV]	104.92
• Minimum [mV]	-28.13
ΔV_{OUT} by varying I_{LOAD} (*)	
• Maximum [mV]	16.33
• Minimum [mV]	-134.38
Line regulation [µV/V] (*)	132.04
Load regulation [µV/mA] (*)	4.06

Table 3 summarizes the performances of the proposed regulator, while Tables 4 and 5 show comparison with other reported LDO regulators. In addition, Table 5 offers a comparison of the previous references and the proposed LDO under the same test conditions.

From Table 4, it can be concluded that the proposed structure shows a load and line regulations in the state of the art. In order to evaluate the performance of different designs, the figure of merit (FOM) proposed in [13] is used. It is given by (9), where T_r is the response time and it is defined by (10). The smaller FOM value, the better is the performance metric. As it can be observed in Table 4, the proposed LDO achieves FOM close to state of the art. In addition, according to Table 5, the structure also shows similar performances in terms of output variation for input variations.

$$FOM = T_r \frac{I_q + I_{LOAD,\min}}{I_{LOAD,\max}} \tag{9}$$

$$T_r = \frac{C_{OUT}\Delta V_{OUT}}{I_{LOAD,\max}} \tag{10}$$

Note that, when compared to the rest of LDOs reported in the literature, the proposed circuit occupies a larger silicon area. However, when only active area is considered, this value is reduced to 0.36 mm2. Furthermore, the pass transistor of the proposed structure was oversized. Simulation results show that the area of the pass transistor could be reduced up to 40% with no significant degradation in the LDO performances, so that the total area of the circuit could be reduced to 0.43 mm^2.

Table 4. Comparison of recently published LDO regulators

Parameter	[2]	[5]	[6]	[7]	[8]	This work
Technology [µm]	0.35	0.18	0.35	0.35	0.35	0.5
Input range V_{IN} [V]	3	1	2.5-4	1.642-5	1.2-1.5	2-5
Output range V_{OUT} [V]	2.8	0.9	2.35	1.5	1	1.8
Dropout [V]	0.2	0.1	0.15	0.142	0.2	0.2
I_{LOAD} max [mA]	50	50	100	100	50	100
Quiescent current consumption [µA]	65	1.2	7	27	95	78.21
Efficiency at $I_{LOAD,max}$	93.21%	90.0%	-------[c]	91.33%	83.18%	90.0%
C_{LOAD} [pF]	0-100	100	0-100	0-100	0 -10 [µF]	0-100
Area [mm2]	0.29	0.09	0.064	0.2	0.0448	0.7
Settling time[a] [µs]	15	~4	~0.15	-	~5	~2.5
ΔV_{OUT} by varying V_{IN}[b]						
• Maximum [mV]	85	200	176	6.5	-	104.92
• Minimum [mV]	-12	-130	-190	-4	-	-28.13
(ΔV_{OUT} /Excitation rise time) [V/µs]	1/1	0.5/1	0.5/0.5	1/5		3/1
ΔV_{OUT} by varying I_{LOAD}[b]						
• Maximum [mV]	90	300	236	5	125	16.33
• Minimum [mV]	-90	-400	-227	-25	-150	-134.38
(ΔI_{LOAD}/Excitation rise time) [mA/µs]	50/1	49.95/0.1	99.95/0.5	100/1	50/0.2	100/1
Line regulation[b] [µV/V]	-	3625	1000	1046	18000	132.04
Load regulation[b] [µV/mA]	-	148	80	75.2	280	4.06
Open loop gain [dB]	55-62	-	-	-	50-60	71.44-99.85
Phase margin[b] [deg]	>50	-	>45	-	>60	>51.32
FOM [ps]	0.468	1.40	2.64	0.00810	1.045	0.118

[a]This time has been calculated as the setting time to reach 0.1% of V_{OUT}.

[b]Worst-case

[c]This value has not been calculated due to authors do not provide enough information.

Table 5 Comparison under the same test conditions

Para-meter	[2]	This Work	[3]	This Work	[4]	This Work	[5]	This Work	[6]	This Work	[7]	This Work	[8]	This Work
V_{IN}	+85 -128	+18.87 -15.32	+175 -1	+9.68 -13.54	- -	- -	+200 -130	+23.4 -23.7	+176 -190	+21.29 -21.33	+6.5 -4	+4.04 -4.19	- -	- -
I_{LOAD}	+90 -90	+24.19 -122.58	+100 -85	+14.19 -37.9	+35 -35	+18.45 -150.0	+300 -400	+18.45 -159.67	+236 -227	+23.5 -201.9	+5 -25	+18.55 -150.1	+125 -150	+14.19 -201.9

5. Conclusions

In this paper a new LDO regulator based on the cascoded version of the FVF cell has been proposed. It has been designed in a standard 0.5µm CMOS technology. The drop-out voltage is very low (lower than 0.2V), and the DC power consumption of the driving circuitry is 78.21 µA achieving a 90% efficiency and a FOM in the state of the art. Moreover, the quiescent power consumption is constant with independency of the I_{LOAD}.

Acknowledgments

This work has been financed by the Spanish Ministry of Economy and Competitiveness, under project TEC2011-28724-C03-01, and by the Andalousian "Consejería de Economía, Innovación y Ciencia", under project TIC-6323.

References

[1] G. Giustolisi, G. Palumbo, and E. Spitale, LDO compensation Strategy based on current buffer/amplifier, in: Proc. of the European Conference on Circuit Theory and Design, ECCTD (2007)

[2] R. Miliken, J. Silva-Martinez, and E. Sánchez-Sinencio, Full On-Chip CMOS Low-Dropout voltage regulator, IEEE Transactions on Circuits and Systems I: Regular Papers 54 (9) (2007) 1549-8328

[3] Ka Nang Leung and P. Mok, A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation, IEEE Journal of Solid-State Circuits 38 (10) (2003) 1691-1702

[4] Sai Kit Lau, P. K. T. Mok, and Ka Nang Leung, A low-Droput Regulator for SoC with Q-Reduction, IEEE Journal of Solid-State Circuits 42 (3) (2007) 658-664

[5] Tsz Tin Man, P. K. T. Mok, and Mansun Chan, A High Slew-Rate Push-Pull Output Amplifier for Low-Quiescent Current Low-Dropout Regulators With Transient Response Improvement, IEEE Transactions on Circuits and Systems II: Express Briefs 54 (9) (2007) 1549-7747

[6] Xin Ming, Qiang Li, Ze-kun Zhou, and Bo Zhang, An Ultrafast Adaptively Biased Capacitorless LDO with Dynamic Charging Control, IEEE Transactions on Circuits and Systems II: Express Briefs 59 (1) (2012) 40-44

[7] Chia-Min Chen and Chung-Chih Hung, A Fast Self-Reacting Capactior-less Low-Dropout Regulator, in: Proc. Of the European Solid State Circuits Conference, ESSCIRC (2011) 375-378

[8] Tsz Yin Man, Ka Nang Leung, Chi Yat Leung, P.K.T. Mok, and Mansun Chan, Development of Single-Transistor-Control LDO based on Flipped Voltage Follower for SOC, IEEE Transactions on Circuits and Systems I: Regular Papers 55 (5) (2008) 1392-1401

[9] Hua Chen and Ka Nang Leung, A fast-transient LDO based on buffered Flipped Voltage Follower, in: Proc. Of the IEEE International Conference of Electron Devices and Solid-State Circuits, EDSS (2010).

[10] R. G. Carvajal, J. Ramirez-Angulo, A. J. López-Martín, A. Torralba, J. A. G. Galan, A. Carlosena, and F. M. Chavero, The flipped voltage follower: a useful cell for low-voltage low-power circuit design, IEEE Transactions on Circuits and Systems I: Regular Papers 52 (7) (2005) 1276-1291

[11] J. Ramirez-Angulo, S. Gupta, I. Padilla, R. G. Carvajal, A. Torralba, M. Jimenez, and F. Munoz, Comparison of conventional and new flipped voltage structures with increased input/output signal swing and current sourcing/sinking capabilities, in: Proc. The 48th Midwest Symposium on Circuits and Systems, MWSCAS 2 (2005) 1151-1154

[12] Pui Ying Or and Ka Nang Leung, An output-capacitorless low-dropout regulator with direct voltage-spike detection, IEEE Journal of Solid State Circuits. 45 (2) (2010) 458-466

[13] Harish Valapala and Paul M. Furth, Analysis and Design of Fully Integrated Very Low Quiescent Current LDOs, in IEEE 55th International Midwest Symposium on Circuits and Systems, MWCAS (2012) 230-234