Trabajo Fin de Máster
Máster Universitario en Sistemas de Energía Eléctrica

# Advanced Non-Inverting Rogowski Integrator Design for SMART Tokamak Current Measurement

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**Dpto. Ingeniería Electrónica**
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**Universidad de Sevilla**

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PSFT
Plasma Science and Fusion Technology

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El tribunal nombrado para juzgar el Proyecto arriba indicado, compuesto por los siguientes miembros:

Presidente:

Vocales:

Secretario:

Acuerdan otorgarle la calificación de:

Sevilla, 2023

El Secretario del Tribunal

*A mi familia*

# Agradecimientos

A lo largo de la historia, la investigación ha permitido un avance sin precedentes de las técnicas, conocimiento y habilidades de los seres humanos. En los últimos siglos, el avance de la ciencia, fundamentado en el método científico, ha propiciado un crecimiento exponencial en todos los campos. La cuestión de refutar o no las concepciones inicialmente planteadas es central en este proceso, pero ¿debe ser para el investigador/a su único y principal objetivo? La historia ha dejado patente que la autenticidad de los descubrimientos debe abrazar este principio único, con el fin de desentrañar la verdad inherente a la naturaleza. Así se concibió en los albores de este método, cuando la filosofía y la ciencia coexistían como una entidad única. No obstante, el método científico es meramente una herramienta en manos del investigador, como Carl Sagan solía expresar con elocuencia: «*nuestra pasión por el conocimiento es el instrumento de supervivencia que nos define*».

Mi pasión por aprender no es más que la esencia de hacerme sentirme vivo en el modo que Sagan lo definía como supervivencia. De cerca, personas me han hecho crecer en todo mi trayecto hasta el día de hoy. Agradecer a mi familia el aporte continuo e incondicional de experiencia, emociones y acompañamiento. A Jorge, por su entrega continua y desinteresada de conocimiento y motivación. A los tutores de este trabajo M.ª Ángeles y a Juanma, por introducirme en el mundo de la fusión y darme esta enorme oportunidad. Y al resto de personas que de una forma u otra me han acompañado en esta experiencia de la investigación y las que aún quedan por descubrir.

«*Los pigmeos colocados en los hombros de gigantes ven más que los gigantes mismos*».

*(Robert Burtonen, 1624)*

*Pablo Vicente Torres*

*Sevilla, 2023*

# Resumen

En el último siglo el enorme consumo energético basado en combustibles fósiles ha causado un gran impacto en el medio ambiente. Las energías renovables juegan un papel protagonista en la transición energética. Sin embargo, su alta dependencia de las condiciones climáticas impide que sean la solución definitiva. La entrada de nuevas centrales como base en la matriz energética es unos de los mayores intereses actuales. La fusión nuclear podría ofrecer una solución en este campo, tratándose de una energía que no genera gases de efecto invernadero, no genera residuos radiactivos de vida larga y su combustible es abundante. En las próximas décadas se espera poder tener disponibles plantas de fusión nuclear para la generación comercial con las que generar energía de forma deslocalizada.

La posibilidad de construir reactores de fusión nuclear como fuente de energía desde fue considerada desde mediados el siglo XX. Los reactores de tipo tokamak han permitido realizar numerosos experimentos en este campo. En su aplicación, es necesario un adecuado control sobre el confinamiento del plasma de acuerdo con las restricciones impuestas por el experimento y las restricciones de seguridad a las que está sometida la máquina, ya que fluctuaciones o inestabilidades del plasma ponen en riesgo el funcionamiento normal de la máquina.

Los sistemas de adquisición de datos son responsables de recopilar toda la información en tiempo real de los parámetros en estudio, estos permiten evaluar el estado del plasma y tomar decisiones instantáneas para ajustar los campos magnéticos y otros parámetros del tokamak. Los sistemas desempeñan un papel fundamental en la optimización y estabilización del plasma, así como mantener las condiciones necesarias para que la fusión nuclear ocurra de manera sostenible y eficiente. Además, los datos recopilados son esenciales para investigar y comprender mejor el comportamiento del plasma en condiciones extremas, lo que a su vez contribuye al avance en la investigación de la fusión nuclear como fuente de energía limpia y abundante.

El tokamak SMART requiere nuevos diseños para los sistemas de adquisición y adaptación de señales. Se ha realizado una revisión de la bibliografía existente sobre métodos y arquitecturas de integración de señales y su instrumentación electrónica. Se han construido integradores analógicos para medidas de corriente de plasma en tiempo real, que serán incluidos en los lazos de control que modifican la forma y posición del plasma. Se han definido las características básicas del integrador analógico para su aplicación y se ha reducido el número de componentes activos con respecto a las arquitecturas ya planteadas, ofreciendo una solución más económica y compacta con las mismas prestaciones. Se ha creado un modelo genérico en Matlab y se han realizado simulaciones en LSpice sobre el ancho de banda y el nivel de ruido de un prototipo de circuito. Finalmente, se ha construido la placa de circuito impreso para su instalación y prueba.

# Abstract

In the last century, enormous energy consumption based on fossil fuels has had a huge impact on the environment. Renewable energy plays a key role in the energy transition. However, their high dependence on climatic conditions prevents them from being the definitive solution. The entry of new power plants as a base for the energy matrix is one of the major current concerns. Nuclear fusion could offer a solution in this field, as it is an energy that does not generate greenhouse gases, does not generate long-lived radioactive waste, and is fuel-abundant. Fusion power plants for off-site power generation are expected to become available in the next few decades.

The possibility of building nuclear fusion reactors as a source of energy has been considered since the mid-20th century. Numerous experiments have been conducted in this field with tokamak reactors. In their application, adequate control over the plasma confinement is necessary according to the constraints imposed by the experiment and the safety restrictions to which the machine is subjected, as plasma fluctuations or instabilities put the normal operation of the machine at risk.

Data acquisition systems are responsible for collecting all real-time information on critical parameters, allowing the state of the plasma to be assessed and instantaneous decisions to be made to adjust the magnetic fields and other parameters of the tokamak. These systems have a fundamental role in the optimisation and stabilisation of the plasma, making it possible to maintain the conditions necessary for nuclear fusion to occur sustainably and efficiently. Furthermore, the collected data are essential to investigate and better understand the behaviour of plasma under extreme conditions, which in turn contributes to the advancement of nuclear fusion research as a clean and abundant energy source.

The SMART tokamak requires new designs for signal acquisition and adaptation systems. A review of the existing literature on signal integration methods and architectures and their electronic instrumentation has been conducted. Analogue integrators have been built for real-time plasma measurements, allowing for the creation of control loops that modify the shape and position of the plasma. The basic characteristics of the analogue integrator for its application have been defined, and the number of active components has been reduced compared to the previous architectures, offering a more cost-effective and compact solution with the same features. A generic model has been created in MATLAB and simulations in LSpice on bandwidth and noise level of a circuit prototype. Finally, the PCB is built to be installed and evaluated.

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# Glossary

| | |
|---|---|
| VDE | Vertical Displacement Event |
| TOKAMAK | TOroidal'naya KAmera MAgnitnymi Katushkami |
| SMART | SMall Aspect Ratio Tokamak |
| NBI | Neutral Bean Injection |
| PCS | Plasma Control System |
| RWM | Resistive Wall Mode |
| SISO | Single input single output |
| NTM | Neoclassical Tearing Modes |
| a | Plasma minor radius |
| $R_o$ | Plasma minor radius |
| PS | Power Supply |
| ADC | Analog-Digital Converter |
| SAS | Signal Acquisition Systems |
| OP-AMP | Operational amplifier |
| PWM | Pulse Width Modulation |
| SMA | SubMiniature version A |
| RMS | Root Mean Square |
| PID | Proportional Integral Derivative |
| HIL | Hardware in the Loop |
| $A$ | Aspect ratio |

# 1 INTRODUCTION

## 1.1 Nuclear fusion and fusion reactors

Nuclear fusion of light atomic nuclei to form heavier atomic nuclei is one of the most common nuclear reactions in the universe. The mass deficit results in the release of energy according to Einstein's equation; therefore, the mass of the nucleus is directly related to both its potential energy and its binding energy, the energy needed to disassemble the atomic nucleus into its individual components.

In fusion reactions, two nuclei must overcome the Coulombic interaction (electrostatic repulsion). The particles must come close enough and with enough energy to overcome the electrostatic repulsion between the positively charged nuclei for the fusion reaction to take place.

In the case of stars, because of their enormous mass, the force of gravity is extreme, fusion reactions can occur simultaneously and spontaneously. On Earth, the force of gravity is low and, for fusion to take place, it is necessary to compensate for this fact by heating and compressing the material. The fuel of the fusion reactions (a mixture of Deuterium and Tritium in a D-T reaction) at elevated temperature is in a plasma state; in this case the electrons are separated from the ions, obtaining a fluid with electromagnetic properties.

Under the proper conditions, the products of the D-T reaction are one Helium nucleus ($^4_2He$ ) with a kinetic energy of 3.5 MeV and one neutron ($^1_0n$) with 14.1 MeV represented in Equation (1–1).

$$^2_1D + {}^3_1T \rightarrow {}^4_2He + {}^1_0n + 17MeV \qquad (1–1)$$

Strong magnetic fields contain the plasma at very high temperatures, allowing it to be compressed away from the walls of the vessel. Otherwise, the surface would be damaged by the enormous temperatures. This method is known as magnetic confinement method. The use of powerful lasers to compress a small fuel bullet is known as the inertial method. A conceptual fusion power plant as shown in Figure 1-1, where the thermal energy generated from the fusion reaction is converted into electrical energy through a traditional steam cycle, as a traditional thermal power plant.

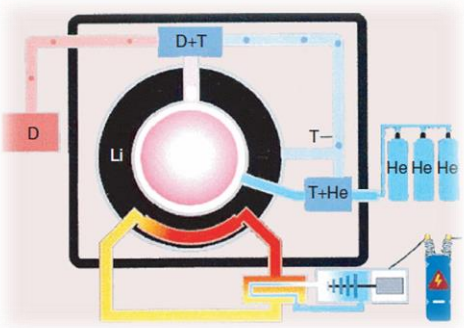



Figure 1-1 : Fusion power plant concept [1]

## 1.2 Magnetic confinement

In nuclear fusion, the D-T mixture in plasma state can be confined, as mentioned in the previous section, through strong magnetic fields that keep the plasma away from the surface of the tank. The main characteristics of this technique will be described in this section.

Magnetic confinement makes it possible to contain and maintain plasma at extremely high temperatures in a controlled medium, where the nuclei can fuse and release the massive amount of energy. There are two main topologies for achieving magnetic confinement: tokamaks and stellarators. Tokamaks are toroidal-shaped magnetic confinement devices that use a strong toroidal magnetic field combined with a poloidal magnetic field to keep the plasma in a circular trajectory. However, stellarators are more complex devices that employ helical magnetic fields to achieve plasma stability.

The **TOKAMAK** (**TO**roidal'naya **KA**mera **MA**gnitnymi **K**atushkami) is the most investigated technology for fusion reactors. A summary of their parts is described in Figure 1-2. This device was devised by Soviet physicists in the 1950s. The inaugural tokamak, known as T-1, began operation in 1958. By the mid-1960s, tokamak designs began to demonstrate markedly superior performance. Promising results attracted further investment, leading to the development of larger devices such as the JET, JT-60, and TFTR in the 1980s. The largest example of public project investment is with ITER (International Thermonuclear Experimental Reactor), with a capital budget of more than 24 billion euros, it will start operations in 2025 [2]. Recently, private sector investments have formed private companies along the same lines, such as **C**ommonwealth **F**usion **S**ystems (CFS), funded in 2018 with an investment of $1.8 billion according to The Wall Street Journal [3].

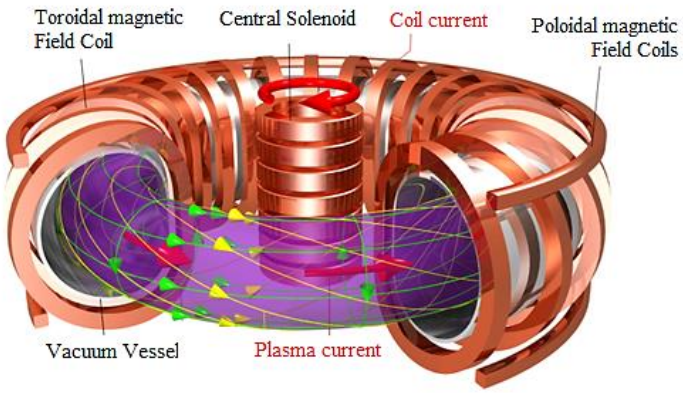



Figure 1-2 : Archetype of a tokamak structure [4]

The basic structure of a tokamak is usually composed of the same elements:

- **Toroidal magnetic Fiel Coils:** its main function is to confine the plasma, as it is the major component of the magnetic field in a tokamak.
- **Poloidal magnetic Field Coils:** the poloidal field generated by the coils is perpendicular to the main toroidal magnetic field created by the toroidal coils (next point), critical to control and stabilise the plasma, as well as its shape, position, and possible parasitic currents mitigations.
- **Central Solenoid**: like the primary of a transformer, the solenoid induces an electromotive force that initiates and maintains the plasma current producing a poloidal magnetic field. The slope of its current makes it possible to modify the plasma current. It is constituted by an air core in order to avoid saturation regimes.
- **Vacuum Vessel:** The plasma generated is housed inside, it is the physical tank, the interior of which is under ultra-high vacuum and is usually made of non-ferromagnetic materials. It is used as a chassis for auxiliary elements and must support important loads, materials such as Stainless Steel (SS) - 316 are normally used.

The topology of the vacuum vessel is closely related to the plasma shape to be obtained. The tokamaks are

classified according to the ratio between their major and minor radii, described in Figure 1-3. The minor radius is defined as the distance between the centre of the plasma and its surface. The major radius is defined as the distance between the centre of the plasma and the axis of revolution. They are classified as: low aspect ratio (spherical tokamak) and large aspect ratio (standard tokamak), they are described in Figure 1-3.

The spherical topology allows for greater simplicity of parts and maintenance. The natural elongation shape (without shaping fields) of the plasma makes it less susceptible to vertical instabilities. The more compact design makes the use of external magnetic fields more efficient [5], [6]. Projects like Spherical Torus Experiment (STX) previously known as START, ST-40, NSTX-U or Pegasus have contributed to the testing of spherical tokamaks. In Spain, **SMART** (**SM**all **A**spect **R**atio **T**okamak) is being built, it is described in the next Section 2. It is a compact design tokamak that aims to obtain different plasma geometries that were not previously studied in this tokamak topology [7].

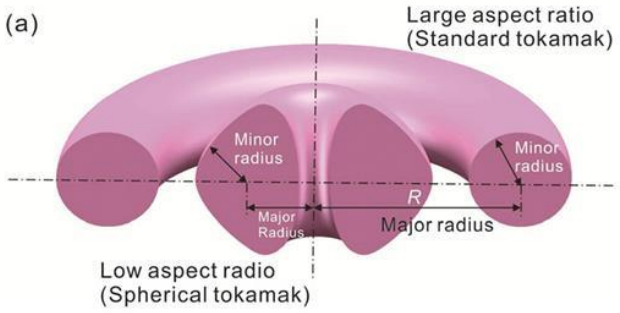



Figure 1-3 : Topology comparison of tokamaks: spherical and standard [4]

Once the general parts of a tokamak have been outlined, it is necessary to define other parts or elements that have to be considered for their operation. First, a power supply is needed to generate and control the huge currents (>1 kA ) flowing through each of the coils to generate the required magnetic fields. Obtaining an ultra-high vacuum ($10^{-10}$ Torr) inside the chamber is essential for successful operation. On the other hand, it is possible to increase the plasma temperature by means of the ohmic effect and the use of the central solenoid, but this technique is not sufficient and, for this purpose, radio frequencies, such as microwaves (~kW) or high energy particle injections with the Neutral Bean Injection (NBI) are used.

## 1.3 Tokamak plasma control

The hot ionised gas (plasma) is confined inside of the vessel for a specific period to facilitate the fusion reactions. A combination of externally applied toroidal and poloidal magnetic fields, together with a poloidal magnetic field generated by a substantial current flowing within the plasma itself, is used to contain this ionised gas away from the vessel walls. The synchrony between the solenoid, coils, fuel control, and NBI enables plasma regimes to be achieved according to the case studies.

The 2D position control is a basic control in the poloidal plane, where the magnetic field generated by the poloidal coils is adjusted in combination with the current induced by the solenoid to adjust the plasma to the required position and shape. It is one of the most simple and primary controls, and it will be described in the following section.

### 1.3.1 Plasma current control

The central solenoid, as described before, generates an electromotive force that establishes the plasma current. There is consequently a correlation between the voltage applied to the solenoid ($V_c$) and the plasma current obtained ($I_p$). Values such as inductance ($L_c$) and resistance ($R_c$) of the solenoid and the plasma ($L_p, R_p$) as well as their mutual inductance ($M_{pc}$) are values which influence according to the next transfer function SISO presented in Equation (1–2).

$$\frac{I_p(s)}{V_c(s)} = \frac{M_{pc}s}{M_{pc}^2 s^2 - (L_c s + R_c)(L_p s + R_p)} \quad (1–2)$$

### 1.3.2 Radial and vertical position control

The plasma changes its geometry and position because of the interaction of the current induced by the solenoid and the external magnetic fields created by the coils. Forces can be applied to it through magnetic fields (self-generated or external), known as Lorentz forces. The electromagnetic force, which is equal to the vector product of the plasma current density and the magnetic field vector, is balanced with the plasma pressure gradient [8]. The balance of forces moves the plasma into a particular shape and position, known as the magnetohydrodynamic (MHD) force balance. Plasmas with an elongated vertical cross section increase the confinement energy, but their instability level increases [9], [10]. **V**ertical **D**isplacement **E**vents (**VDE**) are a long-lasting plasma instability, the plasma contacts the walls of the Vessel, top or bottom, and the plasma current is rapidly forced to zero [11]. A solution proposed for the control of VDE was the installation of simple short-circuited conductors in the same position as the poloidal coils [12], [13]. This passive control system is very simple, although it is important to study the correct position of the coils and the maximum vertical stabilisation capacity it can offer [14]. Predefined confinement reference values are used to supply the current references to the power supplies connected to the coils but may not be sufficient to manage events of instabilities or adjustments in the desired shape. In this case, the current of the poloidal coils and the current induced by the central solenoid are modified by basic control (PID). This control is the fastest; its response time depends on the type of machine and the duration of the pulse. It uses data collected principally by magnetic sensors and partially reconstructs the position of the plasma, actuating on the current of the coils [15].

For plasma control and coordination of auxiliary elements, there are multi-purpose frameworks such as MARTe. MARTe includes open-source C++ code and defines the communication architecture between code modules with different functions. There are other applications such as the **P**lasma **C**ontrol **S**ystem (**PCS**) initially developed for the tokamak DIII-D and currently in ITER and NSTX-Upgrade [16]. PCS allows real fusion reactor models to be introduced into the control loop simulation, allowing the **H**ardware **in** the **L**oop (**HIL**) to be simulated and facilitating development and fine-tuning. A conceptual model of the implementation of the simulation and the real tokamak control model is shown in the picture Figure 1-4.

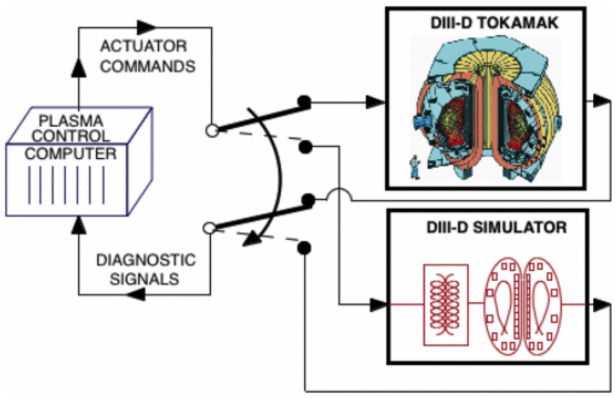



Figure 1-4 : PCS control hardware in the loop model [17]

In practice it is usual to include plasma current, vertical, and radial position in the same control loop. According to Figure 1-5. The inputs of the control loop are: the predefined currents exported by the plasma reconstruction and equilibrium algorithms defined by ($\mathbf{I_{FF}}$) and the expected current and position values ($\mathbf{I_{pl}}$, $\mathbf{R_c}$, $\mathbf{Z_c}$)$_{ref.}$ These values are compared with the output values at the end of the loop in the excited coils, **I**. The error **Iref** is evaluated by a controller (PID) that adjusts the switch-on and switch-off times of the power electronics in the power supply block. This loop operates as a programmable current source.

Externally to this control, a second loop is connected to the first one; it evaluates plasma characteristics such as

position and current and compares them with predefined values. The output value is transformed into a current value **IFB,** which needs to be obtained at the output of the active coils in order to modify the plasma characteristics.

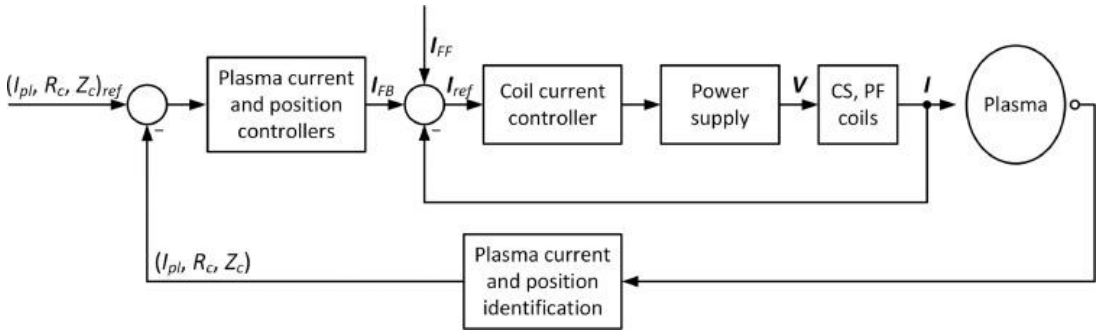



Figure 1-5 : Concept closed loop control [18]

Simulation of these controls is essential to optimise and adjust them; tunings, PID, and transfer functions are solved in other areas such as systems engineering, but the transfer function of the plasma performance (plasma current and position identification) can be overly complex. A simple model consisting of a rigid plasma model is validated in [19] using a control for the vertical position of the plasma.

Figure 1-6 describes the result of a simulation of the control systems using an $RZI_p$ model. In the first two cases (#12012 #11961) we have a centred plasma with positive and negative triangularity, respectively, which shows its functionality to change the shape of the plasma by adjusting its triangularity. In the last two cases (#9849 #10007), it is obtained an off-centre plasma, without triangularity and with circular shapes, without elongation and with elongation, respectively.

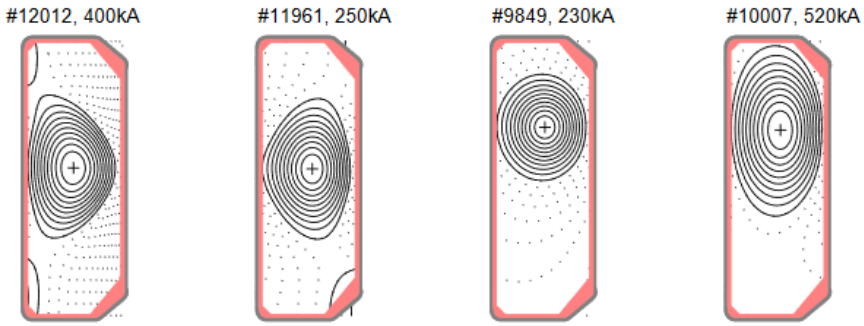



Figure 1-6 : Simulation of the control of the $RZI_p$ rigid plasma model [20]

In this section, basic and essential controls for the operation of a tokamak have been described. There are advanced controls that adjust values in 3D dimensions such as error field, RWM control, Sawtooth and NTM control, or Plasma Profiles control [8]. At the highest level of control is the management of the reaction mixture, which adjusts the reaction between the fuels and the residues [21].

## 1.4 Plasma diagnostics

Numerous parameters are involved in the fusion reaction and must be monitored. According to the experiment and the physical characteristics, it is necessary to include diagnostics sensitive to each measurement parameter. Plasma diagnostics have been developed for the study of temperature, density, confinement, and other properties in fusion reactors such as ITER [22], COMPASS-U [23] or JET. There is a lot of valuable information that can be collected from the data exported from plasma discharge, facilitating the operation, and control of nuclear fusion reactors. These data are used to study, understand and mitigate instabilities, such as disruptions, rapid and violent loss of plasma confinement, and control in

a fusion reactor [11], caused by the interaction with magnetic fields. Finally, the objective is to develop efficient nuclear reactors with high-safety protocols [24], [25].

The sub-elements generated in the high-energy reaction can be evaluated by particle diagnostics. The energy distribution of the particles can provide information on the reaction efficiency, the quantity of energy generated, and the fusion rate. A similar but lower energy study consists of introducing an electrical contact inside the plasma, known as a *Langmuir probe*, to obtain information about the electron density in the plasma and its potential. Other studies based on spectroscopy (λ ~ 10 m -10 pm) can assess the plasma temperature, its density, or its impurity content due to the wide measurement range. There are also other techniques based on laser-aided or microwave diagnostics with equivalent results, each with a different frequency range and therefore a different level of penetration. Finally, magnetic diagnostics are used to evaluate plasma current, position, and shape. Their data are used for detection of instabilities, post-reconstruction, and real-time operation [26]–[28].

This work focusses on the electrical adaptation of magnetic sensors' measurement, in particular those for the measurement of plasma current. An introduction will be described in the following section.

## 1.5 Magnetic measurement

Magnetic sensors provide important information about magnetic fields and variables such as position or plasma current can be measured. They are simple and inexpensive and are a common measurement element in fusion reactors. They allow to obtain information about the plasma, essential data for plasma equilibrium reconstruction, real time operation [29], current sensorisation and safety [30]. Two diagnostics for magnetic sensor are principally used: hall effect sensor and inductive sensor.

### 1.5.1 Hall-effect sensor

Those sensors are based on the interaction between moving charges and magnetic fields (Lorentz force). A semiconductor is placed under the influence of a magnetic field, the moving electric charge (the charge carriers, which can be electrons or holes) experiences a force due to the magnetic field, and this force causes a potential difference (voltage) in the direction perpendicular to both the magnetic field and the electric current. Therefore, this voltage is related to the magnetic field [31].
They have good repeatability, are encapsulated, and are solid-state, and their size can be very small. There is no drift in the measurement because they do not need integration (an operation that is required for inductive sensors and is described in the next chapter), the voltage output is proportional to the magnetic field [32]. As a disadvantage, they require a power supply and the semiconductor base can be affected by extreme radiation and temperatures. Research on these sensors, shown in Figure 1-7, has shown interesting results in ultra-high vacuum and ultra-high temperature environments [33].

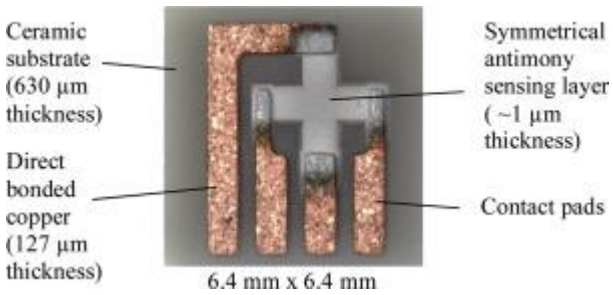



Figure 1-7 : Example of a Hall-effect sensor produced by the Institute of Plasma Physics of the Czech Academy of Sciences [33]

### 1.5.2 Inductive sensor

The principle of operation of these sensors is Faraday's law of induction. They are widely used in many applications because of their simple and cost-effective construction. Its simplicity, consisting of metal and insulation, makes it highly compatible with high temperatures, radiation, and ultra-high vacuum. Can be one single (or multiple) loops of conductive wire. However, a good understanding of their frequency behaviour and electrical quantities is required. An example of its building application is shown in Figure 1-8. In this case, there are three enamelled copper coils that measure the magnetic field in three different axes mounted on the same housing. They will be described in more detail in the following section.

Figure 1-8 : Example of a three-axis inductive sensor from the manufacturer NEOSID

## 1.6 Inductive sensor theory

Inductive sensors have large applications in the field of nuclear fusion. The magnetic field to be measured and the working environment determine their topology and construction materials. These are different of the types and position of magnetic coils; it is shown in Figure 1-9. The most common are the following: Diamagnetic Loop, Rogowski Coil, Saddle Loop, Flux Loop and Magnetic Field Probe.

- The Rogowski coil consisting of multiple toroidal shaped coils encloses all or part of the plasma and allows the plasma current variation to be evaluated. Its return from the last coil loop is driven through the inside of the coil with the two ends at the same point. This feature is important to avoid the formation of a ring with a poloidal cross-section, which would be affected by the toroidal magnetic field. The materials used are usually flexible in order to be moulded to the shape of the vessel. Some models made on **printed circuit boards (PCBs)** have had interesting results in terms of price-performance ratio [34].
- The Flux Loop consisting of a single wire, it measures the poloidal magnetic flux. Among other applications, they are used to measure the position and energy of plasma and the toroidal electromotive force.
- The Diamagnetic loop is a simple wire around the poloidal section to measure variations in the poloidal magnetic field and magnetic field probes used for high-frequency measurements to monitor singular locations in the plasma [29].

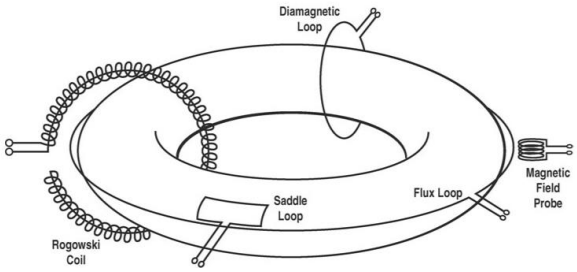



Figure 1-9 : Topology and distribution of inductive sensors: poloidal flux loop, Rogowski coil, diamagnetic loop, magnetic field probe and saddle loop [29]

The general electrical model of the inductive sensor is very simple and can be described through basic circuit theory introduced in Figure 1-10. First, there is a variable power supply that simulates the voltage induced by the variable effect of the magnetic field. Secondly, there are passive elements such as an inductance, due to the

nature of the coil, a resistance due to the copper wire and a parasitic capacitance that simulates the capacitive coupling of the wires. Finally, for more accuracy, it is possible to include the casing, composed of its magnetic coupling, a small inductance and resistance where the energy is dissipated by the joule effect [35].

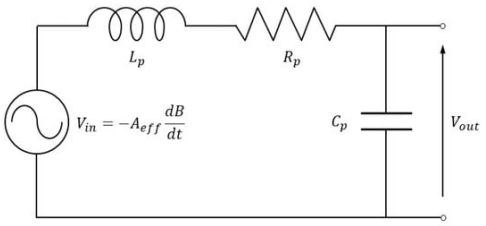



Figure 1-10 : Generic model of concentrated parameters of a magnetic coil. Self-parameters: inductance (Lp), resistance (Rp) and capacitance (Cp) [35]

The transfer function allows to evaluate how the frequency response of these sensors is. To correctly evaluate these types of sensors, each coil must be characterised in order to know the correlation between the induced voltage and the variation of the magnetic field. Where the transfer function is defined by Equation (1–3).

$$H(\omega) = \frac{1}{1 + j\omega R_p C_p - \omega^2 L_p C_p} \tag{1–3}$$

A generic representation of the transfer function is shown in Figure 1-11. The first linear part (0 to ~0.5 $f/f_0$) is the zone of interest or bandwidth of the coil, the region where measurements are made. The other frequency areas must be filtered by the acquisition system to avoid erroneous measurements.

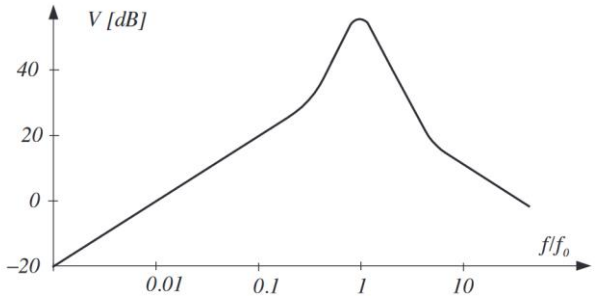



Figure 1-11 : Generic Bode diagram of a sensor coil [36]

The voltage induced in the coil is directly proportional to the magnetic flux variation. In the case of magnetic diagnostics, it is necessary to know the value of the flux, and not its derivative. For this reason, the signal has to be integrated. There are different methods of integration that will be described in Section 3.1 and this is one of the objectives of this document.

## 1.7 Transmission line

In tokamak reactors it is normal to install the measuring diagnostics inside the vessel and the data acquisition devices at a prudential distance. Strong magnetic fields and radiation are emitted from the reactor and can damage sensitive electronics. For this reason, it is necessary to place electronic devices at a safe distance connected through a cable, as this may cause a signal delay.

The distance is not usually fixed and might depend on the setup of the experiment. The topology of the cable, as well as the medium and length, influence its characteristic impedance and bandwidth. The characteristic impedance is defined by Equation (1–4) and the propagation constant of the wave is defined by Equation (1–5).

$$Z_\ell = \sqrt{(\mathcal{R} + i\omega\mathcal{L})/(\mathcal{G} + i\omega\mathcal{C})} \tag{1–4}$$

$$\gamma = \sqrt{(\mathcal{R} + i\omega\mathcal{L}) * (\mathcal{G} + i\omega\mathcal{C})} \tag{1–5}$$

It should be considered that there is no variation in inductance $\mathcal{L}$, or series resistance $\mathcal{R}$, per unit length, as well as parallel capacitance $\mathcal{C}$, or conductance $\mathcal{G}$, as described in Figure 1-12. In the application it is considered that there is no significant effect due to the transmission of the cable signal when it is a short line $\ell \ll 1/|\gamma|$.

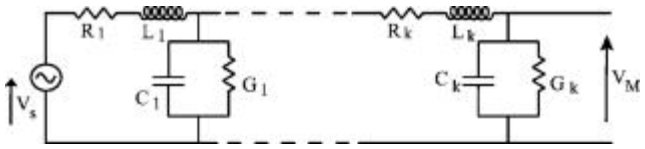



Figure 1-12 : Distributed parameter model of a connection line [37]

The input impedance of the acquisition system must be adjusted with the same impedance of the line. An impedance adapter is used to avoid reflections and resonance along the lines, in order to get to a stationary state as fast as possible. Adjusting this impedance adapter can require more than one channel with different bandwidth for a single signal and a low dependence of resistance on temperature [35][37].

Basic concepts of nuclear fusion, sensors, and magnetic coils have been revised. The objectives of this work will be described in the following section.

## 1.8 Objectives and scope

The main objectives of this work are:

- Revision of installed elements for tokamaks control systems
- Study of the state-of-the-art study of integrators
- Design of a preliminary plasma displacement control loop for SMART operation
- Design of a functional integrator for the first phases of SMART operation
- Definition, design, and construction of the set-up to test magnetic diagnostics.

The outlined objectives will be further explored in the upcoming chapters of this document, which has been structured as follows.

- **Chapter 2:** the different active elements for plasma control in the SMART tokamak are analysed. The requirements of the SMART tokamak plasma displacement control loop are described.
- **Charter 3:** describes the instruments used to integrate the signals provided by inductive sensors, as well as the different architectures and methods, comparing different alternatives.
- **Charter 4**: a solution is proposed through an analogue integrator, describing its characteristics, theoretical models, simulations, and development of the PCB.
- **Charter 5**: PCB verification tests are defined to evaluate the correct operation.
- **Charter 6:** the conclusions of the work conducted, as well as the expected future work, are presented.

# 2 TOKAMAK SMART

This chapter provides a more detailed description of the implementation of a first control system for the SMART Tokamak. A review of the confinement coils installed in the tokamak is carried out, as well as the PS used to supply the required current. The response times of the PS are evaluated as a function of their architecture.

## 2.1 Overview

The Tokamak SMART has a compact design ($R_o$ = 0.4 m, $a$ = 0.25 m, $A$<2) with the aim of being cost-effective, having educational purposes, and providing a high versatility in nuclear fusion research. It will explore positive and negative triangularity in this spherical topology, as well as serve as a platform in control system development, diagnostics, high elongation (κ<2.3) and different divertor configuration (single/double null divertor). This will provide an excellent training ground for researchers in this area [38]. SMART tokamak is currently in the assembly and testing phase. Figure 2-1 describes the construction parts of SMART.

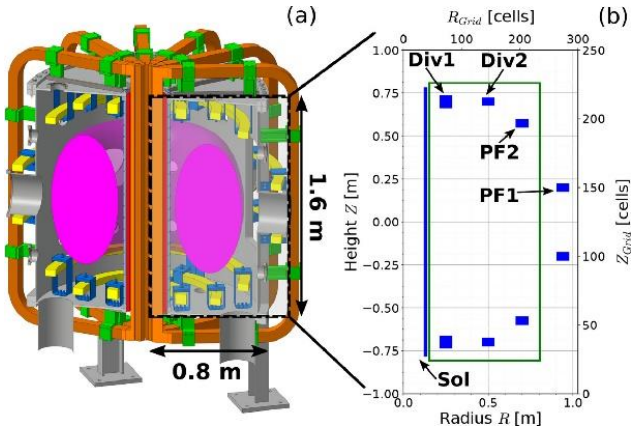



Figure 2-1 : Overall SMART architecture: (a)CAD model of the Vessel and Coils and (b) poloidal section of the tokamak [38]

Firstly, the vessel, made of AISI 316 L, is coloured in grey. All the coils necessary for the operation are mechanically installed on it [39]. The solenoid was installed in the central part, where toroidal field coils are connected on the inside (coloured orange). The structure must support the combined stresses, interesting studies have validated these designs [7]. Finally, the coils in the toroidal section (coloured yellow) consist of poloidal field coils (PFC) and divertor coils (Div).

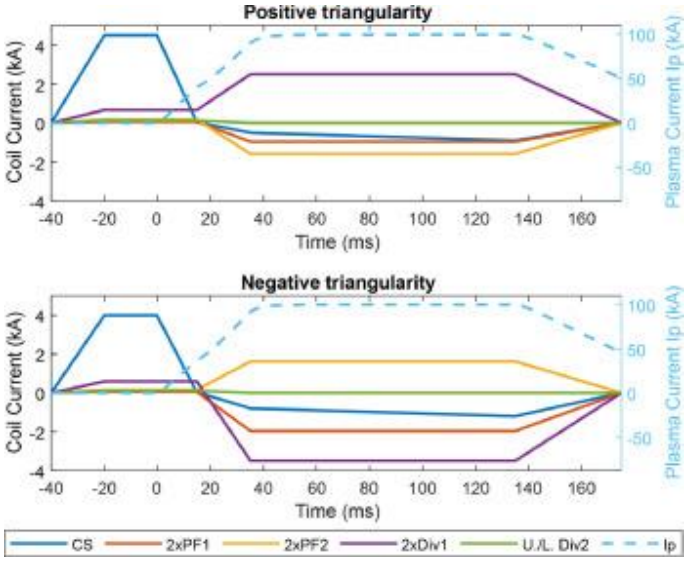



Figure 2-2 : Current forms of the coils and plasma current [40]

The currents required for the operation have been obtained through axisymmetric Grad-Shafranov force balance solver (FIESTA) in conjunction with the rigid current displacement model ($RZI_p$) [41]. The currents exported from the simulations (Figure 2-2) will be transferred to the control systems of the power supplies connected to each coil in order to sequence and manage all the coils [42]. The installed power supplies require a detailed analysis which will be described in the following section.

## 2.2 Power supplies

**P**ower **S**upplies (**PS**) are connected to the coils to obtain the expected magnetic fields. There are many topologies and architectures that solve this need. In SMART, a modular design has been created that allows scaling and increasing the design power by adding a greater number of units. Its technology is based on supercapacitors such as energy storage systems and **I**nsulated **G**ate **Bi**polar **T**ransistors (**IGBT**s) with modulation for power control (**PWM**).

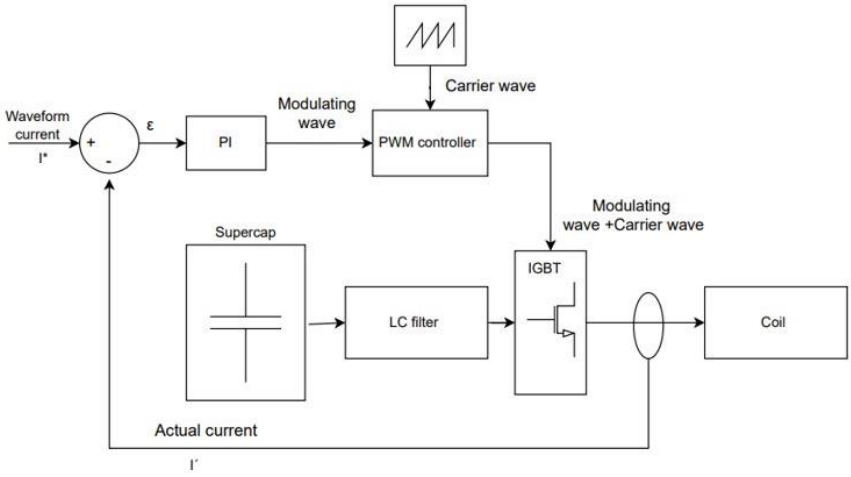



Figure 2-3 : Voltage-controlled current source architecture of PS

All architectures are based on a voltage controlled current source as described in Figure 2-3. The function of the control loop is to measure the output current and adjust the trigger times of the PWM control to adjust the output voltage and thus obtain the required current. The predefined current curves are transferred through an ethernet cable to each module that manages a specific group of coils. A master PC sequences all the power supplies that control each coil through a trigger signal. Each of the PS provides the specified current at the specified time.

Toroidal, divertor, poloidal, and solenoid coils have a crucial role in the operation of the fusion reactor, and they are powered independently by the PS, as illustrated in Figure 2-4. These coils are integral components of the

magnetic confinement system, which is at the core of controlling and stabilising the superheated plasma within the reactor vessel. A centralised control system manages the operation of these coils and ensures that they are supplied with the appropriate currents according to predefined curves. These predefined curves are derived from extensive simulations and research, providing a baseline for plasma control. However, it is important to note that a real discharge operation within the fusion reactor cannot be completely predefined.

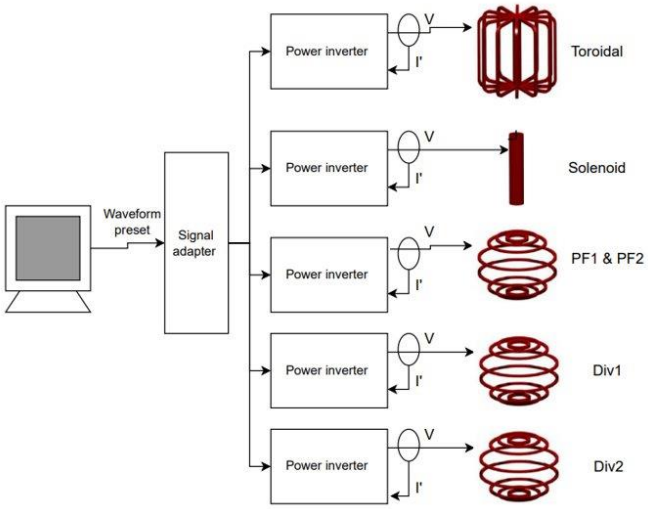



Figure 2-4 : Summary of coil and PS connections in SMART

The complex and dynamic nature of plasma behaviour implies that unexpected variations and instabilities can occur. The use of real-time data and feedback mechanisms to adjust and fine-tune the operation is fundamental to control of the plasma and to obtain the required specifications, ensuring that it remains stable, confined, and at the necessary temperature. For this reason, real-time control of the coils in SMART is necessary. By design, the PS of the Div2 coils have a fast communication bus to inject the current setpoints in real time.

## 2.3 First control loop design

There are many control architectures, an adaptation of the control loop presented in Figure 1-5 will be made in this section. For this purpose, two loops are connected, one after the other. The first loop is the current control loop, already defined in Figure 2-3. On top of this loop is the adjustment and reconstruction control loop.

A simple control model has been proposed in Figure 2-5. This loop is intended to give a general idea of the operating times at which the system can operate and, therefore, what its expected response speed can be. Firstly, the measurements are defined by the $T_{C.m.s}$ and $T_{P.m.s}$ time constants, these time constants are determined by the type of sensor (Section 1.5), as well as by the capacitances and inductances in the conduction as described in Section 1.7; the use of signal adaptive electronics such as integrators up to the data acquisition systems.

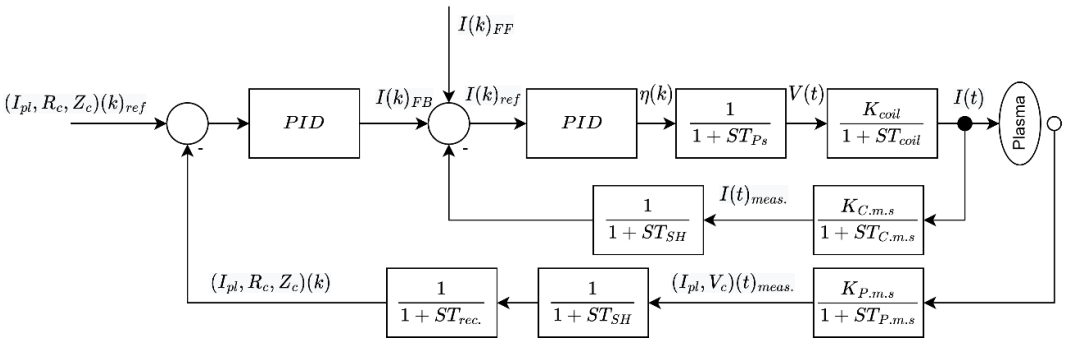



Figure 2-5 : Closed-loop control of plasma position and current

Signals are digitised through the **A**nalog **D**igital **C**onverter (**ADC)** and are delayed by the sample and hold method used to capture the signal level, represented by $T_{SH}$ constant. The time constant $T_{rec}$ , represents the specific value of time that the reconstruction code takes. It adds the times of communication between buses,

signal concentration, processing, and obtaining the value of the plasma current $I_{pl}(k)$ or position $R_c Z_c(k)$. $T_{coil}$ represents the time constant due to the RL circuit formed by the active coil. And finally, $T_{Ps}$ represents the time constant associated with the switching of the IGBT and the time constant of the filter at the output of the PS. Once the control loop is defined, the actual characteristics of the installed components will be analysed in order to evaluate their response time.

### 2.3.1 Control loop features

This section describes some actual characteristics of components already installed or under design. It is intended to provide a preliminary calculation guide to be used in the future as a basic calculation for more robust and better-defined control systems. According to the loop presented in the previous chapter (Figure 2-5) it is proposed to define the current control loop and the current control bubble. For this case, two control circuits have been analysed: DIV2 and solenoid PS.

#### 2.3.1.1 Current loop

Open-loop control mainly involves PID control, the switching circuit, and the active coils. The PID, consisting only of its proportional and derivative part, has a time constant of $\tau_{cl} = 0.63 * 0.5$ ms[43]. The rest of the constants are obtained through the values of the installed physical components.

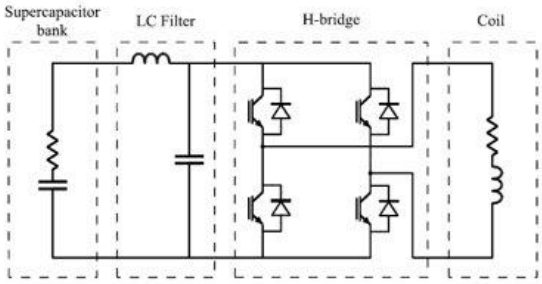



Figure 2-6 : General architecture of SMART tokamak power suppliers

The construction of all PS installed in SMART is similar, although there are differences according to the needs or requirements of the coil to which it is connected, an example of this architecture is presented in Figure 2-6, and will be taken as a reference for the calculation of the time constants. In this model some elements have been simplified, but it is enough to obtain an approximate value.

The LC filter installed in both PS have the same constructive characteristics of different value as expressed in the Table 2-1. It consists of an LC circuit and its transfer function presented in Equation (2–1).

$$\frac{V_o(s)}{V_i(s)} = \frac{1/L_f C_f}{s^2 + \frac{R_s}{L_f} s + \frac{1}{L_f C_f}} \tag{2–1}$$

The resistance of the supercapacitor bank is presented by $R_s$ where it is connected in series with the filter. The supercapacitor has a capacitance of several farads, does not consider the possible discharge, and is considered as an ideal source. The IGBTs used (5SNA 3600E170300) have a response time of 10 µs according to the datasheet.

The output of the PS is connected to a coil which creates a magnetic field according to the needs imposed by the control. This magnetic field is created through a variable current ($I_c$) imposed by the voltage variations of the PS ($V_{ps}$). The active coil, disregarding the characteristics of the connection cables, behaves like a basic LR circuit presented in Equation (2–2). The values are described in the Table 2-1.

$$\frac{I_c(s)}{V_{ps}(s)} = \frac{1/R_c}{\frac{L_c}{R_c} s + 1} \tag{2–2}$$

A transducer from the HAX1000-S range from the manufacturer LEN was used to capture the signal. According

to the datasheet, it has a response time of less than 5 µs. This value has been taken as its delay constant. The discretisation time is considered to be well below this value and will therefore not be taken into account in the control loop.

The complete transfer function of this control loop has been obtained, according to the characteristics of the components presented in Table 2-1, also considering the delays introduced by the switching of the IGBTs. The total time constant is 725.3 µs for the solenoid loop and 775.7 µs for the DIV2 control loop (Table 2-1). Both constants have been considered to give 63% of the final target value.

Table 2-1 : Power supply features

| **Parameter** | **C. Solenoid** | **2xDiv2** |
|---|---|---|
| Coil resistance (mΩ) | 33.4 | 2*14.9 |
| Coil inductance (mH) | 1.93 | 2*1.42 |
| Filter L (µH) | 15.0 | 6.7 |
| Filter C (mF) | 13.5 | 30.2 |
| Number of supercapacitors in the bank | 4 | 5 |
| Serie bank resistance (mΩ) | 6.2 | 3.3 |
| Constant open loop (µs) | 725.3 | 775.7 |

### 2.3.1.2 Position loop

The position loop has as a strategy to adjust the error made in both the current and the plasma position. By having two nested loops and for correct tuning, the integration constant of the PI control is set to a value 10 higher than the constant taken for the current control loop. The PI integration constant is therefore $\tau_{cl} = 3.15$ ms. The time constants of the sensors cannot be included in this section, as they have not yet been prototyped and are still in the design phase. The signal adaptation is performed by an analogue integrator which is described in the next chapter. The digitiser used is a PXIe-6349 from the supplier National Instrument, with a latency of 2 µs. The reconstruction of the plasma can introduce a long delay in the loop; therefore, the following formula should be considered to evaluate its time constant: $\tau = \sum_0^N (T_{fun})$. It is therefore considered that the minimum value that the whole calculation will take is equal to the sum of all the times associated with each individual operation ($T_{fun}$), considering basic mathematical operations (addition, subtraction...).

In the literature, control operations range from 50 µs to 10 ms actuation [44]. Parameters such as the total pulse duration or the plasma constant (maximum flow variation that can occur in a differential time) determine the individual reactor constants. These parameters are currently being studied for the SMART tokamak.

# 3 REFERENCE INTEGRATOR DEVICE

The voltage induced in the magnetic coils must be integrated to measure the value of the magnetic field generated and not the differential value with respect to time. There are different integration techniques with their associated hardware and software solutions. In this chapter, an introduction to integrators and their application in nuclear fusion is introduced.

## 3.1 Introduction

As described in Section 1.6, the output signal of the magnetic sensors must be integrated. A simplified bode diagram is shown in Figure 3-1. The transfer function of the *Rogowski coil*, which works as a high-pass filter up to its cut-off frequency $f_H$. On the other side, *the integrator* has a transfer function similar to that of a low-pass filter with cut-off frequency $f_L$. The conjunction of both transfer functions has a constant gain between the frequencies $f_L$ and $f_H$. These frequencies define the bandwidth of the integrator. The magnetic flux measured by the magnetic sensor has a constant gain that is not dependent on the frequency of the signal at the output of the integrator.

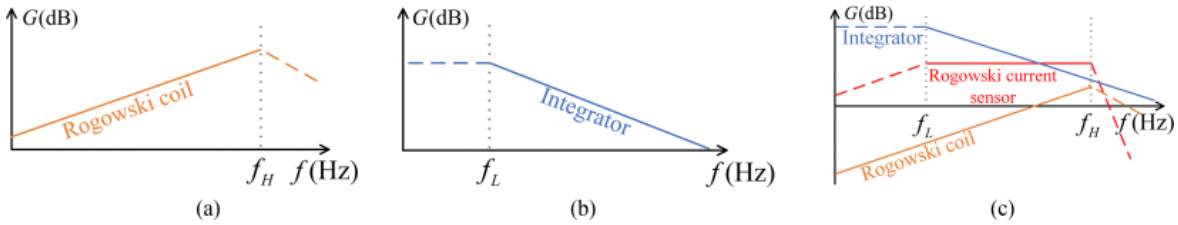



Figure 3-1 : Representation of the transfer function in the frequency domain: (a) Rogowski coil, (b) Integrator, and (c) Combination of both [45]

There are different methods (Figure 3-2) to perform the mathematical function of integration function such as software as hardware. Each offer advantages and disadvantages in terms of complexity, cost, speed, noise immunity, and bandwidth.

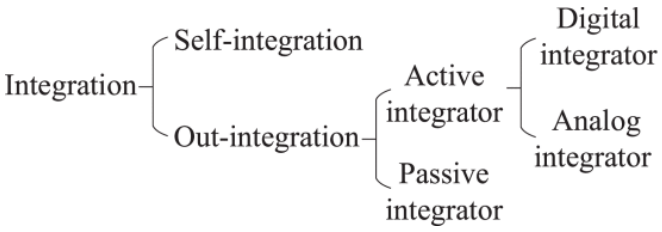



Figure 3-2 : Scheme of integration techniques [45]

Out-Integration techniques require special consideration. They can be categorised into two main groups: active and passive integrators. Digital integration is the use of computer codes and programmes based on mathematical algorithms to integrate the signal. Analogue integration uses electronic components to perform mathematical functions. The components can be active or passive, and each of them has different characteristics. All these integrators are described in the following sections.

In an ideal situation, the integrated output is only due to the integration of the signal being measured. In a real application an additional voltage is known as drift voltage. The value of the drift voltage induces errors that must be identified. It is one of the main characteristics taken into account in integration systems.

## 3.2 Digital integrator

Digital integration has been used as a method to perform real-time integration of magnetic sensor signals. The mathematical operation in the continuous domain must be adapted to the discrete-time domain. An algorithm based on summations [46], is represented by Equation (3-1).

$$y_k = \frac{1}{R}\sum_{n=0}^{k}(x_n - X) - \frac{1}{R}\sum_{n=0}^{k}(b_n - B) \tag{3–1}$$

The integral is defined as a sum of the values sampled divided by the number of samples collected in the interval. The parameter $x_n$ describes the digitized value in the at time k, $b_n$ defines the measured parameter, and X and B are constant setting value. R defines the number of samples in the range k. The integrated output value is $y_k$.

Sampled signals have an important process from the physical domain to the digital domain. First the signal is adapted to the appropriate voltage levels, in this case the hardware architecture depends very much on the type of signal. The signal can be amplified, attenuated, or converted (current level to voltage) [47]. The signal is filtered according to the signal bandwidth and sampling frequency of the analogue-to-digital converter (anti-aliasing filter). At this stage, signals that are not of interest for the measurement are filtered out. The frequencies that exceed half of the sampling frequency according to the Nyquist-Shannon theorem are filtered [48] and finally it is digitized through an **A**nalog-**D**igital **C**onverter (**ADC**).

Two main processes involve: quantification and encoding. In quantisation, the signal is divided into different voltage levels, and coding is the assignment of a binary value according to specific hardware and software considerations. According to the conversion speed and bit size of the encoding, there are different architectures such as: Flash ADC, Pipeline ADC or Sigma-Delta ADC and others [49]. The signal part is isolated from the control part by galvanic isolation. It also includes auxiliary memories or registers to store data such as the sum of the integration. The data have two routes, the storage for post-processing and for the real-time control process described in Figure 3-3.

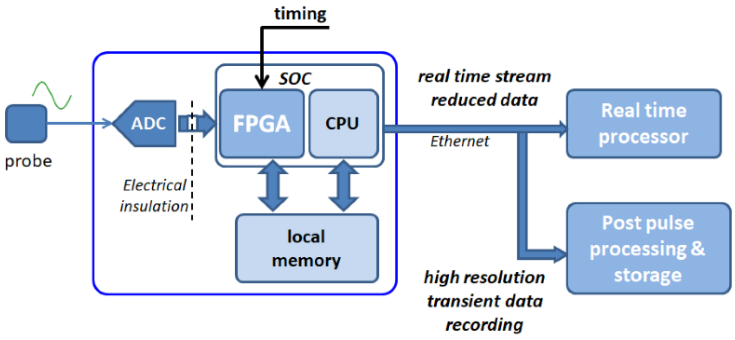



Figure 3-3 : Digital integrator architecture [35]

A prototype integrator on the DIII-D tokamak was proposed and designed for use in ITER. It allows a pulse integration of up to 1200 s whit 5 mVs of drift error approximately. It has an RC filter with the objective of eliminating high frequencies and attenuating the overvoltage produced in the measurement of the magnetic sensors. It also includes an amplifier stage and an ADC [46].

To mitigate the effect of drift, the chopper technique was introduced. This method allows attenuating the offset errors as well as the variations due to thermal drifts. These integrators allow to obtain a high accuracy.

In [50] is described a chopper integrator used in the tokamak EAST, with a 300 μVs drift in pulse duration of 1000 s. The input signal is switched according to a clock signal (the input signal is inverted at a specific frequency by a switch written in the circuit of Figure 3-4) but different topologies are possible. Switching constants are stored for use in signal demodulation. The signal is integrated according to the programme algorithms used for synchronous rectification of the chopped signal, resulting in a significant elimination of the drift voltage and reduction of the 1 / f of the noise signal. Can be used as a high-pass filter if the switching frequency is appropriate [51]. The use of this technique has also been done in ITER [52], with remarkably positive results. Twelve architectures were evaluated, with various types of anti-aliasing filters and types of ADCs (SAR, ΔS and ΔΣ). The maximum drift achieved was 250 μVs. Other results taken from the COMPAS experiments show that there

is no large drift or loss of information due to chopper noise. COMPASS experiments show that there is no large drift or loss of information due to chopper noise. The experience gathered in these tests will be the basis for the construction of the new acquisition systems to be installed in COMPASS-U based on ATCA [53].

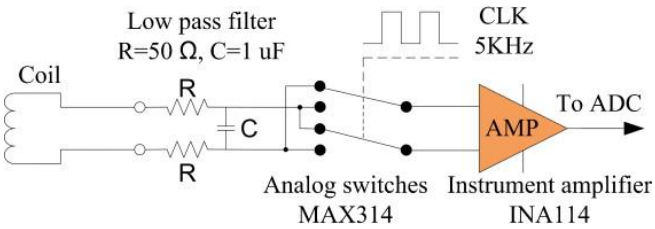



Figure 3-4 : Example of a chopper integrator [50]

Recent research in this area has introduced digital integration algorithms using high-speed analogue-to-digital converters with very satisfactory results [54]. This technology allows for rapid development and simple simulation; in addition, it introduces the possibility of using specialised digital filters for the type of signal being measured, introducing the quantised signal directly into the control loop. As a disadvantage, to comply with high quality indexes it needs a high bandwidth and immunity to strong magnetic fields.

## 3.3 Analogue integrator

Analog integrators need a different external component to operate. A timing decoder is essential to synchronise the integration and analogue-to-digital conversion. The analogue integrator is connected to the ADC as shown for digital integrators. The signals are captured by two acquisition system, for real time processing and for post pulse processing shows in Figure 3-5.

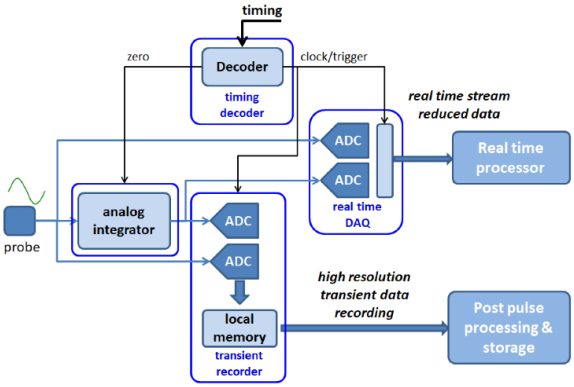



Figure 3-5 : Analogue integrator architecture [35]

The signal integration module may be composed of simple a circuit formed by passive elements as a resistor and capacitor shown in Figure 3-6 a). This would function as a low pass filter and is considered one of the simple ways to achieve integration, however, it introduces a natural attenuation of the signal and a low input impedance [55]. These types of integrators have been used in the field of partial discharges because of their simplicity and bandwidth of up to 500 MHz [56]. Passive integrators are consequently used for high frequency applications, while active integrators, based on operational amplifiers (Figure 3-6 b), are used in lower frequency applications [57].

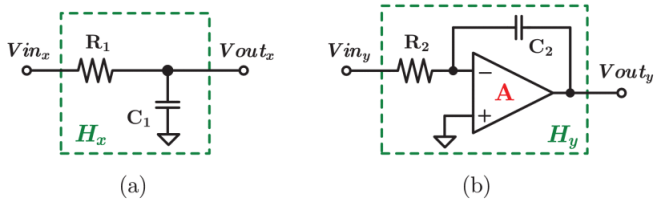



Figure 3-6 : Analogue integrator circuit: (a) Passive and (b) Active [55]

The use of **Op**erational **Amp**lifiers (**OP-AMP**) for the construction of integrators allows eliminating the natural attenuation that passive integrators had, in order to introduce a necessary gain. They have greater flexibility and allow for simpler adjustment. In addition, they are less temperature dependent, which reduces thermal drift. Different configurations of op-amps are shown in Figure 3-7.

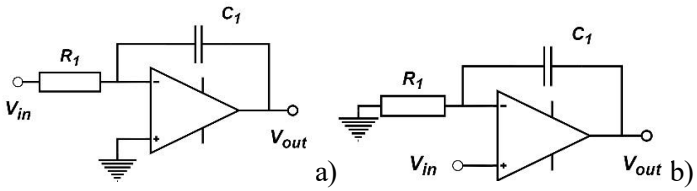



Figure 3-7 : Configuration of operational amplifiers: (a) Inverting and (b) Non-inverting

Inverting and non-inverting operational amplifier configurations represent two fundamental approaches in analog electronics, each offering distinct characteristics. In the inverting configuration (Figure 3-7 a), the input signal is applied to the inverting terminal (-)of the operational amplifier, while the non-inverting (+) terminal is grounded. This results in an output that is 180 degrees out of phase with the input, and the gain can be easily controlled by external resistors. On the other hand, the non-inverting configuration (Figure 3-7 b), involves applying the input signal to the non-inverting terminal, making the output in phase with the input. The gain in this setup is determined by the ratio of two resistors. Non-inverting amplifiers provide higher input impedance, making them suitable for applications where signal loading is a concern.

$$v_o(t) = -\frac{1}{RC}\int_{t_o}^{t}[v_i(t) + RI_{os} - V_{os}]dt \tag{3–2}$$

On the other hand, special attention must be taken to attenuate the effects of the bias current and offset voltages, which can be integrated and can saturate the amplifier. In most cases, this effect is observed as an increasing value at the output of the circuit shown in Figure 3-8. The drift effect is due to the integration of the polarisation constants ($I_{os}$) and the offset voltage ($V_{os}$) of the operational integrators, as described in Equation (3–2) [58]. There are other sources that are included in the drift but of lesser significance, such as temperature drift or integrated noise. These values are influenced by the integration constants according to the RC values. An experiment was performed to measure the drift of integrators to be incorporated into the Tore Supra (now WEST) tokamak; a standard deviation of 5 mV was obtained, with a maximum of 15 mV in 1000 s of integration. These results were got through two tests with fourteen integrators. Figure 3-8, shows the result of another experiment with two racks of seventeen integrators each [59].

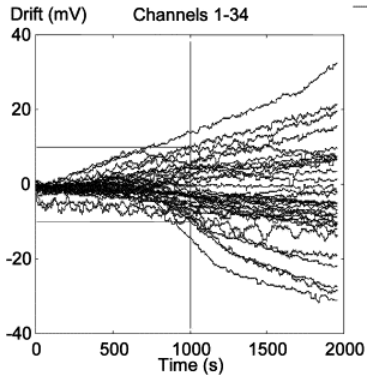



Figure 3-8 : Tore Supra reactor integrator drift test [59]

In bibliography there are different architectures that aim to eliminate or attenuate the effect of drift. One technique is based on the differential compensation of two symmetric stages [60], the circuit shown in Figure 3-9 is an example of this technique. An op-amp is connected to the signal to be integrated, while another amplifier is connected to the reference. The two stages are both connected to a differential amplifier. This method could be considered as an *analogue self-compensation,* and it is a simple form to reduce the drift effect. It is implemented in EAST [58], Tore Supra [59] or in WEST [61].

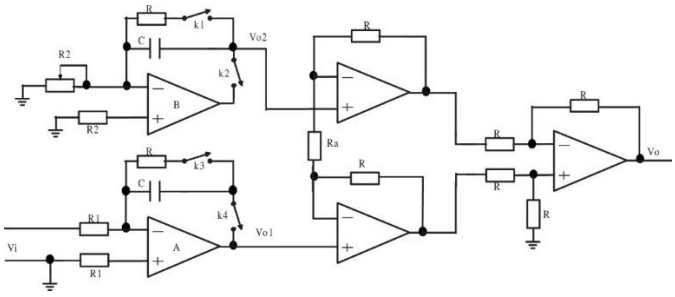



Figure 3-9 : EAST integrator circuit design [58]

As part of the EAST experiment, four hundred integrators were installed. This set of integrators was instrumental in implementing plasma control and facilitating diagnostic procedure, its circuits are as indicated in Figure 3-9. Implement an instrumentation amplifier which inputs are connected to an integrator shorted to the reference and another integrator, connected to the input signal. In the calibration tests, a maximum deviation of 10 mV was obtained in 10 s [58]. Other interesting parts of the design installed in EAST is its design that provided a remote and automated calibration and gain adjustment. Automation of the calibration of a large number of signals improves and speeds up the process. It was implemented using a master-slave block architecture and ethernet communications as shown in Figure 3-10 and Figure 3-13. The integrator circuit was covered by overvoltage protection, an essential part in the first designs and tests. It is composed of a transient voltage suppressor (TVS diode) shown in Figure 3-10.

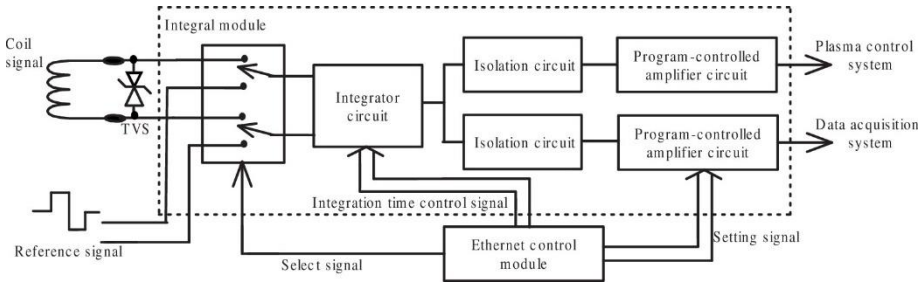



Figure 3-10 : Integrator architecture installed in EAST [58]

Other designs such as the prototypes for the WEST tokamak [61] propose servo offset voltage compensation techniques through analogue and digital circuits. The first design (Figure 3-11 a) holds the voltage on a capacitor and feeds it back negatively. The other design (Figure 3-11 b) is the same operation but is based on a digital analogue converter and then an analogue digital converter. In both cases, the objective is to evaluate the offset voltage at the output and inject it at the start of the loop to self-cancel. The minimum voltage drift in 1000 s of integration was 1.10 mV of the different prototypes designed. Therefore, they have a very low deviation; however they include more complexity within the active analogue integrators.

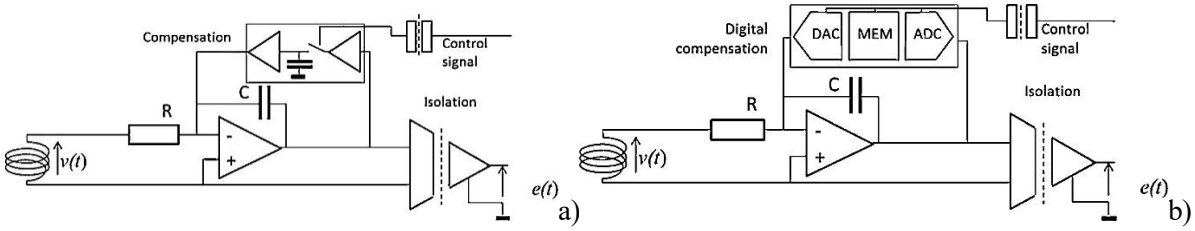



Figure 3-11 : Servo compensation system on the WEST tokamak: (a) Analogue design (b) Digital design [61]

## 3.4 Application architectures

Integrators are not elements installed as individual systems; they are usually part of a superior system with different functionalities. These functionalities determine the architecture of an entire signal acquisition and management system. This section describes some of the system layouts that are installed around the integrators and magnetic sensor signals to facilitate their measurement, control, and archiving.

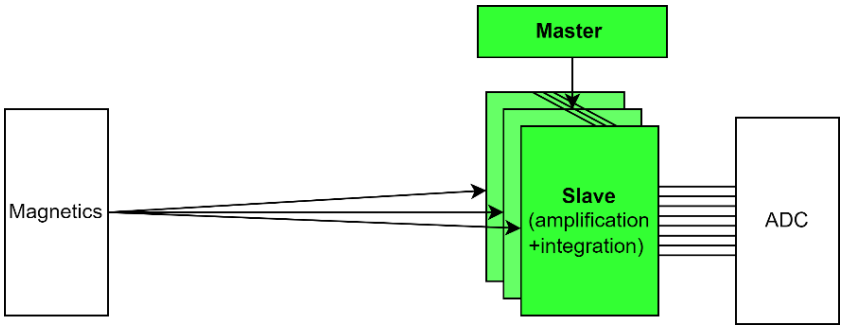



Figure 3-12 : General master-slave integrator architecture

This condition can be significant for architectures with a large number of magnetic sensors, in some cases more than 200 channels are required [62]. The design consists of independent integrators connected on a motherboard, a master control board communicates with the rest of the slave boards through the motherboard, and with the control system via ethernet [63], represented in Figure 3-12.

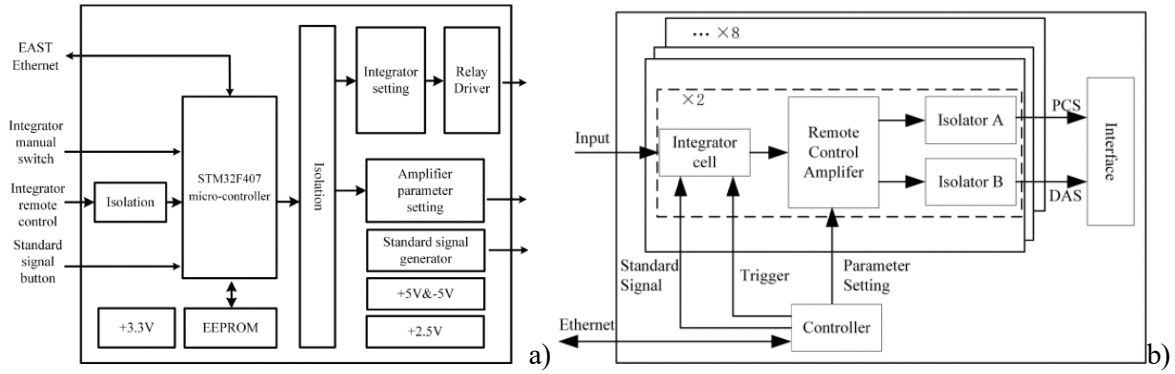



Figure 3-13 : System architecture: (a) Master and (b) Slave integrator [63]

Because of the large number of signals to be processed, it is essential that the systems can be monitored and automated. Figure 3-13 shows an example used in EAST, its design is based on a master-slave architecture, where a main node consisting of a STM32F07 microcontroller manages the communications with the remote control and executes the actions on each of the integrators. Possible actions include gain change, integration reset, predefined signal injection, and manual operation, among others [63]. This module is only designed for analogue signal adaptation; therefore, it would have to be connected to an external digitalisation module. On the other hand, there are onboard systems in which the integrator circuit is together with the signal adaptation and acquisition system, in both analogue [64] and digital [53]solutions.

Data acquisition systems with an integrator design on-board are an interesting compact and modular solution. Figure 3-14 describes this architecture recently used for a second design in EAST. Each integration module is composed of ten integrator boards, managed by a single master board that is actuated by a trigger for the start of integration.

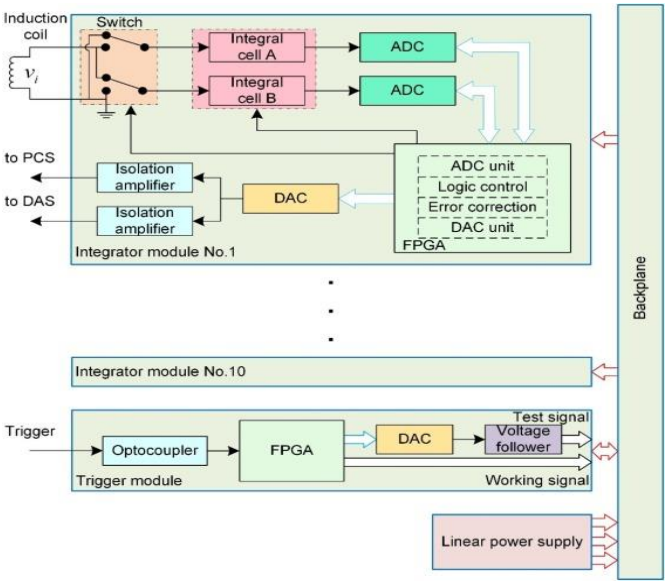



Figure 3-14 : System architectures with ADCs on the integrator board [64]

Every board functions autonomously, as it integrates an FPGAs, ADC, analogue integrators, and all elements for different functionalities. The actuation signals are directly connected to the **P**lasma **C**ontrol **S**ystems (**PCS**) and **D**ata **A**cquisition **S**ystems (**DAS**). The hardware solution for these systems is usually not trivial due to the number of signals to be supported and the high performance against noise and mechanical robustness. In the following section, it will be described.

## 3.5 Integrator chassis design

Instrumentation systems located in nuclear environments must have high levels of safety. Radiation, dust, temperature variations, ground reference, overvoltage, high number of signals and their distance to the tokamak, and electromagnetic compatibility. All these considerations lead to an increase in the uncertainty of the signals due to the introduction of noise. In addition, these systems are expected to not require continuous human intervention or can be performed remotely.

In addition to electromagnetic noise immunity, these systems must maintain mechanical robustness due to the industrial environment. It is essential to have remote information on the status of the platform, manage alarms, and maintain fast communication with the central control modules. That is why software and hardware architectures are essential for provide greater security and safety [65].

There are a multitude of solutions for compact instrumentation systems that must meet specific constraints.

- **Custom designs**: a customized solution can be adapted to each of the experiments needs [64]. In the bibliography, a specific design with eight integrator plates is presented. The design is presented in Figure 3-15 refers to the system shown in Figure 3-13. It consists of a generic housing where all the internal communications part has been built using custom PCBs designs [63].

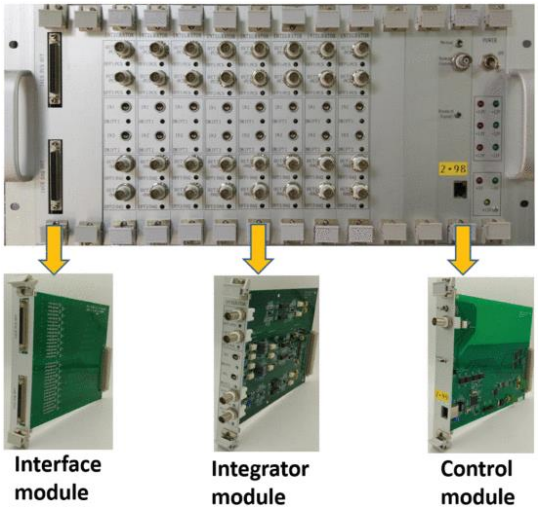



Figure 3-15 : Hardware design of the integration system [63]

- **CompactPCI® (cPCI):** They are based on Eurocard's standard 3U or 6U industrial computers, PCI architecture and where all cards are connected via a passive backplane. It is an open specification supported by the **O**pen **S**tandards for **E**mbedded **C**omputing **A**pplications (**PCIMG**) [66]. With a diverse range of industrial, aerospace, commercial, military, and other applications, has been used in the LIPAc linear accelerator [67] or in the EAST tokamak [68].
- **Versatile Performance Switching (VPX or VITA 46/48):** Based on Eurocard standards. It is orientated to abrupt environments such as military applications, where size, weight, and reliability are critical. Although it has excellent characteristics, other lower cost platforms are being used [69].
- **PXI (PCI eXtensions for Instrumentation):** It is a standardised communication bus for the instrumentation and control industry. It allows to support different applications due to the large number of functional boards that can be connected. Its use is very extended in the development of signal acquisition and control systems in the context of nuclear fusion, as in TJ-II [70] or ITER [71].
- **Advanced Telecommunications Computing Architecture (ATCA):** Defines PCI Industrial Computer Manufacturers Group (PICMG) specifications. It has an open, multi-vendor architecture and establishes communication and production standards for chassis and communication modules [69], [72].
- **National Instruments (NI**): is a supplier of standard PXI and PXIe hardware, with a wide range of data acquisition solutions, virtual instrumentation, and automated test systems.
- **Keysight Technologies:** It is a supplier that offers test and measurement solutions, including modular systems based on standards such as PXI and AXIe (AdvancedTCA Extensions for Instrumentation and Test).
- **Advantech:** It is not a supplier of any standard but has robust solutions in industrial environments for power pc.

Table 3-1 : Platform comparison: ATCA, VPX and cPCI Express [69]

| | ATCA | VPX | cPCI Express |
|---|---|---|---|
| Dimensions | 8U | 3U and 6U | 3U and 6U |
| Nr analogue channels (front panel) | 32 | 16 | 16 |
| Fabric | Agnostic | Agnostic | PCIe |
| Backplane | Full-mesh | Full-mesh | Star |
| RTM | Yes | Yes | Yes |
| Mezzanines | Yes | Yes | Yes |
| Power dissipation/ slot | 200 W | Shelf dependent | Shelf dependent |
| Redundant power supplies | Backplane level | External | External |
| Redundant cooling fans | Yes | No | No |
| Hot swap | Yes | Yes | Yes |
| Shelf management | Redundant IPMI | IPMI | IPMI |
| EMC shielding | Yes | Yes | Yes |
| Availability | 99.99% | - | - |
| Foreseen main application | Telecom industry | Military | Industry |

A comparison of the main architectures such as ATCA, VPX and cPCI Express is described in the Table 3-1. One of the main advantages of these systems is the **I**ntelligent **P**latform **M**anagement **I**nterface (**IPMI**), which allows to manage all the devices connected to the motherboard by means of standardised messages through a hardware controller called **BMC**. (**B**aseboard **M**anagement **C**ontroller). Consequently, it is possible to supervise all the hardware, understanding its status and its communications on the bus [73]. ATCA has a redundant n+1 system with high availability, which offers greater robustness and security to the control and monitoring system in real time. ATCA is the most interesting feature platform, which makes it one of the main development technologies for scientific experiments such as ATLAS, CERN, large telescopes and ocean observatories according to [69].

The **I**nstituto de **P**lasmas e **F**usão **N**uclear (**IPFN**) developed an acquisition board (Figure 3-16) to integrated into ATCA. It had thirty-two analogue input channels, a DDR memory, and an FPGA, which were connected to six other control boards via the PCI Express interface. This device was used in the tokamak Jet for vertical stabilisation as well as in COMPASS for different control and signal acquisition routines.

Figure 3-16 : Example of an ATCA-MIMO-ISOL board developed by IPFN [69]

A digital integrator has been developed to mount on the board presented previously. A PCB was designed with the same topology as the modules intended for signal adaptation and digitisation, this new design had the function of a digital integrator with very significant results and will be used in COMPASS-U [53].

It is important to take into account all existing architectures to guide future designs that will be supported by these platforms. The following chapter will describe the design of an analogue integrator prototype.

# 4 INTEGRATOR DESIGN

In this chapter, the integration function required to adapt the signal from the Rogowski coil to the current measurement in the tokamak SMART will be solved. According to functionality and cost, an analogue integrator will be used. A non-inverting configuration of op-amp has been selected due to the unavailability of components. The design and construction of this circuit will allow to gain a lot of experience in PCB design, as well as, to allow to make modifications and to be the basis for signal adaption systems for future designs.

The possibility of a digital integrator is discarded as the data acquisition system is already built and the addition of a chopper system for drift control could be complex. The development of a separate acquisition system is also not justified due to the high cost and time required for its development. Therefore, the criteria of simplicity, economy, and development efficiency have been chosen.

The workflow is described in Figure 4-1, first of all, the basic requirements of the integrator were defined, as well as some electrical and mechanical quantities. An architecture was designed to meet the described needs, and the components to be used were selected. MATLAB together with Simulink® supported the theoretical analysis part of the design, offering a high speed in the design calculation. Once the theoretical model were correct, the data was exported to LTspice, where the real components were simulated. The data exported from the real simulation was checked to be within the limits imposed by the requirements. For the manufacturing of the physical circuit, all the hardware was designed in EasyEda and manufactured by JLPCB.

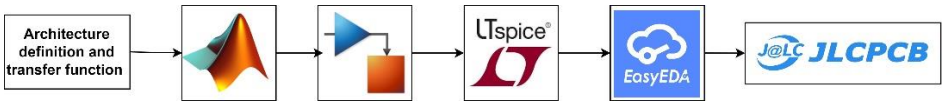



Figure 4-1 : Work rout map

## 4.1 Integrator requirements

For integrator design, it is necessary to delineate the prerequisites of the system under evaluation. They are as follows.

- The system must execute the mathematical integration function.
- The system must be modular and configurable.
- The system must provide the internal temperature of its circuits.
- The system must have a high input impedance.
- The system must maintain a relation between functionality and cost.
- The system must have a reference isolated from the physical ground.

The technical requirements of the system, which are specific to certain functions, are also described:

- The system must operate with a range of input voltages from 1 to 50 v.
- The system shall have a full-scale output of ±10 V.
- The system shall be capable of operating at a DC voltage of 12 V.
- The system shall withstand an overvoltage of 1000 V.
- The system shall filter overvoltage.

- The system shall have SMA type connections for signal inputs and outputs.
- The system shall guarantee a maximum operating deviation of 0.5 % of full voltage scale during operation.
- The system will have a reset to remote integration.

## 4.2 Architecture

According to the specifications, a conceptual diagram is presented in Figure 4-2, a **TVS** diode (**T**ransient **V**oltage **S**uppressor) will be installed [58], and a **L**ow **P**ass **F**ilter (**LPF**) will further attenuate the overvoltage that may occur in the magnetic sensors. The board will be connected through an AC-DC 220 V 50hz voltage source. Relays will be used to reset the integration time. A temperature sensor will be connected and installed in the circuit to provide board status information, the data obtained will be processed by high-level algorithms to correct for temperature deviations and increase the calibration speed in real operation, and a set of op-amps will provide the necessary integration function.

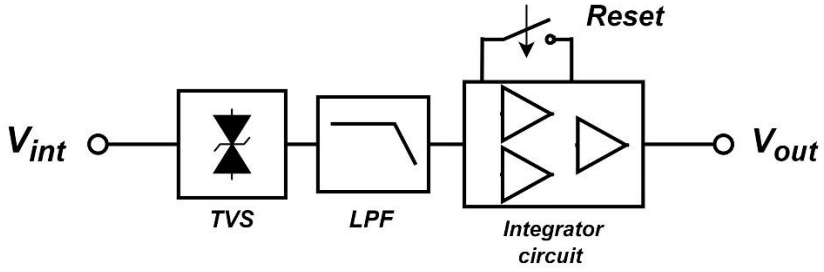



Figure 4-2 : Block diagram of the integrator system

Due to the current geopolitical situation and international markets, there is an important deficit in electronic components. In this context, the circuit has had to address these considerations. One of the most significant points was the galvanic isolation between the signals. As the construction of a digital integrator was discarded, optocoupling is not an option. Analogue isolation amplifiers could be used, but those available on the market at the time of development did not satisfy the requirements. For this reason, the integrator circuit is based on a non-inverting configuration of op-amps. To mitigate the drift effect, an architecture similar to the one presented in [74] has been selected, but with a new configuration of the integrating op-amps as described in Figure 4-3.

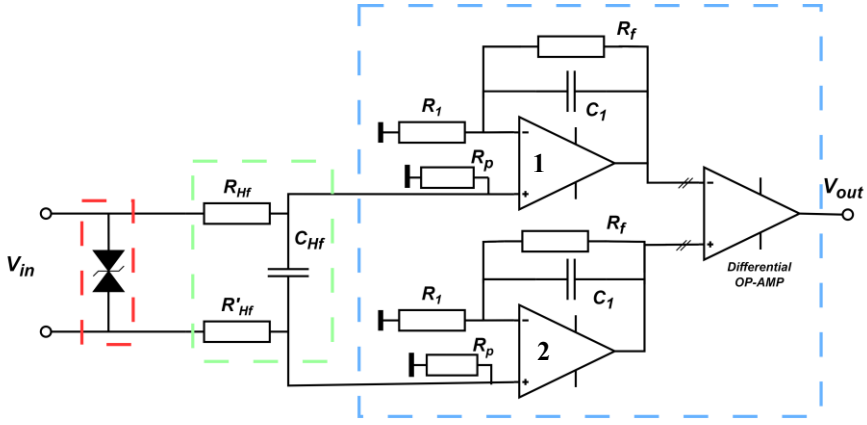



Figure 4-3 : Schematic of the op-amp configuration in the integrator circuit. Reprinted from [74]

The architecture presented in Figure 4-3 offers a reduction in the components used compared to the one already presented in the bibliography [58], based on the self-compensation of the drift from a symmetric circuit (two op-amps have been removed). The high impedance is achieved with a non-inverting configuration, and no instrumentation amplifier is used. Compared to the architecture presented in [74], the isolation amplifier is eliminated because of the impedance offered by this configuration. Therefore, this configuration is cheaper and initially with less latency. In addition, the TVS is maintained to protect against possible overvoltage.

### 4.2.1 Resetting architecture

The integration time is the instant at which the signal is to be evaluated and, therefore, integrated. The main signal is integrated, as well as the sum of all signal levels at the input of the op-amp, regardless of the input signal being connected or not. For this reason, the instant of integration must begin when evaluating the input signal, and there are many strategies for this purpose. One strategy is to short-circuit the integrating capacitor, ideally obtaining a voltage of 0 V. A MOSFET transistor can be used as a switching element, but the polarisation of the capacitor can change according to the signal and a high impedance is necessary so as not to affect the established transfer function. In addition, it induces parasitic capacities characteristic of these elements. Non-desirable effects. As a solution, it is proposed to use a relay connected to both terminals of the capacitor as described in Figure 4-4.

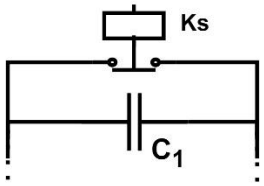



Figure 4-4 : Reset circuit model

The relay will be used in its normally connected format, and once it is energised, it will open to start the integration period. This device has a high resistance when opened and can accept the short-circuit current of the capacitor. It also has galvanic isolation from the control signal. The disadvantage is that it has a certain latency or delay in the opening time that must be evaluated in order to include it in the control time margins of the device.

## 4.3 Component selection

Depending on the requirements of the circuit, different components were used; an overview is given in this chapter. The Annex C can be used as a guide for clarity. These included miniature KEMET EC2/EE2 signal relays to reset the integration time. Its small format and low power consumption offer excellent characteristics to be implemented in this circuit. There are many other types of relays on the market, and this component should be reviewed to reduce its size as much as possible. It is expected that in future circuits only one instead of two will be used. To operate the relays, the DRDNB21D-7 drivers were installed from the manufacturer Diodes Incorporated.

An Ultralow Noise and EMI enhanced ADA4522-1 op-amp was used, serving in the integrator circuit. Capacitors for energy storage, based on polypropylene material with low dielectric loss and low leakage current are used. The TVS diode is SMCJ45, from manufacturer Littelfuse®, protecting the input from transients of up to 1KV. The sensor for PCB temperature monitoring is TMP1075 with Digital interfaces: SMBus and I2C. SMA connectors for input and output signals, a DB-9 connector for data transmission, a DC-DC switching power supply for efficient voltage insolation (RS PRO 1W isolated DC-DC converter), voltage regulators to maintain stable power levels, and various passive components. Each component played a crucial role in achieving the circuit's intended functionality, with specific attributes and specifications tailored to their respective tasks. The total circuit component is described in Annex C.

## 4.4 Theorical model

In this section, a theoretical model of the different characteristics of the circuit is described, such as the transfer function (voltage gain), the voltage drift, the input impedance, CMRR, or the random noise introduced by the resistors.

### 4.4.1 Voltage gain

The gain of the low-pass filter in the Laplace domain is defined by:

$$G_1(s) = \frac{V_{hf}(s)}{V_{in}(s)} = \frac{1}{R_{hf}C_{hf}} \frac{1}{s + 1/R_{hf}C_{hf}} \tag{4–1}$$

The gain of the integrator circuit (1 and 2 op-amp) in the Laplace domain is defined by:

$$G_2(s) = \frac{V_{O3}(s)}{V_{hf}(s)} = \frac{s + (R_1 + R_f)/(R_1R_fC_1)}{s + 1/R_fC_1} \tag{4–2}$$

The Laplace domain differential amplifier gain is defined by:

$$G_3(s) = \frac{V_{out}}{V_{op1} - V_{op2}} = \frac{R_a}{R_b} \tag{4–3}$$

$$If\ R_a = R_b \rightarrow\ G_3(s) = 1 \tag{4–4}$$

The final gain of the system in the Laplace domain is expressed as:

$$G(s) = G_1(s) * \ G_2(s) = \frac{1}{R_{hf}C_{hf}} \frac{1}{s + 1/R_{hf}C_{hf}} \frac{s + (R_1 + R_f)/(R_1R_fC)}{s + 1/R_fC} \tag{4–5}$$

$$If\ R_{hf}C_{hf} = (R_1R_fC)/(R_1 + R_f) \rightarrow\ G(s) = \frac{(R_1 + R_f)/(R_1R_fC)}{s + 1/R_fC} \tag{4–6}$$

### 4.4.2 Voltage drift

The integrator circuit by the design of the op-amp has a bias current, an offset current, and an offset voltage. These quantities, in addition to the measured signal, are integrated and cause an increasing linear offset over time in the integration output, known as drift (described in Section 3.3). It was presented in Figure 4-5.

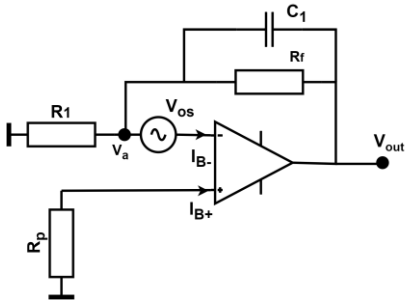



Figure 4-5 : Op-Amp total offset voltage model

The mathematical models are described. Offset voltage $V_{off}$, $IB_+$, as bias current in the non-inverting connection, and $I_{B-}$, as bias current in the inverting connection.

$$V_{out}(t) = \ -\frac{\int I_c dt}{C} + V_a(t) \tag{4–7}$$

$$V_{out}(t) = \ R_f I_{R1}(t) + V_a(t) \tag{4–8}$$

$$I_{c1}(t) = I_{R1} - I_B^- - I_{Rf} \tag{4–9}$$

$$V_{out}(t) = -\frac{1}{C}\int \left[\frac{V_a}{R_1} - I_B^- - \left(\frac{V_{out} - V_a}{R_f}\right)\right] + V_a(t) \tag{4–10}$$

$$OFFSET\ (RTO) = V_{out}(t, I_B, V_{os}) = \frac{1}{R_f C_1}\left[\left(1 + \frac{R_1}{R_f}\right)V_{os} + \left(1 + \frac{R_1}{R_f}\right)R_p I_B^+ - R_1 I_B^-\right](1 - e^{\frac{-t}{R_f C_1}}) \quad (4\text{–}11)$$

The OFFSET (RTO) value describes how the output voltage is due to offset currents and voltages. Both a large capacitor and a high resistance ($R_f C_1$) lead to long charging periods and therefore to a decrease of the drift slope. Although capacitor and resistor values are defined by the bandwidth and integration characteristics, it is possible to attenuate the effect of these voltages and currents by evaluating the input level. Therefore, the input offset value, $OFFSET\ (RTI)$, is defined as follows:

$$OFFSET\ (RTI) = V_{os} + I_{B_+}R_p - I_{B_-}\frac{R_f R_1}{R_f + R_1} \quad (4\text{–}12)$$

$$OFFSET\ (RTI) = V_{os}\ if\ \ I_{B_+} = I_{B_-}\ and\ \ R_p = \frac{R_f R_1}{R_f + R_1} \quad (4\text{–}13)$$

An adequate ratio between the biasing resistors ($R_p$) and the other resistors allows to reduce the input value of the offset voltage of the operational amplifier.

### 4.4.3 Input impedance

The equivalent input impedance circuit is shown in Figure 4-6, the op-amp has been considered to have an infinite impedance at its non-inverting input. On the other hand, it has been considered that the TVS does not have any parallel impedance. In the experimental models, its real impact will have to be evaluated.

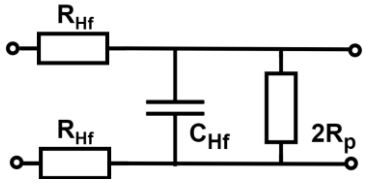



Figure 4-6 : Equivalent input circuit

The final value of the impedance in the Laplace domain is expressed as:

$$Z_{in}(s) = 2R_{Hf} + \frac{2R_p s}{s + \frac{2R_p}{C_{Hf}}} \quad (4\text{–}14)$$

### 4.4.4 CMRR

It is considered that for a CMRR = ∞, the resistance ratio must be $R_1 = R_3$ and $R_2 = R_4$, due to the different configuration of the op-amp in the last section (Figure 4-3). This consideration should be measured in the actual implementation of the circuit [74].

### 4.4.5 Random noise

Thermal agitation of charge carriers in electrical conductors has influence on electronic devices. When electrical resistance is applied at a certain temperature, the inherent randomness of the kinetic energy of the electrons leads to voltage variations known as Johnson noise [75]. Equation (4–15) shows that the power spectral density $E_n(V/Hz)$ of the voltage noise is directly proportional to the absolute temperature $T\ (K)$, the resistance $E_n(\Omega)$, and the observation bandwidth $\Delta f\ (Hz)$. The higher the temperature, resistance or bandwidth, the higher the voltage noise level.

$$E_n = \sqrt{4kTR\,\Delta f} \quad (4\text{–}15)$$

According to [76] integrator circuits, the effect of Johnson noise on the resistors can be neglected, due to the large capacitor connected as feedback. In the final stage of the differential amplifier, the noise introduced by resistors must be calculated.

## 4.5 Circuit simulation

MATLAB has been used in the initial phase to allow simple analysis of circuit behaviour, transfer functions, and characteristics in the Laplace domain. As a design condition, the high capacitor $C_1$ value is set; this causes the resistance $R_1$ values to be as small as possible and mitigates the impact of the offset current. For this purpose, it is set to 10 µF (in the reference [60] the value is 1 µF). The effect of the capacitor on the overall transfer function is to increase the cutoff frequency as its value decreases [77]. The time constant is defined as 20 ms (27 ms in [59]) according to the current curve to be integrated. According to [78] it is described as a criterion that $R_f = 1000 * R_1$. Taking these considerations and the one already described by the transfer function G(s) in Section 4.4.1. The set values are described in Table 4-1.

Table 4-1 : Circuit component values

| Component | Value |
|---|---|
| $R_f$ (MΩ) | 33.4 |
| $R_1$(KΩ) | 3.33 |
| $R_{hf}$ (KΩ) | 33.3 |
| $R_p$(KΩ) | 10 |
| $C_1$(µF) | 10 |
| $C_{hf}$(µF) | 1 |

The exported value was substituted into the integrator function G (s), which providing the transfer function described in Figure 4-7. Signals with frequencies below 50 Hz are attenuated by 1 dB, but not integrated. This behaviour has been achieved by the $R_f$ resistor which prevents low frequency signals from saturating the integrator. All other frequencies are integrated. Phase characteristics over the entire integration range are important, as this avoids different delays depending on the signal being measured. At low frequencies there is some transition from 0 to 90 degrees, and it stays static over most of the integration range.

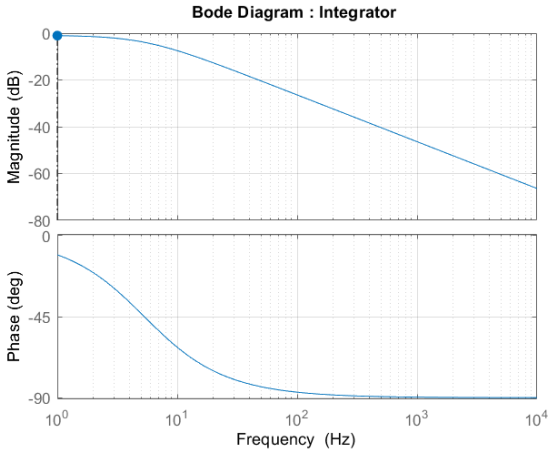



Figure 4-7 : Frequency response of the theoretical model of the integrator and the low-pass filter

A similar circuit shown in Figure 4-3 was implemented in the MATLAB tool through Simulink® and Simscape™. The selected values from Table 4-1 were substituted. The expected current curve was recreated, and a derivative function was applied to it, obtaining the signal expected by the Rogowski coil; this signal was connected to the circuit and the signal at the output of the integrator was similar to that of the plasma currents illustrated in Figure 4-8, results that were expected according to the simulated specifications.

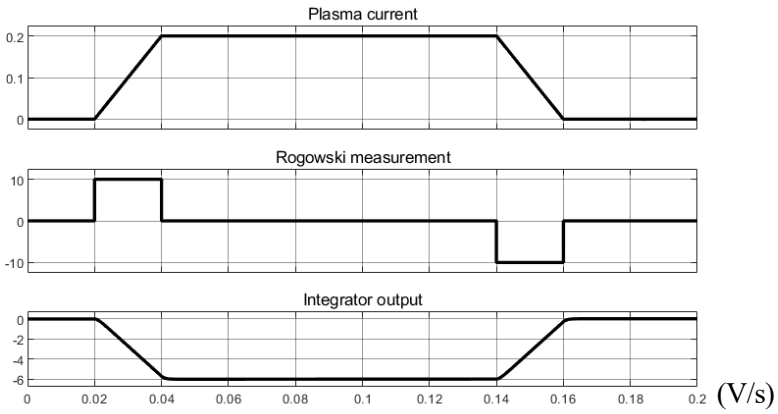



Figure 4-8 : The results of the curves of the theoretical circuit simulated in Simulink®

A higher fidelity of reality was achieved with the LTspice® electronic circuit simulator which is a powerful free software from the distributor Analog Devices. The op-amp models specified (ADA4522-1) are the same as those used in the simulation including non-ideal characteristics. This simulation has provided a better understanding of the behaviour of the complete system. The study circuit was made according to the architecture presented in Figure 4-4, for further clarification see Annex B.

First, a verification test was performed with the same input signal (Rogowski measurement) on the circuit used in the MATLAB simulation (Figure 4-8). In the real component simulation presented in Figure 4-9 an offset voltage was also found at the output not higher than 150 µV, conforms with the requirements imposed, and that the integration is perfectly obtained, thus the plasma current with the characteristic shape.

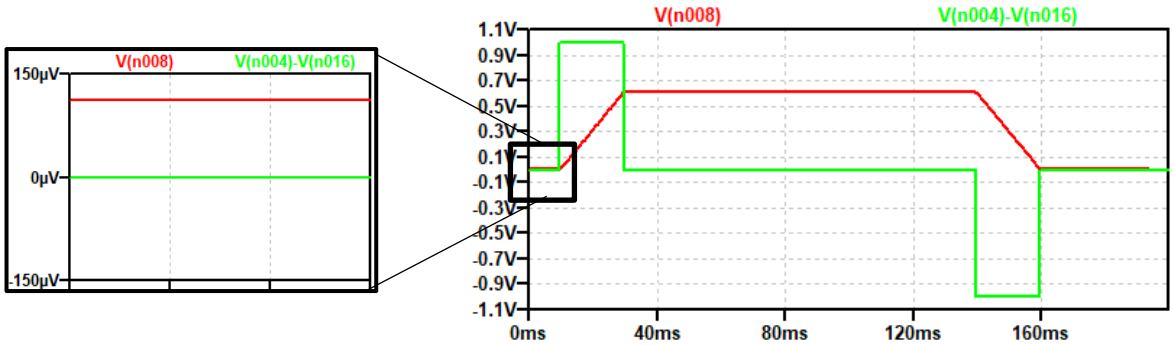



Figure 4-9 : Result of integration into LTspice simulation.

Red line the input signal; green line the input signal.

The frequency response is shown in Figure 4-10, and values that differ somewhat from those exported in the theoretical model expressed in Figure 4-7 have been obtained; this is due to the readjustments that have had to be made to the component values.

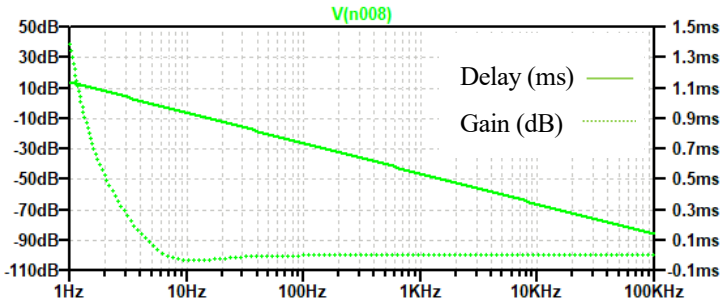



Figure 4-10 : Frequency response of the complete system in the LTspice simulation

There has been a vertical shift in the frequency response upward as the value of the resistance $R_f$ has increased. The latency of the system is <800 ns over the full bandwidth of 10 Hz to 100 kHz.

The noise density of the circuit has been evaluated. This noise comes mainly from the installed resistors, a high value or a high temperature leads to a higher noise level (previously described in Section 4.4.5). In Figure 4-11 is described the noise level of the whole circuit.

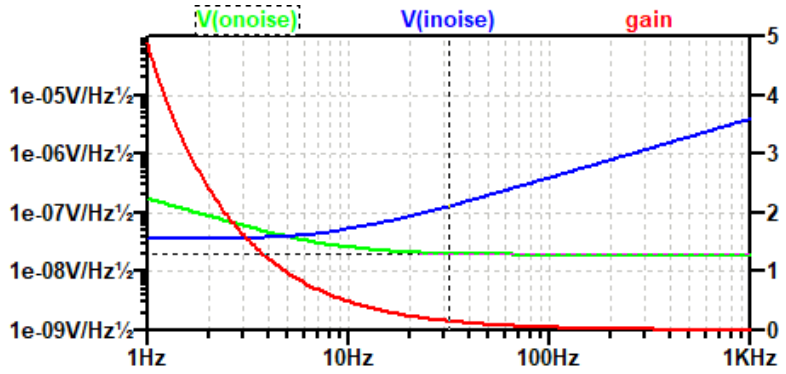



Figure 4-11 : Voltage Noise Density vs Frequency LTspice simulation

The total rms noise level at the output (green line) is 6.04 V. in the range from 1-100 kHz. The allowed input noise level (blue line) must be below 72.224 mV rms; in this case, the output noise will be less than 6.04 µV and will be masked by the noise of the integrator circuit itself. The gain of the system is described by the red line; it works as a low-pass filter, as described in the integration function, with the noise level it has the same behaviour.

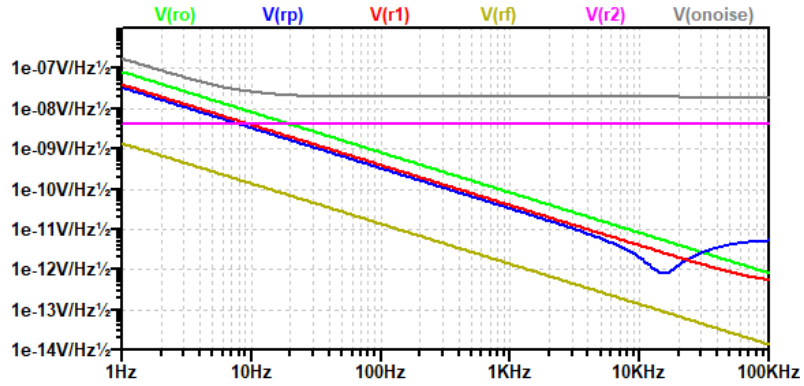



Figure 4-12 : Contribution to noise density by individual resistors

The spectral density of each individual resistor was obtained to evaluate the influence of each resistor as described in Figure 4-12. The major contribution between 0-19.6 Hz is provided by the resistor associated with the low-pass filter circuit (green line). In the rest of the band, the major influence is provided by the amplifier resistors in differential configuration (pink line).

Table 4-2 : Individual noise density values of installed resistance

| **Component** | **Voltage(rms)** |
|---|---|
| $R_f$ | 1.34 nV |
| $R_1$ | 38.72 nV |
| $R_o$ | 80.53 nV |
| $R_p$ | 32.72 nV |

An analysis was performed to evaluate the effect of the drift. For this purpose, it was simulated in transient mode for 200 s (with short-circuited input signal). As described in 4.4.2, it has an exponential response until it reaches a value determined by the offset currents and voltages and the ratio of the connected resistors. The results at the output of each op-amp are depicted in Figure 4-13 according to the voltage reference of Figure 4-3. Taking into account the output of the two op-amps, which is very similar, it tends to a final value of 0.537 mV, starting from an initial voltage of -3.737 mV, with the time constant value as the period in which 63% of the final signal $\tau = \sim 22\ \mathrm{ms/V}$ is reached.

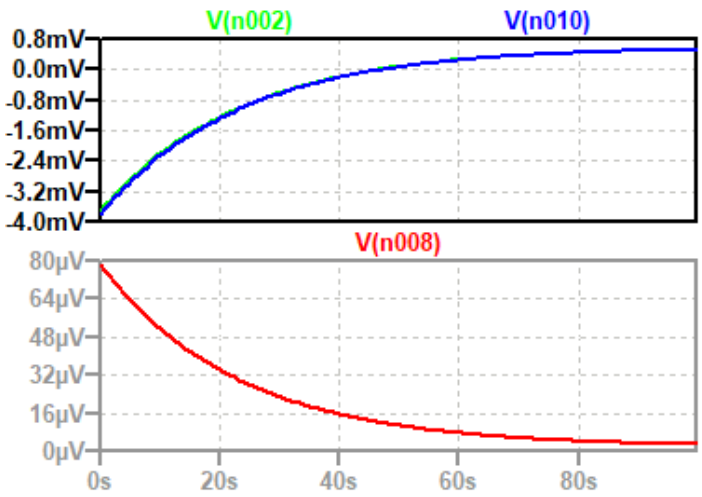



Figure 4-13 : Evolution of drift voltage: op-amp 1 (green), op-amp 2 (blue) and Output(red)

The difference between the two integrated signals is described by the red line in Figure 4-13, which represents the voltage at the output of the operational amplifier in differential configuration. The differential voltage starts around 80 µV but tends to zero as the current flowing through each of the integrators decreases. This characteristic needs to be studied in more detail experimentally to evaluate the real impact of these currents and voltages. It is suggested that the system could evolve to steady state, and thus the reference could be taken as an offset and not as a drift. The value at the output of the complete circuit is 27.351 µV rms. This simulation does not consider the effects caused by the temperature rise of the components or the effect of their tolerances.

## 4.6 PCB circuit construction

For the first prototype, a through-hole component design was proposed. This approach facilitates the re-deployment and monitoring of all installed components. Elements that would not be replaced, such as the temperature sensor or the driver for the relays, were surface-mounted components. For the design of the printed circuit board, a simple free online programme known as EasyEDA was used. This programme has a large repository of elements and datasheet that are linked by an internal distributor.

Basic design rules were used for the PCB design. The board consists of 4 layers, distributed in: signal, +12V, -12V, and GND. For correct isolation, an individual DC/DC supply was used for each integrator board. This is a feasible solution to increase the galvanic isolation between the signals and the rest of the power supplies. Its dimensions are 100*80 mm, it has a width of 1.6 mm (±10 %), constructed with FR4-Standard Tg 130-140 material and with an Outer Copper Weight of 1 oz. These characteristics are based on economic criteria and imposed specifications, in accordance with the supplier standards (JLPC).

For the assembly of the components, the following steps will be taken:

- PCB cleaning: in this case, it was not necessary because the PCB supplied was vacuum packed and cleaned at the factory. It is always necessary to check the cleanliness of the solder area to facilitate the soldering process and allow the solder to distribute correctly.
- SMD parts assembly: the smaller surface mount elements were assembled first (Figure 4-14). For this, the SMD stencil (Solder paste stencil) supplied by the PCB manufacturer was used to place the solder paste on each pad correctly. The solder used was Chipquik® smd291. All electronic components were placed and soldered with a heated air tool according to the soldering curves provided by the manufacturer.

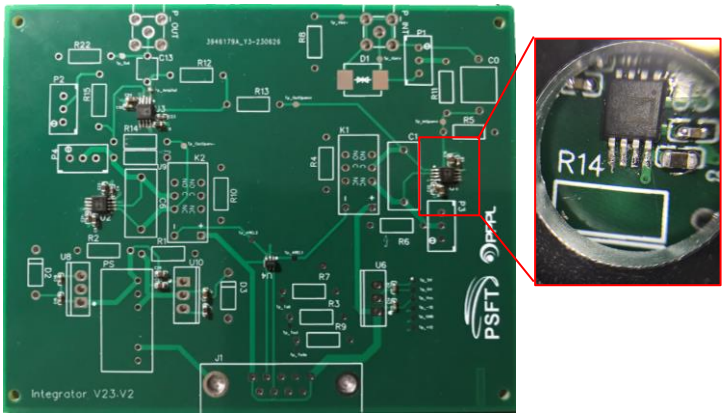



Figure 4-14 : Assembly of SMD components

- Assembly of Through-Hole parts: larger components with through-hole technology are placed last. Soldering iron and tin wire were used for their placement (Figure 4-15).

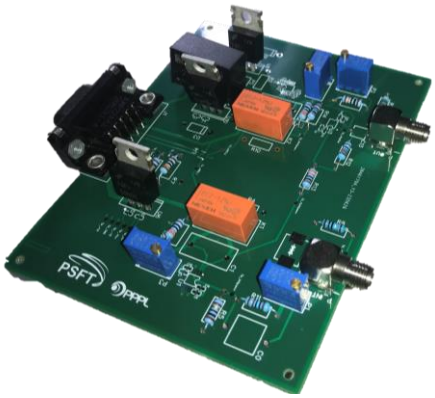


Figure 4-15 : Assembly of through-hole components

- PCB cleaning: Finally, the board is cleaned to remove any flux or subcompounds generated in the soldering process, using a generic product based on a synthetic solvent for this purpose.

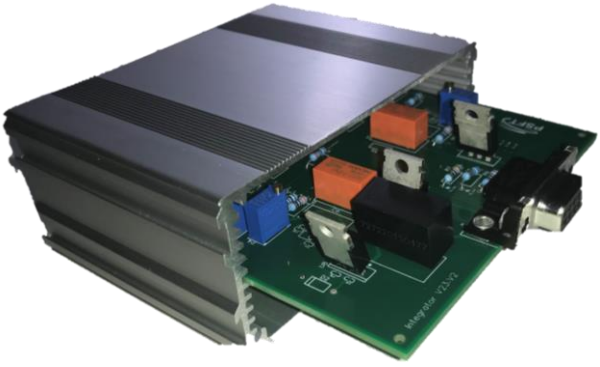


Figure 4-16 : PCB inside the shielding case

The final prototype is enclosed in a metal box to shield electromagnetic noise (Figure 4-16). It has the signal inputs and output at one end, and the control part is at the other end. This design has been made to be able to take this same architecture for embedded systems where the control is done on the back of the board. In Figure 4-17 shows the layout of the inputs and outputs when the box is closed. The power supply as 12 V and GND, the signals to drive the relays as REL1, REL2, and the sensor output signal.


Figure 4-17 : Layout of input and output signals

# 5 PCB TESTING

This section describes the tests that will be performed to verify the correct functioning of the physical PCB. According to the theoretical studies and simulations performed, it is necessary to evaluate its frequency response, drift, and noise level. For further clarification, see Annex A.

## 5.1 Wiring test

Before installing the components, the points described in Table 5-1 must be checked for short circuits and errors in layout design. The method is through continuity and with the use of a multimeter in continuity mode.

Table 5-1 : Measurement points for the wiring test

| **Measurement point** | **Reference point** |
|---|---|
| Input pad +12 V RS AC/DC | Tp_VCC |
| Input pad GND RS AC/DC | Tp_0V |
| Output pad GND RS AC/DC | Tp_GND |
| Output pad +15V RS AC/DC | Int U8 |
| Tp_12+ | Out U8 |
| Tp_GND | GND U8 |

On larger PCBs, impedance, capacitance, and resistance tests are usually performed after all components have been assembled. This process allows to detect deviations and distortions, as well as to prevent possible design or component failures at very early stages of the manufacturing process, reducing the economic cost in case of failure. In this case, this technique has not been implemented due to the simplicity of the circuit, but it should be considered for future designs of greater complexity.

## 5.2 Power supply test

Once the connection test has been performed, the components are soldered in accordance with the described design and the circuit is connected through the VCC and 0V inputs. With a multimeter in the voltage function, the voltage at the test points must be measured according to Table 5-2.

Table 5-2 : Test voltage points and values

| Measurement point | Reference point | Value (V) |
|---|---|---|
| Tp_VCC | Tp_0V | +12 |
| Tp_5V | Tp_0V | +5 |
| Tp_-12 | Tp_GND | -12 |
| Tp_+12 | Tp_GND | +12 |

This test is performed to correctly assess that the supply voltages of the entire board are correct.

### 5.2.1 Power quality test

At this stage, the quality of the entire power supply stage must be examined. With the use of an oscilloscope, the noise level reached in each power supply stage should be measured. For this operation, the measuring points described in Table 5-2 should be taken. A high noise level can cause coupling to the signal that is measured through the op-amps. In addition, the DC-DC converter must have a minimum load to function correctly. It is important to perform these checks so that they do not introduce errors in the following tests described below.

## 5.3 Relay test

Relay system are one of the main parts of this integrator; without their correct operation, it is not possible to integrate successfully at the right time. This test allows to see that they work correctly and that the installed DRDNB21D-7 driver (U4) is compatible. For control, the board must be powered (VCC, 0V). To activate K1, REL1 must be connected to 5V, and to activate K2, REL2 must be connected to 5 V (see Annex C). A small mechanical connection sound should be produced. The internal connection of the contacts can be verified through the pads of each relay by referring to the manufacturer's datasheet on their connections. It is recommended to verify with a thermographic camera the temperature evolution of the DRDNB21D-7 component in operation.

## 5.4 Noise and drift test

With the PCB powered and the relays in the normally closed position (Rel1, Rel2, Off) the voltage at the output of the board will be measured, the integrators will behave as voltage followers, and the differential amplifier will function as designed. The output voltage will show the level of noise introduced by the components. Considering that there is noise radiated to the board and to the measuring instruments.

For drift evaluation it will be necessary to connect the board and short-circuit the signal input. With the oscilloscope connected to the output, the REL1 and REL2 signals shall be activated for 100 s; the output voltage (P_out) shall be the drift voltage.

## 5.5 Integration test

This section describes the main functionality of the circuit, the integration function. For this, it must be powered. The input signal must be injected with a signal according to Table 5-3, it is similar to the input signal of the simulation presented in Figure 4-9 or Figure 4-8. At the same time that the signal is connected, the signals of the rest relays must be activated as described in the Table 5-3. Both input and output must be recorded by means of an acquisition system such as an oscilloscope.

Table 5-3 : Integration test signal values

| **Time** | **P_int (V)** | **RE1, RE2 (V)** |
|---|---|---|
| 0 | 0 | +5 |
| 0.01 | +1 | +5 |
| 0.02 | 0 | +5 |
| 0.14 | -1 | +5 |
| 0.16 | 0 | +5 |

The signal measured at the output should be similar to that expected in the simulations (Figure 4-9). At this point, it should be considered whether the integration is in accordance with the expected results and whether or not to validate this design for implementation in the SMART tokamak control system.

# 6 CONCLUSIONS AND FUTURE WORK

## 6.1 Conclusions

All the objectives of this document have been fulfilled successfully. A concise review of the current needs for SMART control has been made, as well as a general review of the state of the art of integration systems with main application in nuclear fusion.

The requirements for the design of analogue integrators have been defined, and their theoretical behaviour has been evaluated by means of simple mathematical models. The evaluation of these models has allowed to obtain the values of some essential passive components for the circuit. Simulations of these values have been conducted in LTspice to evaluate if the requirements imposed are complied with.

Similar curves to those in operation have been simulated and responded with an excellent level of integration, near-zero latency over the entire bandwidth. A noise analysis has been performed, and it is below the limits imposed by the specifications. The drift has been measured and is below the imposed levels.

Therefore, it is concluded that the architecture presented, works according to the theoretical models and the simulations carried out, which has made it possible to have an integrator with the same characteristics as the bibliography presented but with greater simplicity and, therefore, a reduction in costs and latency than the existing integrators.

## 6.2 Future work

The following tasks are defined as a continuation of the work described in this document.

- The next steps are to connect the board in a real environment and to perform real drift and operation tests. It is expected to gain experience from these tests and thus improve future designs of greater complexity and train engineers in this field.

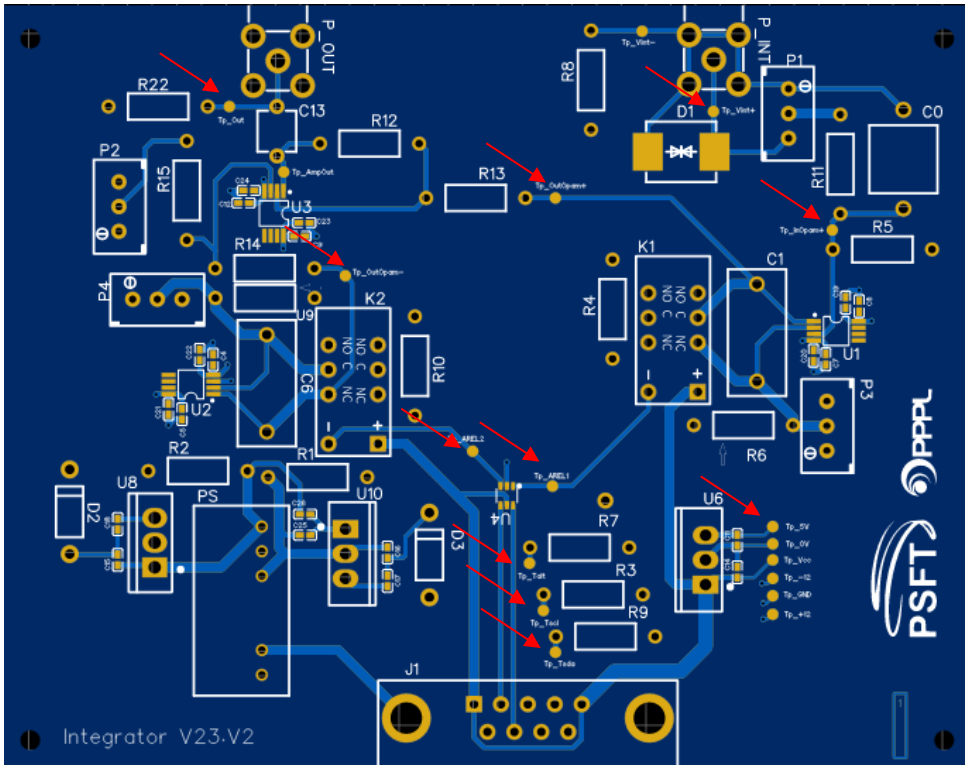
- It is anticipated that embedded systems with a larger number of inputs and functions will be able to be developed, facilitating remote operation, calibration, and commissioning, as well as error detection and redundancy.

- Further research is expected to bring together the necessary components to realise a real-time plasma monitoring system. New institutions see SMART as an opportunity in this field and are expected to develop these with possible collaborations.

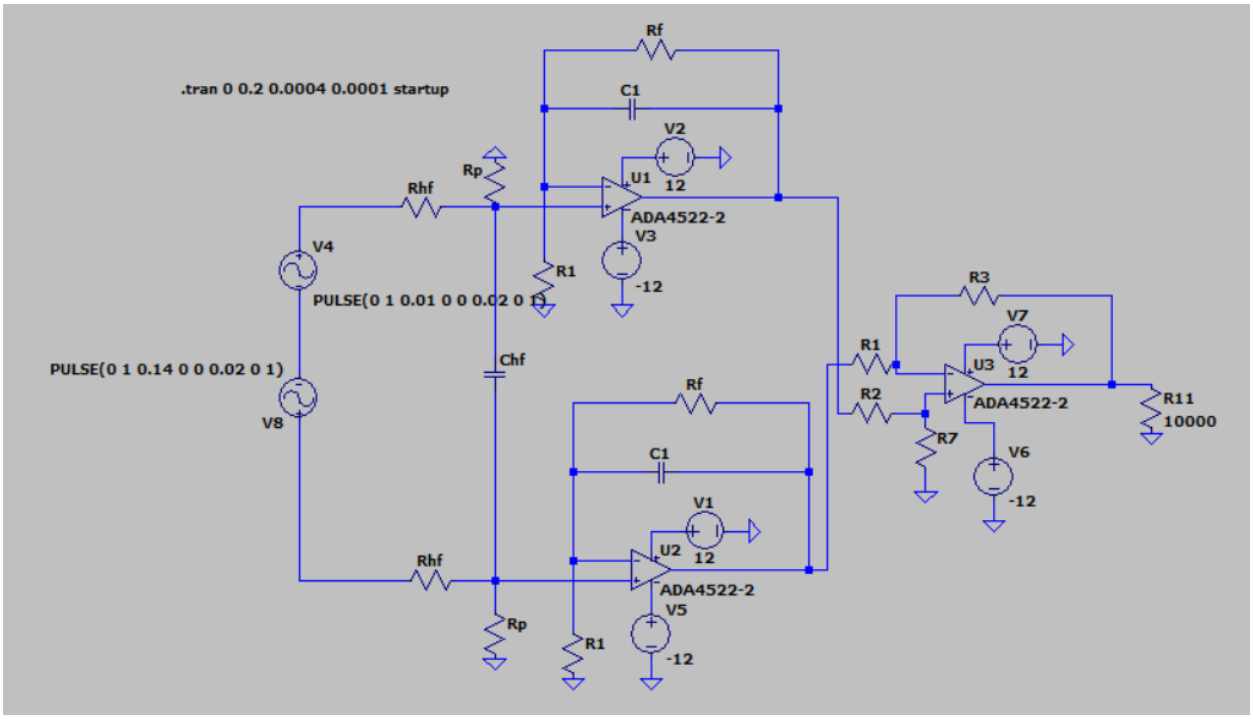
# ANNEX A

Test points on a PCB, or Printed Circuit Board, are strategic locations designed to facilitate verification and diagnosis of potential circuit problems. These points are often connected to critical power or signal sources to perform voltage, current or digital signal measurements during manufacturing, assembly, or maintenance. This appendix describes the points used and their location on the board.

| **Test point** | **Description** |
|---|---|
| Tp_Vint+ | Input signal + |
| Tp_Vint- | Input signal - |
| Tp_InOpam+ | U1.1 Input |
| Tp_OutOpam+ | U1.2 output |
| Tp_inOpam- | U2.1 input |
| Tp_OutOpam- | U2.1 output |
| Tp_Out | U3.1 output |
| Tp_5V | Output signal + |
| Tp_0V | ext. 5V ref. |
| Tp_Vcc | ext. GND ref. |
| Tp_-12 | ext. 12V ref. |
| Tp_GND | PCB -12V |
| Tp_+12 | PCB GND |
| Tp_+15 | PCB +12V |
| Tp_-15 | PCB +15V |
| Tp_Talt | PCB -15V |
| Tp_Tscl | ext. ALT T. sensor |
| Tp_Tsda | ext. SCL T. sensor |
| Tp_AREL1 | ext. SDA T. sensor |
| Tp_AREL1 | ext. relay |

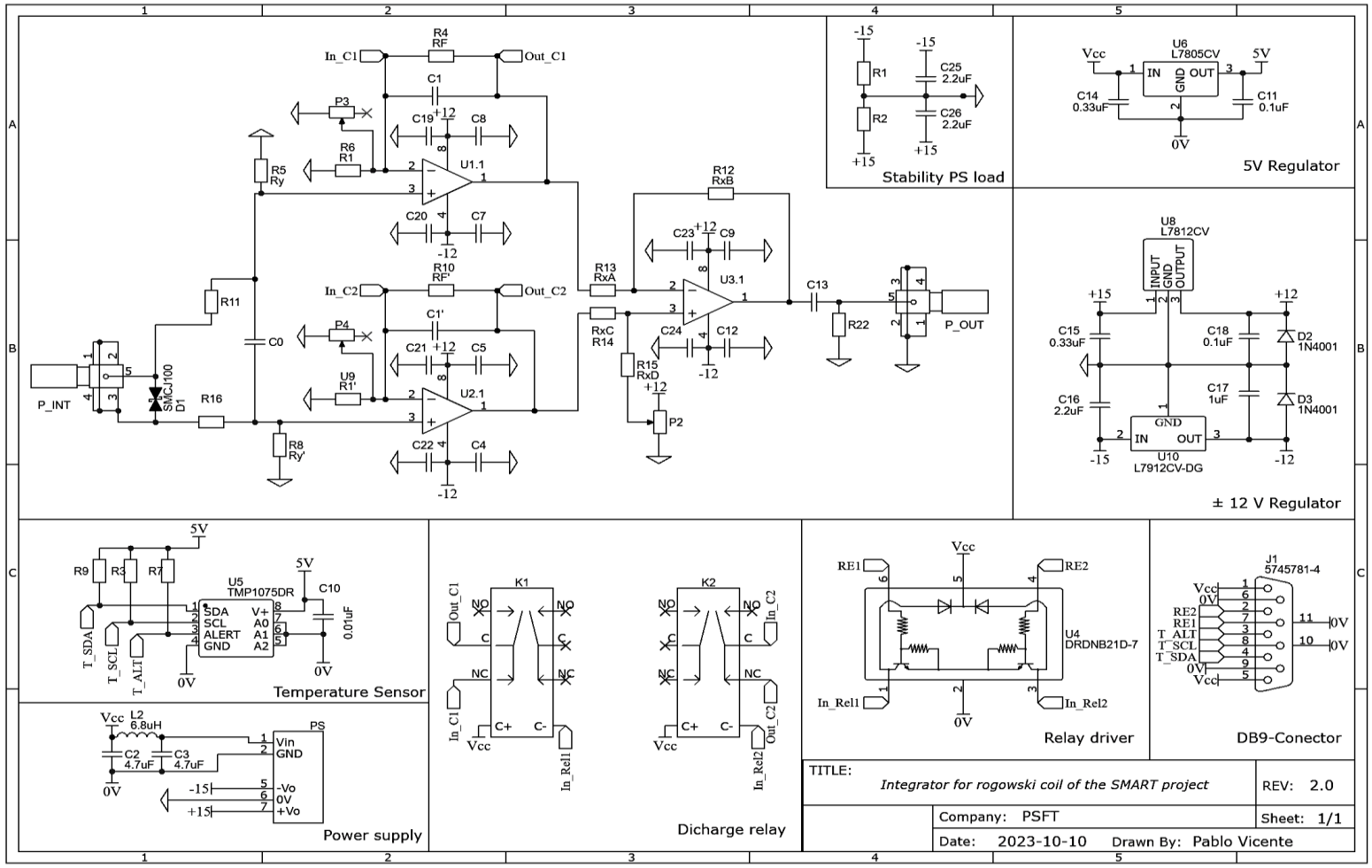

P_OUT
P_INT
P1
P2
P3
P4
R22
C13
R12
R13
R8
D1
C0
R15
U3
R14
R11
R5
C1
K1
K2
R4
U9
C6
R10
U1
U2
R2
R1
R6
U8
PS
U10
U4
R7
R3
R9
U6
D2
D3
J1
PSFT
PPPL
Integrator V23.V2

# ANNEX B




Circuit model in LTspice

# ANNEX C




PCB schematic

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