Fully differential implementation of a Delta-Sigma Modulator based on the Pseudo-Pseudo Differential Technique

Elena Cabrera-Bernal, Fernando Muñoz, Antonio Torralba, Clara Luján-Martínez

Abstract— Flicker noise and distortion are the main limitations in biomedical applications, especially for Switched Capacitor implementations, where the flicker noise is folded into the signal band. To remove the flicker noise and increase the linearity, the Pseudo-Pseudo Differential (P2D) technique has been proposed, where a single-ended signal is processed in a differential way. This paper presents the first silicon implementation of a second order Comparator-Based Switched-Capacitor (CBSC) delta-sigma modulator based on a variation of the P2D technique. Experimental results in a standard 180 nm CMOS technology show an improvement of 10 dB in the Peak SNDR, 5 dB in the DR, and 9 dB in the SFDR over its pseudo differential counterpart, which is the preferred differential implementation for CBSC circuits. Moreover, it is achieved with a reduction in the power consumption.

Keywords— Differential circuits, analog-to-digital conversion, switched-capacitor circuits, delta-sigma modulators, pseudo-pseudo differential circuits.

1. INTRODUCTION

Switched Capacitor (SC) circuits have been widely used since the early days of integrated electronics. They find application in filters [1], power converters [2], and analogue-to-digital converters [3], among others. Differential signal processing is usually preferred when targeting high performances, as it achieves large signal swing, high linearity, and immunity against extrinsic disturbances. Moreover, some of the problems that arise in the implementation of SC circuits, such as those caused by charge injection are significantly attenuated in a differential implementation. However,

in addition to an increase in area and power consumption, a differential circuit has a larger intrinsic noise than its single-ended counterpart.

Even so, a larger Dynamic Range (DR) is still achieved because the differential circuit has twice the signal range than its single-ended version [4]. Concerning linearity, a differential implementation eliminates the even order harmonics if the two branches of the differential circuit perfectly match. Unfortunately, the downscaling of technology aggravates the mismatch problem.

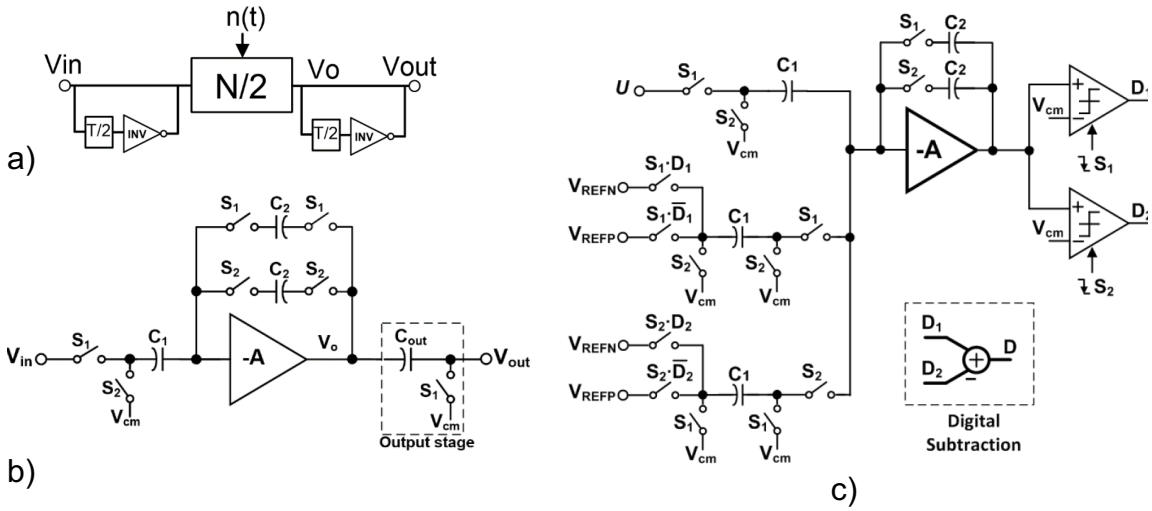

Fig. 1. (a) P2D circuits. (b) P2D integrator [6]. (c) P2D 1st order ΔΣ modulator [7].

A new Pseudo-pseudo differential (P2D) technique has been recently proposed to process a single-ended signal in a differential way, reusing the same single-ended circuitry in different clock phases [5]-[7], Fig. 1(a). In its original implementation [5], a single-ended input was applied in both clock phases with inverse polarity to an alternating integrating capacitor, providing a single-ended output. In [6], Fig. 1(b), the alternating integrating capacitor was replaced by two integrating capacitors with a subtracting output stage. Even more, in [7], the subtracting output stage was removed in the implementation of a 1st order Delta-Sigma (ΔΣ) modulator, so that the analog

part of the modulator provided the positive and negative values of the output signal in successive clock phases, Fig. 1(c). Authors did not mention how to deal with the output common-mode, as they only provided simulation results. In every case a Correlated Double Sampling (CDS) effect was achieved that attenuates low frequency non-idealities such as flicker noise and amplifier offset. Moreover, the same sampling capacitor was used in both phases, which also attenuates the mismatch problems owned to conventional pseudo-differential structures.

In this paper, the Single-ended Processing Differential (SeP-D) technique is presented, where both, input and output, are differential signals processed by the same single-ended (SE) circuitry in alternating clock phases. The proposed technique maintains the advantages of differential processing. The SeP-D technique can be considered to be a variation of the P2D one, where input and output are differential signals, and just like other P2D techniques, it has an inherent CDS behavior, and low harmonic distortion.

This paper is organized as follows. In Section 2 the proposed technique is introduced. Section 3 describes the design of a Comparator Based SC (CBSC) $\Delta\Sigma$ modulator using the SeP-D technique in a standard 180 nm CMOS technology. In the authors´ knowledge, this is the first silicon implementation of a P2D circuit ever reported. Section 4 shows some experimental results, and compares them with those obtained with the conventional pseudo differential version of the same modulator. Finally, some conclusions are drawn in Section 5.

2. SINGLE-ENDED-PROCESSED (SeP) DIFFERENTIAL SC CIRCUITS.

There are two basic ways to implement a circuit structure: single-ended (SE) and differential. At the same time, differential structures can be either, pseudo differential

(P-D) or fully differential (F-D). Recently, the P2D technique has been proposed to process a single-ended signal in a differential way (Fig. 1). This paper presents a new technique, termed SeP-D, which is a variation of the P2D technique.

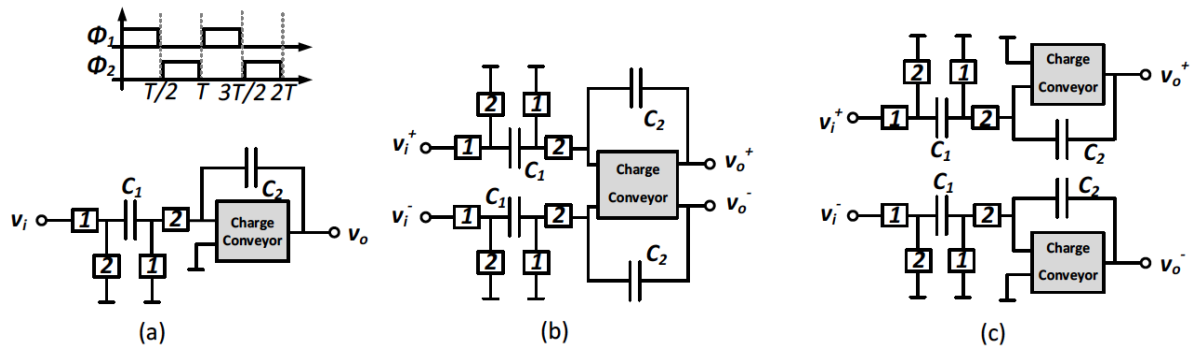

Fig. 2. Classical SC integrator structures: (a) Single-Ended (SE), (b) Fully Differential (F-D), and (c) Pseudo Differential (P-D).

For the sake of simplicity, and without loss of generality, the basic SC integrator is taken as an example. Generic SC integrator structures (SE, P-D and F-D versions) are shown in Fig. 2, where the Charge Conveyor (CC) block is usually implemented with an Operational Amplifier (OpAmp), although other implementations, such as the Comparator-Based one, are possible.

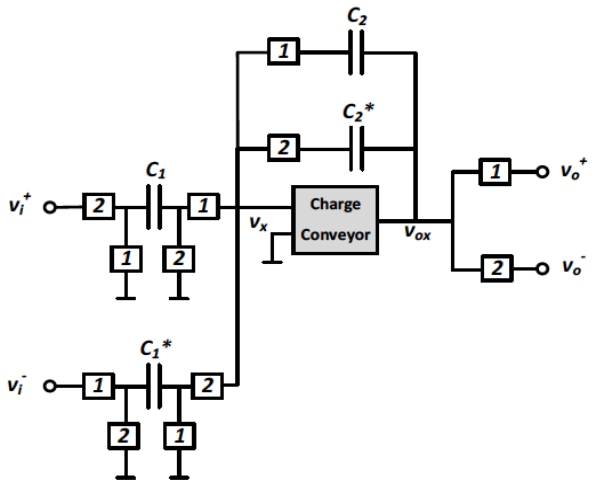

Fig. 3. Single-ended Processed Differential (SeP-D) SC integrator.

In Fig. 3, the proposed SeP-D SC integrator is depicted. This structure achieves a truly differential operation through SE signal processing. Operation is as follows; during Φ_1 the positive branch is in the charge transfer phase, while the negative one is in the sampling phase. The opposite happens during Φ_2.

Unlike P-D structures, in SeP-D circuits the active part (charge conveyor) of both single-ended models (Fig. 3) is implemented with the same circuitry (although in a different phase). When compared to F-D and P-D circuits, SeP-D ones share the same features of large signal swing, high linearity and dynamic range. However, there are two different charge conveyor outputs in F-D and P-D structures, while there is a single output in a SeP-D one. Compared to the P2D implementations of Fig. 1, the SeP-D one maintains differential input and output signals, which facilitates the integration with conventional fully differential circuits and eliminates the non-idealities introduced in the differential to single-ended conversion.

Note that F-D structures are preferred for OpAmp based implementations. On the other hand, P-D structures are preferred for CBSC implementations, since the errors due to comparator and current source non-idealities are translated to the common mode signal, while in a F-D implementation they appear in the differential signal [8].

Since the SeP-D technique is a version of the P2D one, it inherits the same benefits in low-frequency noise and harmonic distortion. In terms of power consumption, SeP-D circuits use the same SE CCs to process both signal branches, so that they must be operational in both clock phases. However, in F-D and P-D implementations the CCs need to be active only during the charge transfer phase, so that some power reduction techniques, like switched-OpAmp, can be applied.

3. COMPARATOR-BASED SWITCHED CAPACITOR ΔΣ MODULATOR

In order to demonstrate the feasibility of the proposed 2nd order structure, a SeP-D CBSC ΔΣ modulator for biomedical applications has been designed and fabricated in a standard 180 nm CMOS technology. To allow a fair comparison between the proposed structure and the classical ones, the P-D equivalent modulator has also been designed and fabricated in the same technology. The F-D structure was not included in the comparison since, in a differential implementation of a CBSC modulator, the P-D structure is preferred [8]. The modulator of Fig. 4, with typical coefficients [9], has been chosen (Table I).

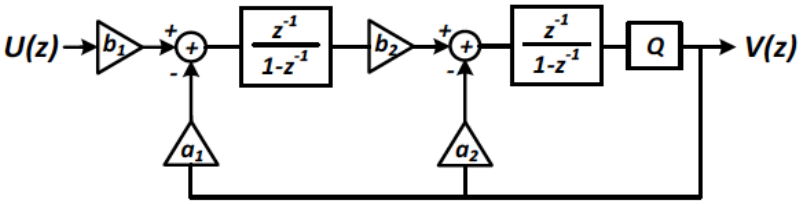

Fig. 4. 2nd order ΔΣ modulator structure.

TABLE I 2ND ORDER ΔΣ MODULATOR DESIGN PARAMETERS

Name	Symbol	Quantity
Integrators coefficients	a_1, b_1, b_2	0.25
	a_2	0.5
Oversampling Ratio	OSR	64
Sampling Rate [Hz]	f_s	12800
Capacitors [pF] (Modulator)	C_1, C_3, C_L	1.5
	C_2, C_4	6
Capacitors [pF] (CMFB circuit)	C_{s_PD}	1
	C_{c_PD}	2
	C_{s_SePD}, C_{c_SePD}	0.5
Voltages [V]	V_{DD}, V_{refP}	1.8
	V_{cm}	0.9
	V_{SS}, V_{refN}	0

The implementation of the P-D version of the modulator of Fig. 4 is depicted in Fig. 5. The values of reference voltages and capacitors are also given in Table I. Clock

phases are also depicted in Fig. 5, where Φ_{1a} and Φ_{2a} are the advanced versions of Φ_1 and Φ_2, respectively, P_1 and P_2 are the preset phases required in a CBSC implementation, and Φ_{1q} is the quantizer control signal. For the P-D case, given the quantizer outputs D_{out}^+ and D_{out}^-, the digital-to-analog converter (DAC) decides the feedback voltage (V_{refN} or V_{refP}) to be applied, using control signals A_1, B_1, A_2, B_2 [9].

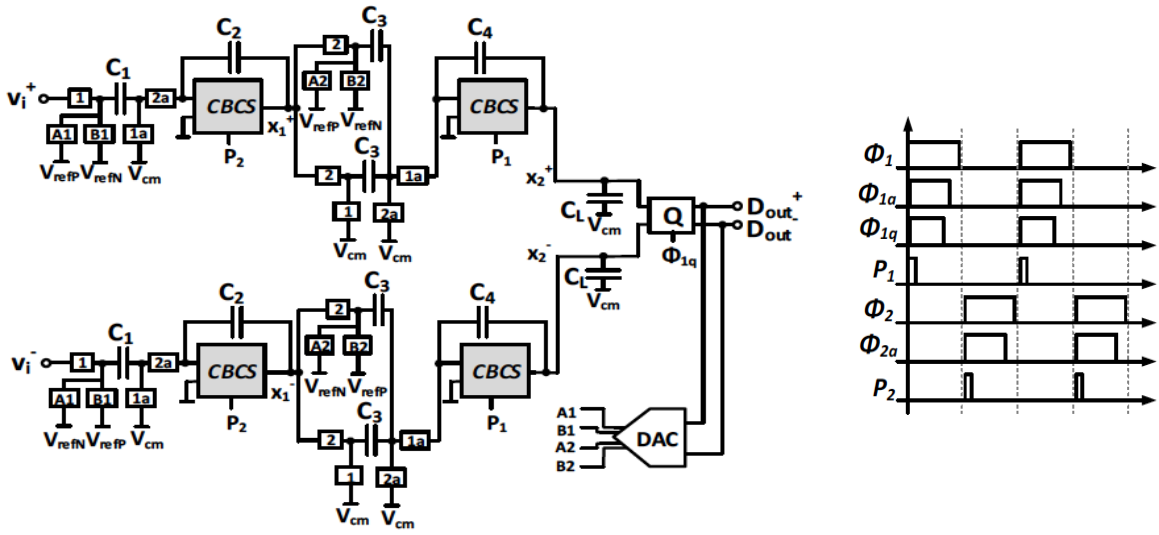

Fig. 5. 2nd order P-D implementation of the ΔΣ modulator and clock phases.

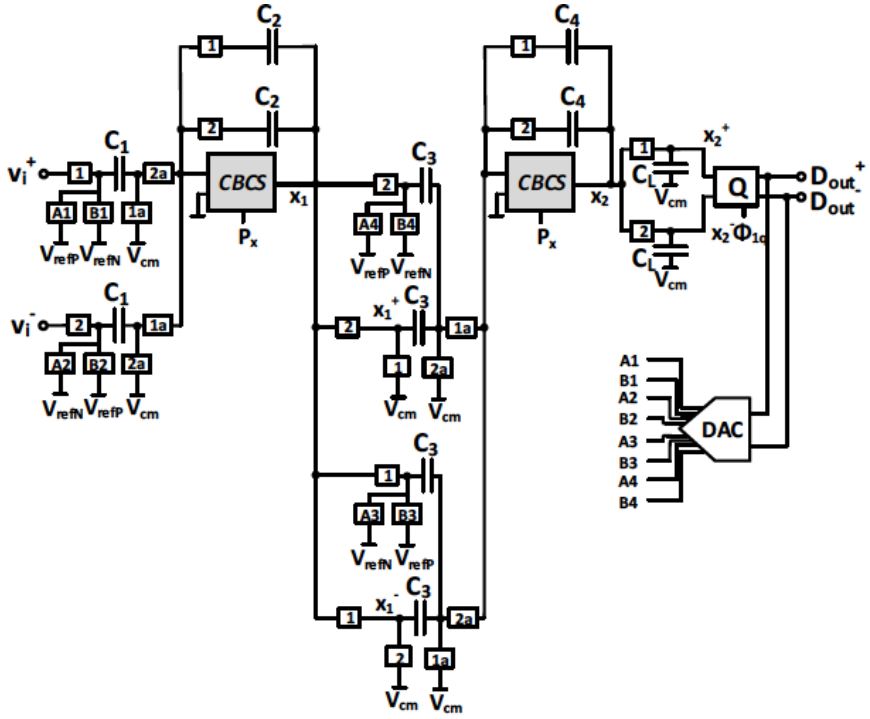

Fig. 6. 2nd order SeP-D implementation of the ΔΣ modulator.

The straightforward SeP-D implementation of the modulator of Fig. 4 is depicted in Fig. 6. Capacitor values and reference voltages are the same as in the P-D implementation. However, the timing of the SeP-D implementation forces a change in the modulator structure, as it will be explained next.

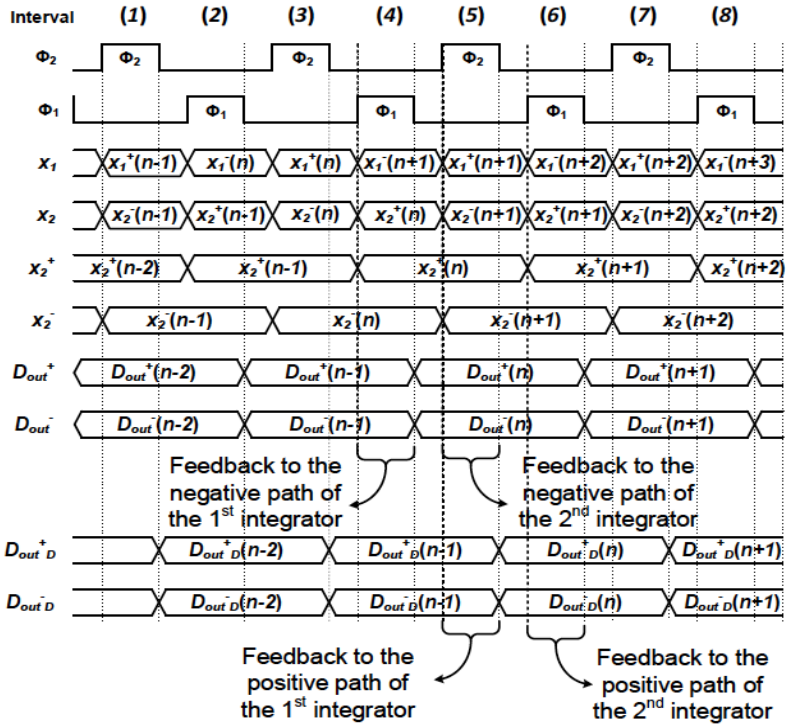

Fig. 7. 2nd order SeP-D ΔΣ modulator timing.

Fig. 7 shows the timing of the SeP-D modulator. Once again, given the quantizer outputs D_{out}^{+} and D_{out}^{-}, the DAC has to decide which feedback voltage (V_{refN} or V_{refP}) is to be applied to each integrator in the two signal paths. It can be observed that it is in the falling edge of Φ_1, interval (*4*), when the quantizer input signals corresponding to the *n*-th period, $x_2^{+}(n)$ and $x_2^{-}(n)$, are available.

For the first integrator, the outputs $D_{out}^{+}(n)$ and $D_{out}^{-}(n)$ should be available during intervals (*4*) and (*5*), but, as shown in Fig. 7, at interval (*4*), $D_{out}^{+}(n)$ is not available yet. Due to the sequential operation of the SeP-D modulator, this signal will not be

available until the interval (*5*). This problem can be solved using delayed versions of D_{out}^{+} and D_{out}^{-}, termed $D_{out}^{+}{}_{D}$ and $D_{out}^{-}{}_{D}$, respectively. Then, the first integrator is fed back with $D_{out}(n-1)$, while the second one is fed back with $D_{out}(n)$, as shown in Fig. 7. This means that the SeP-D implementation of the modulator in Fig.4 requires one delay in the feedback path of the first integrator, as shown in Fig. 8.

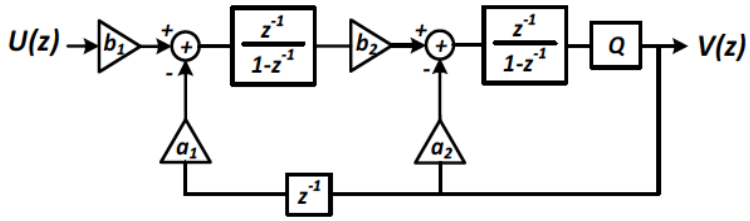

Fig. 8. 2nd order ΔΣ modulator structure with one delay in the feedback path of the first integrator.

Equations (1) show the signal (STF) and noise (NTF) transfer functions for both structures [9]. Subscript *S1* and *S2* stand for the structures of Fig. 4 and Fig. 8, respectively.

$$STF_{S1}(z)=\frac{b_1b_2}{z^2+z(a_2-2)+(1+a_1b_2-a_2)} \qquad STF_{S2}(z)=\frac{b_1b_2z}{z^3+z^2(a_2-2)+z(1-a_2)+(a_1b_2)}$$
$$NTF_{S1}(z)=\frac{z^2-2z+1}{z^2+z(a_2-2)+(1+a_1b_2-a_2)} \qquad NTF_{S2}(z)=\frac{z(z^2-2z+1)}{z^3+z^2(a_2-2)+z(1-a_2)+(a_1b_2)} \quad (1)$$

Given the coefficient values $a_1 = b_1 = b_2 = 0.25$ and $a_2 = 0.5$, the corresponding pole-zero and Bode plots are shown in Fig. 9 and Fig. 10, respectively.

According to Fig. 9, the modulator *S2* has one additional pole and zero, and its conjugate complex poles are closer to the unit circle; still, it is a good approximation to the original modulator (*S1*). In order to better estimate the impact of these changes in the transfer functions, some simulations have been carried out. Fig. 11 shows the

SNR and SNDR (Signal-to-Noise-plus-Distortion Ratio) versus the relative input signal amplitude for a 30 Hz input signal.

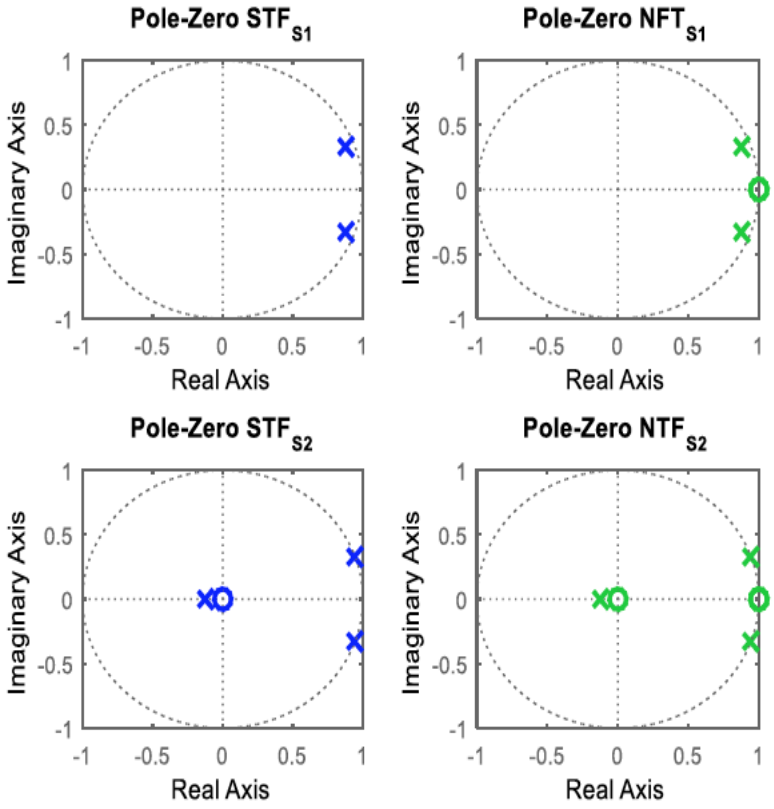

Fig. 9. Pole-Zero plot of the STF and NTF of the 2nd order ΔΣ modulators. Upper row: modulator *S1* in Fig. 4. Lower row: Modulator *S2* in Fig. 8.

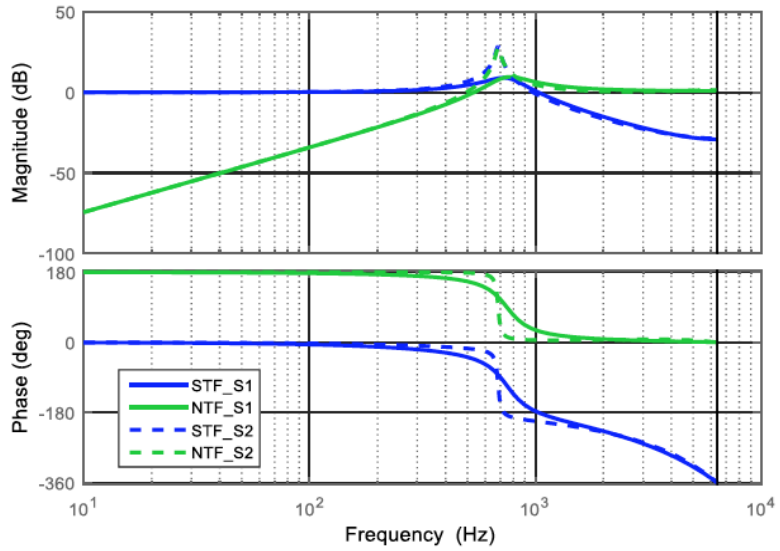

Fig. 10. Bode plot of the STF and NTF of both 2nd order ΔΣ modulators.

It can be seen in Fig. 11 that the SNR and SNDR curves of modulator *S2* have their maxima for amplitudes smaller than those of the original modulator *S1*.

At this point there are two design options:

1) To maintain the modulator coefficients in the SeP-D implementation, so that both implementations share the same components (comparators, current sources and capacitors), but they implement different transfer functions, or
2) To re-compute the modulator coefficients in Fig. 8 to implement a pole-zero map as similar as possible to the original modulator in Fig. 4, changing the components in the SeP-D implementation accordingly.

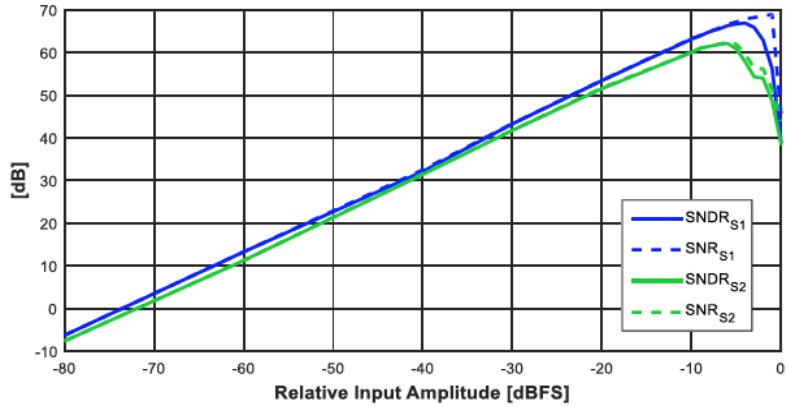

Fig. 11. Simulated SNDR and SNR versus input amplitude of both modulators.

The first option was selected here, since it is the one that allows a comparison of both modulators with the same components, despite the fact that this is the worst case, in terms of performances, for the proposed SeP-D implementation. The second option will be explored in Appendix A.

The implementation of the modulators in Fig. 5 and Fig. 6 is detailed next.

A. Charge Conveyor

The CBSC Charge Conveyor is shown in Fig. 12. Both, the P-D and SeP-D modulators use the same CC.

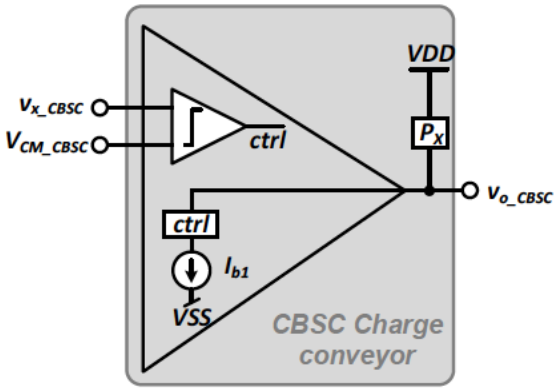

Fig. 12. CBSC Charge Conveyor.

In the preset phase the switch controlled by P_x is closed, taking v_{o_CBSC} to the most positive voltage V_{DD}. In this way, the node v_{x_CBSC} will start the charge transfer phase with a voltage higher than V_{CM_CBSC}. Later, this switch opens and the preset phase ends. The current source I_{b1} is then connected to the *CC* output and discharges the capacitors connected at the *CC* output until the virtual ground condition happens, i.e., until $v_{x\_CBSC} = V_{CM\_CBSC}$. At this moment the comparator output, *ctrl*, is activated, the current source I_{b1} is disconnected from the output, and the charge transfer phase ends. The current source I_{b1} is implemented as a simple cascode current source, and the comparator is a two-stage amplifier.

B. Common Mode Feedback Circuit (CMFC)

Unlike the charge conveyor, which is the same for both, the P-D and SeP-D implementations, the common mode feedback circuit (CMFB) differs from one implementation to another due to the timing difference that exists between both structures. The classical CMFB implementation for a P-D integrator depicted in Fig. 13(a) provides the well-known common mode voltage control signal of Eq. (2).

$$V_{cm\_ctrl} = \frac{C_{s\_PD}}{(C_{s\_PD} + C_{C\_PD})} \cdot \frac{(x_1^+ + x_1^-)}{2} \tag{2}$$

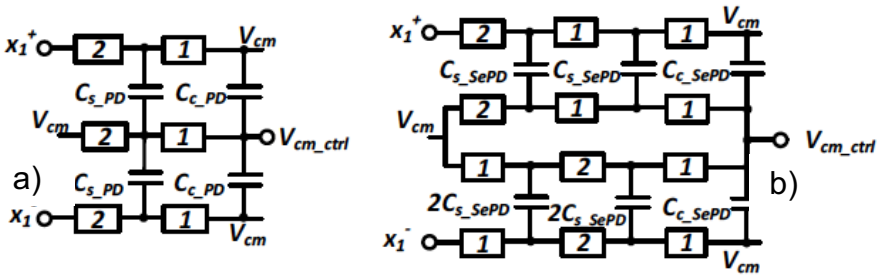

Fig. 13. CMFB circuits: (a) For the P-D integrator, and (b) for the SeP-D one.

For the proposed SeP-D implementation, a modified version of the classical CMFB circuit is proposed in Fig. 13(b) that provides the common-mode voltage of Eq. (3). For capacitor values in Table I, V_{cm_ctrl} has the same value in Eq. (2) and Eq. (3).

$$V_{cm\_ctrl} = \frac{C_{s\_SePD}}{(2C_{s\_SePD} + C_{C\_SePD})} \cdot \frac{(x_1^+ + x_1^-)}{2} \tag{3}$$

In Fig. 14 the related timing for the first integrator is shown. Dummy capacitors can be used to balance the loading in both signal branches.

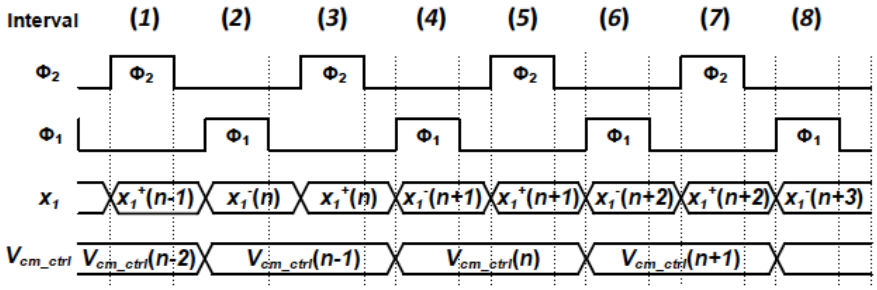

Fig. 14. Timing of the CMFB circuit for the first integrator of the SeP-D structure.

C. Digital to Analog Converter (DAC)

Due to the previously discussed timing differences between the P-D and SeP-D modulators, the DAC implementations are different, Fig. 15. The DAC SeP-D must generate an output for each integrator and phase, while in the PD modulator, the DAC only need to generate two outputs, one per integrator.

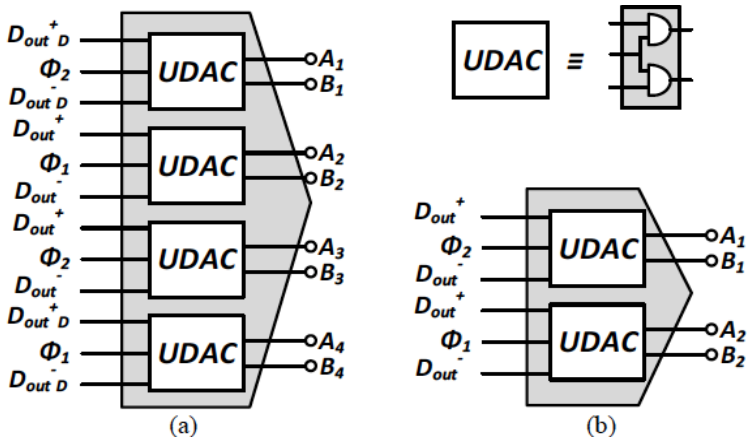

Fig. 15. DAC implementation: (a) SeP-D modulator, and (b) P-D modulator.

4. EXPERIMENTAL RESULTS

Both modulators were fabricated in a standard 180 nm CMOS technology in different chips of the same multiproject run, Fig. 16. Ten samples per design were tested. Fig. 17 shows the output Power Spectral Density (PSD) for a sinusoidal input of -11 dBFS and -16 dBFS for the SeP-D and P-D modulators, respectively. These are the amplitudes where the best SFDR was measured in both modulators. As expected, the noise floor in the SeP-D modulator is lower than in its P-D counterpart.

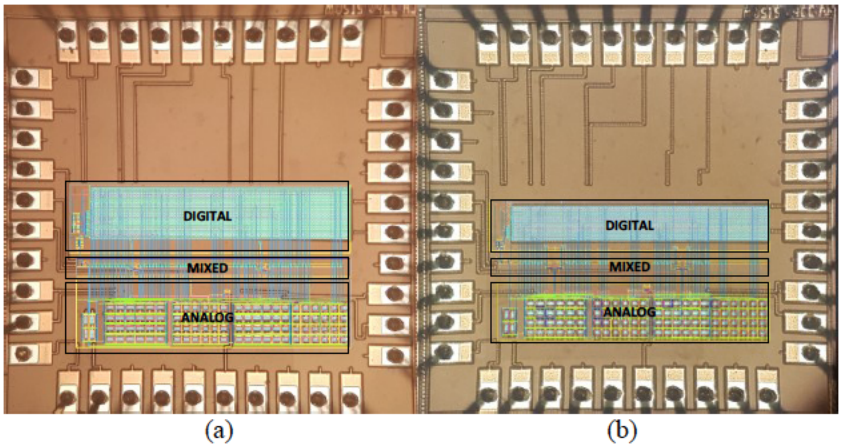

Fig.16. Chip microphotographs: (a) SeP-D modulator, and (b) P-D modulator.

Fig.18 shows the average SNR and SNDR curves versus the relative input signal amplitude at 30 Hz for both modulators, along with their 1-σ band. The SeP-D version shows lower noise than the P-D version. It also has a lower variability (i.e., a narrower 1-σ band) due to the attenuation of the flicker component.

The average measured performances are summarized in Table II. An increase of 10 dB in the peak SNDR is achieved, as well as 5 dB in the DR, and 9 dB in the SFDR. Using the Figures Of Merit proposed by Schreier [9] (FOM_S) and Walden [10] (FOM_W) where, once again, the SeP-D modulator obtains better results.

$$FOM_S = SNDR + 10\log\left(\frac{BW}{P}\right) \qquad FOM_W = \frac{P}{2BW \cdot 2^{\frac{SNDR-1.76}{6.02}}} \tag{4}$$

TABLE II MEASURED PERFORMANCES (AVERAGE VALUES FOR 10 SAMPLES)

Modulator version	**P-D**	**SeP-D**
Voltage Supply [V]	1.8	
Power Consumption [μW]	*8.86*	*6.43*
Sampling rate [Hz]	12800	
OSR (Oversampling Rate)	64	
Peak SNDR [dB]	*53*	*63*
DR [dB]	*62*	*67*
SFDR [dBc]	*61*	*70*
FOM_S [dB]	*123.8*	*135.3*
FOM_W [pJ/step]	*117.2*	*26.59*

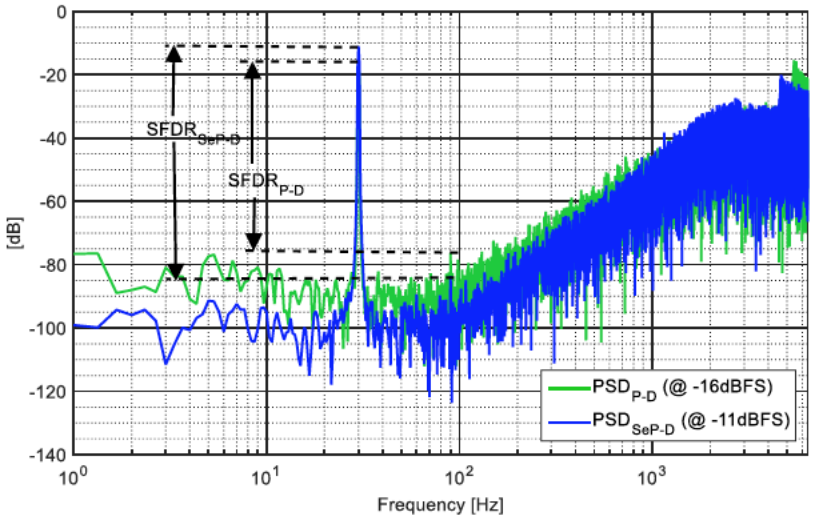

Fig. 17. Measured output PSD showing the SFDR in both modulators.

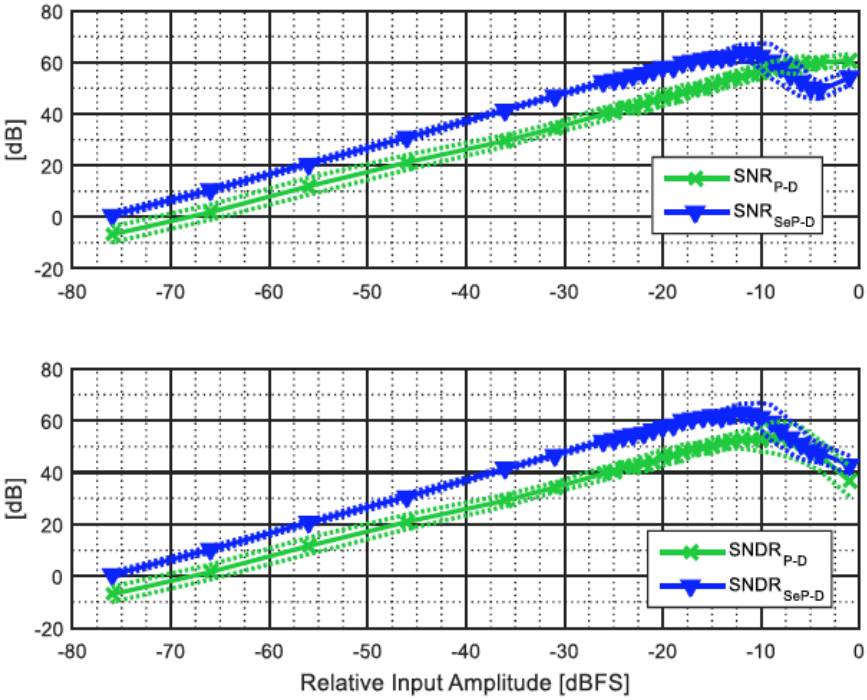

Fig. 18. Measured average SNR and SNDR curves versus input signal amplitude, along with the 1-σ band.

It should be mentioned that no power reduction techniques were applied to the P-D version; thus, its quiescent power consumption is twice as much as that of the SeP-D one, except for the contribution of the biasing circuits. Note that, even if the P-D

version had been implemented with a similar power consumption (by using a power reduction technique like switched OpAmp), both FOMs would still have been better for the SeP-D version, due to its larger SNDR peak. Moreover, the SeP-D version implements a modulator with a transfer function less favorable than its P-D counterpart. If, as stated above, its coefficients were recomputed to implement similar transfer functions, it would yield even larger DR and peak SNDR.

TABLE III COMPARISON WITH OTHER RECENT ADC CONVERTERS DESIGNED FOR BANDWIDTHS BELOW 1KHz

	This Work	**[11]**	**[12]**	**[13]**	**[14]**	**[16]**	**[17]**	**[18]**	**[19]**	**[20]**
Type	CBSC	Incr.	Incr.	SDSC	SDSC	SAR	VCO	SAR	Incr.	SDCT
Year	2018	2013	2013	2015	2016	2016	2016	2017	2018	2018
Tech. (m)	180n	160n	160n	180n	0,35u	55n	40n	180n	160n	65n
Power Cons [µW]	6,43	20	6,3	505	127	15,7	7	2,7 e-3	278	0,8
Sampling rate [Hz]	12,8K	1,33K	50K	150K	640K	1M	3K	1K	2M	32K
OSR	64	1	2000	750	320	500	8	1	1000	32
Peak SNDR [dB]	63	-	-	100,6	-	101	74	48,3	118,1	66,2
DR [dB]	67	-	-	-	136,3	-	-	-	120	92
SFDR [dBc]	70	-	-	100,8	-	105	79	60	-	-
SNR [dB]	-	81,9	119,8	110	-	104	-	-	119,1	-
FOM_S [dB]	135,3	157,1	182,8	153,6	165	179	148,6	161	183,7	154
FOM_W [pJ/step]	26,59	1,47	0,31	28,8	12,3	0,08	4,27	0,012	0,21	0,48

Although the objective of this work is to show the advantages of the proposed technique for SC circuits when compared to the conventional ones, the fabricated converter is near the state of the art for this kind of converters. Table III shows the most recent SC-SD converters [13], [14] with a bandwidth lower than 1kHz reported

in the Murmann ADC survey [15]. Both the Walden (FOM_W) and Schreiber (FOM_S) Figures of Merit show that our converter has similar or slightly lower values than those converters. Note that this work has deliberately not compensated the decrease of performances due to the appearance of an unwanted delay in the feedback path, that would have increased the DR in, approximately, 9 dBs. Even more, the active blocks have been slightly oversized in order to avoid possible second-order effects, since we focused our attention only in proposed technique. In any case, as shown in [11]-[12] and [16]-[20], it is well known that SC-SD converters are not the best candidates for such very low bandwidths.

5. CONCLUSIONS

In this paper, a new structure for the implementation of differential SC circuits is proposed, where the positive and negative components of the differential signal are processed by the same single-ended active circuitry. The proposed technique, called Single-Ended-Processed Differential (SeP-D) technique, can be considered to be a version of the Pseudo-Pseudo Differential (P2D) one, where the input and output are differential signals. Just like the P2D circuits, when compared to a conventional differential implementation either pseudo-or fully- differential, SeP-D circuits feature lower distortion and less noise. As a proof of concept, a 2^{nd} order, SeP-D CBSC $\Delta\Sigma$ modulator for biomedical applications (100Hz bandwidth) has been fabricated. Experimental results have confirmed the feasibility of the proposed technique, being the first silicon implementation of a P2D $\Delta\Sigma$ modulator.

Despite an additional delay in the feedback path of the first integrator, an average increase of 10 dB in the SNDR peak, 5 dB in the DR, and 9 dB in the SFDR have been achieved when compared to the pseudo-differential implementation of the same

modulator in the same technology. Additional improvements would be expected if the coefficients of the SeP-D version were recomputed to compensate for the change in the modulator structure.

APPENDIX A

Re-computing the coefficients of the modulator of Fig. 8 (*S2*), a pole zero map closer to that of the classical modulator of Fig. 4 (*S1*) can be obtained. In Fig. 19 simulation results obtained with $a_1 = 0.25$, $a_2 = 0.375$, $b_1 = 0.25$, and $b_2 = 0.5$ (*S2,new*), are plotted along with those of structures *S1* and *S2*.

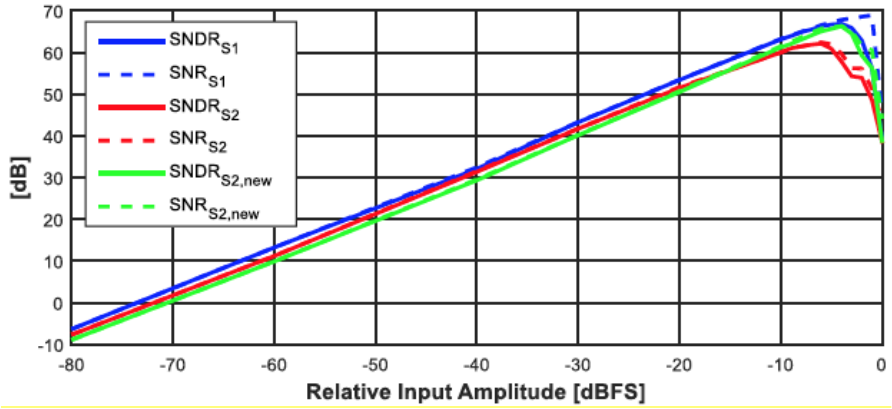

Fig. 19. Simulated SNR and SNDR curves for the three 2nd order ΔΣ modulators.

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Vitae

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Passport-type Photographs

			
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