A Robust and Automated Methodology for the Analysis of Time-Dependent Variability at Transistor Level

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***Abstract*- In the past few years, Time-Dependent Variability has become a subject of growing concern in CMOS technologies. In particular, phenomena such as Bias Temperature Instability, Hot-Carrier Injection and Random Telegraph Noise can largely affect circuit reliability. It becomes therefore imperative to develop reliability-aware design tools to mitigate their impact on circuits. To this end, these phenomena must be first accurately characterized and modeled. And, since all these phenomena reveal a stochastic nature for deeply-scaled integration technologies, they must be characterized massively on devices to extract the probability distribution functions associated to their characteristic parameters. In this work, a complete methodology to characterize these phenomena experimentally, and then extract the necessary parameters to construct a Time-Dependent Variability model, is presented. This model can be used by a reliability simulator.**

Keywords—time-dependent variability, TDV, random telegraph noise, RTN, bias temperature instability, BTI, characterization, hot-carrier injection, HCI, CMOS, reliability, simulation

I. INTRODUCTION

In the last years, Time-Dependent Variability (TDV) has become an important concern for both analog and digital circuit designers due to its growing impact on circuit reliability [1]. TDV comprises both transient effects, such as Random Telegraph Noise (RTN) [2], and aging phenomena, such as Bias Temperature Instability (BTI) or Hot-Carrier Injection (HCI) [3], [4].

RTN, BTI and HCI have been associated to the stochastic trapping/detrapping of charge carriers in/from defects present in the oxide or silicon-oxide interface of the devices. These defects can be originated during the manufacturing process or generated during the device operation [5]. All these phenomena cause shifts in the transistor parameters. These shifts display a discrete and stochastic nature in deeply-scaled CMOS technologies, and originate variations in the circuit performances over time [6], [7].

To mitigate the impact of the different TDV effects on circuits, it is crucial to develop reliability simulators to predict how these TDV phenomena will affect the performance of a given circuit over time. Such a simulator must include a model that describes and quantifies these phenomena in an accurate manner. And, to construct this model, the TDV effects must be characterized experimentally at device level to extract the necessary parameters.

Due to the afore-mentioned stochastic behavior of TDV phenomena, their experimental characterization must be performed in a massive manner, which means that hundreds or even thousands of transistors must be characterized under different conditions. These include both nominal conditions (in the case of RTN tests) and stress conditions, where voltages over the nominal value of the technology are applied (in the case of BTI and HCI tests) to age the circuits in an accelerated manner. This accelerated aging allows to study in feasible experimental times phenomena that would require much longer times (i.e., months or years) under nominal operating conditions. This massive characterization gives rise to challenges of different nature, mainly in terms of the experimental setup and the processing of the characterization data.

The experimental setup used for the TDV characterization includes a transistor array chip with a large number of devices, therefore reducing the total area needed in opposition to wafer level approaches, which require an individual pad for each terminal of each device. The setup must also fulfill a set of requirements, such as the possibility of applying accurately different temperatures and voltages (accounting for the unavoidable IR drops between the

chip pads and the individual device terminals), or measuring a large number (i.e., thousands) of transistors in feasible times. The first transistor array that allows the massive characterization of all phenomena, RTN, BTI, HCI and Process Variability (PV), was introduced in [8], together with a fully-customized experimental setup presented in [9]. Each sample of the characterization chip contains more than 3,000 transistors, which enables an extensive study of the variability phenomena at transistor level. However, this characterization results in enormous amounts of data, which must be analyzed to extract the parameters needed to model the different TDV phenomena. Some techniques have been presented to this end [10]. However, these techniques are often not adequate for the analysis of such extensive amounts of experimental data, since they require supervision of the user, which makes unfeasible their utilization to analyze the thousands of current traces that are generated during the RTN, BTI and HCI experiments [11]. To overcome this issue, in this paper we present the TiDeVa tool, which enables the automated and robust analysis of RTN, BTI and HCI phenomena. TiDeVa extracts from the characterization data the parameters necessary to fit a TDV model without requiring any human supervision. This automation enables this process, which would otherwise be prohibitive in terms of time.

The rest of the paper is structured as follows. In Section II, the different TDV phenomena are described, and the parameters needed to characterize them are highlighted. After that, in Section III, an overview of the complete reliability characterization, modeling and simulation flow is presented, including the IC and characterization setup used in this work, the characterization strategy, the TiDeVa parameter extraction tool, the TDV model and the reliability simulator. Then, in Section IV, the focus is brought to TiDeVa's underlying methodology, which is explained in a greater detail. Finally, in Section V, conclusions are drawn.

II. TDV Phenomena

A. Random Telegraph Noise

The impact of RTN on circuit performance has been reported for circuits such as SRAMs or Ring Oscillators [12]. Moreover, this impact is expected to increase as technology continues to scale [13].

RTN is observed as sudden and random discrete jumps in the drain current of the transistor. These jumps have been associated to changes in the threshold voltage linked to the trapping/detrapping of charge carriers in/from defects in the device. The parameters that characterize an RTN signal are the number of active defects in the transistor, the amplitude of the current jumps (or analogously the amplitude of the threshold voltage shifts) associated to each of these defects, and their time constants. These constants are the capture time (τ_c), which is the average time that a defect takes to capture a charge carrier when it is empty, and the emission time (τ_e), which is the average time that an RTN defect takes to emit the charge carrier once it is occupied. Fig. 1 shows an example of measured RTN trace linked to one defect (i.e., two current levels) with its parameters indicated.

B. Bias Temperature Instability

Bias Temperature Instability is a gate-voltage and temperature activated aging phenomenon that consists in the gradual degradation over time of transistor parameters. Its effect on circuit reliability has been extensively reported [6]. The degradation caused by BTI has a permanent component, and a recoverable component, meaning that the device partially recuperates its original characteristics when the stress decreases. For technology nodes in the nanometer range, BTI displays a discrete and stochastic nature, which has been associated to the charge/discharge of individual defects during high/low gate voltage phases [3]. It is widely accepted that the defects responsible for RTN and for BTI have the same nature [14]. Currently, the BTI phenomenon in deeply scaled technologies is described by defect-centric models, which are able to account for its stochastic nature [15], [16], [17]. One of these models is the Probabilistic Defect Occupancy model (first presented in [15]), which is the one used in this work. This model uses the transistor parameter shifts associated to each captured defect, and the capture and emission time constants to describe the occupancy probability of a defect under given bias and temperature conditions. This, combined with the number of defects per device, allows to calculate the expected transistor parameter shifts under different operating conditions. These parameters, namely amplitudes of the transistor parameter shifts, time constants and number of defects per device, can be extracted from the characterization data.

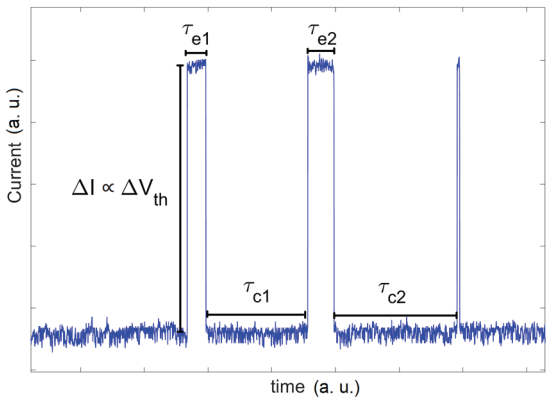

Fig. 1. Measured current trace displaying RTN transitions corresponding to a single defect.

C. Hot-Carrier Injection

Hot-Carrier Injection is both gate- and drain-voltage activated. Like BTI, it causes the progressive degradation over time of device parameters, which translates into the degradation of circuit performances. The degradation of the device parameters is due to the injection of highly-energetic charge carriers into the oxide, and it also has both a permanent and a recoverable component. It can be described with a defect-centric model such as the PDO model.

III. A Complete Reliability Characterization, Modeling and Simulation Flow

Fig. 2 displays the flow diagram for the development of Reliability-Aware Design (RAD) solutions in a schematic manner, indicating also a simple taxonomy of each stage and the combination of expertise that RAD involves. The main steps of this process are the experimental characterization of the TDV effects, the modelling of these phenomena, and the simulation of circuit reliability taking into account these phenomena. The reliability simulation then allows the designer to study and to take into account the impact of TDV phenomena on a given design (e.g. following an optimization-based approach or with a knobs-&-monitors solution). TiDeVa, the solution presented in this paper, and as Fig. 2 points out, helps bridging the flow between the TDV Characterization phase and the Modeling phase. In this Section, the approach taken in this work for this flow (all but the final reliability-aware design phase, out of the scope of this paper) is described.

A. Characterization Setup

The setup used for the experimental characterization of the different variability phenomena discussed in this

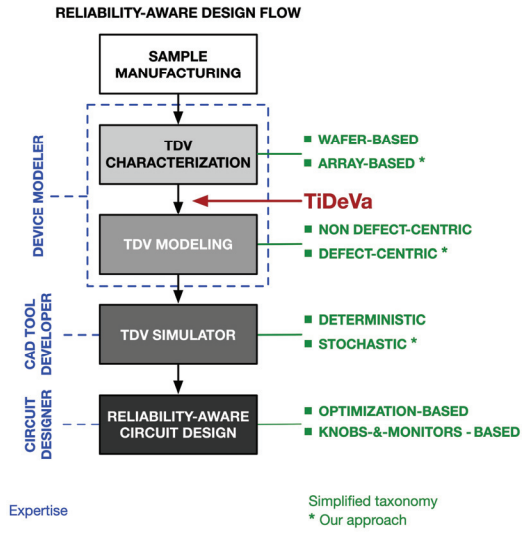

Fig. 2. Block diagram for the development of RAD solutions, indicating a simple taxonomy of each stage and the different areas of expertise that RAD involves.

work comprises a characterization chip [8], and a dedicated, customized experimental setup [9], the schematic representation of which is depicted in Fig. 3. There is a set of requirements that this characterization system should fulfil to enable an adequate characterization of TDV phenomena:

- Due to the stochasticity of TDV phenomena in transistors in the nanometer range, and to the necessity of studying different phenomena, the transistor array should include a large number of devices so that statistically significant results can be obtained for each of these phenomena. Furthermore, both NMOS and PMOS transistors should be included.
- The characterization chip and the experimental setup should be designed so that the characterization of the different TDV phenomena, namely RTN, BTI and HCI, together with PV, is possible.
- The characterization system should allow individual access to each device, and the accurate application of the desired voltages, overcoming the voltage drops that may appear in the setup, in particular in array-based IC structures such as the one used in this work, since the TDV phenomena are highly bias-dependent.
- Accurate application of different temperatures should be possible, since TDV is highly dependent on temperature.
- It should allow a smart parallelization approach for the aging (BTI and HCI) tests, since these would otherwise extend over an excessively long period of time. With this parallelization scheme, a large number of devices can be stressed (i.e., voltages over the nominal value of the technology can be applied to them) at the same
- A customized software aimed at the automation of these experiments is fundamental, since its alternatives (manual definition and launching of the tests, or individual input of the commands that control the instrumentation) become unattainable when hundreds or thousands of devices must be measured at varying operation conditions with a known and exact timing.

All these requirements are addressed in a combined manner by the characterization chip and the experimental setup used in this work. The characterization chip reported in [8] was fabricated in a 1.2-V, 65-nm CMOS technology, and has a chip area of 1.8 mm x 1.8 mm. It contains 3,136 MOS devices, half of which are NMOS and half of which are PMOS. The number of transistors per chip is limited by the chip area and the necessary control circuitry surrounding each device. This high number of transistors per chip sample

helps with the statistically-significant characterization that the stochastic nature of the different variability phenomena requires. The architecture of the chip allows the individual access to the terminals of each device under test, thus allowing the study of the different phenomena by applying the desired voltages to the different terminals of a given device. Furthermore, the chip and the semiconductor parameter analyzer included in the setup allow a Force&Sense system that compensates the potential voltage drops that may appear and allows the precise application of the desired voltages. For the temperature application, a T-2650BV Thermonics precision temperature system, which allows the accurate application of temperatures in the range between -40ºC and 170ºC, is employed.

In order to speed up the aging characterization tests described in Section II, a smart parallelization architecture is implemented, by means of which a large number of devices can be simultaneously stressed, while an individual transistor is being measured [9]. Appropriate scheduling of stress, measurement and stand-by periods allows the application of the same stress periods and the measurement of the same recovery phase of every device. This allows to shorten the otherwise unfeasible experimental time to an attainable one.

In order to control the different pieces of equipment shown in Fig. 3, namely the power supply for the chip and the Printed Circuit Board, the Keysight B1500 Semiconductor Parameter Analyzer (to apply the desired voltages and measure the currents), and the Thermonics temperature system (to apply the desired temperature), an IEEE 488.1 GPIB BUS is used. A Data Acquisition System is used to send the signals that control the digital circuitry of the characterization chip. For a normal RTN or aging test, tens of thousands of GPIB command lines are usually needed. Not only that, but a very precise timing must be achieved so that all the transistors in a given test are measured under the exact same conditions. To achieve this, a toolbox for the automatic definition and control of the different tests has been developed [18]. This software works under the Matlab® programming environment, and allows the user to define and launch the desired characterization tests in just a few seconds.

B. Characterization Strategy

To measure RTN in this work, each terminal of a transistor has been kept at a given voltage and the drain current flowing through the device has been measured. This has been done under diverse conditions, e.g. varying V_{GS} and V_{DS}. An example of a real RTN current trace measured for this work is displayed in Fig. 1. This is a simple case with only one detectable RTN defect which causes the current trace to alternate between two

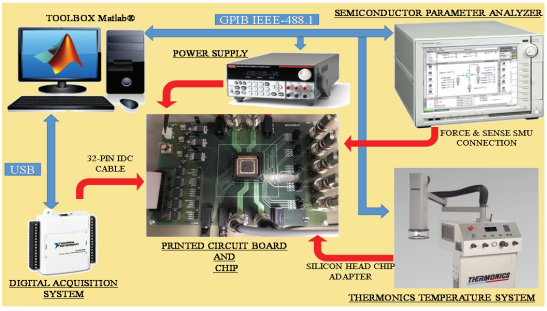

Fig. 3. Schematic representation of the experimental setup used in this work.

levels. The parameters that must be extracted to characterize that RTN signal are the amplitude of the transition, the capture time (average time that the current stays at its lowest level) and emission time (average time that the current stays at its highest level). The analysis becomes obviously much more complex when several defects with different amplitudes and time constants within the same experimental window coexist in the same device.

The characterization of BTI for this work has been performed in the following manner: first, the "fresh" device has been characterized before the stress (i.e., accelerated aging) by means of a drain current vs. gate voltage (I_{DS}-V_{GS}) curve to account for the process variability. Then, successive stress and recovery cycles have been applied to each transistor. During the stress phases, V_{GS} is kept at a high value (between 1.2V and 2.5V for the transistors with 1.2V nominal supply voltage in the 65nm CMOS technology) and V_{DS} at 0V. The duration of the stress phase has been increased exponentially (1s, 10s, 100s, 1,000s…) while the recovery phase duration has been kept constant (usually 100s). After each stress cycle, the current during the recovery phase has been measured, and the discrete current jumps caused by BTI detrapping events have been registered. The goal of the analysis is to extract the information related to the recoverable component (time constants and amplitudes of the emissions) and the permanent component of the degradation. The analysis can become more complex since different phenomena, such as RTN and BTI, may appear together. In Fig. 4, there are two examples of measured BTI recovery traces: at the top, a BTI recovery trace in which only BTI emission transitions are present; and, at the bottom, a BTI recovery trace in which RTN events appear together with the BTI emission transitions.

The methodology employed in this work to characterize HCI is analogous to the one used for BTI, except that V_{DS} is not kept at 0V during the stress phase, but rather is set to a stress value.

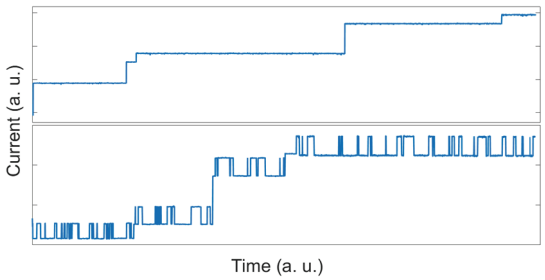

Fig. 4. Measured BTI recovery traces. At the top, only BTI detrapping events are present. At the bottom, the BTI detrapping events are mixed with RTN transitions.

To highlight the importance of the stress parallelization technique discussed previously, a typical BTI or HCI experiment in which 784 devices are characterized with 5 stress-recovery cycles (with stress times of 1s, 10s, 100s, 1,000s and 10,000s, and recovery times of 100s for all cycles) can be considered. Such an experiment would require more than 100 days if no parallelization is implemented. With the parallelization technique presented in [9] and used in this work, the same experiment takes only 4 days.

C. *Parameter Extraction*

The parameters are extracted from the characterization data by the TiDeVa tool [18], which makes use of a Maximum Likelihood Estimation (MLE)-based method. This method allows the fully-automated extraction of the RTN, BTI and HCI parameters, namely time constants and amplitudes of the current shifts, and, in the case of BTI and HCI, also information about the permanent component of degradation. This automation makes the parameter extraction feasible, because otherwise it would be too time consuming. This tool will be discussed in depth later on in Section IV.

D. *Time-Dependent Variability Model*

The parameters extracted with TiDeVa can be used to construct a model for TDV. In this work, they have been used to fit the Probabilistic Defect Occupancy model [15], although they can be alternatively used to construct any other defect-centric model based in the number of defects per device, and the time constants and parameter shifts associated to these defects. The PDO model assigns discrete threshold voltage shifts to charge trapping/detrapping in/from defects in the device. To construct this model, first the distribution of the defects in the (τ_e, τ_c)-space and its dependence on the operation conditions can be extracted from the aging and the RTN experiments. An example of that distribution is shown in Fig. 5. The time constants of a defect determine its occupancy probability under any given conditions. Additionally, the distribution corresponding to the transistor threshold voltage shift associated to each

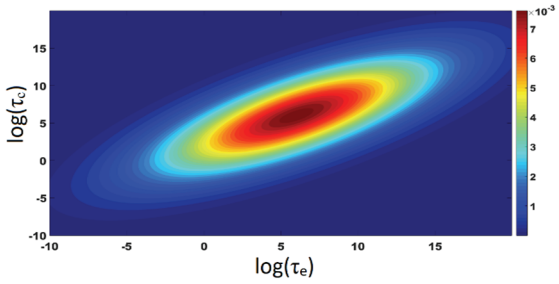

Fig. 5. Example of a defect distribution in the (τ_e, τ_c)-space.

defect is also extracted by TiDeVa from the experimental characterization, as well as the distribution of the number of defects per device. Fig. 6 shows the experimental distribution of threshold voltage shifts associated to RTN defects for one of the measured bias conditions, namely V_{GS} = |1V| and V_{DS} = |0.1V|. All these parameter distributions allow to fill the PDO model while accounting for the stochasticity of these phenomena in nanometer technologies. The model can then be integrated in a simulator to study the effect of these variability phenomena on circuits.

E. *A stochastic reliability simulator*

The challenges that a reliability simulator should address in order to properly deal with nanometer-scale technologies are [19]:

- It should include both a stochastic TDV model to account for the randomness of these phenomena, and a stochastic model for PV, taking into account the combined effect of these two sources of variability.
- It should include the dynamic bidirectional link that exists between aging and biasing (that is, stress) conditions.
- Lastly, it should fulfil all the previous requirements in a computationally efficient manner.

A circuit reliability simulator with a full stochastic model for both PV and TDV has been presented in [20]. It uses the foundry-provided model parameters for PV, and the Probabilistic Defect Occupancy model to

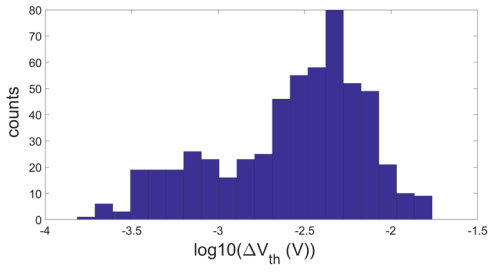

Fig. 6. Experimental distribution of ΔV_{th} associated to RTN defects for PMOS transistors with W = 80nm, L = 60nm, measured at V_{GS} = |1V| and V_{DS} = |0.1V|.

account for the stochastic nature of TDV, being the first reported simulator to take into consideration this combined stochasticity. Based on this model, it is possible to generate a number of transistor samples, each one with a given number of defects, each of which will have a pair of time constants and cause a certain transistor parameter degradation when occupied. In this manner, if the bias and temperature conditions during a given operation time are known, it is possible to simulate if these defects are empty or occupied, calculate the degradation of each transistor sample and, with it, the degradation of the circuit performances.

As it was listed in the set of requirements that a reliability simulator should fulfil, there is a link between aging and biasing. Due to the degradation of transistors during the circuit operation, the transistor biasing and, therefore, the stress conditions, change. To account for this dynamic variation, a number of intermediate time steps are necessary to update the stress conditions. Stress condition calculation and update is commonly performed by using an electrical simulator, e.g. Cadence Spectre [21] or Synopsys HSPICE [22]. The schematic representation of this process is displayed in Fig. 7. The incorporation of a series of intermediate time steps is an option included by most commercial simulators, such as RelXpert (Cadence) [23] or MOSRA (Synopsys) [24]. However, these tools use a fixed time scale (usually a linear or logarithmic distribution of the time steps) that may not fit adequately the general behavior of the degradation. This may result either in a lack of accuracy (if the number of steps is not enough) or in an excess of computational time (if the lack of fitting is compensated with an excessively large number of steps). To avoid this, the reliability simulator uses an algorithm that adapts the size of the time steps with the progressive aging of the circuit [25]. In this manner, an accurate result is achieved while keeping the computational time as low as possible. A dynamic step size has also been used in [26]. However, the simulator used in that work is deterministic, which is not appropriate when technologies in the nanometer range are considered. The adaptive step algorithm presented in the current paper works by setting a threshold value for the degradation of the devices before triggering a re-calculation of the stress conditions. From the degradation of the transistor parameters, the degradation of the circuit performances can be obtained by using a circuit simulator with the suitable analysis types for the performances of interest. Furthermore, this reliability simulator includes a smart technique to speed-up the evaluation of the lifetime of a circuit, according to which Monte-Carlo analysis with a low number of samples are performed until it is estimated that the circuit is close to reaching its lifetime. At this point, Monte-Carlo analysis is performed with a larger number of samples in order to attain more precision [27].

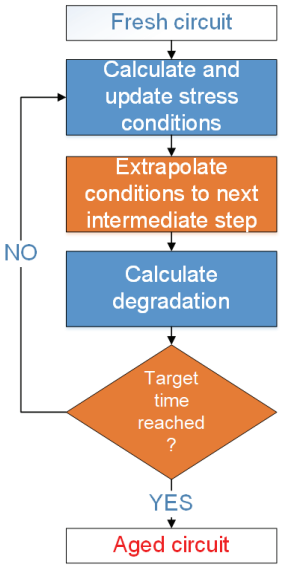

Fig. 7. Simulation flow of the stochastic reliability simulator, which includes a set of intermediate time steps to update the stress conditions to account for the link between aging and biasing.

IV. TiDeVa: A Toolbox for the Analysis of Time-Dependent Variability

The complex characterization setup and the accurate but efficient simulation strategies are useless unless proper procedures for analyzing the thousands of TDV traces are available. TiDeVa is a tool developed to analyze the enormous amounts of data generated during the different TDV tests and extract the necessary information to construct the appropriate models for the TDV phenomena. The tool performs this analysis in a fully-automated manner. Additionally, it is equipped with an intuitive and user-friendly Graphical User Interface (GUI) to facilitate that task. In this Section, the main features of the tool are presented.

A. *The TiDeVa toolbox engine*

To extract the information from the experimental current traces corresponding to RTN, BTI and HCI, TiDeVa uses an MLE-based method [11]. This method estimates the parameters of a statistical model (in this case the current levels of the experimental trace) given the known outcome (in this case, the measured current samples). Assuming that the background noise of the experimental data can be approximated by a Gaussian distribution that is independent of the different current levels, the measured current trace can be reasonably considered as samples of the following probability density function (PDF):

$$f(I|\theta)=\frac{1}{K\sqrt{2\pi\sigma^2}}\sum_{j=1}^{M}A_j e^{\frac{(I-I_{Lj})^2}{2\sigma^2}} \quad (1)$$

where θ is the vector of parameters of the probability density function, σ represents the standard deviation of the background noise, I_{Lj} is the value of each current level, A_j the value of its height, and K a normalization constant so that the area below the PDF is unity. Then, for an experimental trace with N current samples, the joint density function of all observations is:

$$f(I_1,\cdots,I_N|\theta)=\prod_{i=1}^{N}f(I_i|\theta) \quad (2)$$

The likelihood of a set of parameters θ, given the observed results, is equal to the probability of obtaining those results as a function of θ, which means:

$$L(\theta)=\prod_{i=1}^{N}f(I_i|\theta) \quad (3)$$

The goal of the MLE method is to identify the parameter values θ that make the measured data $\{I_1, \ldots, I_N\}$ the most probable, that is, that maximize (3). Note that the number of experimental current samples can amount to thousands or even millions. It is therefore convenient to work with the natural logarithm of (3) to convert the multiplication in that equation into a summation. Since the logarithm is a monotonically increasing function, this implies no difference in terms of finding the maximum of (3).

Once the current levels have been obtained through the MLE-based method, a background-noise-free or processed trace can be generated by assigning to each experimental current point the closest of the M detected levels. Examples of this processed trace superimposed with the experimental current trace are displayed in Fig. 8 and Fig. 9 for a RTN and a BTI recovery test, respectively.

In the case of the characterization of RTN, it is possible to extract both the time constants and the amplitude of the current jumps directly from the processed current trace. In the case of the BTI and HCI experiments, one further step, in which the RTN transitions are removed, is performed. Transitions in which the absolute value of the current decreases can be directly labeled as RTN transitions, since detrapping events in the recovery phase of BTI and HCI will cause an increase in the absolute value of the current. Additionally, transitions in which the absolute value of the current increases can be associated to RTN

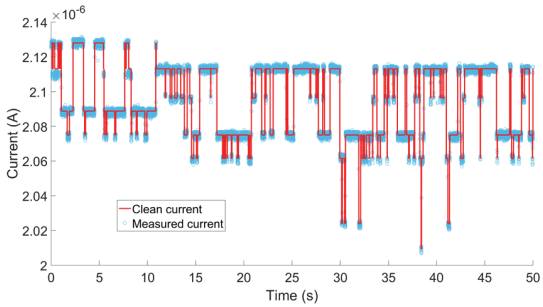

Fig. 8. Measured (blue) and processed (red) RTN current trace, measured at V_{GS} = 0.7V and V_{DS} = 0.1V and analyzed with TiDeVa.

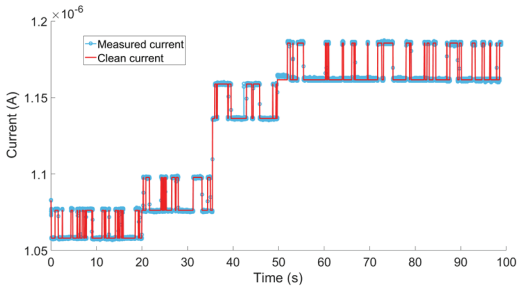

Fig. 9. Measured (blue) and processed (red) BTI recovery trace measured at V_{GS} = 0.6V and V_{DS} = 0.1V after a stress phase at V_{GS} = 2.5V.

(detrapping) events if an inverse RTN (trapping) event of the same amplitude but opposite direction takes place. An example of a processed BTI recovery trace, in which the RTN transitions have been removed, can be found in Fig. 10.

Once the processed current has been obtained (and the RTN transitions removed in the case of the aging experiments), the next step is to extract the parameters that characterize the diverse TDV phenomena. The time constants (capture and emission times for RTN, emission times for aging experiments) can be directly extracted from the traces. However, the current jump amplitude has to be converted to the transistor threshold voltage shift associated to each trapping/detrapping event. To this end, the methodology presented in [28] is employed. This methodology allows the accurate conversion of current jumps into discrete shifts of the transistor parameters by comparing the experimental current traces to a set of 100,000 simulated I_{DS}-V_{GS} curves, generated by uniformly sampling the threshold voltage and the mobility of the transistor. In this manner, the discrete change in the transistor threshold voltage associated to each defect is determined.

B. Graphical User Interface and automation of TiDeVa

Although a skilled user could attempt to visually analyze the TDV experimental data in a manual manner, this task becomes unattainable when one considers that thousands of traces, corresponding to the different TDV phenomena measured at different bias conditions,

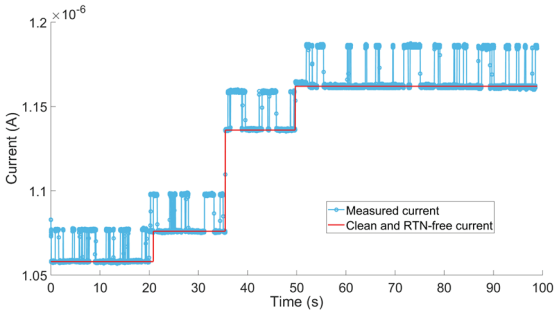

Fig. 10. Measured (blue) and processed (red) BTI recovery trace, in which the RTN transitions have been removed, measured at V_{GS} = 0.6V and V_{DS} = 0.1V after a stress phase at V_{GS} = 2.5V.

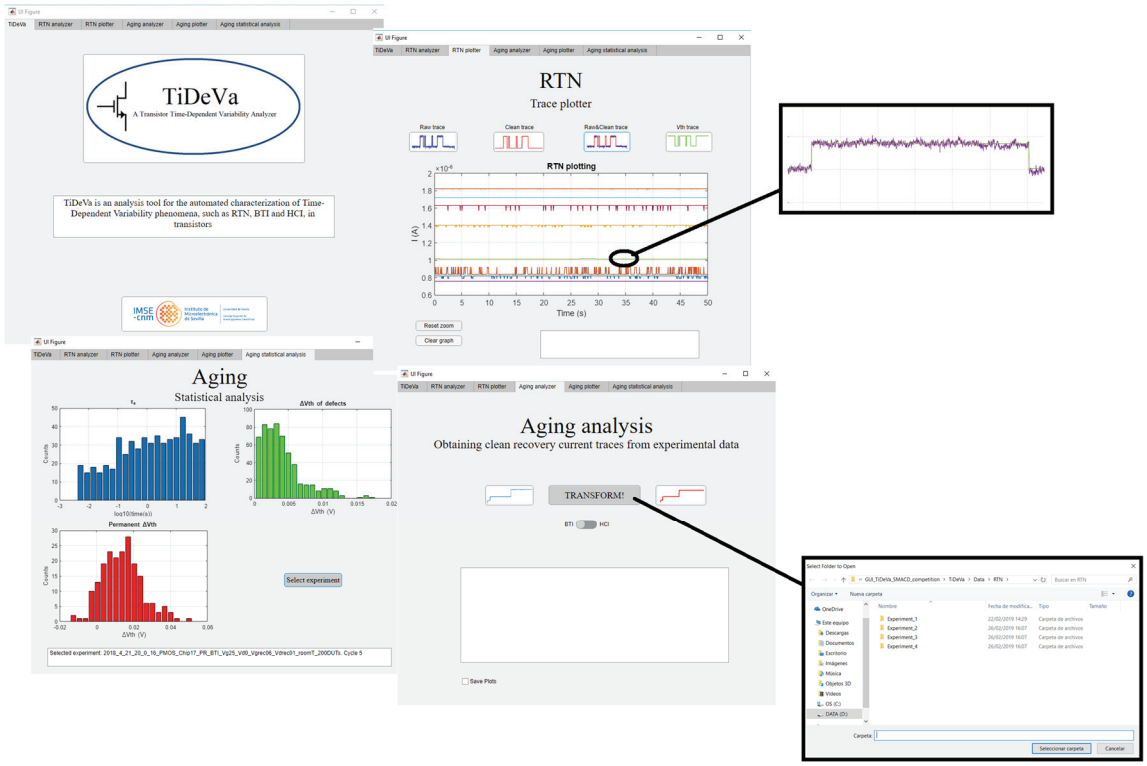

Fig. 11. Some tabs of TiDeVa. The one at the top-left corner is the one to open when the user launches TiDeVa. Then, clockwise, there is the tab for the graphical visualization of the RTN current traces, the tab for the analysis of aging experiments data, and the tab for the visualization of the statistical distributions obtained for the parameters of an aging experiment.

temperatures, in different transistor types (NMOS and PMOS), will have to be analysed. Due to this, the automation that TiDeVa provides for this analysis is one of the most important features of the tool. For the sake of illustration, to fit the Probabilistic Defect Occupancy model for TDV [15], more than 20,000 experimental traces have been measured and analyzed. Considering that a skilled user could need around 5 minutes in average to analyse each current trace, this would take 70 days of work (24 hours a day) to accomplish. From this estimation, the need for automation of this task becomes clear. The methodology employed by TiDeVa is much faster than this, since it requires approximately 10s in a single processor core to process with Matlab each of the examples shown in this work. In addition to this speed-up, an important advantage of the solution presented in this paper is that it requires no supervision by the user and can run in parallel to the experimental measurements, so that the processing does not translate into any additional effective time cost.

Furthermore, TiDeVa has been provided with a Graphical User Interface (GUI) developed in Matlab®. This GUI is multi-tabbed, and each tab oversees a specific operation. There are two tabs dedicated to the processing of RTN and aging experiments, respectively, two tabs for the graphical representation of the RTN and the aging tests, and one additional tab for the graphical representation of the statistical distribution of the parameters extracted for a given test. Some of these tabs are depicted in Fig. 11. The simplicity of the GUI of TiDeVa results in a very steep learning curve for the tool, which means that any user can master it within a short time and with very little effort.

C. *Selected TiDeVa results*

From the processing of the experimental data from the TDV tests, the TiDeVa toolbox generates the necessary information to construct the TDV model. This information is contained in a set of numeric result files that contain information about the extracted parameters.

g1Vg250Vd000s1.defect

1	1.4860000e+01	6.5000000e-03	1.5000000e+01
2	1.2000000e-02	2.0000000e-03	1.5000000e+01
3	1.3062000e+01	2.0000000e-03	1.8000000e+01
4	1.2760000e+00	2.5000000e-03	1.8000000e+01
5	8.7718000e+01	1.0500000e-02	1.9000000e+01
6	1.3406000e+01	4.0000000e-03	2.0000000e+01
7	1.1622000e+01	2.5000000e-03	2.0000000e+01
8	6.9000000e-01	5.0000000e-04	2.0000000e+01
9	1.8000000e-02	7.0000000e-03	2.0000000e+01
10	6.0200000e-01	5.0000000e-04	2.2000000e+01
11	1.8000000e-02	3.5000000e-03	2.2000000e+01
12	5.2000000e-02	1.0000000e-03	2.3000000e+01
13	3.6680000e+01	1.7000000e-02	2.5000000e+01
14	3.2000000e-02	3.0000000e-03	2.5000000e+01

Fig. 12. Detail of one of the result files generated for a BTI experiment. Each row corresponds to a detected defect. The left-most column corresponds to the emission time (τ_e) of that defect, the middle one to the associated threshold voltage shift (ΔV_{th}), and the right-most one to the transistor index within the transistor array.

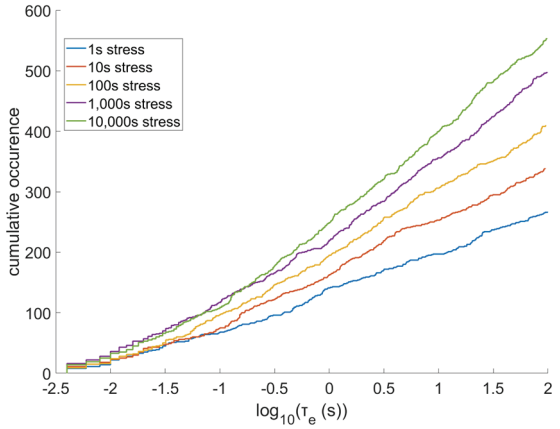

Fig. 13. Cumulative occurrence of the emission times for each of the five recovery phases in a BTI experiment with V_{GS} = 2.5V during the stress phase, and V_{GS} = 0.6V and V_{DS} = 0.1V during the recovery phase.

Fig. 12 displays such a file, obtained for a real BTI experiment, performed with the characterization system presented in Section III, on 200 devices with 5 stress-recovery cycles, where the stress time increases exponentially (1s, 10s, 100s, 1,000s and 10,000s) and the recovery phase remains constant (100s) for each cycle; the device is biased during the stress phases with V_{GS} = 2.5V and V_{DS} = 0V, and during the recovery phase with V_{GS} = 0.6V and V_{DS} = 0.1V. Fig. 13 displays the cumulative occurrence of the emission times τ_e for the defects extracted by the TiDeVa tool at each of the recovery cycles for that same experiment. As expected, the longer the stress phase is, the larger number of charged defects within it that are discharged during the recovery phase.

V. Conclusions

In this work, a complete methodology to characterize, model and simulate TDV, enabling reliability-aware design, has been presented. This methodology includes several steps, namely the experimental characterization of the TDV phenomena, the parameter extraction from those tests, the construction of a TDV model with those parameters, and the inclusion of such a model in a reliability simulator. In particular, the main focus is set on the parameter extraction, which is performed in an automated and robust manner by TiDeVa, an MLE-based tool. The automation of this tool proves to be fundamental for the complete process, since thousands of devices are measured during the characterization process, and a manual extraction of the parameters would be prohibitively time consuming.

Acknowledgements

This work has been supported by project TEC2016-75151-C3-R (AEI/FEDER, UE). Pablo Sarazá Canflanca acknowledges MINECO for supporting his research activity through the predoctoral grant BES-2017-080160.

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