Rail to Rail Fully Differential Track and Hold Based on Clocked Differential Difference Amplifier Using Resistive Local Common Mode Feedback

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Abstract.

An efficient clocked class AB fully differential rail to rail differential difference amplifier is introduced. It is based on a two stage operational amplifier architecture with resistive local common mode feedback, floating gate transistors in the input stages and in the common mode feedback network. Its application in fully differential rail to rail high performance sample and hold circuits is discussed.

Other applications discussed include fully differential buffers and single ended to fully differential converters with enable input. Experimental results of a test chip prototype fabricated in 0.5µm CMOS technology validate the proposed scheme. The fabricated track and hold has an SFDR=69.5dB with a clock frequency of 2MHz and $2V_{pp}$, 200KHz input signals.

I. Introduction.

Differential Difference Amplifiers (DDA) [1]-[2] are versatile analog building blocks with a host of applications in analog signal processing, for example, in CMOS line drivers [3]. A DDA can be considered an extension of the conventional op-amp with two differential inputs instead of one (Fig. 1). Here, with negative feedback, the op-amp virtual short circuit rule *(V_d=0)* is replaced by the more general expression $V_{d1}+V_{d2}=0$ (where V_{d1}, V_{d2} are the two differential input voltages, see Figs. 1a and 1b).

Fully differential DDAs (denoted here, FD-DDAs) as well as generalized (universal) op-amps with "n" differential weighted inputs have also been reported [4],[5]. An FD-DDA has two differential input stages (Fig. 1b) with equal voltage gain A_1. Their outputs are connected in parallel and they share a common output stage with gain A_2. Negative feedback with large open loop gain $A_{ol}=A_1A_2$ leads to the condition indicated above $V_{d1}+V_{d2} = 0$ that is demonstrated by (1).

The output voltage of the FD-DDA is given by

$$V_o = A_2V_{dx} = A_1A_2\left(V_{d1}+V_{d2}\right)= A_{o1}\left(V_{d1}+V_{d2}\right) \quad (1)$$

where V_{dx} is the common output voltage of the first stage and given by

$$V_{dx} = A_1\left(V_{d1}+V_{d2}\right) \quad (2)$$

Nowadays, no rail to rail DDA or FD-DDA implementations have been reported. In this paper we propose a clocked rail to rail FD-DDA that uses resistive local common mode feedback [6]-[7] to achieve class AB operation. It also uses the floating gate technique reported in [8]-[10] to achieve rail to rail input/output signal swing and to implement a rail to rail continuous-time common mode capacitive sensing network.

The paper is organized as follows: In Section II, we discuss the application of the CFD-DDA for the implementation of high performance rail to rail track and hold, sample and hold circuits, fully differential buffers and single ended to fully differential converters with enable inputs. In Section II and III the principles of CFDDA and its applications are presented. Simulation and experimental results are detailed in Section IV. Finally, some conclusions are drawn in Section V.

II. Principles and Operation of the Clocked Fully differential DDA.

Fig. 1c shows the symbol of the proposed clocked DDA, it has two additional terminals used to apply non overlapping clock signals *phi* and phi_{no}, while Fig. 1d shows the internal structure of the proposed clocked FD-DDA (CFD-DDA).
FD-DDA structure includes six switches: two pairs, controlled by *phi*, one pair to connect the output of the first stage (V_{dx}) to the input of the second stage and another one to connect the output of the second stage to the CFD-DDA output terminals. The remaining two switches are controlled by phi_{no} and connect the output of the first stage to an AC ground.

Operation.

Fig. 3 shows the implementation of the clocked fully differential DDA. Floating gate transistors M_1-M_2 and M_3-M_4 form two differential pairs (amplifiers A_1) that generate current signals $i_I = (g_mV_{d1})/2$ and $i_{II}=(g_mV_{d2})/2$, respectively. Their outputs are connected in parallel to common nodes A and B. Resistors R form a resistive local common mode feedback network [7] that has zero current under quiescent conditions

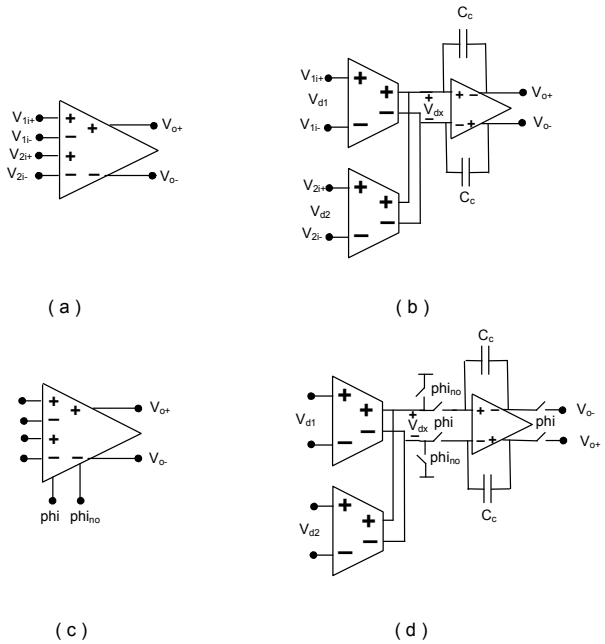

Fig. 1 Fully differential difference amplifier (FD-DDA) (a) Symbol,. (b) Internal structure. (c) Clocked Fully Differential DDA or CFD-DDA (d) Internal structure of CFD-DDA

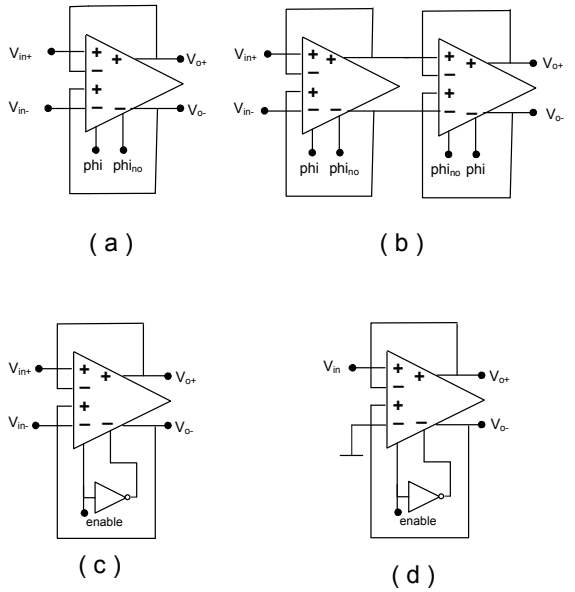

Fig. 2 Applications of Clocked Fully Differential Difference Amplifier (CFD-DDA): (a) Track and hold amplifier (b) Sample and Hold amplifier (c) Fully differential buffer with enable (d) Single ended to differential converter enable

($V_{d1}=V_{d2}=0$, $V_{dx}=V_A-V_B=0$) and generates equal quiescent voltages with values $V_Y=V_A=V_B=V_{DD}-V_{SG5,6}$ at nodes Y, A and B respectively; where $V_{SG5,6}$ is the quiescent source-gate voltage of M_5-M_6. These transistors (M_5-M_6) have always a constant current I_b and a constant voltage V_Y.

Upon application of differential signals V_{d1}, V_{d2} currents, $i_I=(g_mV_{d1})/2$ and $i_{II}=(gmV_{d2})/2$, are generated in M_1-M_2 and M_3-M_5 respectively (where g_m is the transconductance gain of M_1-M_4). The division by a factor of 2 is due to the attenuation of the capacitive divider at the input of the floating gate transistors. This capacitive divider uses two equal valued capacitors C at the input of each floating gate transistors in M_1-M_4 (Fig. 3c) and it has two purposes:

a) To increase the headroom for the differential pair by shifting, in the positive direction, the DC quiescent gate voltage of M_1-M_4 as the result of connecting one of the inputs of the divider to the upper rail, V_{DD}.
b) To attenuate the differential signals V_{d1} and V_{d2}.

The combined effect of a) and b) allows input rail to rail operation with low supply voltages according to the technique reported in [8]-[10].

Signals V_{d1} and V_{d2} generate complementary signal voltages $v_A=(i_I-i_{II})R$, $v_B=-(i_I-i_{II})R$ at nodes A and B while node Y remains at a constant voltage $V_Y = V_{DD}-V_{SG5,6}$. The differential voltage $v_{dX}=v_A-v_B=2(i_I-i_{II})(R\|r_{o5,6}) =A_1V_d$ is applied to the output stage formed by M_7-M_9 and M_8-M_{10}. This stage has a gain $A_2= g_{m7,8}(\ r_{o7,8}\|r_{o9,10})$. As reported in [6], the complementary and large signal swing at nodes A and B caused by the local common mode feedback network provide class AB operation to the output stage, due to the fact that the swing at A and B is only limited by the upper rail V_{DD}. This allows output transistors to generate signal currents which are essentially larger than their quiescent current and provides high slew rate to the CFD-DDA.

In order to operate as a track and hold and buffer, the common mode sensing network must be able to operate also with rail to rail output signals. Fig. 3b shows a rail to rail continuous time capacitive common-mode feedback network proposed in [10] and used in the CFD-DDA. It senses the common mode output voltage using a capacitive divider formed by capacitors C at the input of the floating gate transistors $V_{oCM}=(V_{o+}+V_{o-})/2$. This voltage is compared to the reference value V_{refCM} and generates a signal V_{cntCM}, proportional to the difference $V_{oCM}-V_{refCM}$. This control signal is applied at the gates of M_9-M_{10} and sets the output common mode voltage to the reference value V_{refCM}. Rail to rail operation of the output common mode sensing circuit is based on the same principle discussed above. The circuit of Fig. 3 can operate with rail to rail signals and a single supply voltages $V_{DD}=2V_{TPMOS}+3V_{DSsat}$ (This assumes a maximum swing at nodes A, B with value V_{TPMOS}). The gain bandwidth product of the DDA is given by the same expression as a two stage amplifier, $GBW=(1/4\pi)(g_{m1}/C_C)$. The additional attenuation factor of 2 is due to the capacitive dividers at the input of M_1-M_4.

Slew Rate Analysis.

Slew rate is determined by the maximum gate source voltage of M_7-M_8, which happens when the current through resistors R is maximum, equal to I_B. For a large input step voltage,

$$V_{SG7,8}^{\max} = V_{SG5,6}^{Q} + RI_B = |V_{THP}| + \sqrt{\frac{2I_B}{\beta_{5,6}}} + RI_B \qquad (3)$$

Assuming output transistors M_7-M_8 have the same dimensions as transistors M_5-M_6 the maximum output current is given

$$I_o^{\max} = \frac{\beta_{7,8}}{2}\left(V_{SG7,8}^{\max} - |V_{THP}|\right)^2 = \frac{\beta_{7,8}}{2}\left(\sqrt{\frac{2I_B}{\beta_{5,6}}} + RI_B\right)^2 \quad (4)$$

$$= \frac{\beta_{7,8}}{\beta_{5,6}} I_B\left(1 + R\sqrt{\frac{\beta_{5,6} I_B}{2}}\right)^2 = I_B\left(1 + R\sqrt{\frac{\beta_{5,6} I_B}{2}}\right)^2$$

and, finally, the slew rate is given by $SR = \dfrac{I_o^{\max}}{(C_C + C_L)^2}$

Remarks on CMRR and offset compensation.

Local common mode feedback provides high CMRR to the CFD-DDA. Due to symmetry, the effective load for common mode signals is relatively low and given by $R_{LCM}=1/g_{m5,6}$ while the effective load for differential signals is relatively high and given by $R_{Ld}=R||r_{o5,6} \sim r_o/2$. CMRR can be demonstrated that is given by

$$CMRR = \left(g_{m1,2} R \| r_{o5,6}\right)\left(gm_{5,6} \cdot 2r_{bias}\right)$$

where r_{bias} is the impedance of the current biasing source I_B.

Accurate offset compensation can be done in the CFD-DDA by adding two capacitors C_{os} between node A (B) and switches S_2,S_4 (S_1,S_3), (see Fig. 4). These capacitors store an amplified version A_1V_{os} of the input offset voltage V_{os} during the hold phase, phi_{no} in which both inputs are connected to ground through two additional switches (not shown in Fig. 4). Offset is compensated by the voltage stored capacitors C_{os} during the sampling phase *phi*.

III. Applications of CFD-DDA

Track and Hold and Sample and Hold amplifiers.

The circuit of Fig. 3 has three pairs of switches which are controlled by non-overlapping clock phases *phi* and phi_{no}, these are used to operate the circuit as a Track and Hold amplifier as illustrated in Fig. 2a.

In this application, nodes A and B are connected to the gates of M_7 and M_8 during phase *phi* and two output switches establish global negative feedback by connecting the outputs of the CFD-DDA to their inputs (Fig. 3a). Also in this phase, the signals at nodes A and B are amplified by the second stage providing the circuit a large open loop gain so that the DDA rule $V_{d1}+V_{d2}=0$ is satisfied and causes the output differential voltage to follow the input differential voltage $(V_o=V_{in})$. During the non-overlapping phase, phi_{no}, the output switches are turned off so gates of M_7 and M_8 are disconnected from nodes A and B that provides the output voltage of the previous phase held in the compensation capacitors Cc. In this phase nodes A and B are connected to node Y; this bypasses resistors R and prevents nodes A and B from saturating which otherwise would slow down the operation of the circuit.

Clock injection at the gates of M_7 and M_8, caused by turning off switches S_1 and S_2, is approximately equal and signal independent. This injection introduces an approximately equal offset error at both positive and negative outputs $(V_{o+}$ and $V_{o-})$ and does not introduce an error in the differential output voltage $V_o=V_{o+} - V_{o-}$ during the hold phase phi_{no}.

A sample and hold amplifier can be implemented by connecting in cascade two track and hold amplifiers with complementary control signals as shown in Fig. 2b. This technique is in a similar line to the single ended sample and hold based on a two stage op-amp reported originally in [11].

Fully differential buffers and single ended to differential and differential to single ended converters.

Fig. 2c and 2d show the application of the CFD-DDA as a low voltage rail to rail fully differential buffer and as single ended to differential converter with enable input. In this case, terminals *phi* and phi_{no} can be used as enable inputs (with enable signals $(phi=Vdd, phi_{no}=Vss)$, in that way the global feedback and connection of the output of the first stage to the input of the second stage is enabled and the rule $V_{d1}+V_{d2}=0$ applies leading to $V_{d1}=V_{d2}=0$ or equivalently to $V_{o+}=V_{in+}$, $V_{o-}=V_{in-}$ or $V_o=V_{in}$ in the case of the fully differential buffer.

However, for the single ended to fully differential buffered converter it leads to $V_{o+}=-V_{in}/2$, $V_{o-}=V_{in}/2$ and $V_o=V_{in}$ (with $V_{d1}=V_{in}/2$ and $V_{d2}=-V_{in}/2$). A simple reconnection (not shown for the sake of space) allows the same circuit to be used as a differential to single ended buffered converter.

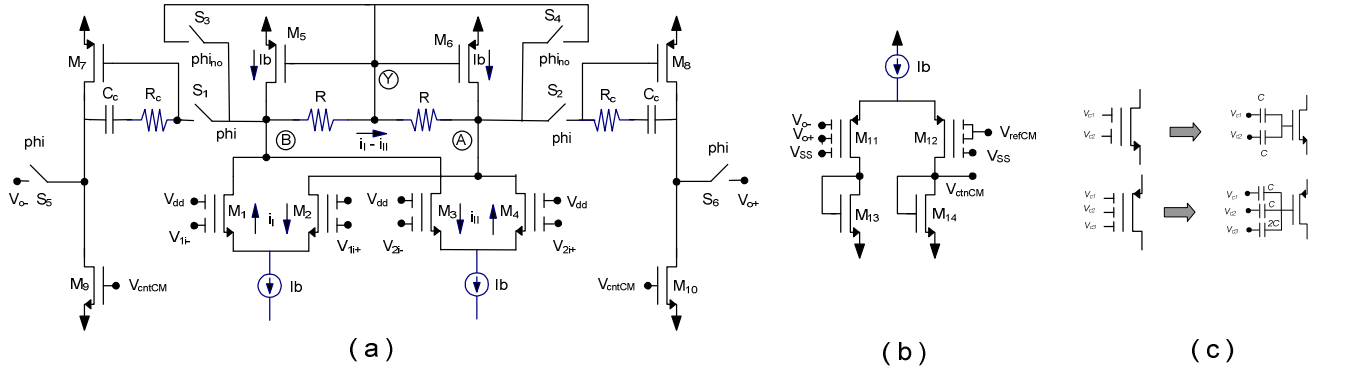

Fig. 3 (a) Rail to rail two stage fully differential difference amplifier using local resistive common mode feedback, (b) Rail to rail capacitive Common mode feedback network (c) Symbols and equivalent circuits of 2 and 3 input floating gate transistors

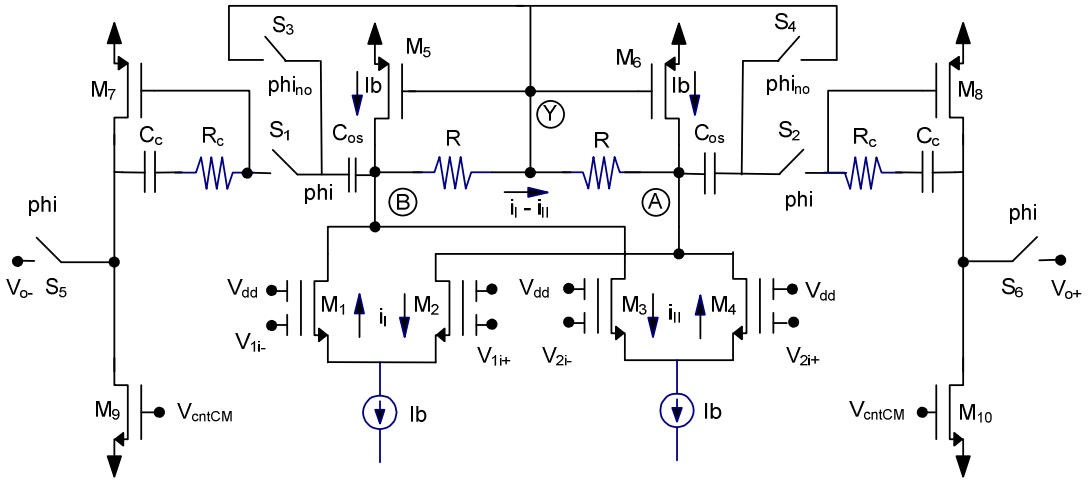

Fig. 4 CFD-DDA with offset compensation capacitors C_{os} at output of first stage

Considerations for implementation of the CFD-DDA in deep submicrometer CMOS technology.

The blocks described above can be very useful in low-voltage fully differential analog signal processing. Their two stage architecture, class AB operation with rail to rail characteristics and low supply requirements, make them specially attractive in deep submicrometer CMOS technologies that uses single supply voltages close to 1V. In these technologies, the amplifier gain has a strong dependence on the drain-source voltage [13]-[14]. Small drain source voltages lead to low gains and, for this reason, conventional cascode architectures that operate with low V_{DS} on each transistor (like the folded cascode or telescopic op-amp) cannot achieve high gain. This makes two stage architectures like that in Fig. 3 (where transistors can have high V_{DS}) attractive to achieve high open loop gain and accuracy.

As example it can be considered typical 90nm CMOS technology with $V_{TPMOS} \approx V_{TNMOS} \approx 0.35V$, $V_{DSsat}=0.1V$. In this case operation with high slew rate can be achieved with a single supply $V_{DD}=1V$. Output switches can be replaced by straight connections and gate leakage can be compensated for by including two additional switches that connect (refresh) the gates of M_1-M_4 to V_{DD} (or some other bias voltage) during phi_{no}.

IV. Simulation and experimental results

A test chip prototype of the circuit of Fig. 3 has been fabricated in the MOSIS available 0.5µm CMOS technology with nMOS and pMOS threshold voltages of 0.76 and -0.94V, respectively. The circuit was tested with $V_{DD}=2.5V$, $V_{SS}=0V$, $V_{refCM}=1.3V$, $I_b=200\mu A$ and $C_L=5pF$. Transistors sizes and values of devices are detailed in Table I.

The circuit had only one clock input terminal and included a conventional circuit to generate non overlapping clocks *phi* and phi_{no} from the external clock [12]. Fig. 5 shows a microphotograph of the fabricated chip.

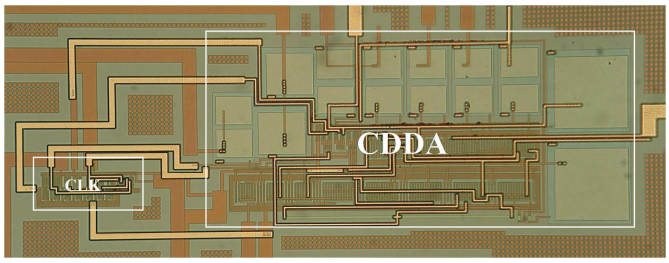

Fig. 5 Microphotograph of fabricated chip. White boxes outline clocked DDA (CDDA area 740x310um^2) and non overlapping clock generator (clk area: 180x70um^2)

TABLE I. TRANSISTORS DIMENSIONS AND DEVICES VALUES

Transistor	***W/L (µm/µm)***
M_1-M_4, M_{13}-M_14	50/1
M_5-M_8	240/1
M_9-M_{10}	100/1
M_{11}-M_{12}	120/1
Other devices	***Value***
R	50 KΩ
R_c	1.5 KΩ
C_c	1 pF
C_L	5 pF

Simulation results.

Simulations of the DDA had been performed with the same testing conditions that the fabricated prototype had been measured, obtaining 52.8 dB DC open loop gain and 88.6º of phase margin with a GBW of 14.4MHz (featuring under 20nV/√Hz noise spectral density at this frequency). Simulations were performed with *phi* set to V_{dd} and phi_{no} to V_{ss}.

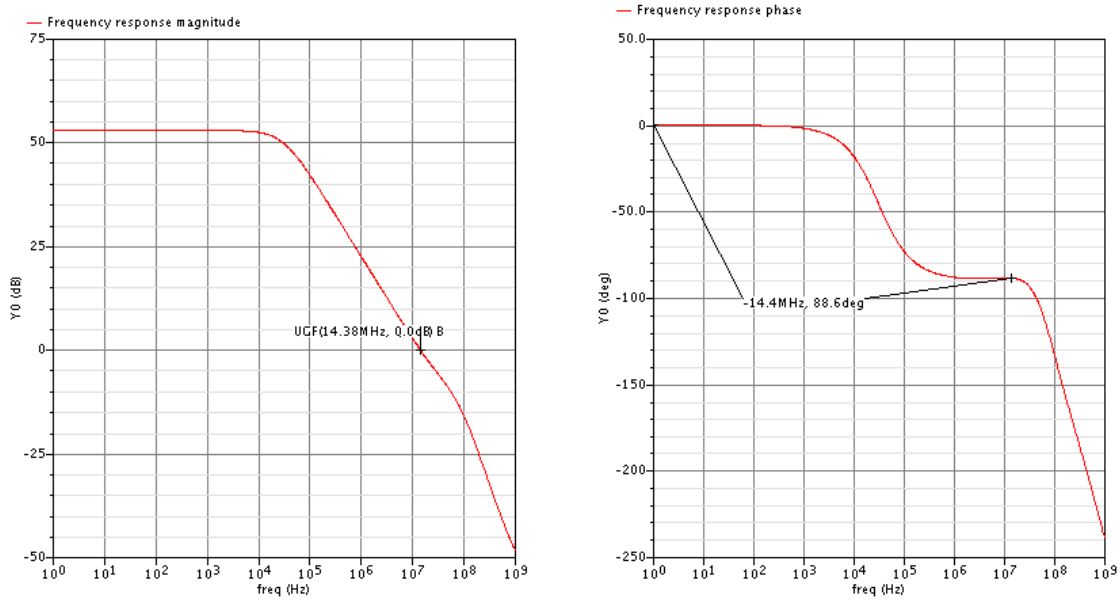

Fig. 6 Open-loop frequency response

The transient unit gain configuration response showed a slew rate of 61V/µs and total harmonic distortion (THD) under -82dB up to 2MHz for 2.5Vpp input (Fig. 7).

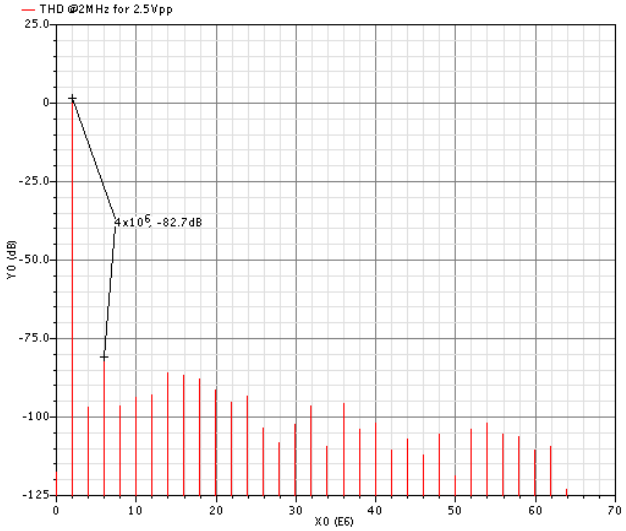

Fig. 7 THD @ 2MHz for 2.5Vpp input-output

Experimental Results.

Figs. 8 show experimental input and output waveforms for a $2V_{pp}$ 500kHz input signal and a 5MHz clock frequency. Fig. 9 shows the spectrum of the output signal for a $1V_{pp}$ 200kHz input signal with a 2MHz, clock. Fig. 10 shows a detail of the transient response with a $1V_{pp}$ 200KHz input signal and 2MHz clock. According to measurements, the circuit features SFDR of 70dB for 2Vpp at 200 KHz input and 2MHz with only 75ns of settling time for the 5pF-load capacitance.

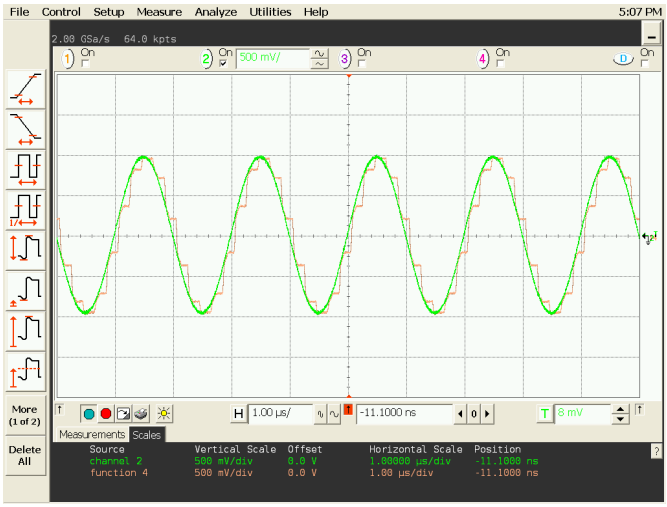

Fig. 8. Experimental input and output differential waveform of the fabricated circuit ($2V_{pp}$ @ 500kHz input signal and 5MHz input clock). Horizontal 1µs/div, vertical 0.5V/div

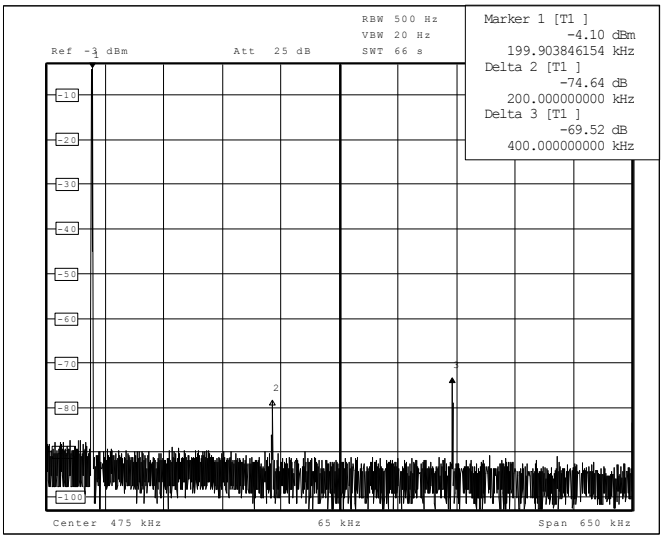

Fig. 9. Experimental THD for 2Vpp input signal at 200kHz and 2MHz input clock.

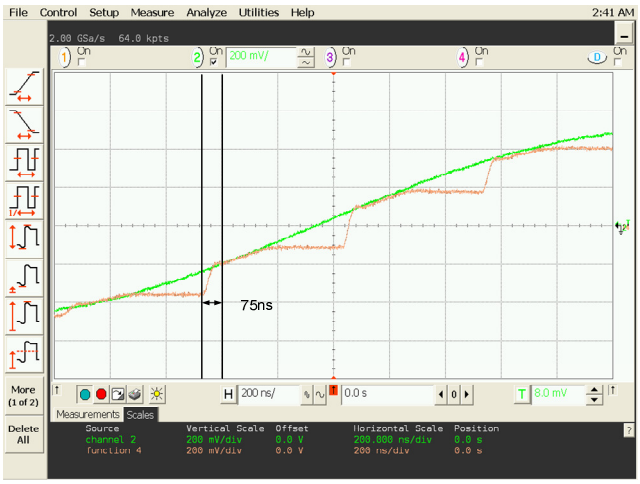

Fig. 10. Detail of the experimental transient response for 1Vpp 200kHz Input signal and 2 MHz clock.

V. Conclusions

A very compact implementation of a class AB low voltage rail to rail fully differential DDA was introduced. Its application as a track and hold, sample and hold fully differential buffer and single ended to differential converters with enable inputs was discussed. The implementation of the circuit in deep sub-micrometer CMOS technology was also discussed. Experimental results of a test chip prototype in 0.5µm validated experimentally the circuit operating with rail to rail signals and a 2MHz clock frequency with SFDR=69.5dB.

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