Adaptive Miller Compensation under Extreme Load Variations in IC-LDO regulators

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***Abstract*— A new frequency compensation technique for output buffers able to manage a wide range of loads, is proposed in this paper. To improve the stability, this technique implements a variable zero nulling resistor in a classical Miller compensation. A replica circuit senses the operating region of the output stage and generates the required value of the nulling resistor. In order to validate the effectiveness of the proposed technique, an Internally Compensated Low Dropout (IC-LDO) regulator based on a classical topology has been chosen and designed in a 65 nm standard CMOS technology. Results show that the proposed compensation scheme improves the Phase Margin of the IC-LDO regulator keeping it higher than 54º for load currents from 0 to 100mA at the cost of increasing only 10% the total quiescent power consumption and negligible area.**

Keywords*— *Adaptive compensation, low dropout (IC-LDO) regulator, stability, Miller compensation.

I. Introduction

Stability has been a key concern in electronic design, as it determines the performances of linear feedback systems [1]. In modern electronics, the stability has become a technical challenge as, in addition to the high performance and efficiency that the market demands for electronic systems, the designer faces the constraints coming from the downscaling of CMOS technologies. This is of especial interest in the design of low power, highly efficient buffers, which should be able to handle the wide range of loads required for the power supply and input/output circuitry [2].

A significant circuit intended to efficiently handle a wide range of loads with low power consumption is the Internally Compensated Low Dropout (IC-LDO) regulator, whose stability is a major issue. These circuits play a key role in power management and in System-on-Chip designs, and they are attracting a lot of attention for new compensation methods [3]–[7]. IC-LDO regulators require small area, low power consumption, low supply voltage, good line and load regulation, short settling time and high efficiency and, at the same time, they are required to remain stable under extreme variations of the line voltage (V_{IN}), load current (I_{LOAD}) and load capacitance (C_{LOAD}).

This paper proposes an adaptive and continuous compensation scheme that adjusts the value of the nulling resistor of a Miller-based compensation scheme to keep the nulling zero close to the unit gain frequency (UGF), regardless the working conditions. As a proof of concept, this technique has been applied to a classical IC-LDO regulator topology, which has been designed and implemented in a standard 65 nm CMOS technology.

The document is organized as follows: first of all, a brief review of different compensation schemes applied to IC-LDO regulators is made in Section II. Then, the proposed compensation method is described in Section III. Section IV and V focus on an IC-LDO regulator designed to evaluate the proposed technique, showing both, post-layout simulations and experimental results. Finally, some conclusions are drawn in Section VI.

II. Review of Compensation Schemes Applied to IC-LDO regulators for Stability Improvement

In order to enhance the Phase Margin (PM), a pole-splitting technique such as the Miller-based compensation scheme can be used. It is well known that the Miller compensation introduces a Right-Half-Plane (RHP) zero, which depends on the ratio between gm_{PASS}, and the total Miller capacitance $C_{gd,PASS}+C_C$. The negative effects of this RHP zero can be neutralized by means of a nulling resistor (R_C) in series with the compensation capacitor. Unfortunately, as both, gm_{PASS} and $C_{gd,PASS}$, are strongly dependent on I_{LOAD}, the value of R_C that stabilizes the IC-LDO regulator for zero-load current is not adequate for middle-range load currents, as it is shown in Fig. 1 where the variation of the PM versus I_{LOAD} in the case of an uncompensated IC-LDO regulator, and a compensated Miller version with, and without, ZNR. It can be observed that there is range of values of I_{LOAD} where the PM is not large enough. Consequently, the IC-LDO regulator is not stable for the whole range of I_{LOAD}.

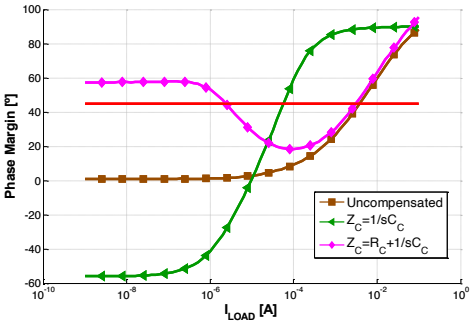

Fig. 1. PM variation vs I_{LOAD} for an uncompensated IC-LDO regulator, and Miller compensated IC-LDO regulator with, and without, ZNR.

TABLE IV. COMPARISON OF RECENTLY PUBLISHED IC-LDO REGULATORS

		[4]	[5]	[6]	[7]	[8]	[14]	[13]	**This Work**	
Technology	[µm]	0.065	0.35	0.18	0.065	0.35	0.6	0.5	**0.065**	
V_{IN}	[V]	1.2	1.2-1.5	1.1-1.5	1.2	1.2	1.5-4.5	1.4-4.2	**1.0-1.2**	
V_{OUT}	[V]	1.0	1.0	1.0	1.0	1.0	1.3	1.21	**0.8**	
$V_{DROPOUT}$	[mV]	200	200	100	200	200	200	200	**200**	
$I_{LOAD,max}$	[mA]	50	50	50	100	50	100	100	**100**	
$I_{q\|max}$	[µA]	23.7	45	54	82.4	65	38	45	**17.88**	
C_{LOAD}	[pF]	10000	1000	100	100	100	100	10^5	**100**	
Area	[mm^2]	-	0.263	-	0.017	0.350	0.307	0.400	**0.0436**	
On-chip Capacitor	[pF]	8.0	41	5	4.5	7	12	67	**18.48**	
Settling time	[µs]	1.65	5	2	6	15	2	4	**17.05**	
ΔV_{OUT} varying V_{IN}										
• maximum	[mV]	-	23	-	8.91	90	160	-	**78.4**	
• minimum	[mV]	-	-12	-	-10.63	-10	-1.5	-	**-49.3**	
ΔV_{IN}/tr	[mV/µs]	-	1/0.1	-	0.2/10	1/1	3/6	-	**0.2/0.1**	
ΔV_{OUT} varying I_{LOAD}										
• maximum	[mV]	19	47	100	0	80	100	70	**242**	**96.39**
• minimum	[mV]	-58	-48	-80	-68.8	-80	-90	-70	**-336**	**-39.36**
ΔI_{LOAD}/tr	[mA/µs]	50/0.1	100/0.1	50/0.1	100/0.3	50/1	90/0.5	49/1	**100/0.1**	**90/0.5**
Load Regulation	[µV/mA]	-	250	-	300	-	-	408	**780.57**	
Line Regulation	[mV/V]	8.8	0.098	-	4.7	-	-	-	**26.5**	
FOM	[fs]	7300	2331	388.80	56.69	416	72.20	63000	**103.35**	**24.37**

In order to validate the effectiveness of this technique, an IC-LDO regulator was designed. It is a representative example, as these cells suffer, not only from large variations of the load current, but also from variations in the input voltage and in the output capacitance. When the proposed technique is particularized to IC-LDO regulators, it results in a simple, robust and power-efficient solution. This circuit has been designed and manufactured in a 65 nm standard CMOS technology. The measured value of a typical FOM shows that it is in the state of the art. Even more, additional transient response enhancement techniques could also be applied to improve the transient response, although it is beyond the interest of this paper. Regarding current and area consumption, the circuitry required by the proposed compensation method only requires 10% of the total quiescent consumption and negligible area.

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