IC-LDO Regulator with 600 nA Quiescent Current Using a Class AB Buffer

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***Abstract*— An ultra-low power Internally Compensated Low-Dropout (IC-LDO) regulator with a quiescent current consumption lower than 600 nA is proposed. It is based on the classical IC-LDO topology, which has been modified to include a class AB buffer between the output of the error amplifier and the gate of the pass transistor (M_{PASS}). This way, a fast charge/discharge of its parasitic capacitance is achieved with the inherent low quiescent power consumption of class AB circuits. The proposed regulator has been fabricated in a standard 0.18-µm CMOS technology. Experimental results show that the proposed regulator has a Figure of Merit in the state of the art.**

Keywords*— *Internally Compensated Low-Dropout Regulator, ultra-low power

I. INTRODUCTION

Power management systems have become very important in recent years, especially in the design of System-on-Chips (SoCs) for low power applications [1], [2]. Of special interest is their use in Wireless Sensor Networks (WSNs) [3], where the sensor nodes are usually powered by batteries and, in some cases, the energy they consume is harvested from the environment [4]. In this scenario, reducing the energy consumption of the blocks that build these nodes means prolonging the lifetime of the batteries, and/or reducing the requirements of the energy harvester [5].

Within the power management circuits, one of the most critical blocks is the voltage regulator, as it supplies sensitive subsystems such as RF stages or analog-to-digital converters. When the main design requirement for a Low-Dropout (LDO) regulator is ultra-low-power consumption (for instance, a quiescent current lower than 1 µA), two critical aspects must be taken into account. Firstly, extremely low bias currents make the output impedance of the error amplifier (as well as that of the intermediate stages) very high. This translate into low frequency poles that degrade the frequency response and, hence, the stability. Compensation techniques based on active blocks, like those presented in [6], [7] should be avoided due to the extra power they consume. Secondly, extremely low quiescent currents slow down the transient response, as they are not sufficient to rapidly charge / discharge the high gate capacitance of the pass transistor.

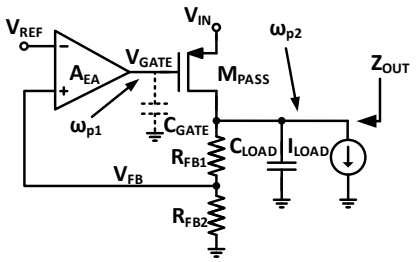

Fig. 1. Classical topology for an IC-LDO regulator.

In order to deal with this limitations, several approaches have been proposed in the literature to achieve high performance in ultra-low power internally compensated LDO (IC-LDO) regulators. They include adaptive biasing [8]–[10], splitting of the pass transistor [11], push-pull stages [12], and RC coupling [13], [14]. Attending to these solutions, a low quiescent power buffer placed between the error amplifier (EA) and the pass transistor (M_{PASS}) is appropriate to improve the stability and transient response. Based on this idea, a new Internally Compensated Low-Dropout (IC-LDO) regulator with ultra-low quiescent power consumption is presented. It is based on the classical LDO topology, Fig. 1, where a class AB buffer, placed at the output of the EA, provides the large currents necessary to charge / discharge the parasitic gate capacitance of M_{PASS} (C_{GATE}) with a low quiescent consumption.

This paper is organized as follows: the proposed ultra-low power IC-LDO regulator is presented in Section II, while its frequency response is studied in section III. Experimental results are shown in Section IV. Finally, some conclusions are drawn in Section V.

II. PROPOSED IC-LDO REGULATOR

The proposed LDO regulator is shown in Fig. 2. As it can be seen in Fig. 3, the EA consists of a Folded Cascode operational amplifier, including the in-built A_0 and A_1 amplifiers. They are low voltage, high signal range amplifiers [15] that improve the open-loop gain of the whole system. For the sake of completeness, their schematics are reproduced in Fig. 4.a and Fig. 4.b, respectively.

TABLE III. COMPARISON OF RECENTLY PUBLISHED LDO REGULATORS

		[8]	[9]	[10]	[11]	[19]	**This Work**
Technology	[μm]	0.35	0.35	0.11	0.065	0.35	**0.18**
V_{IN}	[V]	1.0-1.8	2.5-4.0	1.8-3.8	1.2	1.28-3.3	**1.164-1.8**
V_{OUT}	[V]	0.9	2.35	1.6-3.6	1.0	1.1	**1.0**
$V_{DROPOUT}$	[mV]	100	150	200	200	180	**164**
$I_{LOAD,max}$	[mA]	50	100	200	100	100	**100**
$I_{q\|max}$[a]	[μA]	1.2	7.0	41.5	82.4	25	**0.585**
C_{LOAD}	[pF]	1e2	1e2	4e1	1e2	1e2	**1e2**
Settling time	[μs]	4.0	0.15	0.65	6.00	1.4	**731.6**
ΔV_{OUT} varying V_{IN}							
• Maximum	[mV]	200[d]	196	-[e]	8.91	20	**246**
• Minimum	[mV]	-120[d]	-183	-[e]	-10.63	0	**-281**
$\Delta V_{IN}/t_r$[f]	[mV/μs]	0.5/1[d]	0.5/0.5	-[e]	0.2/10	1/100	**0.6/1**
ΔV_{OUT} varying I_{LOAD}							
• Maximum	[mV]	200[d]	231	200	0.00	31	**274**
• Minimum	[mV]	-425[d]	-243	-385	-68.8	-80	**-368**
$\Delta I_{LOAD}/t_r$[f]	[mA/μs]	49.50/0.2[d]	99.95/0.5	199.5/0.5	100/0.3	100/0.5	**99.9/1**
Load Regulation	[μV/mA]	148	80	108	300	190	**85.44**
Line Regulation	[mV/V]	3.625	1.0	8.9	4.70	-[e]	**2.50**
FOM	[fs]	30	33.18	24.28	56.7	27.75	**3.76**

[a] [a]Worst-case, [b]Effective area, [c]PADS are included, [d]Estimation based on published results, [e]Not available, and [f]t_r: Rise time

the pass transistor to provide the large currents required to ensure a good transient response while maintaining ultra-low quiescent power consumption. Experimental results show that the proposed regulator features, in the authors' knowledge, the best Figure of Merit of the IC-LDO regulators published to date.

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