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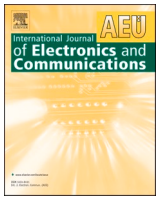

Regular paper

Effect of ionizing radiation on quasi-floating gate transistors

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ABSTRACT

Low power and low voltage are key in modern design. The quasi-floating gate (QFG) has proven to be an adequate choice in numerous applications. However, so far, its use has not spread in high-radiation environments because of the lack of studies on the performance of this technique under radiation. This work addresses the effect of ionizing radiation in the QFG transistor. To this end, a specific DUT has been designed and irradiated up to 2,25 Mrad. The experimental results show a tolerable reduction in the equivalent resistivity of the pseudoresistor (a reverse biased n-well PN junction). The effect is due to the increase in the reverse saturation current of the diode present between the pseudoresistor's terminals, which is consistent with Displacement Damage Dose (DDD).

1. Introduction

The increasing demand for high-integrated, high-performance, and low-power solutions has led the microelectronics industry to promote aggressive downscaling of the CMOS technology in recent decades. Digital CMOS circuits have been successfully adapted to modern processes. Increased transistor switching frequency has allowed improving the performance of microprocessors and digital memories, while power consumption has been reduced [1]. However, analog and mixed-signal circuits do not benefit from downscaling [1,2]. Shrinking the gate-oxide thickness implies a non-proportional reduction of the threshold voltage with respect to the supply voltage. This results in limited signal headroom and poor signal-to-noise ratio [3]. Additionally, the intrinsic gain of transistors is reduced and, therefore poor gain and less precise circuits are expected [4]. Second-order effects that did not have a significant impact in classical technologies, such as undesired gate leakage current [5], large deviation of transistor parameters, and poor matching [6] become now important [7].

In this context, analogue and mixed signal designers face the need to provide novel techniques for high-performance, low-power, and low-voltage solutions that can overcome these new barriers. This challenge is even more extreme in applications such as aerospace, high-energy physics, nuclear, or medical radiation, where there is the need to respond with robustness against radiation.

The most widely used techniques, at circuit level, to achieve low power and low voltage in analogue and mixed signal microelectronics are rail-to-rail operation, level shifters, weak inversion transistor biasing, bulk-driven approaches [8,9] feedback biasing [10] and multiple input floating-gate (FG) [11] and quasi-floating gate (QFG) based structures [12]. The FG and QFG techniques are very interesting proposals for low-voltage solutions, as they do not require extra power consumption. The QFG transistor was proposed in [12] and [13]. Since then, designers have intensively used it to provide low-power solutions that perform: low-voltage operation, rail-to-rail operation [14], high linearity [15], class AB behaviour [14,16,17] high gain-bandwidth product [18], as well as a way to combine in one topology the advantages of low-voltage operation of bulk-driven approaches with the high performance of gate-driven [19,20].

Consequently, a wide number of low-power and low-voltage analogue and mixed-signal circuits are found in the literature that use QFG transistors. For instance: mixers [12], analogue switches [13], programmable gain amplifiers [21-23], rectifiers [24], multipliers [25], filters [26,27], track-and-hold circuits [13], analogue-to-digital and digital-to-analogue converters [28] or logical families [29].

Due to its versatility, the QFG transistor is expected to be relevant in the design of circuits for harsh environments. In fact, [30] proposes a

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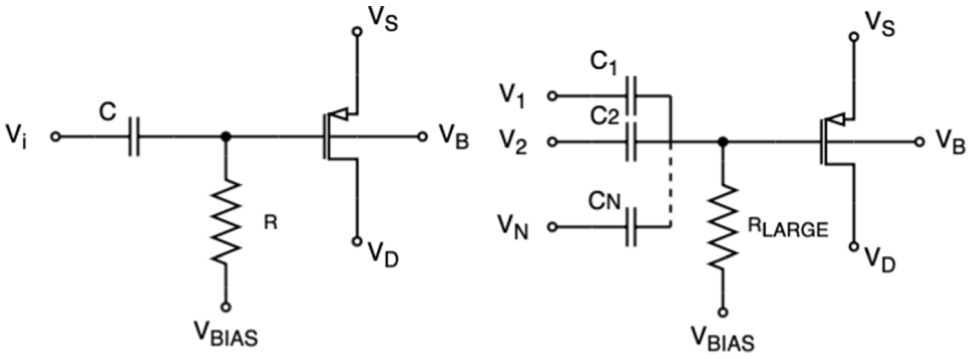

Fig. 1. General structure of a) capacitive coupling and b) multiple input QFG transistor.

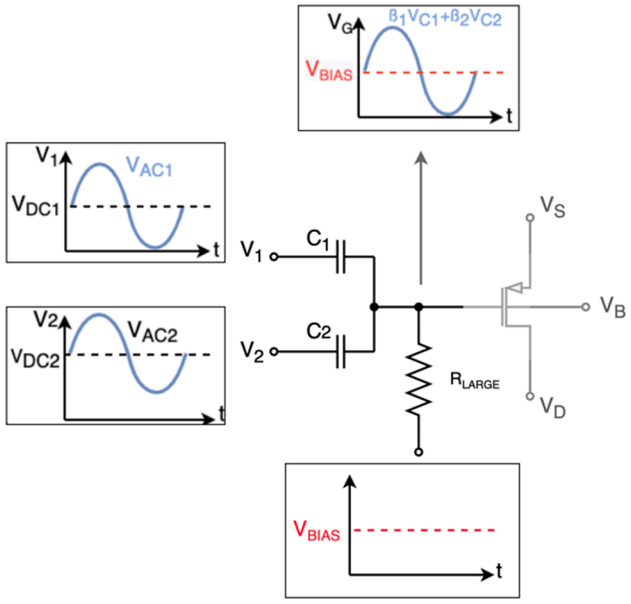

Fig. 2. Detailed behaviour of the QFG transistor ($\beta_k = \frac{C_k}{C_T}$).

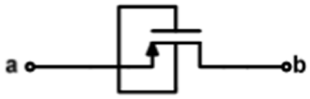

Fig. 3. Reverse-biased n-well PN junction (R_{LARGE}).

Charge Sensitive Amplifier (CSA) that uses QFG transistors to boost the gain of the operational amplifiers. Regarding radiation effects, this reference assesses by simulation the impact of high-energy particles, single-event transients (SETs), on the proposed architecture. However, the authors do not present experimental results on the impact of SETs or accumulative radiation effects on the performance of the QFG technique.

Our work addresses, supported by experimental results, the effect of ionizing radiation on QFG transistors. The document is organized as follows: Section 2 introduces the QFG technique and the implementation of pseudoresistors. Section 3 details the hypothesis and methodology used in this work and describes the proposed device under test (DUT). Section 4 focuses on the experiment, covering from the test requirements to the proposed test setup, while section 5 shows and discusses the experimental results. Finally, some conclusions are drawn in section 6.

2. The quasifloating-gate transistor

2.1. Quasi-floating gate transistor

As stated in the previous section, the QFG transistor was first introduced as a variation of the well-known capacitive coupling. Classical capacitive coupling, Fig. 1a, allows isolating the DC bias setting circuit from the driving signal source, which is very convenient in low-power and/or low-voltage environments. This technique acts as a first-order high-pass filtering from the signal input (Vi) to the gate of the transistor with a cutoff frequency of $1/2\pi RC$.

In the context of integrated circuits, the practical values of resistors and capacitors result in relatively high cut-off frequencies for this filtering, and thus, the use of the technique is limited to RF narrow band applications.

An efficient way to achieve very low cutoff frequencies (or equivalently large time constants) is to replace the resistor with a pseudoresistor [31]. Pseudoresistors are small-area integrated devices that can provide extremely large resistances (in the order of $G\Omega - T\Omega$) when they are properly biased. This significantly extends the use of capacitive coupling even when small capacitors are used. The resulting structure is the so-called QFG transistor, and its more general representation is shown in Fig. 1b where multiple input signals are applied, and weighted averaging is achieved at the gate of the transistor in a simple and compact way. In Fig. 2, the behaviour of the circuit is graphically detailed. In DC, capacitors C_1 and C_2 are open circuits and, since the current flow through the resistor is negligible, the DC voltage at the transistor gate is set to V_{BIAS}. In small signal operation, the capacitors couple the input signals weighted by a factor β_1 or β_2 which will depend on the capacitor value for each of the inputs and the total capacitance. A simple mathematical analysis leads to the following expression for the voltage at the gate of the QFG assuming that the transistor parasitic capacitance is negligible.

$$v_G|_{QFG} = V_{BIAS} + \frac{sR_{LARGE}}{1 + sR_{LARGE}C_T} \sum_{k=1}^{N} C_k v_k \tag{1}$$

where $C_T = \sum_{k=1}^{N} C_k$

The cutoff frequency of the equivalent high-pass filter is.

$$f_{cutoff} = \frac{1}{2\pi R_{LARGE} C_T} \tag{2}$$

Note that the exact value of R_{LARGE} and C_T is not relevant if the designer ensures that f_{cutoff} is at least one order of magnitude lower than the minimum interest frequency in the targeted application.

2.2. Practical implementation of the pseudoresistor

Several ways have been proposed in the literature to implement the above-mentioned pseudoresistor R_{LARGE}. For instance, [12] and [29]

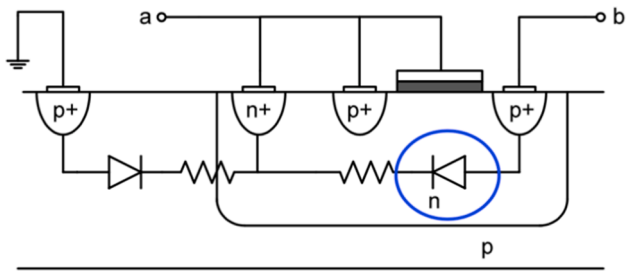

Fig. 4. Reverse biased n-well PN junction physical model.

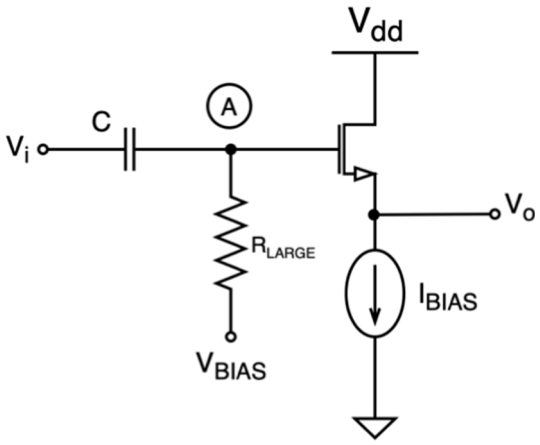

Fig. 5. QFG Voltage Follower.

introduce structures based on the reverse biased n-well PN junction available in a MOS transistor; a diode-connected pMOS or combinations of them. In other cases, the limitations of previous proposals are identified [32,33] or the authors propose to implement sufficient large resistors by biasing MOS transistors in the subthreshold region, either controlling the voltage at the gate of the transistor or imposing a very low current through it [32]. In this study, we will focus our efforts on the reverse biased n-well PN junction (Fig. 3) because it is a very simple structure that provides extremely high resistance and, therefore, a significant settling time (τ). This -elaborated in the next section-will facilitate the test setup and the drawing of conclusions.

3. Hypothesis and methodology

3.1. Hypothesis

The selected pseudoresistor can be modelled as shown in Fig. 4. According to this model, R_{LARGE} is defined by the saturation current, I_S, of the reversed bias diode between terminals 'a' and 'b'.

When a silicon device is irradiated with γ rays, point defects are generated in the silicon crystal proportional to the dose. This phenomenon, well known for silicon detectors [34] based on reverse biased diodes, is referred to as Displacement Damage Dose (DDD). Specifically, and as described in [35], γ photons from a Co-60 source produces Compton electrons that could hit a silicon atom in the lattice. That primary knock-on atom (PKA) has enough energy to generate one Frenkel pair, also called a point defect. The result is the appearance of deep levels in the band energy diagram of the silicon. Co-60 γ rays are responsible for generating at least two deep levels in silicon [36] and it is well known [34], that deep levels in a reverse biased silicon diode produce an extra saturation current, $I_{S\gamma}$.

Specifically, according to semiconductor carrier transport theory [37], the recombination process is proportional to the carrier density. In a reverse biased diode, the carrier concentration in the depletion zone is below the equilibrium concentration, so the recombination process is expected to be negligible. On the contrary, the generation rate (G) in reverse bias is relevant, as it depends on the deep trap concentration.

$$G \equiv \frac{n_i}{\tau_g} = \frac{\sigma_0 v_{th} N_t n_i}{2\cosh\left(\frac{E_t - E_i}{KT}\right)} \tag{3}$$

where n_i is the intrinsic carrier concentration, τ_g is the generation lifetime, σ_0 is the trap capture cross section (assuming, $\sigma_0 = \sigma_P = \sigma_N$ equal trap cross section for holes and electrons), N_t is the trap concentration, E_t is the trap energy level, E_i is the intrinsic Fermi level and KT is the thermal energy unit.

Note that the generation rate is maximum when $E_t = E_i$ and decays exponentially for $E_t < E_i$ and $E_t > E_i$. Therefore, only deep levels near the intrinsic Fermi level contribute to the generation rate. The excess generation current (or saturation current) is given by

$$I_{S\gamma} = \int_0^W qGdx = \frac{n_i}{\tau_g} qW \tag{4}$$

where τ_g comes from equation (3), q is the elementary charge and W is the depletion layer width.In summary, after γ irradiation, we expect an increase in the saturation current for the reverse biased diodes, with a nonlinear dependence on the dose [38] and, consequently, a decrease in the value of R_{LARGE}. This effect will occur for irradiation doses significantly lower than those that will produce total ionizing dose (TID) effects. At low dose, the increase of saturation current is approximately linear and follows the empirical law [39]:

$$\frac{I_{S\gamma}}{V} = \alpha D \tag{5}$$

where $I_{S\gamma}$ is the increase of reverse saturation current with the radiation, V is the effective diode volume, D is the dose and α is the current-related damage factor ($\sim 4 \times 10^{-17}$ A/cm for Silicon, see for example [34]). The aim of this work is to validate the hypothesis that displacement damage mechanisms will affect the pseudoresistor and to evaluate whether the reduction in equivalent resistivity is tolerable from the designer's point of view.

3.2. Proposed device under test

To evaluate the equivalent resistance of a pseudoresistor, the transient response at the gate of the QFG transistor (node A) needs to be observed. However, this is not possible without affecting the measurement. The simplest way to obtain an indirect measurement of this voltage is to apply the QFG technique to the transistor acting as a follower in a classical voltage follower (VF) topology; see Fig. 5.

Theoretically, in a VF, the output voltage will perfectly follow the voltage at node A; specifically, the output will be the same except for the DC level that will be shifted by the V_{GS} drop. Note that in practise, the output voltage amplitude will be slightly attenuated due to the body effect of the nMOS transistor.

The expected transient output of the convectional VF is as follows:

$$v_o = \frac{g_m r_o}{1 + g_m r_o + g_{mb} r_o} v_i \approx \frac{g_m}{g_m + g_{mb}} v_i \tag{6}$$

As $1 + g_m r_o \gg 1$ and $g_m = k g_{mb}$. Note that $k < 1$ and it is dependent on the technology chosen.

In the case of the QFG version, this leads to the following:

$$v_o|_{QFG} \approx \frac{g_m}{g_m + g_{mb}} \cdot \frac{sR_{LARGE}C}{1 + sR_{LARGE}C} v_i \tag{7}$$

As a result of the specificities of this work and to validate our hypothesis, a device under test (DUT) was constructed where we could isolate the effect of the ionizing radiation on the pseudoresistor. Using the structure from Fig. 5 as a starting point, it is noticeable that several devices will suffer the effects of radiation. This is the case of the

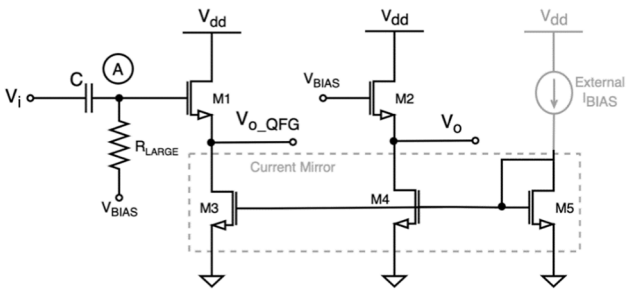

Fig. 6. Device under test (DUT).

Table 1
DUT sizing and biasing conditions.

Device	Value	Unit
M1/M2	50/1.05	μm/μm
M3/M4/M5	100.2/1.05	μm/μm
M_{RLARGE}	15/1.2	μm/μm
I_{BIAS}	100	μA

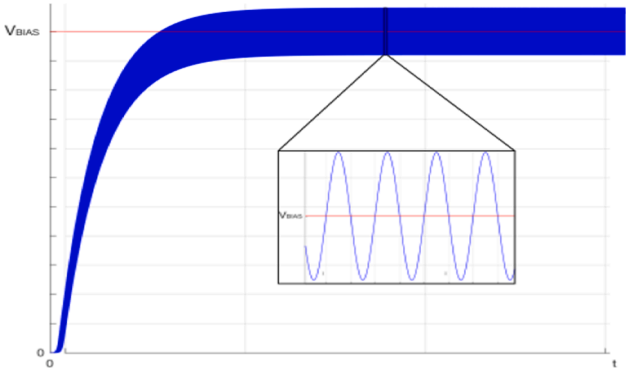

Fig. 7. Expected output (Vo_QFG in blue and Vo in red).

transistor acting as a follower and the bias current which will be implemented by an nMOS transistor with an adequate fixed V_{GS} voltage. The latter can be addressed by using an on-chip current mirror biased with external (non-exposed to radiation) constant current I_{BIAS}. If M3 and M5 are carefully matched in the layout, it is expected that I_{BIAS} will be copied from M5 to M3 without additional error in the presence of radiation.

The effect on the transistor acting as follower (M1) cannot be avoided. To overcome this issue, a conventional VF with the same sizing will be included to serve as a reference and control sample during the experiment. The output voltage of the classical voltage follower provides enough information to determine whether the DUT is performing adequately and, therefore, its performance will be monitored throughout the entire experiment. Moreover, any change in the output of the conventional VF will be a consequence of the effect of the radiation in M2 and thus we will be able to compensate them on M1 as they are expected to be identical. Note that the two VFs have been biased in strong inversion and matched (M1 with M2 and M3, M4 with M5) in the layout to minimize discrepancies between them. Fig. 6 shows the proposed DUT and Table I summarizes the transistors value and biasing conditions.

V_{BIAS} is a DC voltage that will bias both followers, ensuring saturation operation for all the transistors. This means that the expected output voltage for the classical VF will be a constant DC voltage equal to V_{BIAS}-$V_{GS|M1/2}$. V_i is a sinusoidal input signal with amplitude A_i that will be applied to the QFG version to evaluate the technique as in a real application. Note that the pseudoresistor under study has a non-symmetrical behaviour [31] depending on the condition Va > Vb or Va < Vb (see Fig. 3).

Regarding operation, initially, C is fully discharged, and the expected output voltage will increase exponentially from 0 to a final value of V_{BIAS}-$V_{GS|M1/2}$. This DC voltage is superposed with a sinusoidal signal of amplitude $g_m/(g_m + g_{mb})A_i \approx 0.83A_i$ (see Fig. 7). Note that, as we apply an input voltage that will change over time, the R_{LARGE} in the previous expressions will correspond to the average resistance of the pseudoresistor during the experiment. According to (4), the QFG-VF output reaches its final DC value with a time constant of $\tau = R_{LARGE}C$.

Regarding the capacitor, we are considering a poly-poly structure that uses SiO_2 as dielectric [40,41]. In the presence of radiation, the total number of holes generated in the dielectric per cm^2 that escape initial recombination, N_h is given by

$$N_h = f(E)g_0 D{\cdot}t \tag{8}$$

where f(E) is the hole yield as a function of the electric field, g_0 is the density of electron-hole pairs generated per cm^3 and per rad, D is the dose in rad and t is the dielectric thickness in centimetres [40,41]. Note that the presence of holes will translate into an amount of trapped charge or, what is the same, an initial charge in the capacitor but it will not imply a change in the value of the capacitor or in the τ.

According to [40,41], f(E) is extremely small for low electric fields such as the one that we expect during our experiment. So that trapped charge due to the ionizing radiation in the capacitors is negligible at low

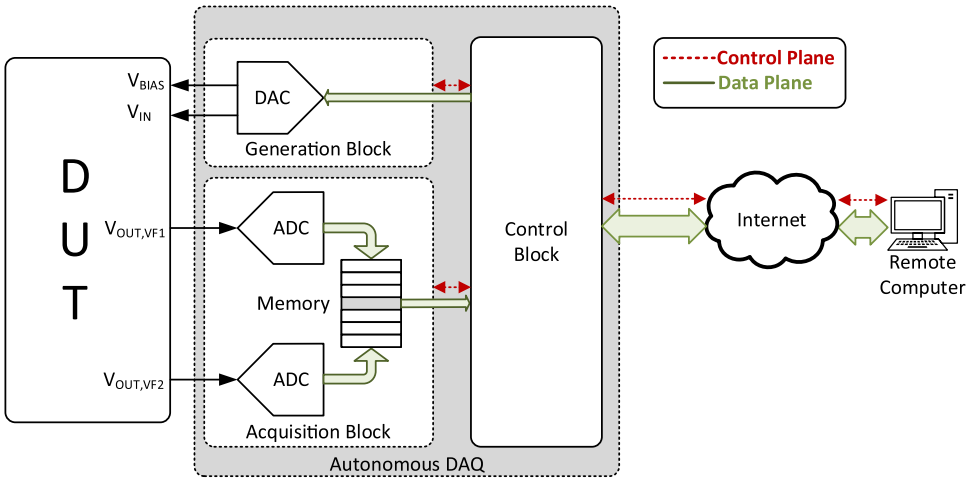

Fig. 8. Logic block diagram of the proposed autonomous data acquisition system.

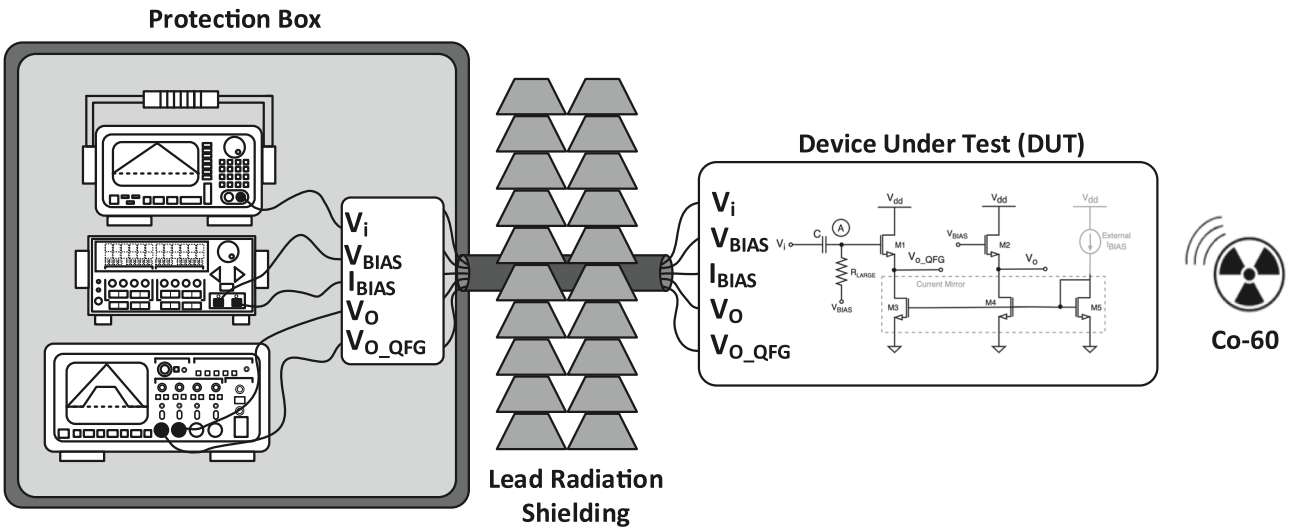

Fig. 9. Test Setup Diagram.

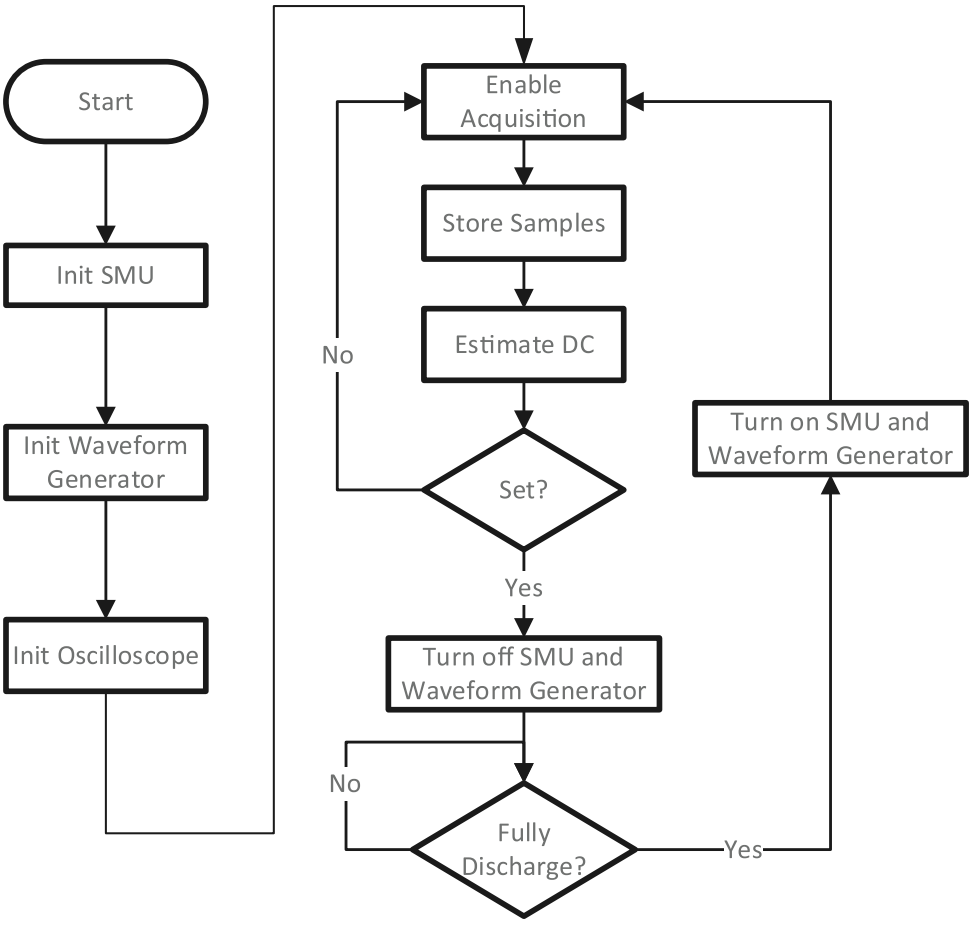

Fig. 10. Flow chart diagram of the control software developed.

doses where we expect a significant variation of R_{LARGE} and, it does not significantly affect the rest of the experiment.

In this scenario, variations in the τ of the QFG-VF are solely and directly caused by the radiation affecting the pseudoresistor. Therefore, τ is an indirect measurement of the average value of R_{LARGE} and we can evaluate the changes of its value due to radiation. Moreover, using an extremely high R_{LARGE} will reduce the input frequency restriction, and consequently the sampling rate of the experiment, as a very large settling time is expected.

4. Experiment and test setup

This section describes the experiment performed to assess the QFG under radiation.

Fig. 11. a) Photograph of the test setup b) detail of the DUT.

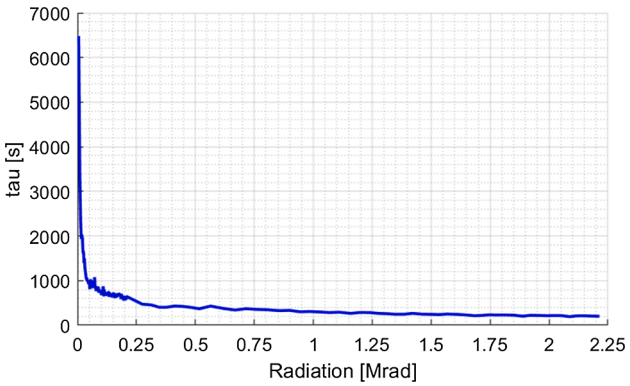

Fig. 12. Time constant versus radiation: 1st and 2nd campaigns.

4.1. Integration technology

As we want to evaluate the effect of ionizing radiation on pseudoresistors, in this experiment specifically gamma radiation, the DUT has been designed and manufactured in a standard CMOS 0.5 μm from ON Semi that uses a SiO_2 gate dielectric material of 13.5 nm thickness. This technology is highly sensitive to radiation due to the local oxide of silicon (LOCOS) process used for its field oxides [35]. To avoid TID effects, the dose of gamma radiation will be limited. In the case of validating the QFG technique under ionizing radiation for this technology, we could extend its use to modern processes where the LOCOS process is not used.

4.2. Test setup

The test setup has been designed according to current regulations and standards for testing cumulative effects of irradiation [42-45]. In these standards, the maximum stop time during the radiation is specified to not exceed two hours; otherwise, we will obtain unreliable intermediate measurements. Normally, measurements are made during stops scheduled for this purpose. However, since we expect settling times greater than the two-hour limit, we need to perform continuous monitoring of the circuit output. Furthermore, for safety reasons, access to the facility where the Co60 source is located is restricted during irradiation. Thus, the measurements must be performed remotely.

To satisfy these restrictions, an autonomous remote data acquisition system (DAQ) has been developed to supervise the experiment and acquire the output voltage of each VF in real time. The DAQ consists of a generation block, which is responsible for generating and injecting the corresponding stimulus to the DUT; an acquisition module, which oversees the acquisition and local storage of the voltage follower outputs; and a control block that supervises and controls the previous blocks and extracts and sends to a remote server the information from the intermediate memory. Fig. 8 shows a logic block diagram of the proposed DAQ system and Fig. 9 depicts its implementation. Note that the DAQ system includes two boards: one that serves as a holder to place the samples in front of the irradiator and another one that acts as an acquisition card, which oversees the distribution of the control signals and the excitation to the previous board and monitors the power supply and the reference voltages including the output. This second board, along with all the instrumentation, is located behind a lead wall to avoid exposure to radiation.

Specifically, the generation block consists of a waveform generator and a Source Measuring Unit (SMU). The first instrument generates the input signal V_i, while the SMU sets a proper biasing voltage V_{BIAS}. The

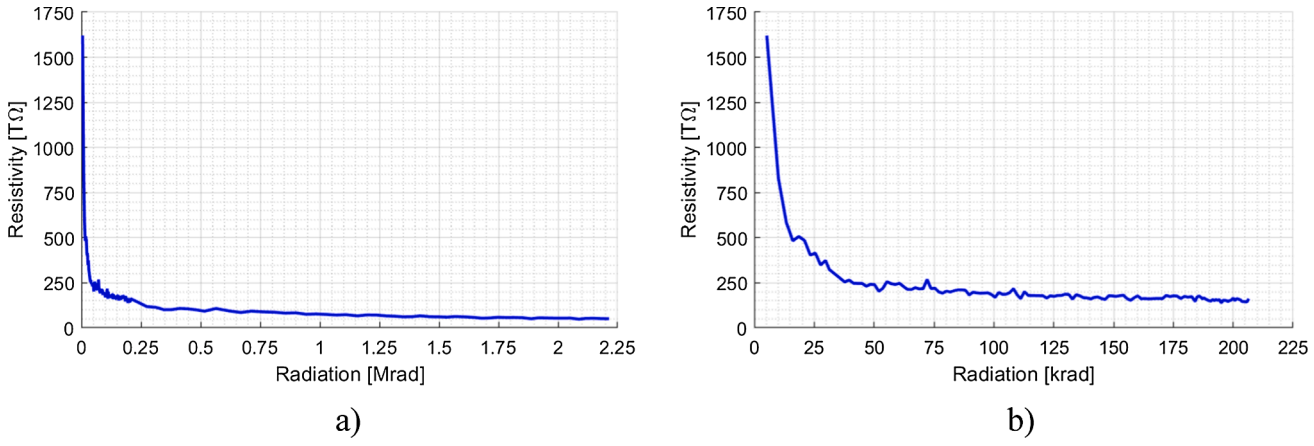

Fig. 13. R_{LARGE} vs radiation: a) 1st and 2nd campaigns and b) detail of the 1st campaign.

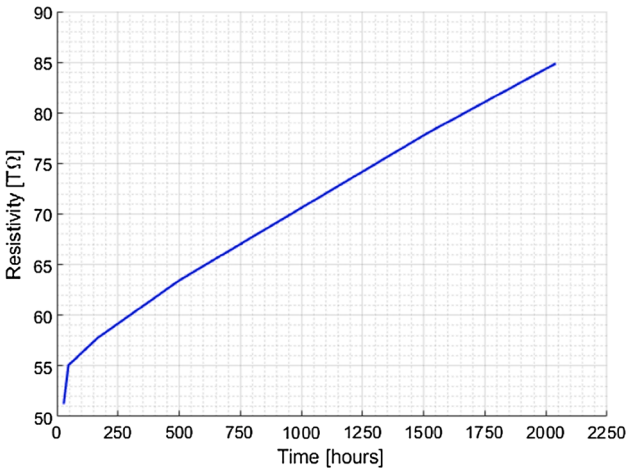

Fig. 14. Variation of R_{LARGE} versus Annealing time.

acquisition module is integrated by an oscilloscope; while the processing block corresponds to a laptop running the control and processing software described in the next section. This instrumentation was located inside a box covered with a layer of lead to protect sensitive equipment from the effects of radiation.

4.3. Control and processing software

This section describes the software developed to assist the implementation of a remote autonomous DAQ. Fig. 10 shows a flow chart that describes the software operation. First, the software initializes the instrumentation (waveform generator, SMU, and oscilloscope). To minimize errors during acquisition, the SMU is first configured, since it is responsible for providing the supply voltage (VDD = 5 V) and the biasing voltage (V_{BIAS} = 2.8 V). Next, the waveform generator is configured to inject a sinusoidal input signal of 200 mV amplitude and 50 Hz frequency. Finally, the oscilloscope is initialized to start the acquisition process at a rate of 25Kbps. Each acquisition window contains 10 signal cycles and 4096 samples. Once the acquisition is complete, the software extracts the information from the oscilloscope for further processing and storage on a remote server. The first step of processing is based on the estimate of the average value of the voltage follower output that includes the QFG transistor. Since the expected response of the system is equivalent to that of an overdamped system, it was considered that the circuit output had reached its steady state when the change in the mean is negligible. At that moment, the input stimuli and the bias voltage are turned off to ensure complete discharge of all the capacitances present in the circuit. This condition is guaranteed by waiting a time equivalent to the previous measurement time. Once the acquisition process is completed, it starts again.

4.4. Irradiation details

To measure the sensitivity of the QFG transistor to ionizing radiation, a source of Co-60, located inside a Gamma beam X200 irradiator from Best Theratronics, was used.

The DUTs were exposed to two irradiation campaigns at a controlled temperature of 22 °C. In the first, the DUTs were irradiated at a low rate to enhance the evaluation of the DUT. Note that we expected a significant variation in the behaviour of the device for low doses. Therefore, a lower radiation dose was required to accurately assess the effects of irradiation. Specifically, a dose rate of 218,4 rad (Si)/h was selected and applied for 948,84 h, resulting in a total dose of approximately 207 krad (Si). The second campaign was carried out at a standard radiation rate [42] and its duration was determined to assess the impact of high-dose accumulation on the DUT but it was limited to around 2 Mrad (Si) to avoid significant TID effects. As minimal variation is expected in this case, a greater accumulation between acquisitions does not imply information loss. Therefore, the samples were irradiated at a dose rate of 14.611 rad(Si)/h for 140 h, resulting in a total dose of 2,045 Mrad(Si). Finally, the samples were annealed at room temperature for 2040 h and additional results are provided from this period. Note that two samples were irradiated in this experiment. One was biased during the whole experiment, while the other was off during both irradiation campaigns. This implies that, in the case of the second sample, only the annealing information was obtained. Fig. 11 shows the final test setup at the Spanish National Center of Accelerators.

5. Experimental results and discussion

This section discusses the experimental results. The raw data stored from the measurements were visualized, analyzed, and processed. This post-processing calculates the DUT time constant and the equivalent resistor of R_{LARGE}. Fig. 12 and Fig. 13 show the time constant versus radiation and the average R_{LARGE} versus radiation, respectively. Annealing measurements were performed using the same setup as that used for the radiation experiment. The results for both samples are in perfect agreement, and no significant recovery is seen (Fig. 14 and Fig. 15).

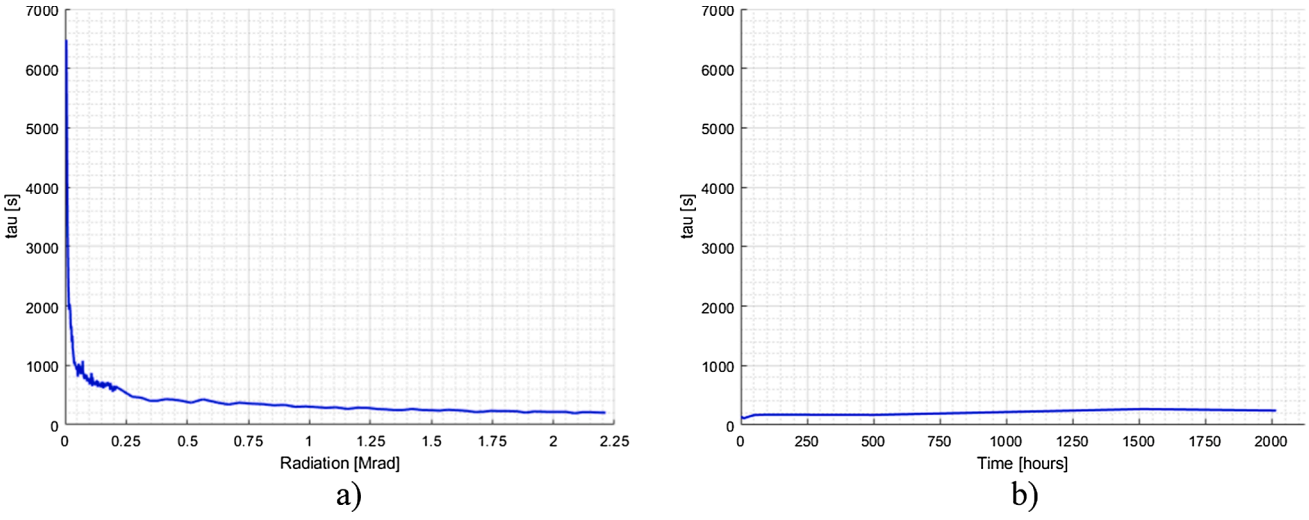

Fig. 15. Comparison of τ during a)1st and 2nd radiation campaigns and b) after 2040 h of annealing.

Based on the results, we can state that the resistivity of R_{LARGE} decreases with the increasing in γ-ray dose. Specifically, from around 1600 T Ω before irradiation to 50 T Ω at 2, 25 Mrad(Si). Note that this reduction is not linear and falls steeply in the first 50 krad(Si) (down to 200 T Ω), long before any expected TID effect. Therefore, our hypothesis has been validated and radiation displacement damage is responsible for the increase in the I_S of a reverse biased diode. As the observed effect is related to a body diode, it is reasonable to expect a similar behaviour in deep submicron technologies that are intrinsically TID resistant.

From the designer point of view, the decrease in R_{LARGE} implies an increase in the cutoff frequency of the high-pass filtering seen from the input to the gate of the transistor. This must be considered, especially in low-frequency applications. However, knowing that every 10 °C the saturation current approximately doubles [46], the effect of the temperature on the pseudoresistor is expected to be greater than the effect of the ionizing radiation, and therefore the former will be the limiting factor.

6. Conclusions

A wide number of applications and environments require low-power and/or low-voltage solutions. In this context, the QFG technique has demonstrated to be an interesting approach. However, until now, there are no studies on the viability of using this technique in high radiation environments. Thus, this work focuses on studying the effect of the ionizing radiation on pseudoresistors.

With this objective, a specific DUT has been designed and manufactured in a highly radiation sensitive technology. The DUT was irradiated with a Co-60 source observing an increase in the saturation current in the reverse biased silicon diode due to the appearance of deep levels in the energy band diagram of the silicon. Namely, displacement damage in the pseudoresistor results in a progressive decrease in resistivity, which is more significant at low radiation rates.

According to the results and for most applications, the variation of R_{LARGE} with temperature is expected to be more significant than with the irradiation and therefore, robust designs to temperature will also tolerate high doses of γ rays. Thus, this work is a starting point to pave the way for the use of QFG in harsh radiation environments.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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