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Monolithic Integration of Graphene in SiC Radiation Sensors for Harsh-Environment Applications

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Abstract. Due to their low leakage current, low noise levels, high thermal conductivity, and potential radiation hardness, SiC devices offer various advantages over Si devices in certain applications. As a result, they are being considered for operation in harsh environments, such as plasma diagnostic systems in future nuclear fusion reactors or in high energy physics applications. We report on relevant results of the GRACE project, which seeks to deliver a new generation of SiC sensors with graphene-enhanced contacts. Such devices are aimed to be radiation-hard and functional at high temperatures. The work presented in this paper focuses on the optimisation of the electrical contacts, along with the electrical characterisation and radiation-tolerance assessment of the first sensor prototypes produced.

Introduction

There is currently a particular interest in the R & D of radiation detectors in different wide bandgap materials, as they present various advantages over silicon devices [1]: low reverse bias voltage operation, even at room temperature after irradiation [2] [3]; potentially greater radiation hardness thanks to its high atomic displacement threshold [4] [5]; higher drift velocity [6]; and higher thermal conductivity [7]. In the past, SiC detectors were discarded due to the lack of high-quality large-area wafers [8]. However, nowadays the widespread use of SiC in power devices has pushed the quality of this material to levels similar to those of silicon. 150-mm wafers with a layer of up to 150 µm of epitaxially-grown SiC are now available [9]. The GRACE project aims to take the production of SiC sensors one step further by enhancing their electrical contacts with an epitaxially-grown graphene layer. This could improve the SiC-metal electrical contact as well as the overall thermal management of the devices. In addition, such a development would permit the production of sensors for heavy-ion detection, where the full active area is covered with graphene and no metal. The production and integration of epitaxial graphene on SiC wafers is one of the central challenges of this project. The epitaxial growth of graphene relies on the decomposition and controlled restructuring of the SiC crystal surface, which acts as the template for the subsequent nucleation and growth of graphene layers. The process involves a high temperature thermal process (>1500ºC) and results in a significant increase of SiC surface roughness [2]. In our case, the graphene is grown from the Al-doped p-type implant in the SiC. Thus, the Al-implanted layer also plays a relevant role, including its relation with the surface micro/nanostructure and metal thin film fabrication. To produce these sensors it was first necessary to identify and validate the best materials to build the devices. We had to address the design of the electrical contacts on p-type SiC, which must be optimised for operation under high levels of radiation and high temperatures. This development included testing the actual impact of enhancing the contacts with graphene, as well as verifying which multilayer alloyed contacts provide the best performance. Irradiation campaigns were carried out to evaluate the radiation hardness of each combination. The results obtained so far from the characterisation of test structures with different

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electrical contact designs are reported in this paper. Also, the initial results from the characterisation of the first production runs of SiC and graphene-enhanced SiC (EG-SiC) devices are presented.

Contact Optimisation

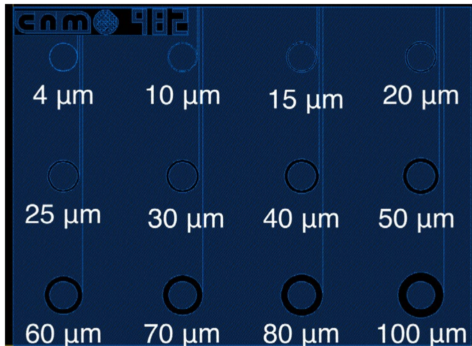

Fig. 1 Design of the CTLM test structures.

The first step towards the production of EG-SiC devices was the development of the fabrication process of test structures for the evaluation of metal contacts on both p-implanted SiC and on p-implanted SiC with a layer of epitaxially grown graphene (EG-SiC). To study the performance of each alloy stack proposed, a test methodology based on the circular transmission line model (CTLM) was used. This method implies the use of test structures comprised by several circular electrodes (inner radius L) encompassed by a non-metallised region (a gap of width d) and surrounded by a conducting (metallised) outer region. The layout of the test structures used can be seen in Fig. 1. The total resistance (R_T) of each circular contact is determined by measuring, through the 4-point method, the voltage drop as a function of the current applied. If these two parameters are linearly dependent, the slope corresponds to the R_T of the contact. Using CTLM, it is possible to extract the values of the sheet resistance (R_{sh}) and the contact resistivity (ρ_c) [10] [11].

In order to optimise the design of the electrical contacts, two different alloy stacks were proposed: Ti/Al/Ti/W (15/90/30/100 nm, deposited through evaporation) and Ti/Pt/Au (20/100/100 nm, sputter deposition). Low-resistivity SiC ohmic contacts based on Ti/Al are well recorded [6] hence the choice, and the cap layer of W is required to avoid oxidation. Graphene-metal ohmic contacts have not been documented to the same extent as their SiC counterparts. Having said that, the Ti/Pt/Au alloy was reported to create an effective ohmic contact with graphene in [12]. To ensure an ohmic behaviour of the contacts, they must be annealed at high temperatures for some minutes. This method is well studied for SiC, and it is known that the contacts must be annealed at temperatures above 900ºC [6], thus the chips were annealed at 960ºC for 2 min. A more conservative approach was taken for the EG-SiC test structures, which were annealed at 450ºC for 15 min. Later studies (not included here) showed that the same annealing process should be applied to both SiC and EG-SiC structures.

The CTLM test structures were produced in chips of about 3×3 cm^2. Optimising their fabrication on EG-SiC was not trivial. As a result, only one EG-SiC chip metallised with Ti/Pt/Au (*EG-SiC Chip 8*), with just three test structures, could be tested. The fabrication of SiC chips was simpler and two chips with tens of CTLM test structures were produced: *SiC Chip 1,* metallised with Ti/Al/Ti/W; and *SiC Chip 2,* metallised with Ti/Pt/Au. All chips were manufactured with the same p-implanted SiC wafer, ensuring equal substrate and implant properties for all. To validate the radiation tolerance of the contacts, two irradiation campaigns with 5-MeV protons were carried out at the Centro Nacional de Aceleradores (Seville, Spain). Table 1 summarises all their details.

The results obtained in terms of R_{sh} and ρ_c as a function of fluence are compiled in Fig. 2. As expected, all devices show a similar degradation upon irradiation of the R_{sh} (related to the doping concentration). At fluences above 10^{15} cm^{-2}, R_{sh} increases significantly. This is a clear sign of irradiation-induced effective acceptor removal in the p-type implant, an effect thoroughly studied in Si [13]. Regarding ρ_c, the degradation is most significant beyond 10^{15} cm^{-2}. However, this degradation was found to be lower in SiC Chip 2. In fact, this chip presented the lowest ρ_c of all, both before and after irradiation. In order to obtain conclusive results as to the behaviour of graphene-enhanced contacts, we are planning the fabrication of more EG-SiC chips for a new irradiation campaign.

Table 1 Details of the irradiation campaigns performed on chips with CTLM test structures.

Device	Metallisation	Annealing	Fluence [cm^{-2}] (nº of samples)
SiC Chip1	Ti/Al/Ti/W (15/90/30/100 nm - evaporation)	2 min 950ºC	0 (2), 10^{13} (5), 10^{14} (10), 10^{15} (10), 10^{16} (10)
SiC Chip 2	Ti/Pt/Au (20/100/100 nm - sputtering)	2 min 950ºC	0 (4), 10^{13} (2), 10^{14} (5), 10^{15} (5), 3×10^{15} (5), 6×10^{15} (5), 10^{16} (5)
EG-SiC Chip8	Ti/Pt/Au (20/100/100 nm - sputtering)	15 min 450ºC	0 (1), 10^{15} (1), 10^{16} (1)

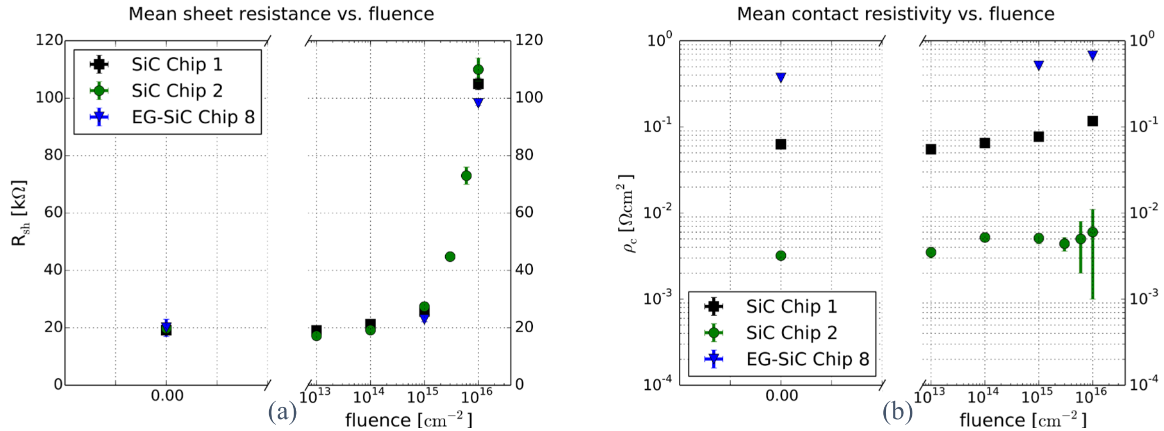

Fig. 2 Mean sheet resistance (a) and mean contact resistivity (b) as a function of fluence for three types of substrate-metal contacts: Ti/Al/Ti/W on p-implanted SiC (SiC Chip 1), Ti/Pt/Au on p-implanted SiC (SiC Chip 2), and Ti/Pt/Au on epitaxial graphene grown on p-implanted-SiC (EG-SiC Chip 8).

Fabrication and characterisation of sensor prototypes

A mask consisting of simple diodes, 4-quadrant diodes, circular diodes, MOS devices, and microstrip sensors was designed. Its design allows for the fabrication of devices with and without graphene enhanced contacts, see Fig. 3. Firstly, a wafer full of SiC devices without graphene was produced (*run 13575*). The front and back metallisation applied was of Ti/Al/Ti/Ni (10/70/30/80 nm) and Ti/Ni (30/150 nm), respectively. These alloy stacks were chosen for their compatibility with the foreseeing encapsulation for high-temperature-operation testing. The devices were electrically characterised and 8 sensors were irradiated. A new run including EG-SiC devices was produced, but

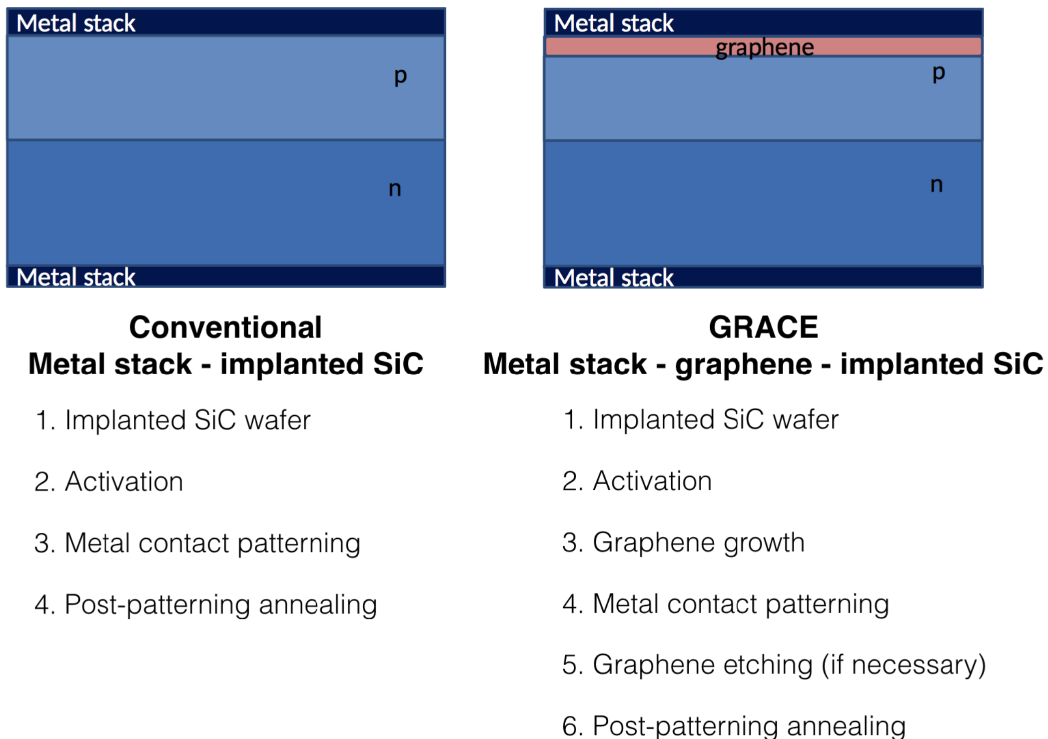

Fig. 3 Cross-section schematic and fabrication steps of SiC (left) and EG-SiC devices.

it was discovered that the fabrication process had to be modified in order to properly integrate the graphene in the detector structure. Thus, a new run (*run 14416*) with a metallisation of Ti/Pt/Au (20/100/100 nm) was produced, using a new and optimised fabrication method. The devices produced were electrically characterised. As a rule, all devices were classified as having high or low leakage current: if the leakage current is lower than 10 nA at 350 V, then they qualify as low current devices. Forward-bias current vs voltage measurements were also performed to verify that all devices worked properly.

SiC prototype sensors: simple diodes. The capacitance (CV) and leakage current (IV) curves with respect to voltage were measured. These measurements were performed using a probe station, where electrical contact is achieved via physical contact between the sensor and both a chuck (back contact) and a tungsten probe needle (front contact). IV measurements require solely the use of a high-voltage source measure unit, together with the aforementioned probe station. On the other hand, CV measurements require a more complex set-up. In addition to the LCR-meter needed for measuring the impedance, two voltage sources must be used simultaneously. One source is used to bias the sensor. The other provides an alternate current, which is necessary to measure the impedance of the device. Furthermore, a custom-made decoupling circuit is connected to both sources in order to disentangle both voltages.

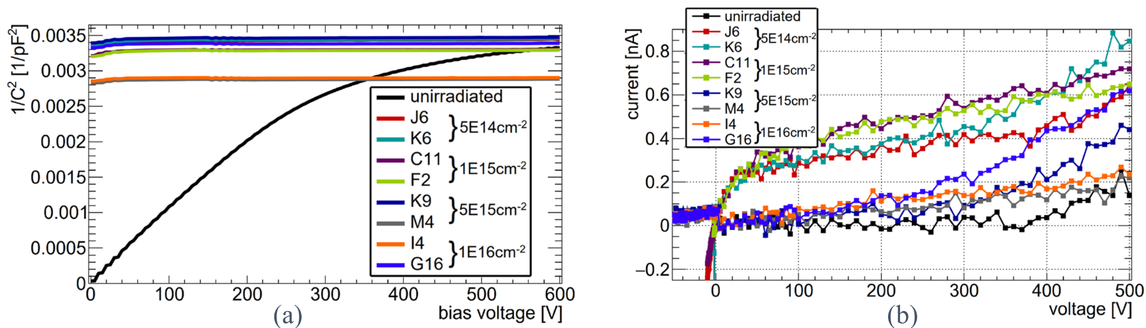

Fig. 4 CV curves at 10 kHz (a) and IV curves (b) for the diodes from run 13575 used in the irradiation campaign. SiC devices metallised with Ti/Al/Ti/Ni, no graphene enhancement.

The full depletion voltage, extracted from the CV curves (at 10 kHz), is of ~300 V. 61.5% of the sensors have a low leakage current. No correlation was found between the location of the devices within the wafer and their leakage current levels. A set of eight diodes were irradiated in pairs with thermal neutrons up to four fluences: 5×10^{14}, 10^{15}, 5×10^{15}, 10^{16} cm^{-2}. The irradiations were performed at the ATI Triga Mark II nuclear reactor [14]. Fig. 4 shows the CV and IV curves of the devices. At a fluence of 5×10^{15} cm^{-2} and beyond, the measured currents are higher than before irradiation, but significantly lower than those of lower fluences. Analysing the forward-bias region of the curves, no surge in current is observed. This indicates a loss of the pn-junction due to the materials becoming intrinsic after irradiation [15]. This is confirmed by the flat CV curves: a behaviour consistent with a parallel plate capacitor rather than a diode.

EG-SiC sensor prototypes. For this run only a quarter of a 4" SiC wafer was used. A few of the sensors had serious metallisation defects and could not be measured. These defects appeared mainly on the EG-SiC devices. In fact, it has been found that the presence of graphene tends to make the metallisation more fragile. CV/IV measurements were carried out on all the simple diodes and microstrip sensors that had no metallisation issues, see Fig. 5. To measure the microstrip sensors only one middle strip was contacted, the rest were left floating. The depletion voltage of the devices was of ~300 V. 85.3% of all simple diodes and 75% of all microstrip sensors had low leakage current. The overall results from this run are promising. The next step would be to produce a full wafer with SiC and EG-SiC devices and to perform an exhaustive irradiation campaign.

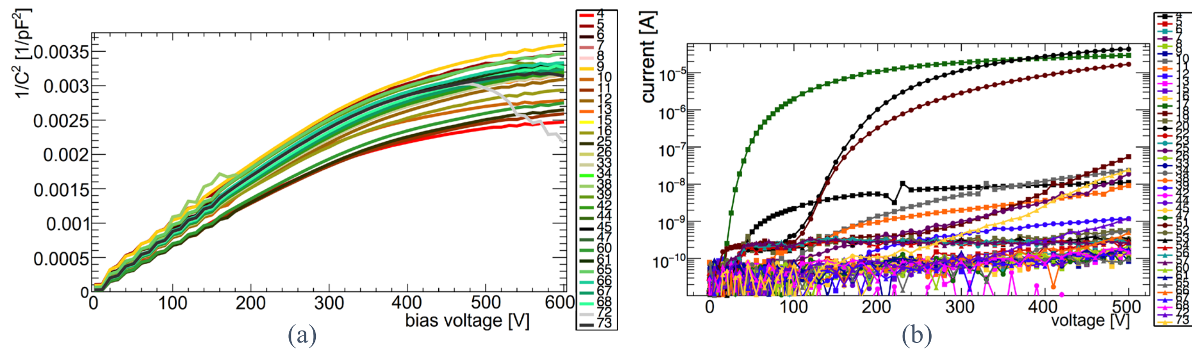

Fig. 5 CV curves at 10 kHz for the simple diodes (a) and IV curves for the simple diodes and microstrips (b) from run 14416. SiC and EG-SiC devices, all metallised with Ti/Pt/Au.

Conclusions

We observe low contact degradation with proton irradiation up to 10^{15} cm^{-2}. The best resistivity results were obtained with the Ti/Pt/Au alloy stack, although further studies are required for EG-SiC. SiC and EG-SiC prototype sensors were successfully fabricated. Neutron-irradiated SiC diodes (fluence $\geq 5\times10^{14}$ cm^{-2}) show signs of pn-junction loss due to the materials becoming intrinsic. An irradiation campaign of EG-SiC devices must be carried out to validate the technology.

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