Phase Transition Device for Phase Storing

María J. Avedillo, José María Quintana and Juan Núñez

***Abstract*— Nano-oscillators based on phase transitions materials (PTM) are being explored for the implementation of different non-conventional computing paradigms. This paper describes the capability of such autonomous non-linear oscillators to store phase-encoded information. A latch based in sub-harmonic injection locking using an oscillator composed of a PTM device and a transistor is described. Resistive coupling is used to inject both a required synchronization signal and the input to be stored. Operation of the proposed latch implementation, the embedding of functionality into the latch and its application to frequency division are illustrated and validated by simulation.**

***Keywords*—Phase transition materials, VO_2, Nano-oscillators, Sub-Harmonic injection locking, Phase-encoded logic.**

I. INTRODUCTION

Phase-Transition Materials (PTMs), with their abrupt switching between states with very different resistivity, are being explored both for implementing emerging devices, and for developing non-boolean computational paradigms.

Concerning the device application area, Phase-Change transistors (PCFETs) have been proposed by connecting a PTM to the source terminal of a FET. The abrupt insulator-metal transitions of the PTM are used as a mechanism to obtain steep switching and a boost in the I_{ON}/I_{OFF} [1], [2]. Several PCFETs exhibiting subthreshold slope (SS) under 60mV/dec have been experimentally obtained [3]-[5]. The combination of a PTM with Tunnel FETs (TFET) is also being explored to enhance the limited I_{ON} exhibited by TFETs [6]. In addition to reducing power consumption in conventional logic computation, associated with SS reduction [7], [8], recently, the mentioned PCFETs distinguishing features, such as improved I_{ON}-I_{OFF} ratio and steep switching, are starting to be exploited to enhance specific circuit topologies [9], [10].

In addition, PTMs are considered as potential candidates to enable new computational paradigms such as neuromorphic architectures. In particular, different groups are exploiting the capability of a PTM device in series with a resistor to oscillate (under certain constraints on the resistor value [11]) in the implementation of coupled-oscillator based processing [12]-[17]. In many cases, VO_2 PTM devices are proposed to be used for their implementation. This paper shows a different application for the PTM-based oscillators in the context of Phase-encoded Logic (PeL).

PeL is an old idea [18] based on von Neumann´s oscillatory computer. Instead of using voltage levels, logic values are encoded in the phase of an oscillating signal. This coding has advantages in terms of noise immunity over level-logic coding for low voltage applications [19]. Key components of PeL logic are oscillators, which oscillating phase depends on the phases of the applied inputs. That is, the resulting phase is a logic function of the inputs. It was demonstrated that PeL can implement any logic functionality [20]. The lack of suitable on-chip oscillators limited their commercial application.

Recently, PeL has received renewed interest due to the opportunity that novel nanodevices offer for the compact and energy-efficient implementation of oscillators [21]. In particular, in [19], [22], a PeL latch based on Sub-Harmonic Injection Locking (SHIL) is proposed. They report the use of CMOS ring oscillators and demonstrates a sequential circuit but other oscillators can be used. In [21], many oscillators are evaluated as potential building blocks of oscillatory computing architectures. In terms of energy, relaxation oscillators based on PTMs exhibit good performance. They are reported to consume more than one order of magnitude less energy per cycle than ultra-low-power ring oscillators. They occupy the second position (together with spin-hall oscillators) in terms of energy efficiency, just after superconducting oscillators. In this simulation based paper, we show that the above-mentioned SHIL latch can be implemented with the PTM based oscillator and illustrates different functionalities build upon it.

This paper is organized as follows: Section II is devoted to the background on both the phase change based oscillator and the SHIL phenomena. Section III describes the operation of the proposed PTM based PeL Latch and results of electrical Spectre [23] simulations carried out are described and analyzed. Finally, key conclusions are provided in Section V.

II. BACKGROUND

A. PTM based Oscillator

PTMs undergo insulator-metal transitions under given electrical stimuli. That is, they experience abrupt switching from/to a high resistivity state (insulating phase) to/from a low resistivity state (metallic phase). PTMs tend to stabilize in the insulating phase under no electrical stimuli. When the applied voltage increases and so the current density that flows through it reaches $J_{C\text{-}IMT}$, Insulator to Metal Transition (IMT) occurs. Once in the metallic state, when the voltage decreases and so the current density reduces below $J_{C\text{-}MIT}$, the Metal to Insulator Transition (MIT) takes place. Fig 1 shows the I-V characteristic of a PTM device. It corresponds to the PTM-Sim reported in [2], [7] with area $A=42\cdot21nm^2$ and length L=40nm. It has been obtained with a Verilog-A model inspired by the macro-model proposed in [2]. Material properties of this device, as well as electrical parameters of its model, are depicted in Table I. V_{IMT} (V_{MIT}) is the voltage at which the IMT (MIT) transition occurs. R_{INS} (R_{MET}) is the resistance of the PTM in the insulating (metallic) state. This is the PTM used in the work described in this paper. Since MIT and IMT transitions are abrupt but not instantaneous, a

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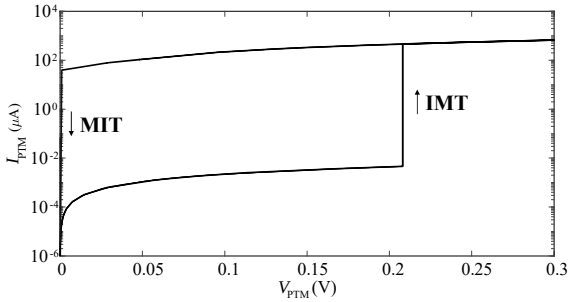


Fig 1. PTM I-V characteristic.

TABLE I. PHYSICAL AND ELECTRICAL PARAMETERS OF THE SIMULATED PTM DEVICE.

Physical parameters		Electrical parameters	
ρ_{INS}	100Ω·cm	R_{INS}	45.2MΩ
ρ_{MET}	0.001Ω·cm	R_{MET}	452Ω
$J_{C\text{-}MIT}$	8000A/cm^2	V_{MIT}	32μV
$J_{C\text{-}IMT}$	520A/cm^2	V_{IMT}	204mV

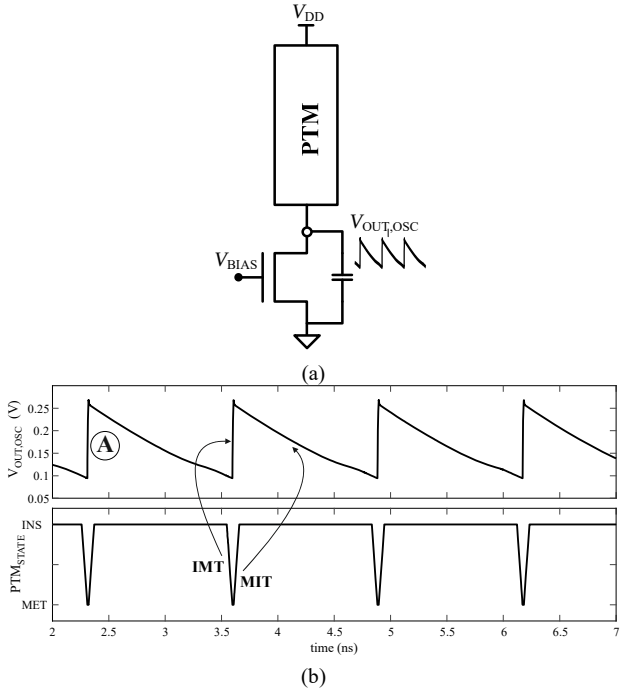


Fig 2. HyperFET oscillator a) topology, b) operation waveforms.

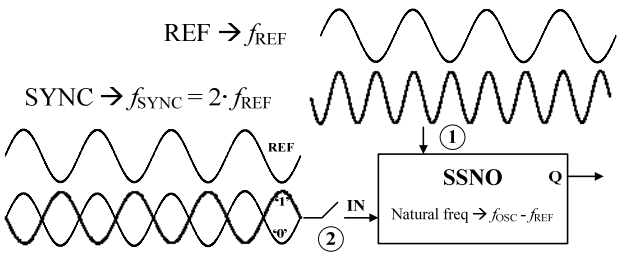


Fig 3. Sub-harmonic injection locking (SHIL) latch (after [19]).

transition time (TT) is also considered. The value reported in [2] (50ps) has been used. Also, a parallel parasitic capacitance of 1fF has been also included, according to [2].

Fig 2a shows a PTM based oscillator [11], [13]. The predictive transistor model of an HP 14nm transistor [25], [26] is used. This transistor has been selected because it is the one used in combination with the PTM-Sim in [2]. The circuit oscillates for a range of V_{BIAS} values. Fig 2b depicts simulated waveforms for the oscillator output, $V_{OUT,OSC}$ with V_{DD}= 0.3V and V_{BIAS}=0.14V. Transistor gate width (length) has been set to 1.12μm (18nm). The state of the PTM is also shown in order to better illustrate the circuit behavior. PTM_{STATE}='INS' means the device is in the insulating state. PTM_{STATE}='MET' corresponds to the device in the metallic state. Assuming the PTM is in an insulating state (point "A" in Fig 2b), the oscillator output is discharged through the transistor. This increases the voltage drop across the PTM (V_{DD} − $V_{OUT,OSC}$) and so current through it increases. Once enough current density circulates ($J_{C\text{-}IMT}$), it switches to the metallic state. Equivalently, using the electrical model, the switching to the metallic state occurs once the PTM voltage reaches V_{IMT}. The output is then charged through the PTM. This charging is very fast because of the low R_{MET} value and reduces the voltage seen by the PTM until it reaches V_{MIT} and the metallic to insulating state transition occurs. Note the frequency of the signal can be controlled with voltage V_{BIAS}. PTM based oscillators using VO_2 have been experimentally shown and are being explored to implement novel computational paradigms as it was already stated in the introductory section.

B. SHIL latch

Fig 3 depicts the sub-harmonic injection locking based latch for phase-encoded information. It is composed of a self-sustainable (autonomous) non-linear oscillator (SSNO), which produce periodic signals without any external frequency reference. When a suitable synchronization signal (SYNC) is injected into the oscillator (1), SHIL occurs and the oscillator adopts a frequency half the frequency of SYNC (f_{SYNC}) and becomes phase synchronized within one of two possible phases that are 180º apart. For this to occur, the natural frequency of the oscillator must be close to $f_{SYNC}/2$. In order to be able to distinguish the two SHIL phases, a REF signal of frequency $f_{SYNC}/2$ and phase-synchronized with SYNC is assumed to be available. The SHIL state in phase with REF represents one of the two logic values and the other one (180º apart) the other value.

The phase can be controlled by injecting a phase-encoded signal, IN (2). The oscillator adopts the phase of IN (logic value) and retains it when IN is no longer applied.

SSNOs (and so SHIL latches) can be built from different material system exploiting distinct physics phenomena. Examples are CMOS ring oscillators, MEMS/NEMS-based oscillators, spin-torque nano-oscillators or mechanical metronomes [24]. In this paper, we show that also PTM based oscillators can be used to implement this phase-encoded latch.

In addition, the SHIL operation of PTM based oscillators demonstrated in this paper could potentially increase robustness of the widely explored coupled oscillators processing architectures mentioned in the introductory section [27].

III. SHIL HYPERFET LATCH

The PTM oscillator described in Part A of Section II has been used to build the SHIL latch in Part B. Fig 4 depicts its schematic. Note that resistive coupling is used to inject the synchronization signal V_{SYNC}. Phase-encoded input to be

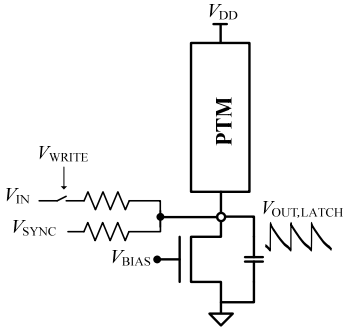


Fig 4. Schematic of the proposed SHIL latch.

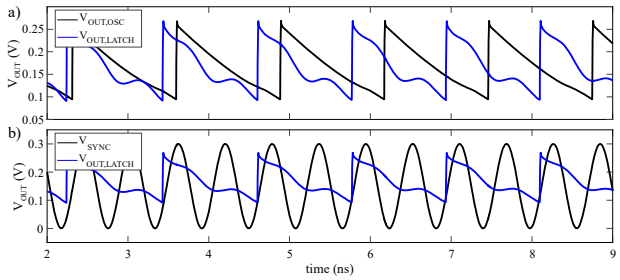


Fig 5. Simulation results for an oscillator with V_{SYNC} injected. a) Comparison of autonomous oscillator output ($V_{OUT,OSC}$) and with V_{SYNC} injected ($V_{OUT,LATCH}$), b) $V_{OUT,LATCH}$ H and V_{SYNC}.

stored (V_{IN}) is also applied through a resistance under the control of signal V_{WRITE}.

Let us first show the effect of applying V_{SYNC}. For that, Fig 5a compares simulation results obtained with Spectre for the autonomous oscillator in Fig 2 ($V_{OUT,OSC}$) and for the latch ($V_{OUT,LATCH}$) with V_{SYNC} injected, with an input resistance of 80kΩ, and no input applied (V_{WRITE} = 0). Note their frequencies are different. As it can be observed in Fig 5b, the latch locks with V_{SYNC} and exhibits a frequency that is half of the V_{SYNC} one. That is, it oscillates with V_{REF} frequency as explained in the previous section. In addition, two phases (180º apart) with respect to V_{REF} are possible for $V_{OUT,LATCH}$. This can be exploited to implement a latch storing phase-encoded information by shortly applying V_{IN} to control the stored phase, as we explain below.

Fig 6 depicts the operation of the latch. Input resistance has been set to 90kΩ. Waveforms for V_{WRITE}, V_{IN} and $V_{OUT,LATCH}$ are shown. To ease analysis, V_{REF} is shown overlapped with both V_{IN} and $V_{OUT,LATCH}$, so that phase information of each signal can be identified. The experiment shown corresponds to first storing V_{REF} shifted by 180º ($\overline{V_{REF}}$) with the first V_{WRITE} pulse shown and then applying V_{REF} (second V_{WRITE} pulse). Each input is applied for a few periods of the V_{SYNC} signal. That is, the switch is closed (V_{WRITE} = '1') for a few periods to store the input information. Correct operation has been obtained if the switch is closed for just one V_{SYNC} period. Note there are two phase-locking states between V_{REF} and $VOUT_{LATCH}$ as we have anticipated. Correct behavior is observed. The phase is stored when V_{WRITE} is activated (for example "A" in the figure) while it is kept if V_{IN} phase changes with V_{WRITE} = '0'. For example, point "B" in the figure in which it is shown that the input phase changes but the output latch phase doesn't. Waveforms at the bottom of the figure depict the transition region from one stored phase to another. V_{REF} ($\overline{V_{REF}}$) is stored as $V_{OUT,LATCH}$ with its maximum value before (after) the closest maximum V_{REF} value.

In order to further illustrate the latch operation, we have alternatively applied V_{REF} and $\overline{V_{REF}}$, and the phase difference

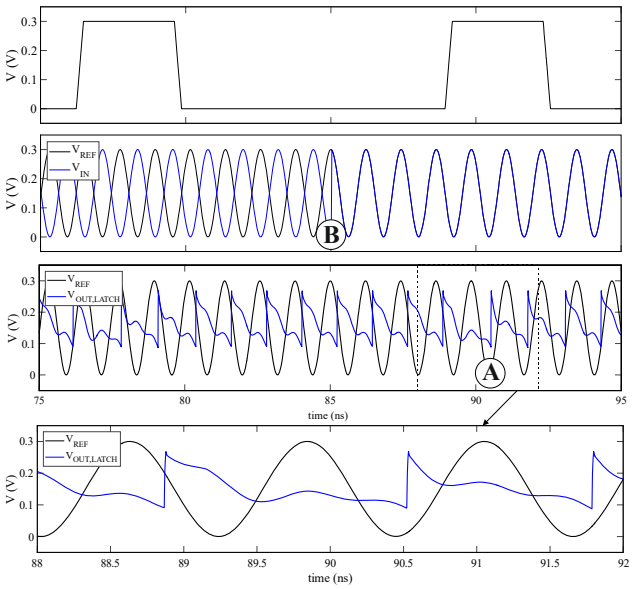


Fig 6. Operation of SHIL latch. Waveforms.

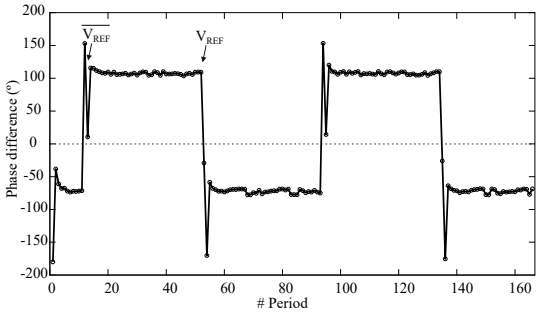


Fig 7. Operation of SHIL latch. Phase difference.

between V_{REF} and $V_{OUT,LATCH}$ has been measured (Fig 7). Reference points for such measurement are the maximum of each signal. Stable 180º apart phase-difference values are obtained when no input is applied. These values are different form 0º and 180º because of the non-sinusoidal latch output and the selected measurement criteria. However, the different sign obtained for both possible phases eases the analysis of the results. A negative (positive) value is associated with the storing of V_{REF} ($\overline{V_{REF}}$). During transitions, other phase-differences occur.

It is relevant exploring operation of the proposed latches under PTM parameter variations because they affect oscillator frequency and it is well known that natural operating frequency of intrinsic oscillator needs to be close enough to V_{REF} frequency for SHIL phenomenon to occur [22]. We have determined a correct behavior of our design of the proposed SHIL latch for V_{IMT} ± 5%. This robustness is similar to reported results of other applications using PTM based oscillators [14]. We have checked that the allowed range for natural frequencies can be optimized by adjusting the values of the coupling resistors, although an exhaustive optimization has not been carried out.

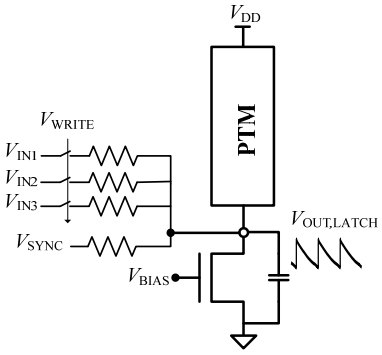
IV. CIRCUITS WITH THE SHIL HYPERFET LATCH

A number of circuits using the SHIL latch described in the previous section are illustrated.

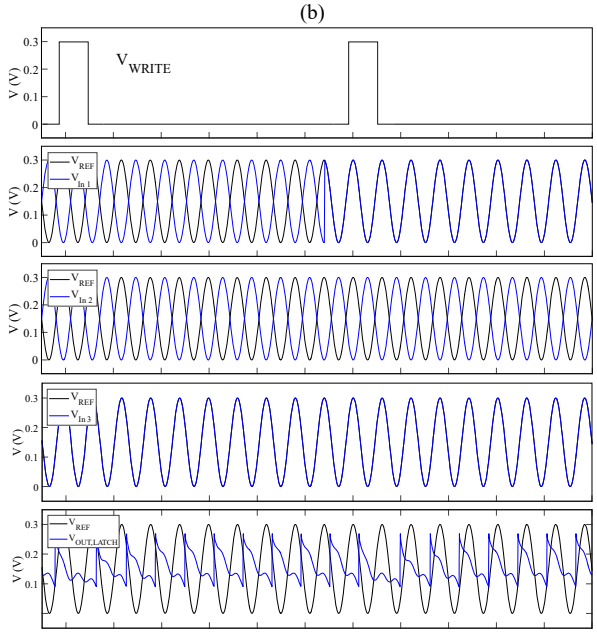
First, it is shown that majority functionality can be easily added to the proposed latch. Fig 8a shows the truth table of a

IN1	IN2	IN3	OUT
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

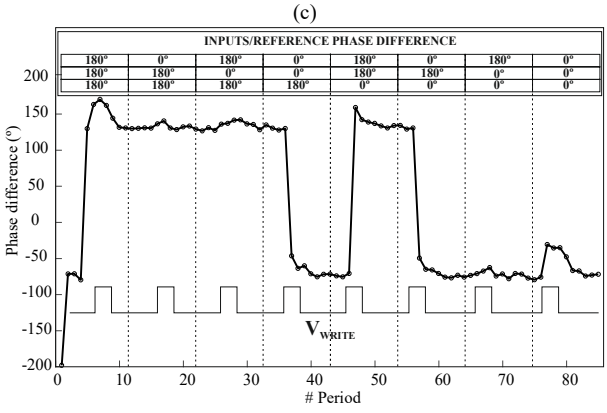
(a)



(b)



(c)



(d)

Fig 8. SHIL three-input majority latch. (a) Truth table (b) Schematic. (v) Waveforms. (d) Phase difference.

three-input majority function and Fig 8b depicts the schematic of a three-input majority latch. This circuit stores the majority phase of its three inputs. For example, for ($V_{IN1,}$ $V_{IN2,}$ V_{IN3}) = ($\overline{V_{REF}}$, $\overline{V_{REF}}$, V_{REF}), the phase corresponding to $\overline{V_{REF}}$ is stored and for ($V_{IN1,}$ $V_{IN2,}$ V_{IN3}) = (V_{REF}, $\overline{V_{REF}}$, V_{REF}) the phase corresponding to V_{REF} is stored. Fig 8c depicts simulation results for those input combinations. Fig 8d shows phase difference (similar to Fig 7) for the eight input combinations. 0º (180º) means that V_{REF} ($\overline{V_{REF}}$) is applied and V_{WRITE} is also displayed. It can be bserved that, again, two 180º apart phase states are stored into the latch. That stored information changes only when V_{WRITE} is activated and according to the applied input combination. A correct operation for all inputs combinations has been obtained.

It is interesting to realize that the boolean CMOS implementation functionally equivalent to this circuit requires seven NAND gates plus one inverter.

Second, the operation of a circuit in which several SHIL latches are chained is depicted. Clearly it is not possible to directly connect the output of a SHIL latch to the input of another because both of them would interact, and there is no guarantee that the first one forces the phase of the second. However it is possible to build logic circuits if somehow one oscillator is isolated from the other. For that a CMOS inverter (or a pair of them) can be used. Fig 9a shows the concatenation of two latches using an inverter between them. That is the inversion of the stored signal in $Latch_1$ is used as input for $Latch_2$. Fig 9b depicts simulated waveforms using non-overlapped write signals, as it is typical of latch based circuits. The output of each of the two latches (V_{OUT1} and V_{OUT2}) overlapped with V_{REF} are shown. It can be observed that initially (before the V_{WRITE1} pulse), the latches store different values (complementary). With the V_{WRITE1} pulse, the content of $Latch_1$ is changed and now both latches store same value (marked in the figure with a rectangle). With the V_{WRITE2} pulse the “complement” of the $Latch_1$ is stored in $Latch_2$. After, the latches store complementary values again.

It is well known that the majority logic function and NOT form a complete logic system. This means any combinational logic function can be implemented with them. We have shown in previous experiment hat the HyperFET SHIL latch can implement the majority and that the NOT for phase-encoded signals can be implemented with an inverter. In adittion we can connect gates. Thus, any logic circuit could be implemented with the described SHIL building blocks.

Finally, a different application of the SHIL HyperFET latch is illustrated. The behavior of this block applying only the synchronization signal (V_{SYNC}) can be described as dividing the frequency of V_{SYNC} by 2. Division by another factor (N) can be also achieved by applying a V_{SYNC} signal of frequency close to N times the natural frequency of the autonomous oscillator. Alternatively, since the natural frequency of the oscillator can be controlled by the voltage applied to the gate of the transistor, the division factor could be tuned. Fig 10 depicts the output of the latch for different gate voltages. Top waveform (V_{BIAS}=110mV) corresponds to division by 5 and bottom waveform (V_{BIAS}=140mV) to division by 2.

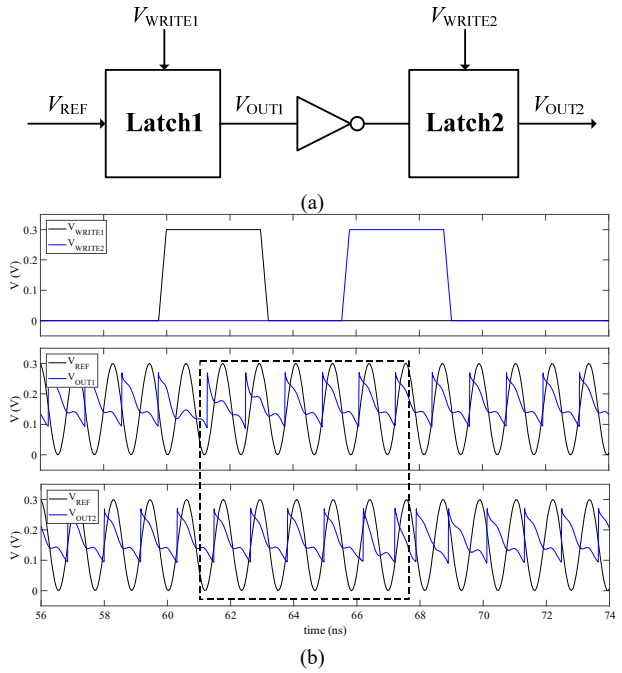


Fig 9. Interconnection of two SHIL latches using a CMOS inverter to isolate them. (a) Schematic (b) Simulated waveforms.

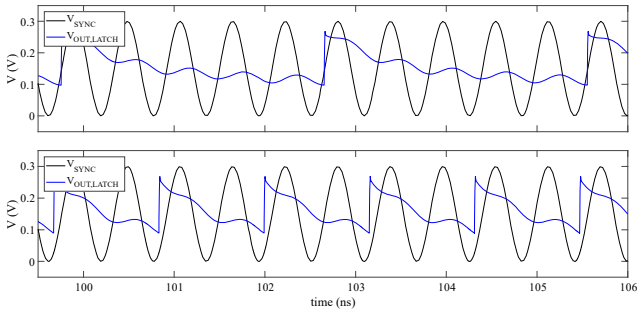


Fig 10. Waveforms illustrating the implementation of a frequency divider from a SHIL HyperFET latch. The upper figure corresponds to a division by 5 and the lower figure by 2.

V. CONCLUSIONS

It has been shown that a PTM based oscillator can be used to store phase-encoded information. For that, sub-harmonic injection locking is exploited. Up to our knowledge, it is the first work showing SHIL with PTM based oscillators. In addition to memory, majority and NOT functionality, that conforms a complete logic set, have been shown. A compact, energy efficient nano-oscillator has been identified as a potential candidate to implement phase encoded logical, although further work is required to evaluate it. Additionally, the showed SIHL operation of PTM based oscillators can have application in neuromorphic networks based on coupled VO2 networks.

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