# 1.5V Rail-to-Rail Programmable-Gain CMOS Amplifier

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**Abstract:** *A 1.5V programmable-gain differential amplifier is implemented using a novel design technique for operating closed-loop amplifier circuits at very low supply voltages. It is based on the use of quasi-floating gate transistors, avoiding issues encountered in true floating-gate structures such as the initial floating-gate charge, offset drift with temperature, and gain-bandwidth product degradation. A prototype fabricated in a 0.5-μm CMOS technology shows a 0.6% THD for almost rail-to-rail outputs and a 4 MHz unity-gain bandwidth.*

## 1. Introduction

Reliability and power consumption issues in modern submicron digital CMOS circuits, as well as increased demands of battery-operated portable equipment, are forcing CMOS analog circuits to operate at supply voltages close to the MOS threshold voltage. Signal swings comparable to the supply voltage are also required in order to minimize dynamic range degradation. In this scenario, analog design using Multiple-Input Floating Gate (MIFG) transistors has been proposed with some success [1,2]. These devices implement capacitive voltage dividers with relatively large attenuation factors at the transistor gates to reduce supply requirements. The dividers use a large biasing capacitance to set the floating gate DC voltage close to one of the supply rails. Unfortunately these dividers lead to a reduction of the effective transconductance and Gain-Bandwidth (GB) product of the circuit. Moreover, floating gates can trap a significant charge during fabrication that can produce large DC offsets [3] if it is not removed using additional processing steps (e.g., UV exposure).

An alternative approach proposed recently by some of the authors [4], is the use of circuits based on Quasi-Floating Gate (QFG) transistors. Similarly to MIFG transistors, inputs are capacitively coupled to the transistor gate, but a very large valued resistor weakly connects this gate to one of the supply rails. Therefore, this pull-up or pull-down resistor sets the DC gate voltage to one of the power rails, thus avoiding initial charge issues and minimizing simultaneously the supply voltage requirements. The large resistance value employed makes the gate effectively floating from signal frequencies of about 0.05 Hz, so that AC operation is unaffected even for very low frequencies. At the same time, GB degradation effects are avoided since a large biasing capacitor is no longer required. Moreover, input signals swing around the supply rail selected, favoring very low voltage operation. The resulting QFG circuits feature wideband operation at very low supply voltages, as experimentally demonstrated in [4] for feed-forward structures.

In this work, we propose the extension of this technique to feedback amplifier structures, exemplified by the design and implementation of a 1.5V fully differential programmable-gain amplifier (PGA).

## 2. QFG transistors

The equivalent circuit of an *N*-input QFG PMOS transistor (including parasitics) is shown in Fig. 1b, and its corresponding layout for the particular case of a 2-input QFG PMOS transistor in N-well technology is shown in Fig. 1a. The input terminals are capacitively coupled to the quasi-floating gate, which is weakly connected to one of the power rails (in this case $V_{SS}$) by a large valued resistor $R_{leak}$. As will be justified elsewhere, this pull-down resistor can be implemented in practice by the large (and nonlinear) leakage resistance of reverse-biased PN junctions of NMOS transistors operating in cutoff region, as shown in Fig. 1. This fact leads to significant savings in terms of area with regard to the MIFG case, based on a large biasing capacitor.

A simple analysis reveals that the AC voltage at the floating gate is given by

$$V_G = \frac{sR_{leak}}{1+sR_{leak}C_T}\left(\sum_{k=1}^{N} C_k V_k + C_{GS}V_S + C_{GD}V_D + C_{GB}V_B\right) \quad (1)$$

where $C_k$ is the coupling capacitance of the *k*-th input branch. The total capacitance $C_T$ is

$$C_T = \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB} + C'_{GD} \quad (2)$$

Note from (1) that inputs are high-pass filtered with a cutoff frequency $1/2\pi R_{leak} C_T$, which can be made very low. Therefore, even for very low frequencies, (1) becomes a weighted averaging of the AC input voltages

determined by capacitance ratios, plus some parasitic terms.

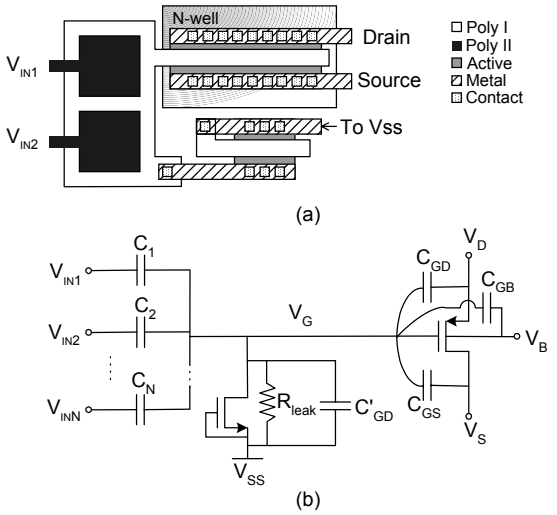


***Figure 1. QFG PMOS a) Layout b) Equivalent circuit***

Note also that the exact value of $R_{leak}$ or its temperature and voltage dependence are unimportant, provided that $R_{leak}$ remains large enough in order not to influence the circuit operation at the lowest frequency required. The exact value of $C_T$ is also unimportant.

The pull-down resistor $R_{leak}$ sets the gate to a DC voltage equal to the negative rail, to which an AC voltage given by (1) is superimposed. Hence, the gate voltage can become lower than $V_{SS}$. This is not a problem (using sub-volt supplies this is even a necessity) as long as it does not exceed the rail by more than the cut-in voltage of the source-body junction of the NMOS implementing $R_{leak}$, so that it never becomes forward-biased. The actual limit can be in practice slightly lower since close to the diode cut-in voltage the resistance value drops significantly, causing distortion. However, these issues do not affect feedback amplifier applications such as the amplifier proposed here, where these AC voltage swings become almost negligible.

The analysis for a QFG NMOS transistor is very similar. In this case, a pull-up resistor is employed (being implemented in practice by a reverse-biased PN junction of a PMOS transistor in cutoff) that sets the DC gate voltage to $V_{DD}$. The AC term (1) can then make the gate voltage larger than $V_{DD}$ (but unnoticeably in feedback amplifier circuits).

Amplifiers based on QFG input differential pairs can operate with very low supply voltages and featuring large GB values. In addition, they lead to very compact AC closed-loop implementations by just connecting one of the QFG input terminals to the output. The resulting capacitive feedback leads to an input resistance considerably larger than in conventional inverting amplifiers with resistive feedback, which are also subject to gain errors if the impedance of the source is not very low. In fact, although the beneficial effects of the QFG transistors were demonstrated experimentally by some of the authors for open-loop (feedforward) applications [4], it is in such closed-loop topologies where some of their most significant advantages arise:

a) Similarly to MIFG circuits [5], since the QFG MOS transistors forming the differential pair have identical source and bulk voltages (and very similar drain voltages), the contribution of parasitic capacitances in (1) is identical and cancels out in the expression of the differential gate voltage:

$$V_{G+} - V_{G-} \cong \frac{sR_{leak}}{1 + sR_{leak}C_T} \sum_{k=1}^{N} C_k \left(V_{k+} - V_{k-}\right) \qquad (3)$$

b) Moreover, as mentioned above, feedback minimizes input signal swings around the rail voltage in the quasi-floating gates, so that very nonlinear resistors can be employed for implementing the QFG resistors (see Fig. 1) without restricting the dynamic range. This leads to very compact circuits.

c) The DC input is set to one of the supply rails by the QFG resistors, and is therefore neither dependent on the DC output level nor set by the feedback loop. This allows the operation of the input differential pair even for minimum supply voltages, and avoids the need for a DC level shifter in the feedback loop for setting the proper input and output DC levels.

Nevertheless, (c) leads to an undesired by-side effect. DC input voltages are set by the pull-down transistors and not by the feedback loop, so that an autozeroing circuit is required in practice in order to prevent that the random amplifier offset subject to the large op-amp DC open loop gain saturates the output. Such practical issues are considered in the next section, where the design of an amplifier based on closed-loop QFG amplifiers is presented.

## 3. Programmable-Gain Amplifier

As an example of the technique proposed, Fig. 2a shows a novel programmable-gain differential amplifier. $N$ voltage gain values $A_1, A_2, \ldots A_N$ are available. Gain $A_i$ is selected by activating switches $SW_i$. Two $N+1$ input QFG transistors form the input differential pair of the amplifier. $N$ input branches with capacitances of values $A_1C, A_2C, \ldots, A_NC$ are connected to the selection switches, whereas the input branch with capacitance $C$ is connected to the output. Assuming a PMOS input amplifier, large valued pull-down resistors are required (for NMOS inputs, pull-up resistors would be necessary). They are implemented using the leakage resistance of reverse-biased PN junctions of NMOS transistors operating in cutoff region (see Fig. 2a), being their voltage dependence of little concern due to the small swings at the input gates (obviously, these junctions never become forward-biased for the same reason). Due to the amplifier feedback, a variation $\Delta v_{din}$ in the differential input voltage leads to a net charge transfer to the feedback capacitors of $A_iC\Delta v_{din}$ ($i=1,2,\ldots, N$ depending on the gain selected), and therefore to a variation $\Delta v_{dout}$ in the differential output voltage of

$$\Delta v_{dout} = A_i \Delta v_{din} \qquad (4)$$

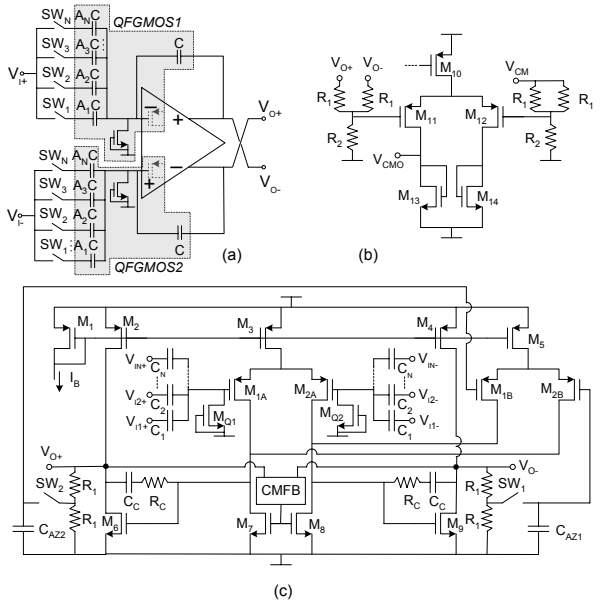


***Figure 2. PGA a) Diagram b) CMFB circuit d) Amplifier schematic***

Hence, a voltage gain of $A_i$ is obtained.

The required amplifier was implemented using a modified version of a differential two-stage Miller topology, as shown in Fig. 2c.

The autozeroing circuit is composed by the differential pair $M_{1B}$-$M_{2B}$, switches $SW_1$ and $SW_2$, capacitors $C_{AZ1}$ and $C_{AZ2}$, and two resistive dividers. The dividers are used to shift the output voltages close to the negative rail. This minimizes the supply requirements of the autozeroing amplifier. The offset cancellation, based on a technique described in [6], is as follows: during an initial phase the input is shorted, so that the differential input voltage corresponds to the amplifier offset. Switches $SW_1$ and $SW_2$ are closed and the output, once attenuated and level-shifted by the resistor dividers, is applied to capacitances $C_{AZ1}$ and $C_{AZ2}$. The resulting feedback sets the voltages at these capacitances so that the differential DC current in the autozeroing pair $M_{1B}$-$M_{2B}$ exactly compensates the differential DC current of the amplifier pair $M_{1A}$-$M_{2A}$ caused by the input DC offset (more exactly, currents in both differential pairs are balanced according to the offsets of both differential pairs). Then, switches $SW_1$ and $SW_2$ are opened, so that capacitors $C_{AZ1}$ and $C_{AZ2}$ keep the charge required for compensating the offset. The input short ceases and normal operation then starts. As will be demonstrated in the next section, the refreshing time required for this autozeroing can be very large (several seconds) since the circuit operates in AC. Hence, a small DC drift of the output caused by a slight discharge of $C_{AZ1} - C_{AZ2}$ is unimportant.

The Common-Mode Feedback (CMFB) circuit is a simple PMOS differential pair with resistive input dividers. These are also used to shift the output voltages close to the negative rail and to minimize supply requirements of the CMFB circuit as shown in Fig. 2b. The gate of transistor $M_{10}$ is connected to these of $M_1$-$M_5$ in the amplifier. Table 1 shows the values of the components employed in the circuits of Fig. 2b-2c.

| *TRANSISTORS, W (μm) , (all L=1μm)* | | | | | |
|---|---|---|---|---|---|
| $M_5$, ,$M_{Q1-2}$ | $M_{1-2A}$, $M_{11-12}$ | $M_{1B}$, $M_{2B}$ | $M_6$,$M_9$ | $M_{7-8}$, $M_{13-14}$ | $M_{10}$ |
| 120 | 200 | 400 | 150 | 15 | 180 |

| *RESISTORS* | | *CAPACITORS* | |
|---|---|---|---|
| $R_2$ | $R_C$ | $C_{AZ}$ | $C_C$ |
| 100k | 4k | 10pF | 0.75pF |

***Table 1. Component parameters in Fig. 1***

## 4. Measurement results

The differential programmable-gain amplifier of Fig. 2 with voltage gains equal to 1, 2, 4, and 8 was fabricated in a 0.5-μm CMOS DPDM n-well process (with transistor threshold voltages of approximately 0.8 V). A single 1.5 V supply voltage was employed, and the common mode output voltage was set to 0.75 V. The unit capacitance $C$ was 0.25 pF. Bias current $I_B$ was set to 20 μA. Fig. 3 shows the measured differential output voltage for a 1 Hz, $0.25V_{pp}$ input sinusoid and the amplifier gain set to 4, as well as the pulses of the autozeroing phase (which takes place when these pulses occur). Note that autozeroing intervals as long as 4 seconds can be employed without significant degradation in the output voltage. Note also how the circuit can operate even for very low frequencies due to the extremely large pull-down QFG resistance values.

Fig. 4 shows the measured differential output voltages obtained for a 10 kHz, 350 $mV_{pp}$ differential input sinusoid when the amplifier gain value is set to 1, 2, 4, and 8. The measured output spectrum for the larger output waveform in Fig. 4 is shown in Fig. 5. Due to the differential topology, distortion is almost exclusively of third order. Note the low distortion value obtained for almost rail-to-rail output swings. A 0.6% THD was measured for this output waveform. The measured unity-gain bandwidth was 4 MHz. The silicon area employed (input pads not included) was 0.20 $mm^2$, and the nominal power consumption was 0.78 mW.

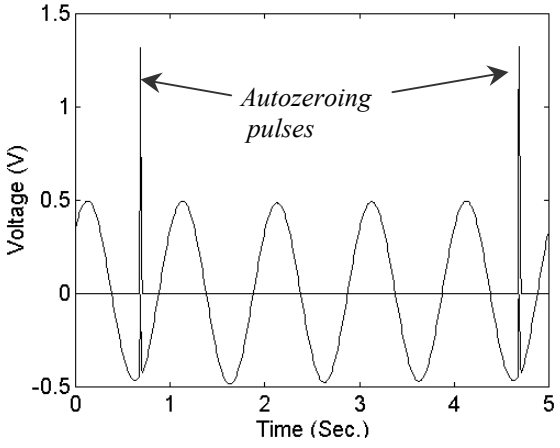


***Figure 3. Amplifier output voltage and autozeroing clock phase***

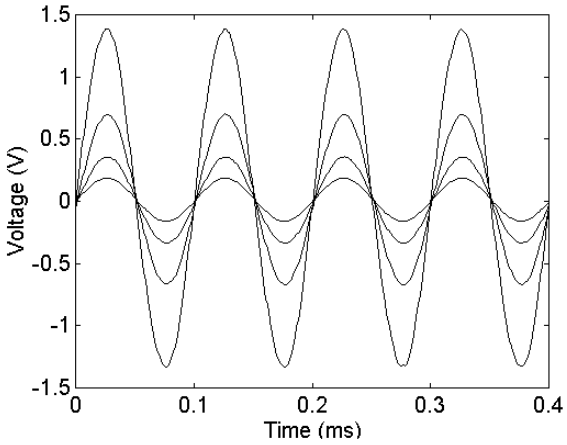


***Figure 4. Amplifier output waveforms for a 10 kHz, 0.35$V_{pp}$ input and different gain values***

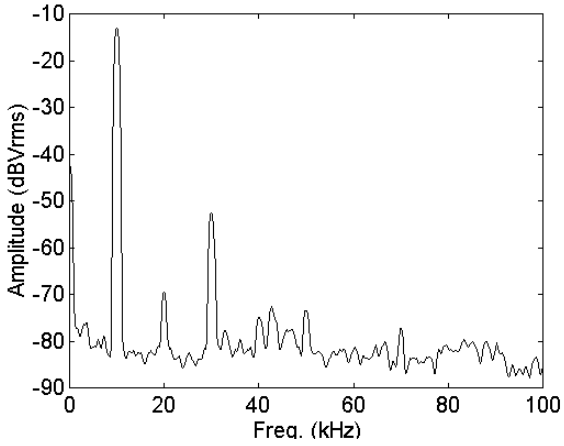


***Figure 5. Measured output spectrum for a 10 kHz, 0.35$V_{pp}$ input and a gain of 8***

A microphotograph of the chip is shown in Fig. 6. Capacitors were formed by interdigitized arrays of square capacitors to improve matching.

## 5. Conclusions

Very low voltage closed-loop CMOS amplifier circuits can be efficiently implemented using QFG transistors. The resulting amplifiers feature low distortion, almost rail-to-rail operation and low power consumption. Measurement results have been presented that confirm the feasibility of QFG devices for this application, as well as the correct operation of the autozeroing technique implemented.

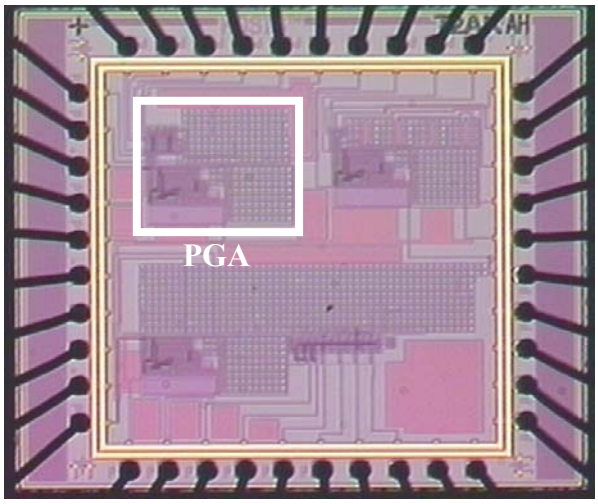


***Figure 6. Microphotograph of the chip***

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