Flexible Setup for the Measurement of CMOS Time-dependent Variability with Array-based Integrated Circuits

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***Abstract*—This paper presents an innovative and automated measurement setup for the characterization of variability effects in CMOS transistors using array-based integrated circuits, through which a better understanding of CMOS reliability could be attained. This setup addresses the issues that come with the need for a trustworthy statistical characterization of these effects: testing a very large number of devices accurately but, also, in a timely manner. The setup consists of software and hardware components that provide a user-friendly interface to perform the statistical characterization of CMOS transistors. Five different electrical tests, comprehending time-zero and time-dependent variability effects, can be carried out. Test preparation is, with the described setup, reduced to a few seconds. Moreover, smart parallelization techniques allow reducing the typically time-consuming aging characterization from months to days or even hours. The scope of this paper thus encompasses the methodology and practice of measurement of CMOS time-dependent variability, as well as the development of appropriate measurement systems and components used in efficiently generating and acquiring the necessary electrical signals.**

Keywords—* *Variability, Aging, BTI, HCI, RTN, Device Modelling, Automated characterization lab.

I. INTRODUCTION

In the last decades, CMOS technologies have experienced a steady scaling predicted by Moore's law, hugely improving the device performances. In this dive into the nanometer scale, dealing with (time-zero) variability (TZV) has been a constant struggle [1]. However, while manufacturing process variations have been kept under control (by steadily innovating in manufacturing tools and improvement strategies), random variations (like Random Discrete Dopants, Line Edge Roughness, Metal Grain Granularity, …), arising from the discreteness of charge and matter granularity, have become a critical concern for circuit design in advanced nodes, since they cause fluctuations that result in transistor electrical parameter mismatches between identically designed devices (e.g., threshold voltage mismatch) [2],[3]. Though (planar or 3D) SOI technologies mitigate this problem, it remains an important concern [4],[5].

Another source of transistor variability, known as time dependent variability (TDV), appears during circuit operation, and can be temporary or permanent. TDV phenomena, like Bias Temperature Instability (BTI) [6], Hot Carrier Injection (HCI) [7], [8], or time-dependent dielectric breakdown (TDDB) [9], which have been intensively investigated in the last decades, are reflected in the progressive degradation of the transistor parameters over time. All these phenomena become intrinsically stochastic at the nanometer scale. Another TDV phenomenon is the Random Telegraph Noise (RTN) [10], [11] transient effect, which consists in current fluctuations between two or more differentiated levels.

Today, all TDV phenomena are a serious concern because their inherent variability impact on circuit and system variability in advanced integration nodes [12],[13]. Therefore, statistical modeling and characterization of the device degradation produced by these sources of variability is mandatory. This degradation has been captured in several models reported so far, such as the Probabilistic Defect Occupancy (PDO) model [14], representing a key step in variability-aware design methodologies [15]. One major challenge related to the intrinsic random nature of the variability mechanisms is that a large number of transistors should be characterized to get statistically significant results. Thus, when thousands of devices should be tested, traditional on-wafer device testing techniques based on serial device characterization result in unfeasible testing times. In this scenario, integrated circuits (IC) with transistor arrays have been proposed for massive device characterization of TZV [16] and aging (BTI/HCI) [17]-[23], to reduce test times significantly. Array-based ICs for RTN characterization have been also developed [24],[25]. Recently, the first array-based IC enabling the characterization of all these effects has been proposed [26],[27].

Despite the advantages over conventional wafer-based techniques, array-based solutions bring new challenges (e.g., IR drops on internal chip metal lines, large number of devices or individual device access), critical not only for the design of the IC itself but also for the way in which it will be tested. Therefore, efficient and accurate setups must be developed to provide users with a hardware and software solution for fully-automated device-level variability characterization.

In this scenario, this paper presents a flexible characterization setup that consists in a complete laboratory instrumentation system and a fully-automated characterization software, together with a graphical user interface (GUI), to fulfill the hardware and software requirements for a trustworthy and straightforward transistor characterization.

The rest of this paper is organized as follows. A review of variability phenomena affecting CMOS transistors, along with the suitable characterization procedure, is explained in Section II. Section III briefly shows the features of the fabricated 65-nm CMOS array-based chip for which the measurement setup has been developed. A detailed description of the measurement hardware elements employed for the massive characterization of the chip devices is given in Section IV. Section V describes the design of the characterization software. Illustrative results obtained from the chip with the proposed setup are presented in section VI and, finally, the conclusions are drawn in Section

VII.

II. Variability Characterization in CMOS Transistors

A. I-V characterization

For the characterization of transistor variability, it is critical to obtain the transistor parameters, such as threshold voltage (V_{th0}) or mobility (μ_0), in order to assess their variations. The transistor parameters are extracted from the drain current vs. gate-source voltage (I_{DS}-V_{GS}) and the drain current vs. drain-source voltage (I_{DS}-V_{DS}) characteristics

B. Random Telegraph Noise characterization

Performance of short channel devices is strongly influenced by a random switching of I_{DS} between two or more levels along time. These current fluctuations are related to the capture and emission of charge carriers by oxide and interface traps, showing a large dependence on device biasing and temperature. The RTN phenomenon has been recognized as a significant variability source since it is responsible of device parameter shifts that increase inversely with area scaling [28].

The standard RTN characterization procedure consists in continuously measuring the I_{DS} current while maintaining a constant V_{DS} and V_{GS} bias voltage. Sufficient accuracy of the current measurement is required since the RTN-induced current variation may amount to just a few nanoamps. The time required for a statistically sound characterization of RTN depends on the trap(s) intrinsic capture/emission time constants, which span several orders of magnitude. Most previous efforts have been directed to RTN analysis methods (e.g., [29]) or to the necessary timings for a meaningful estimation of time constants [30]. Although these aspects deserve attention, only recently array-based solutions devised to satisfy the required statistical characterization have been reported [24]-[27]; bringing new challenges, e.g., automation, individual device access, or accurate control of bias voltages for an accurate characterization of the bias voltage dependence of time constants.

C. BTI and HCI characterization

BTI and HCI are both aging phenomena that produce a gradual shift of the device parameters over time: mainly an increase of the threshold voltage (V_{th0}), but also a decrease in the channel mobility (μ_0). Similar to RTN, the capture and emission of charges to/from traps are believed to be behind these shifts, with charges being stochastically trapped when a certain voltage is applied (therefore increasing the threshold voltage), and emitted when the voltage decreases (therefore the threshold voltage starts recovering its original value). Such shifts depend on the local temperature as well as on the (time-varying) voltages applied. The shifts can lead to severe, even fatal, circuit performance degradation. Therefore, in order to predict and mitigate these effects, the study of BTI and HCI phenomena has a renewed interest in nanometric technologies [31],[32]. Proper modelling [14], model parameter extraction [33],[34] and simulation strategies [35]-[37] are essential not only to implement appropriate variability-aware design techniques but for proper design of runtime compensation strategies [15],[38].

BTI/HCI transistor characterization commonly uses a stress-measurement (SM) technique that allows extracting the degraded transistor parameters and computing their shifts from their initial pristine values [6]. The SM technique used in this work follows three steps:

1) *Initial device characterization*: measurement of the pristine I_{DS}-V_{GS} curve (see Section II.A) to extract the device parameters before the application of any kind of stress.

2) *Stress*: BTI and HCI are long-term aging processes that take place while devices operate within their nominal operating voltages. Thus, in order to be able to characterize both aging processes in relatively short and affordable times, the devices must be subject to accelerated stress processes that consist in the application of high temperatures and/or overvoltages, e.g., twice the nominal supply voltage, to the device terminals [7],[39]-[41]. For BTI characterization, a high V_{GS} and V_{DS} = 0V are set, whereas, for HCI, V_{DS} is set at high values.

3) *Measurement:* the evolution of the drain current with time $I_{DS}(t)$ is registered right after the stress is removed, the exact moment at which the parameters of the stressed devices start recovering. During the $I_{DS}(t)$ measurement, the discharges (i.e., recoveries) of the traps previously charged in the stress phase are measured and characterized. The sampling rate during the measurement must be as high as possible in order to capture fast current events that may occur after the stress phase. At the end of each $I_{DS}(t)$ measurement, an additional I_{DS}-V_{GS} characterization is carried out for a complete analysis of the transistor parameter degradation.

As the device parameter degradation depends on the stress time, several SM cycles are applied sequentially to the samples, where the time on each stress cycle is typically increased exponentially. On the other hand, the elapsed time between the stress (second step) and measurement (third step) should be as short as possible and preferably equal for all tested devices because, as soon as the stress is removed, the recovery behavior of the threshold voltage begins.

The characterization of the different phenomena presented in this Section, together with the adopted array-based strategy, leads to a set of instrumentation and measurement challenges that the experimental setup should address:

- Massive characterization of many devices is needed due to the stochastic nature of TDV in nanometer-scale technologies.
- Transistors with different channel geometries should be characterized to study the dependence of TDV phenomena with device size.
- Accurate electrical characterization (which results in the need for canceling leakage currents, applying accurate voltages to the device terminals, minimizing the noise in the measurement lines and ensuring stable biasing) is required in order to correctly study the dependence of TDV with the bias conditions.
- Accurate thermal characterization over a broad range of temperatures is essential, since the TDV phenomena strongly depend on temperature.
- Characterization times must be affordable.
- Due to the large number of devices and the long characterization times, the control of the test process and data analysis must be fully automated.

These requirements are addressed by the combined power of an experimental setup composed of a hardware part (Section

IV) and a software part (Section V) and the array-based IC, named ENDURANCE, reported in [26],[27], and whose major characteristics impacting the experimental setup are reviewed in Section III.

III. Test Structures

The ENDURANCE chip is capable of characterizing TZV, BTI, HCI and RTN phenomena [26],[27]. The chip was fabricated in a 1.2-V, 65-nm CMOS technology with an area of 1800x1800 μm². It includes NMOS and PMOS transistors arranged in two independent arrays, with a total of 3,316 regular threshold voltage transistors, here forth known as the devices under test (DUT). Transistors with different width and length values have been included

Each DUT of the arrays is surrounded by a digital control circuitry, conforming what is called a unit cell of the array. The control circuitry determines how the terminals of the DUT (gate and drain terminals) are connected to the external chip pads.

The chip, which is encapsulated in a JLCC68 package, includes 64 pads, 36 corresponding to analog signals that connect to the DUT terminals, and 28 pads corresponding to digital signals that are connected to the control circuitry of the unit cells. Each array is subdivided in two subarrays that have independent analog signals connected to external pads. Three different paths connect the DUTs with the analog pads: a measurement path, a stress path and a stand-by path, and the gate and drain terminal of each DUT are connected through switches or transmission gates (TG) to all three paths. The drain terminal has Force and Sense [42] connections for both the measurement and the stress paths, so a total of 5 analog signals are connected to this terminal. Since negligible current flows through the gate terminal, it has no Force-&-Sense connection, so only 3 analog signals are connected to this DUT terminal.

The switches connecting the three paths are controlled by the digital control circuitry of the unit cell. Depending on the value of the digital control signals applied, each unit cell will be set in one out of the following four operation modes (OM):

(i) *Measurement mode*: it is designed to measure I-V characteristics, RTN transient effects and post-stress BTI/HCI phenomena. For these tests, only low voltages (i.e. from 0V to 1.2V) are allowed. The physical paths that connect to the DUT terminals are: the drain measure path (designed with Force-&-Sense lines to compensate for the IR drops) and the gate measure path.

(ii) *Stress mode*: it is designed to apply an overvoltage, i.e., from 1.2V to 3.3V, to the gate and/or drain terminals during the stress phase of BTI and HCI tests. The physical on-chip paths for this mode are the drain stress path (designed with Force-&-Sense lines), and the gate stress path. The availability of separate stress and measurement analog paths for the drain terminal enables the implementation of smart parallelization schemes, as detailed in Section V.

(iii) *Stand-by mode*: this mode sets all voltage differences of the DUT terminals at 0V when neither measurement nor stress are conducted, and is intended to avoid any device degradation while other devices are being measured or stressed.

iv) *Off mode*: this mode opens all switches or TGs of the unit cell, disconnecting the DUT from the analog paths. The off OM serves as a bridge between the stand-by mode and the measure/stress modes to prevent short-circuits. It is also used to disconnect non-functional DUTs.

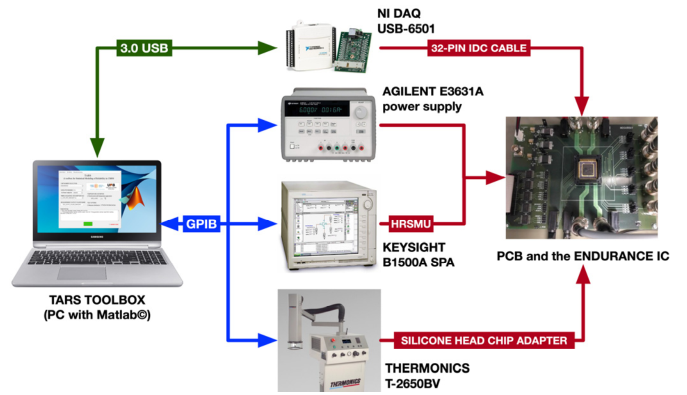

Figure 1. Schematic representation of the laboratory setup.

To avoid aging or degradation of the 8 TGs included in each unit cell due to the overvoltages applied during the stress mode, these are designed with IO transistors capable of withstanding voltages up to 3.3V without significant degradation during the experiments.

IV. Hardware Setup

An experimental setup has been developed for the characterization of the ENDURANCE chip. A schematic representation of this measurement setup is shown in Fig. 1. It consists of the following elements:

- A full-custom printed circuit board (PCB), where the ENDURANCE IC is inserted for DUT measurements.
- The Keysight Semiconductor Parameter Analyser (SPA) model B1500A. The system has 4 High Resolution Sense Measurement Units (HRSMU), with Force-&-Sense outputs for precise voltage application and current measurement [42]. The analog signal pads are connected to the HRSMUs, so that the voltage can be set, and, if necessary, the currents can be measured [43].
- The Agilent E3631A power supply for PCB (and subsequently IC) biasing using a 5V/1A DC biasing voltage [44].
- The T-2650BV Thermonics precision temperature system with a temperature ranging from room temperature to 120ºC [45].
- A USB Digital Acquisition System (DAQ), model USB-

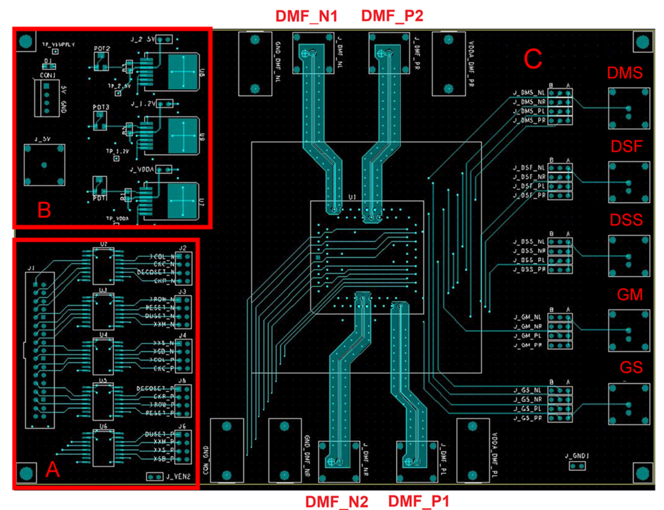

Figure 2. Top layout of the PCB.

6501 from National Instruments, equipped with 24 digital IO channels, that provides the digital signals for the IC control [46].

- A personal computer (PC) equipped with Matlab®.

The Agilent E3631A power supply, the Keysight B1500A SPA and the Thermonics temperature system T-2650BV are connected using an IEEE 488 General Purpose Interface Bus (GPIB) in order to send and receive data during tests executions. For the communication with the DAQ, a 3.0 USB connection is used.

The PCB has been designed to provide easy access to the chip, but preserving the accuracy of the measurements. Figure 2 shows the PCB layout composed of 3 main blocks: the input digital block (Fig. 2, section A), the biasing circuitry block (Fig. 2, section B) and the socket and connectors block (Fig. 2, section C). These blocks are explained in more detail below.

A. Biasing circuitry block

Three precise and stable biasing voltages are needed for the ENDURANCE chip. For this purpose, a dedicated biasing circuitry that uses three CMOS high precision voltage regulators has been implemented in the PCB circuitry (section B in Fig. 2). This circuitry provides, from a single 5V-1A DC power supply voltage, the biasing voltages of all digital circuits of the chip (1.2V), of the digital IO pads (2.5V) and of the transmission gates and analog pads that enable stress voltages up to 3.3V.

B. Input digital block

This block (located in section A in Fig. 2) is in charge of receiving the set of digital signals generated by the DAQ for the chip control. These signals are connected to the PCB through a 32-pin Insulation-Displacement Connector (IDC). A set of 5 digital electromagnetic isolator chips are used to transfer these digital signals to an isolated PCB power domain where the IC is located so that any noise coming from the PC power domain is reduced. This improves the set-up capabilities, especially for low-level current measurements.

C. Socket and connectors block

This block of the PCB includes a 68-pin zero-insertion force socket, where the ENDURANCE chips are inserted for testing, and different triax connectors that provide access to the output signal pads of the four arrays through the B1500 HRSMUs triaxial connectors and cables. The socket allows a large number of chip insertions, ensuring the durability of the test system.

As mentioned in Section III, each DUT terminal (i.e. drain and gate terminals) is connected to three different paths that can be accessed from independent analog pads for each array. Stand-by pads are physically connected to the analog ground or analog power supply voltage, depending on the type of DUT of the subarrays (N- or P-type transistors, respectively). The other pads are accessible through triaxial connectors. For those pads where current has to be measured, i.e. the drain measure force output pads of the four subarrays (DMF_N1, DMF_N2, DMF_P1 and DMF_P2 in Fig. 2), a built-in guard has been implemented between their triaxial connector and the IC socket pin. This guard is connected to the guard shield provided by the triax cables of the B1500 SPA, extending the isolation of the measured current to the PCB. This built-in guard has not been implemented in the other output pads because the current through them is negligible (which happens with the gate measure (GM), drain measure sense (DMS) and drain stress sense (DSS) lines), or are used for stressing the DUTs and the current is not measured (which happens with the gate stress (GS) and drain stress force (DSF) lines). These signals are physically multiplexed along the four DUT subarrays, so that only five additional triaxial connectors are necessary, as seen at the right side of the PCB in Fig. 2.

Finally, a squared area surrounding the IC socket has been left free of connectors. This area is used to place the head of the Thermonics system over the chip, so that temperature inside the head (and therefore, the temperature of the chip) can be controlled.

V. Software Tool

For the tests described in Section II, thousands of properly scheduled instructions are needed to control the hardware setup described in the previous section. Therefore, the need for automating the generation of instructions for the control of the hardware setup becomes patently clear. To this end, a software toolbox that generates all necessary GPIB and DAQ instructions named TARS (A Toolbox for Statistical Reliability Modelling of CMOS Devices) has been implemented using Matlab® scripting language [47]. This toolbox features several user-friendly GUIs (illustrated in Fig. 3) to facilitate the definition of measurement tests.

A. Architecture

The transformation of the test parameters specified by the user in Fig. 3 into a set of GPIB commands for instrumentation control as well as DAQ commands for IC control, follows a modular approach with three main modules and the scripts for the communication between them. These modules are:

(i) *Test plan generation*: this module receives the information about the user-defined tests and generates a script containing a specific test plan. This plan consists of a

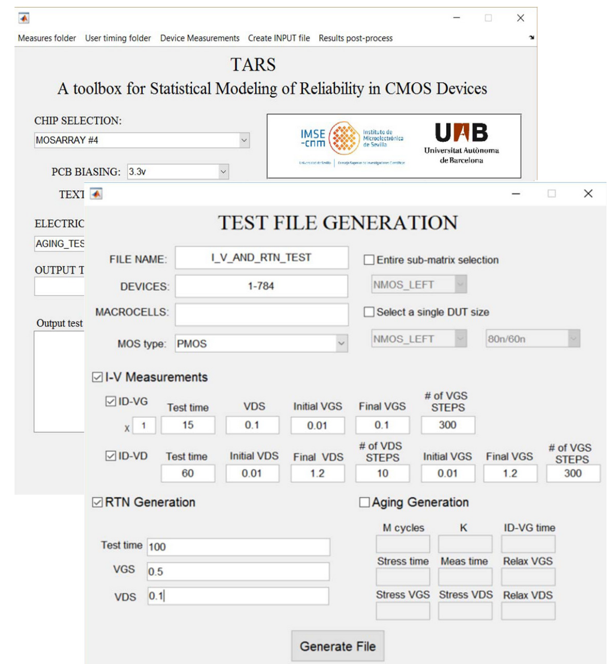

Figure 3. The Test Setup & Monitoring GUI of the TARS toolbox.

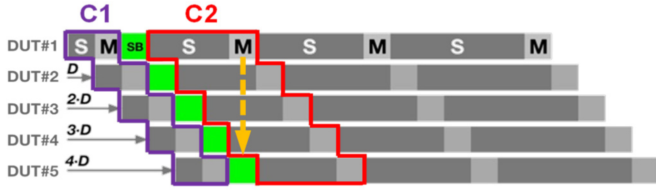

Figure 4. Illustrative example of the ADPSPM technique with 5 DUTs during a 4-cycle SM test. C1 corresponds to the first SM pattern and C2 to the second. The application of the ADPSPM algorithm shows that the measurement phases are not overlapped at any time thanks to the addition of SB periods.

proper sequence of the electrical tests to be applied to each DUT and the range of test conditions.

(ii) *Elementary instruction generation*: this module transforms each command of the test plan into the set of elementary actions that implement such command.

(iii) *Test execution*: this module reads each elementary instruction and generates and sends the corresponding GPIB commands to the instrumentation and the IC control instructions to the DAQ.

These three modules are described in detail in the following subsections. But before doing so, it is important to bring out a major advantage of array-based ICs over conventional probe stations: the possibility of executing parallel stress techniques to characterize HCI and BTI of hundreds of devices. However, it is not sufficient that an array-based IC enables that possibility, but more importantly, that the experimental setup must accurately and efficiently exploit such capability. The setup described in this paper uses the stress parallelization technique named *all-DUT-parallel-stress-pipeline measurements* (ADPSPM), which drastically reduces the total aging test time by stressing devices in parallel while maintaining sequential DUT measurement. This technique is directly involved in the generation of the appropriate test plan and, hence, it is described in the next subsection.

B. Stress parallelization

Parallelization techniques are used to dramatically speed up the aging tests. In this regard, the stress can be parallelized but only one DUT can be measured at a time to assess its degradation. The PSPM technique [48],[49] deals with this constraint by delaying the SM sequence of each DUT with respect to the previous one, resulting in a "place-and-check" algorithm that partially executes simultaneous (parallel) stress phases and pipeline measurement phases depending on the duration of the first stress period. This is done by delaying a complete number of SM cycles, which essentially means repeating the PSPM tests in series until all DUTs are tested. Therefore, the PSPM technique becomes inadequate for certain values of the initial stress time and number of SM cycles.

The ADPSPM parallel testing technique utilizes stand-by (SB) periods that are introduced between certain measurement and stress phases to make the necessary room to accommodate any number of DUTs. Obviously, the length of the SB periods must be accounted for during the postprocessing of measurement data to generate model parameters since the devices may continue their recovery during such period. As depicted in Fig. 4, in order to achieve an accurate and efficient SM parallel test, the algorithm handles each test cycle individually. In the first cycle (C1 polygon in Fig. 4), the SM pattern of each DUT is delayed, like in the PSPM approach, in order to ensure that the measurement phases in all DUTs are pipelined. Once all the SM patterns of cycle C1 have been temporarily allocated, the algorithm starts the distribution of the next cycle (C2 polygon in Fig. 4). The ADPSPM algorithm ensures that the last measurement phase of cycle C1 (for DUT#5 in Fig. 4) does not overlap with the first measurement phase of cycle C2 (for DUT#1), shown in Fig. 4 with a dashed arrow, by inserting the necessary standby periods (SB). Thus the ADPSPM technique can accommodate any number of DUTs.

To illustrate the advantages of this technique, it is interesting to perform a study of the time complexity of the characterization process. Fig. 5 shows the characterization time per device as a function of the number of DUTs for three different combinations of the number of SM cycles, measurement time, and duration of the stress periods. The

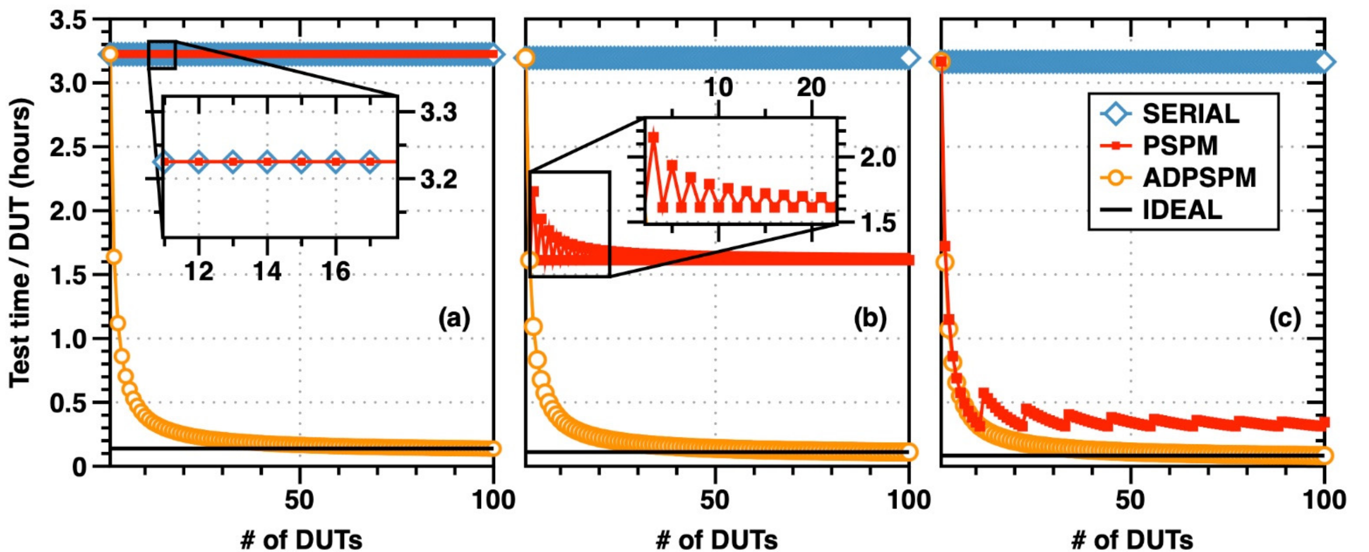

Figure 5. Total test time per device as a function of the number of devices for SERIAL, PSPM and ADPSPM techniques considering a measurement time of 100s and an exponential increase of stress time in SM cycles (base 10) with (a) 5-cycle SM aging test starting with a stress time of 1s, (b) 4-cycle SM aging test starting with a stress time of 10s and (c) 3-cycle SM aging test starting with a stress time of 100s.

measurement time of the SM cycles is 100s in all cases. The three cases use 5, 4 and 3 SM cycles, being the duration of the first stress period 1s, 10s and 100s, respectively, and exponentially increasing in the successive cycles. The blue diamonds represent the time complexity of the SERIAL test, a brute-force approach in which the devices are characterized one at a time, by applying the full sequence of SM cycles. The test of the following DUT does not start until all SM cycles of the previous device have finished. This implies that the test time per device amounts to the sum of stress times and measurement times of all SM cycles. If we consider the place-and-check PSPM technique for the conditions shown in Fig. 5(a) in red squares, no parallel stress can be applied because the initial stress time of 1s only allows to test one single device at a time, thus overlapping with the SERIAL testing time (see inset in Fig. 5(a)). This means that no time improvement when compared with SERIAL test can be achieved. On the contrary, the ADPSPM technique clearly shows a fast decrease of the test time per device when increasing the number of devices, as shown with the orange circles. In Fig. 5(b), the initial stress time is set to 10s allowing the PSPM technique to parallelize only 2 devices whereas in Fig.5(c) the initial stress time is set to 100s and up to 10 devices can be stressed in parallel with the PSPM technique. Correspondingly, the test time per device is reduced to one half or one tenth of the SERIAL procedure, but this 2-device or 10-device parallel scheme must be repeated until all devices are measured. Also in these cases, the ADPSPM technique reveals a significant test time reduction compared to the SERIAL and PSPM techniques, by parallelizing the stress phases whenever possible while maintaining the measurement channel occupied the maximum time (see Fig. 4).

As stated above, only one DUT can be measured at a time. Therefore, even if we ignore the stress times and the necessary parallelization, just the measurement periods imply the number of cycles x the measurement time per cycle. This IDEAL time is indicated as a continuous black line in Fig. 5. It represents an unreachable limit of the test time per device. It can be checked in Fig. 5 that in all test situations, the ADPSPM technique tends asymptotically to the IDEAL time when the number of DUTs increases.

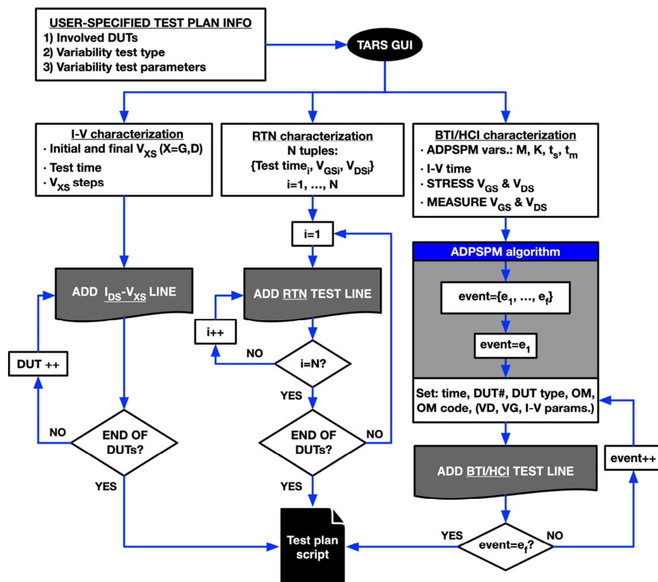

Figure 6. Flow diagram of the test plan generation.

C. *Test plan generation*

From the user-specified tests, e.g., those shown in Fig. 3, a test plan must be built. The test plan contains information about each test performed to each DUT. This information includes the DUT identification, the corresponding test, i.e., I_{DS}-V_{GS}, I_{DS}-V_{DS}, RTN or BTI/HCI, and the variables for the particular tests, i.e., delay time, voltages, temperature, etc. The test plan is written in a script, whose possible codes are displayed in Table I for each type of test.

For the generation of the test plan, the algorithm described by the flow diagram of Fig. 6 is executed. The algorithm is divided into three different branches: the I-V measurement branch, which is dedicated to I_{DS}-V_{GS} and I_{DS}-V_{DS} test plan generation, the RTN test branch, and the BTI/HCI aging branch, which applies the ADPSPM technique to optimally allocate stress, measurement and stand-by periods for all devices. Together with this algorithm, test plan instructions are scheduled with the goal of keeping equal stress/measurement periods for all devices and keeping an equal and minimum delay between the stress and the measurement periods of each device.

For the sake of illustration, let us consider a test example with just 5 devices where the test plan consists of (i) measuring the I_{DS}-V_{GS} curve of all devices, (ii) executing an RTN test with a single V_{GS}/V_{DS} condition and a measurement time of 100s, for all selected devices and, finally, (iii) running a 5-cycle SM BTI measurement with measurement time of 100s and exponentially (base 10) increasing test times starting at 1s using the ADPSPM parallelization algorithm. The resulting test plan script, shown partially in Fig. 7, contains the information that defines all these tests. Lines 2 to 5 show an excerpt of the I_{DS}-V_{GS} test plan. Line 2 sets DUT#1 in measurement mode with a sweep in V_{GS}. Then,

```
1   %IDS-VGS DUT TEST
2   5    1    N    ME   33   1.0e-01 1.5e-02 1.2e+00 0
3   0    1    N    SB   0    0    0
4   5    2    N    ME   33   1.0e-01 1.5e-02 1.2e+00 0
5   0    2    N    SB   0    0    0
6   ...
7
8   %RTN DUT TEST
9   100 1     N    ME 20 6.0e-01    1.0e-01
10  0    1    N    SB   0    0    0
11  100 2     N    ME 20 6.0e-01    1.0e-01
12  0    2    N    SB   0    0    0
13  ...
14
15  %ADPSPM PARALLEL TESTING
16  1    1    N    ST   11   2.5e+00 0
17  99   1    N    ME   23   6.0e-01 1.0e-01
18  0    2    N    ST   11   2.5e+00 0
19  1    1    N    ME   33   1.0e-01 2.0e-01 1.2e+00 0
20  0    1    N    SB   0    0    0
21  99   2    N    ME   23   6.0e-01 1.0e-01
22  0    3    N    ST   11   2.5e+00 0
23  1    2    N    ME   33   1.0e-01 2.0e-01 1.2e+00 0
24  0    2    N    SB   0    0    0
25  99   3    N    ME   23   6.0e-01 1.0e-01
26  0    4    N    ST   11   2.5e+00 0
27  1    3    N    ME   33   1.0e-01 2.0e-01 1.2e+00 0
28  0    3    N    SB   0    0    0
29  99   4    N    ME   23   6.0e-01 1.0e-01
30  0    5    N    ST   11   2.5e+00 0
31  1    4    N    ME   33   1.0e-01 2.0e-01 1.2e+00 0
32  0    4    N    SB   0    0    0
33  90   5    N    ME   23   6.0e-01 1.0e-01
34  0    1    N    ST   11   2.5e+00 0
35  9    5    N    ME   23   6.0e-01 1.0e-01
36  1    5    N    ME   33   1.0e-01 2.0e-01 1.2e+00 0
37  0    5    N    SB   0    0    0
38  90   1    N    ME   23   6.0e-01 1.0e-01
39  ...
```

Figure 7. Example of a test plan including I_{DS}-V_{GS}, RTN and BTI script lines.

TABLE I
CODES AND VARIABLES OF TEST PLAN SCRIPT AND ELEMENTARY INSTRUCTION SCRIPT

Test plan columns										
Electrical test	#1 (s)	#2 (integer)	#3 (ASCII)	#4 OM (ASCII)	#5 OM code (integer)	#6 (V)	#7 (V)	#8 (V)	#9 (V)	#10 (integer)
I_{DS}-V_{GS}	Time	DUT #	PMOS/NMOS	ME	33	V_D	Initial V_G	Final V_G	--	Step V_G
I_{DS}-V_{DS}	Time	DUT #	PMOS/NMOS	ME	44	Initial V_D	Final V_D	Initial V_G	Final V_G	Step V_G
RTN	Time	DUT #	PMOS/NMOS	ME	20	V_G	V_D	--	--	--
BTI	Time	DUT #	PMOS/NMOS	ME/ST	22/11	V_G	V_D	--	--	--
HCI	Time	DUT #	PMOS/NMOS	ME/ST	23/11	V_G	V_D	--	--	--
Stand-by	Time	DUT #	PMOS/NMOS	SB	0	V_G	V_D			
Elementary instruction columns										
	#1 (s)	#2 (integer)	#3 (ASCII)	#4 (ASCII)	#5 (integer)	#6 (V)	#7 (V)			
GPIB/DAQ variables	Test time	DUT #	PMOS/NMOS	OM	OM code	V_G	V_D			

the DUT is set in stand-by mode so that it does not suffer any degradation. Notice that the delay time in line 3 (first column) is 0, meaning that the following script line can be immediately executed. The same sequence is applied to the second DUT (lines 4-5) until we complete all devices. Lines 9 to 12 are an excerpt of the RTN characterization. Each device is sequentially measured for 100 seconds and set at stand-by mode after each measurement. For the implementation of the test plan of the BTI characterization experiment, the ADPSPM algorithm in Section V.B is executed. Lines 16 to 38 are an excerpt of the first BTI script lines of the test plan. Line 16 sets the first device in stress mode for one second. Then, the device must undergo a 100s measurement period. But 1 second before the measurement stage finishes, DUT#2 is set in stress (line 18). After the measurement of DUT#1 finishes it is set in stand-by (line 20). Thanks to setting DUT#2 in stress mode just the required stress time before the measurement of DUT#1 finishes, DUT#2 is ready for measurement just after DUT#1. The same procedure is sequentially applied to the rest of devices. When the allocation of the first SM cycle finishes, then, the second one starts with the first device. Notice that the stress period of the second cycle is 10s. Therefore, 10s before the measurement of DUT#5 finishes (line 33), the stress of DUT#1 is activated (line 34). This way, when the measurement of DUT#5 concludes, also does the stress time of DUT#1 and this device is ready for measurement (line 38). Therefore, we achieve two goals: maximum efficiency as the instruments are taking measurements the maximum possible time, and short and equal delay between stress and measurement.

```
1   %IDS-VGS
2   1.0000000000e-01   1   N   ME   33   2.000000e-01   1.000000e-01
3   2.0000000000e-01   1   N   ME   33   3.111110e-01   1.000000e-01
4   3.0000000000e-01   1   N   ME   33   4.222220e-01   1.000000e-01
5   4.0000000000e-01   1   N   ME   33   5.333330e-01   1.000000e-01
6   5.0000000000e-01   1   N   ME   33   6.444440e-01   1.000000e-01
7   6.0000000000e-01   1   N   ME   33   7.555560e-01   1.000000e-01
8   7.0000000000e-01   1   N   ME   33   8.666670e-01   1.000000e-01
9   8.0000000000e-01   1   N   ME   33   9.777780e-01   1.000000e-01
10  9.0000000000e-01   1   N   ME   33   1.088889e+00   1.000000e-01
11  1.0000000000e+00   1   N   ME   33   1.200000e+00   1.000000e-01
12  1.1000000000e+00   1   N   SB   0    0.000000e+00   0.000000e-00
13  ...
14
15  % ADPSPM parallel distribution
16  5.1000000000e+00   1   N   ST   11   2.500000e+00   0.000000e+00
17  6.1000000000e+00   1   N   ME   21   6.000000e-01   1.000000e-01
18  1.0510000000e+02   2   N   ST   11   2.500000e+00   0.000000e+00
19  1.0610000000e+02   1   N   SB   0    0.000000e+00   0.000000e+00
20  1.0610000000e+02   2   N   ME   21   6.000000e-01   1.000000e-01
21  2.0510000000e+02   3   N   ST   11   2.500000e+00   0.000000e+00
22  2.0610000000e+02   2   N   SB   0    0.000000e+00   0.000000e+00
23  2.0610000000e+02   3   N   ME   21   6.000000e-01   1.000000e-01
24  3.0510000000e+02   4   N   ST   11   2.500000e+00   0.000000e+00
25  3.0610000000e+02   3   N   SB   0    0.000000e+00   0.000000e+00
26  3.0610000000e+02   4   N   ME   21   6.000000e-01   1.000000e-01
27  4.0510000000e+02   5   N   ST   11   2.500000e+00   0.000000e+00
28  4.0610000000e+02   4   N   SB   0    0.000000e+00   0.000000e+00
29  4.0610000000e+02   5   N   ME   21   6.000000e-01   1.000000e-01
30  4.9610000000e+02   1   N   ST   11   2.500000e+00   0.000000e+00
31  4.9610000000e+02   5   N   ME   21   6.000000e-01   1.000000e-01
32  5.0610000000e+02   5   N   SB   0    0.000000e+00   0.000000e+00
33  5.0610000000e+02   1   N   ME   21   6.000000e-01   1.000000e-01
34  5.9610000000e+02   2   N   ST   11   2.500000e+00   0.000000e+00
35  5.9610000000e+02   1   N   ME   21   6.000000e-01   1.000000e-01
36  6.0610000000e+02   1   N   SB   0    0.000000e+00   0.000000e+00
37  6.0610000000e+02   2   N   ME   21   6.000000e-01   1.000000e-01
38  6.9610000000e+02   3   N   ST   11   2.500000e+00   0.000000e+00
39  6.9610000000e+02   2   N   ME   21   6.000000e-01   1.000000e-01
40  7.0610000000e+02   2   N   SB   0    0.000000e+00   0.000000e+00
41  7.0610000000e+02   3   N   ME   21   6.000000e-01   1.000000e-01
42  7.9610000000e+02   4   N   ST   11   2.500000e+00   0.000000e+00
43  7.9610000000e+02   3   N   ME   21   6.000000e-01   1.000000e-01
44  8.0610000000e+02   3   N   SB   0    0.000000e+00   0.000000e+00
45  ...
```

Figure 8. Example of the elementary test instruction script.

D. *Elementary test instruction generation*

The purpose of the test plan is to establish the set and sequence of test actions that have to be performed. The test actions have to be executed through the GPIB commands controlling the different instruments and the control commands of the DAQ for properly selecting and setting the DUTs. However, each line of the test plan script may involve different setting conditions that have to be sequentially established, e.g., each sampling point of the I_{DS}-V_{GS} curve of the test plan line is defined by a different gate voltage. Therefore, this second module transforms the test plan script into a set of sequential elementary instructions. Figure 8 shows an excerpt of the elementary instruction script obtained from the test plan in Fig. 7.

Each elementary instruction contains the information to set instruments and DUTs at the correct configuration. For instance, in the case of an RTN experiment, the variables that define the complete experiment are the test duration time, the temperature, the biasing voltages, the gate voltage and the drain voltage (see Table I, GPIB/DAQ variables row). In the case of an I_{DS}-V_{GS} curve, each sampling point of the sweep is defined by its timing, the drain voltage and the gate voltage. These variables will later be used to construct the GPIB commands that will be sent to the instrumentation and the DAQ commands that will be used to control the IC.

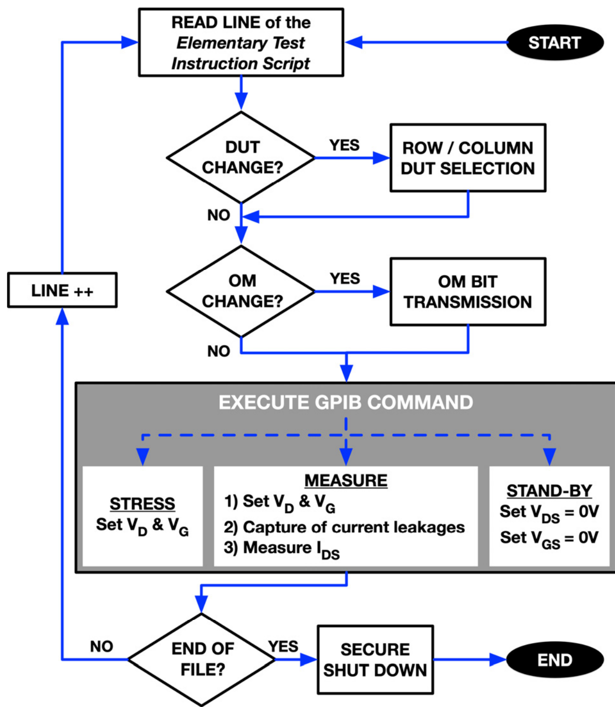

Figure 9. Flow diagram of the test execution module.

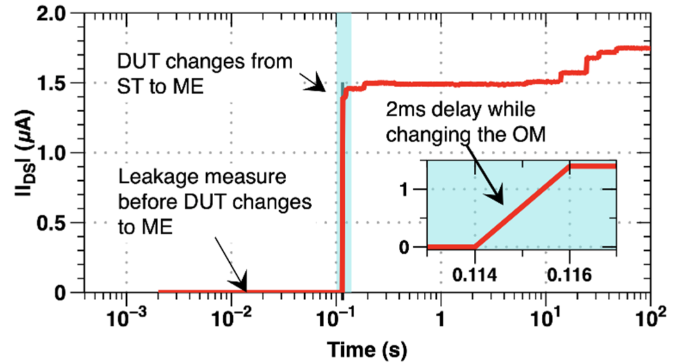

Figure 10. $I_{DS}(t)$ trace measurement after BTI stress executed following the 4-step process when switching from ST to ME.

E. Test execution

The test execution module, illustrated in the flow diagram in Fig. 9, reads and executes the *elementary test instruction script* line by line, converting the test variables into the corresponding GPIB and DAQ commands, and sending these to the measurement instruments and the data acquisition system.

The engine first analyses if the currently selected DUT must be changed. If this is the case, the module sends the corresponding row and column matrix addresses of the new DUT to the serial chip interfaces through the DAQ. Then, it activates the selected operation mode (OM) by connecting the drain and gate DUT terminals to the required analog IC paths. The same operation is performed if the DUT is not changed but a new OM code must be applied to the current DUT.

After the appropriate DUT is activated and the OM set, the test execution module extracts the V_{GS} and V_{DS} voltages and sends the appropriate commands to start a stress (ST) or a measurement (ME) phase:

(i) *Stress*: the stress biasing voltages are set to the drain and gate HRSMUs and no current is measured. The stress biasing voltages selected for the first time will be kept until the end of the selected test ensuring that all DUTs connected in parallel are stressed in the same conditions and without interruptions during the complete test duration.

(ii) *Measurement*: the biasing voltages of this mode can be changed each time a DUT is set into the measurement OM because only one DUT will be measured at any time. The test execution protocol executes the measurement in 4 steps to have a minimum time gap between ST and ME phases and to compensate the current leakage of the IC for the particular test conditions, i.e., DUT biasing and physical location. These four steps are:

1. **PAD biasing:** the algorithm biases the drain and gate measure lines (DMF, DMS and GM in Fig. 2).
2. **Current calibration through leakage measurement:** a leakage current measurement is performed through the DMF path to capture the current leakages happening in the path to the DUT drain (especially those coming from the TGs in that path). This leakage current will be used to calibrate the DUT current measurement.
3. **I_{DS} channel measurement:** the current through the measurement path is captured while the DUT still remains in its previous OM (i.e., stress OM), before digitally changing the OM code of the DUT unit cell. At this step, the drain/gate DUT terminals are still connected to the stress path. This step is obviously skipped if there was not a previous ST phase, e.g., RTN or I-V characterization.
4. **$I_{DS}(t)$ DUT measurement**: after starting the measurement, the OM code of the DUT unit cell is digitally changed to ME mode and the Drain/Gate DUT terminals are physically switched to the measurement paths. This switching procedure ensures that the time gap while changing to the measurement OM will remain minimum and equal for all DUTs involved in the test. The current is measured for the requested time, except in a I-V characterization in which a single current value is measured for the current bias voltage.

Figure 10 illustrates the measurement procedure during any measurement execution. The figure shows how the first measurement points represent only leakage because the DUT is still connected to the stress lines, and how after the leakage current measurement is done, the DUT OM is set to the measurement mode.

For the sake of illustration, when I_{DS}-V_{GS}, RTN and BTI tests are specified for 100 DUTs, a test plan with 2,500 lines is generated. Execution of this test plan produces 20,800 elementary test instructions that trigger the same number of GPIB commands as well as 2,300 instructions for the DAQ.

After the set of test experiments specified in the test plan are completed, a secure shut down protocol is initiated to prevent any electrical damage to the IC. First, a general RESET signal is sent to all unit cells in order to set the secure stand-by operation mode for all DUTs; second, all SPA HRSMU output terminals are set as open circuits; third, the PCB biasing voltage set by the power supply is removed, and, finally, the GPIB connections with the power supply and the B1500A SPA are terminated.

VI. Experimental Results

This section will show some illustrative experimental results obtained for pristine PMOS transistors using the

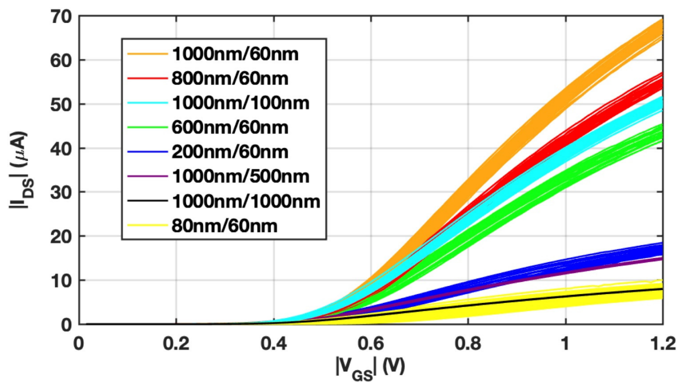

Figure 11. 784 PMOS $|I_{DS}|$-$|V_{GS}|$ curves measured for the eight available geometries in the ENDURANCE IC. The legend indicates the W/L ratio of each device.

proposed hardware setup together with the control software and the use of the ADPSPM parallelization technique.

Figure 11 shows a complete TZV I_{DS}-V_{GS} test executed over 784 devices involving 8 different geometries. Each I_{DS}-V_{GS} curve shown in Fig. 11 has been obtained by sweeping the $|V_{GS}|$ bias voltage from 10mV to 1.2V while maintaining the $|V_{DS}|$ voltage at 100mV. The results show a different current level and a large TZV for each geometry.

Figure 12 shows several measured RTN traces where each device shows unique RTN behavior. For these RTN measurements, the test plan has been created with $|V_{GS}| = 0.5V$ and $|V_{DS}| = 0.1V$ with a measurement time of 100s and a sampling rate of 500 samples per second for each device.

Figure 13 shows some of the measurement traces extracted from a BTI characterization test executed using the ADPSPM parallelization technique involving 100 PMOS DUTs. The stress voltages applied are $|V_{GS}| = 2.5V$ and $|V_{DS}| = 0V$ while the measurement voltages are set to $|V_{GS}| = 0.6V$ and $|V_{DS}| = 0.1V$. The measurements start 2ms after the stress is removed and 500 samples per second were acquired. The presented traces show discrete current steps as a consequence of charge detrapping from traps during the measurement time after the application of overvoltage stress. Thanks to the use of the ADPSPM technique, the total BTI test time is only ~14h whereas it would take ~13.5 days (i.e., ~23 times slower) with the conventional serial test approach.

VII. Conclusions

This paper describes a complete measurement setup for the characterization of CMOS transistors with array-based ICs, and the design of a full-custom user-friendly software, named TARS, for the automated generation and execution of

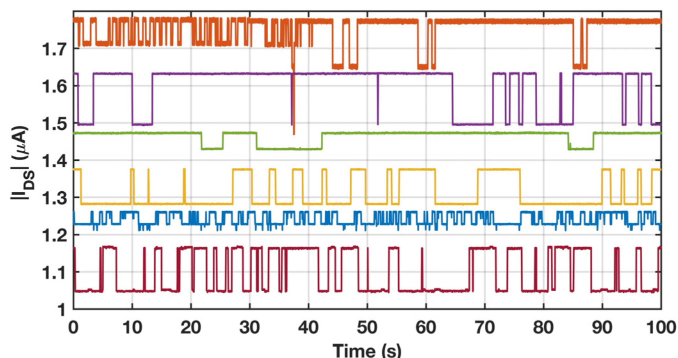

Figure 12. A set of 6 experimental RTN traces.

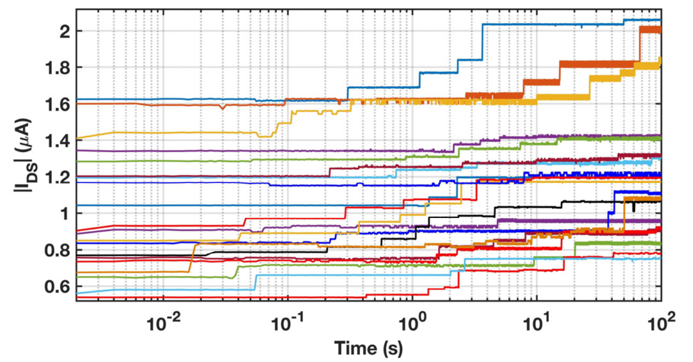

Figure 13. Several recovery traces from a massive BTI test involving 100 transistors with W=80nm and L=60nm, showing discrete current recovery steps.

variability tests. The system has been used to characterize the 65-nm transistors of the ENDURANCE IC, the first of its kind to enable TZV and pipelined TDV characterization, including HCI. The measurement setup enables several tests: ramped voltages (I_{DS}-V_{GS}, I_{DS}-V_{DS}), RTN measurements, and BTI and HCI aging evaluations. These tests can be defined in a matter of seconds and thousands of commands are automatically generated for instrumentation and chip control. The described measurement setup in combination with the ENDURANCE IC, empowered by the ADPSPM algorithm, allows the application of smart stress parallelization techniques to an unlimited number of devices. This testing technique smartly overlaps the stress phases of the aging tests, reducing the measurement time from years to days.

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