High-Voltage Compliant Neurostimulator With On-Chip Power Management in Standard CMOS Technology

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DAVID PALOMEQUE MANGUT

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Directores

MANUEL DELGADO RESTITUTO

ÁNGEL RODRÍGUEZ VÁZQUEZ

Tutor

ÁNGEL RODRÍGUEZ VÁZQUEZ

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Autor
David Palomeque Mangut
Graduado en Ingeniería Electrónica y Automática (Rama Industrial)
Máster en Investigación en Ingeniería y Arquitectura (Rama Industrial)

Director
Manuel Delgado Restituto
Investigador Científico
Instituto de Microelectronica de Sevilla (IMSE)
Consejo Superior de Investigaciones (CSIC)

Director y Tutor
Ángel Rodríguez Vázquez
Catedrático de Universidad
Departamento de Electrónica y Electromagnetismo
Universidad de Sevilla (US)

Instituciones
Universidad de Sevilla (US)
Consejo Superior de Investigaciones Científicas (CSIC)
Centro Nacional de Microelectrónica (CNM)
Instituto de Microelectrónica de Sevilla (IMSE)

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Abstract

This thesis is devoted to the design and development of Application-Specific Integrated Circuits (ASICs) in a standard 1.8V/3.3V CMOS process towards the implementation of a neural stimulator with high compliance voltage, which is a fundamental part of the neural implant that is being developed in this research group. Thus, most of this work deals with circuit-level and block-level techniques for the design and implementation of high-voltage-tolerant circuits in standard CMOS technologies, in the context of implantable systems.

Besides, this thesis preliminary addresses the wireless powering of the neural implant, including: (1) light harvesting with solar cells implemented on a standard CMOS technology and (2) the design and optimization of inductive links for wireless transfer of power and data to/from the neural implant.

Two ASICs were designed an fabricated. One includes the neural stimulator front-end and the power management unit. The other implements a CMOS solar cell with a novel stacked-diode configuration. Experimental results of both ASICs are shown and discussed. Summarising: (1) the neural stimulator front-end delivers currents up to 2.08 mA and has a compliance voltage of roughly 12.5 V; (2) the output voltage of the DC-DC converter in the power management unit ranges from 4.2 V up to 13.2 V, from a 3 V input source; (3) overall peak efficiency is close to 50%; and (4) the measured peak power generation of the CMOS solar cell was around 18 $\mu W\,mm^{-2}$.

Regarding the design and optimization of inductive Wireless Power and Data Transfer (WPDT) systems, a topology for the transmission of mW-power and Mbps-data over a single pair of coils was designed and simulated at the block-level. This topology shows promising results towards the implementation of a millimeter-sized wirelessly-powered neural implant with moderate power consumption and moderate data transmission rate.

Contents

List of Figures

List of Tables

Acronyms

AP Action Potential. 6, 7

ASIC Application-Specific Integrated Circuit. , i, xii, xiii, xv, 13, 68, 69, 79

ASK Amplitude-Shift Keying. 27, 31, 32, 33

CCS Current-Controlled Stimulator. i, 9, 10, 11, 12, 13, 14, 15, 16

CE Counter Electrode. 1, 5

CP Charge-Pump. 36, 37, 40, 41, 42, 43, 44, 52, 54

DAC Digital-to-Analog Converter. , 14, 47, 48, 64, 66, 67

DBS Deep-Brain Stimulation. 1, 5

DDT Downlink Data Transmission. ii, 31, 33

DNL Differential Non-Linearity. ii, 69, 70

DNW Deep N-type Well. 20, 21, 41

ECS Electrical-Cortical Stimulation. 1, 2, 5

ENS Electrical Neural Stimulator. 13, 64

ETI Electrode-Tissue Interface. , i, xi, 1, 2, 4, 5, 10, 13, 14, 16, 35, 61, 62

HCVC High Compliance Voltage Cell. ii, xii, 64, 65, 66, 67, 73

HV High-Voltage. ii, xii, xiii, 16, 36, 59, 63, 64, 74

HV-NSFE High-Voltage Neural Stimulator Front-End. xii, 61, 68, 69, 78

HV-SCRC High-Voltage Switched-Capacitor Regulated DC-DC Converter. ii, xii, xv, 35, 36, 43, 44, 45, 46, 47, 51, 52, 53, 54, 58, 64, 68, 69, 72, 73, 78, 79

HV-FLS High-Voltage Floating Level Shifter. ii, 38, 39, 40, 41, 42, 53, 54, 55, 68

INL Integral Non-Linearity. 69, 70

LED Light-Emitting Diode. 12

LSB Least-Significant Bit. 70

LSK Load-Shift Keying. i, 27, 28, 29, 31, 33

LUT Look-Up Table. 51, 52

LV Low-Voltage. xii, 59, 74

MIM Metal-Insulator-Metal. 24, 41, 48

MOM Metal-Oxide-Metal. 37

ND N-type Diffusion. 21, 24

ONS Optical Neural Stimulator. 13

OTA Operational Transconductance Amplifier. 49

PBS Phosphate-Buffered Saline. , iii, 69, 74

PS P-type Substrate. 21

PTAT Proportional To Absolute Temperature. 49

PW P-type Well. 21, 24

SCS Switched-Capacitor Stimulator. 9, 10, 11, 12, 16

SPI Serial-Peripheral Interface. 51

TC Temperature Coefficient. 49, 50

UDT Uplink Data Transmission. i, 26, 27, 28, 31, 33

VCO Voltage-Controlled Oscillator. 37, 48, 49

VCR Voltage Conversion Ratio. 35, 36

VCS Voltage-Controlled Stimulator. 9, 10, 11, 12, 16, 17

WE Working Electrode. 1, 5

WPDT Wireless Power and Data Transfer. , i, 14, 19, 25, 26, 27, 28, 30

Objectives, contributions, and thesis structure

This chapter outlines the objectives posed at the beginning of this thesis, the contributions made to fulfill those objectives, and the thesis structure.

Objectives

Studying neuronal circuits at cellular level for the understanding of brain functions is a challenging endeavor which requires neural interfaces. These neural interfaces perform two tasks. First, they record the neural activity of the target brain area. Second, they stimulate that brain area in order to modulate neural activity.

Thus, the efficacy of neural interfaces ultimately depends on their ability to trigger a functional response in the target tissue by inducing a flow of current between two or more electrodes. This is typically done by applying a series of biphasic current pulses with cathodic and anodic phases whose amplitudes and durations are adjusted to result in an overall zero net charge in the tissue. A major concern in the implementation of stimulators is the impedance at the Electrode-Tissue Interface (ETI). Such impedance depends on the geometry and materials of the electrodes; the physiological parameters of the tissue; and the degree of electrical contact at the stimulation zone. Further, the interface is not stationary in nature and the impedance changes throughout the life cycle of the implant. These factors make that the stimulation currents practically range from some tens of µA up to some mA and that the voltage compliance of the current drivers vary from a few volts up to over 10 V. The main objective of this thesis was thus the design and development of a neural stimulator with wide stimulation current range and high compliance voltage.

Besides, the neural interface in which the stimulator shall be included should be highly power efficient for two reasons. First, high power consumption translates to high power dissipation in the form of heat, which is undesirable in the context of implantable systems. Second, the neural interface shall be powered through an wireless power link so as to avoid wires, thus minimizing the risk of infection. The specifications of that wireless power link should be relaxed as much as possible so as to reduce its size and complexity.

Another objective of this thesis was to investigate and propose circuit solutions to implement the mentioned high compliance voltage, highly efficient, neural stimulator in a standard 1.8V/3.3V CMOS process. Implementing it in such process instead of using a High-Voltage (HV) CMOS technology was mandatory in order to avoid time-consuming migration of previously designed Low-Voltage (LV) circuitry [1], [2].

Last, this thesis was meant to preliminary explore the possibilities regarding the wireless transfer of both power and data to/from the neural implant by means of inductive links and CMOS solar cells..

Contributions

This thesis introduces several innovative solutions both at the circuit-level and block-level in the field of mixed-signal ASIC design, including:

- A high-voltage-tolerant versatile charge-pump cell has been designed and implemented. It can operate under three different modes: PUMP, PASS, and DISABLE. This enabled the design of a programmable charge-pump array, which is the core of the proposed High-Voltage Switched-Capacitor Regulated DC-DC Converter (HV-SCRC).
- A High-Voltage Neural Stimulator Front-End (HV-NSFE) with roughly 12.5 V compliance voltage has been proposed [3]. Circuit-level contributions include a High Compliance Voltage Cell (HCVC) which adapts its equivalent impedance in order to withstand large voltages or act as a closed switch, as needed.
- A high-voltage-tolerant floating level-shifter with charge refreshing has been designed [4], [5]. This cell is extensively used in the High-Voltage Neural Stimulator Front-End (HV-NSFE) and the HV-SCRC. Its fundamental features are: high-voltage tolerant operation, tracking of the low-supply rail, and handling of non-periodical input signals.

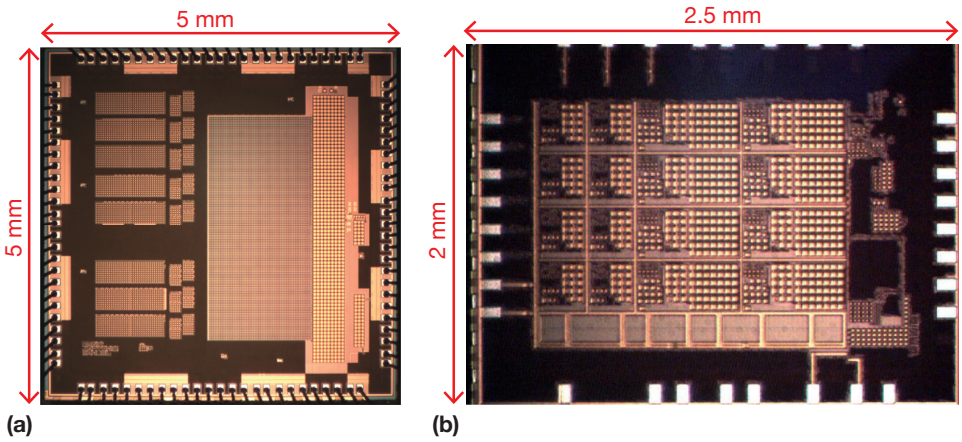


Figure 1: Microphotographs of two ASICs implemented in this thesis. (a) CMOS solar cell. (b) Neural stimulator.

- A novel stacked-photodiode configuration was implemented and characterized. Its use in CMOS solar cells and CMOS image sensors was discussed [6].
- A novel inductive-link topology for the wireless transfer of Mbps-data and mW-power over a single pair of coils has been proposed [7]. It was electrically modeled at the system level. Simulation results have been shown an discussed.

Experimental results shown in this thesis were obtained from two ASICs implemented in the TSMC 180 nm 1.8V/3.3V CMOS process. On the one hand, Fig. 1(a) shows the microphotograph of the ASIC including a CMOS photovoltaic solar cell, which was characterised to determine if it is feasible to power the neural implant with light harvesting. In Chapter 3, the design and characterization of this ASIC is discussed. Further analysis and experimental characterization were carried out to evaluate the performance of the integrated photodiodes in the context of CMOS image sensors. However, since this lies out of the scope of this thesis, the interested reader is referred to [6] for more insights. On the other hand, Fig. 1(b) depicts the proposed neural stimulator with on-chip HV generation, whose design and implementation are discussed in Chapters 4 and 5. Furthermore, for the experimental validation of the neural stimulator, a complete firmware was developed for the nRF52832 microcontroller: ADC, UART, timers, and SPI modules were used for controlling the neural stimulator and measuring its

response, sending commands from a custom MATLAB GUI.

The following publications cover most of the material presented in this thesis.

- R. Gómez-Merchán, **D. Palomeque-Mangut**, J. A. Leñero-Bardallo, M. Delgado-Restituto, and A. Rodríguez-Vázquez, «A Comparative Study of Stacked-Diode Configurations Operating in the Photovoltaic Region», IEEE Sensors Journal, vol. 20, n.º 16, pp. 9105-9113, 2020.

- **D. Palomeque-Mangut**, A. Rodriguez-Vazquez, and M. Delgado-Restituto, «A Wide-Range, High-Voltage, Floating Level Shifter with Charge Refreshing in a Standard 180 nm CMOS Process», IEEE 13th Latin America Symposium on Circuits and System (LASCAS), Puerto Varas, Chile, 2022, pp. 01-04.

- **D. Palomeque-Mangut**, A. Schmid, Á. Rodríguez-Vázquez, and M. Delgado-Restituto, «Electrical Model of a Wireless mW-Power and Mbps-Data Transfer System Over a Single Pair of Coils», International Conference on PhD Research in Microelectronics and Electronics (PRIME), Sardinia (Italy), 2022.

- **D. Palomeque-Mangut**, Á. Rodríguez-Vázquez, and M. Delgado-Restituto, «Experimental Validation of a High-Voltage Compliant Neural Stimulator Implemented in a Standard 1.8V/3.3V CMOS Process», accepted at the IEEE Biomedical Circuits and Systems Conference (BioCAS), Taipei (Taiwan), 2022.

- **D. Palomeque-Mangut**, Á. Rodríguez-Vázquez, and M. Delgado-Restituto, «A High-Voltage Floating Level Shifter for a Multi-stage Charge-Pump in a Standard 1.8V/3.3V CMOS Process», accepted for publication at AEU - International Journal of Electronics and Communications, 2022.

- **D. Palomeque-Mangut**, Á. Rodríguez-Vázquez, and M. Delgado-Restituto, «A Fully Integrated, Power-Efficient, 0.07-2.08 mA, High-Voltage Neural Stimulator in a Standard CMOS Process», accepted for publication at Sensors, 2022.

- **D. Palomeque-Mangut**, Á. Rodríguez-Vázquez, and M. Delgado-Restituto, «A 4.2-13.2 V, On-Chip, Regulated, DC-DC Converter in a Standard 1.8V/3.3V CMOS Process», sent to AEU - International Journal of Electronics and Communications, 2022.

Thesis structure

This thesis work is structured as follows:

- An introduction to fundamental concepts of neural stimulation is given in Chapter 1.
- Chapter 2 discusses the fundamental electrical specifications of neural stimulators and presents a literature review of neural stimulators.
- Chapter 3 presents the preliminary work carried out regarding the wireless transfer of power and data to/from the neural implant. First, the designed and implemented CMOS solar cell shown in Fig. 1(a) is discussed, including experimental results. Second, an inductive-link topology over a single pair of coils is proposed. In this case, simulation results are discussed.
- In Chapter 4, the proposed HV-SCRC –included in the ASIC presented in Fig. 1(b)– is discussed. Experimental results are also given.
- The proposed neural stimulator –i.e. the whole ASIC shown in Fig. 1(b)– is presented in Chapter 5, where experimental results are also shown and discussed.
- Finally, Chapter 6 presents the conclusions of the thesis as well as an overview of the possible future works.

Chapter 1

Fundamentals of Neural Stimulation

In this chapter, fundamental neural stimulation concepts are discussed. First, Section 1.1 introduces the topic. Then, Section 1.2 describes the Electrode-Tissue Interface (ETI). Methods for assuring efficacy and safety of electrical stimulation are shown in Section 1.3. Finally, optogenetic stimulation is introduced in Section 1.4.

1.1 Introduction

Electrical neurostimulation techniques consist on forcing an electrical current to flow from an electrode –the Working Electrode (WE)– through extracellular fluid of some excitable tissue of the nervous system. This current is finally sought by a distant Counter Electrode (CE). The final purpose of such technique is the alteration of neural activity. This is also called *neuromodulation*. In this work, we are interested in two neuromodulation techniques: Deep-Brain Stimulation (DBS) and Electrical-Cortical Stimulation (ECS).

DBS is a neuromodulation technique in which precise amounts of electrical charge are delivered to specific deep anatomical structures of the central nervous system [8]. Clinical applications of DBS include Parkinson's disease, essential tremor, dystonia, neuro-behavioral disorders, epilepsy, pain, and others [8]–[10].

ECS is also a neuromodulation technique in which electrical charge is delivered thorugh electrodes placed on the cerebral cortex. The main clinical application of ECS is the identification of functional brain regions [11]. Besides, it has been used for inducing vestibular responses [12], treating epilepsy [13], and others [14].

1.2 The Electrode-Tissue Interface (ETI)

The ETI is formed when the metal electrode is placed inside extracellular fluid of the neural tissue [15], [16]. In this interface, electrode's electronic charge is transduced into ionic charge. Even though the ETI has non-linear impedance, it can be electrically modeled as a parallel resistor-capacitor. On the one hand, the resistive element R_f models the faradaic current generated by the chemical reactions taking part in the interface. On the other hand, the capacitive element C_{dl} models the electrical double layer that is formed. Besides, Φ_E stands for the potential that exists across the interface at equilibrium. Finally, the electrolyte (extracellular fluid) can be electrically modeled as a linear resistor R_s. This electrical model is depicted in Fig. 1.1.

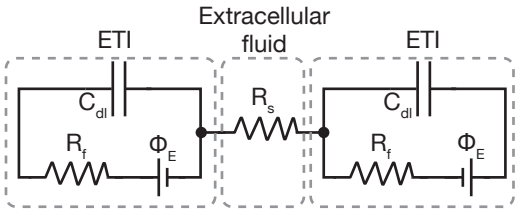


Figure 1.1: Electrical model of the ETI and the extracellular fluid [15], [16].

1.2.1 Faradaic and non-faradaic charge transfer

As previously said, both faradaic and non-faradaic reactions occur in the ETI. On the one hand, faradaic currents result from the direct transfer of electronics via reduction or oxidation reactions at the ETI. On the other hand, non-faradaic currents include currents that result from other processes where direct transfer of electrodes does not occur in the ETI [17].

During stimulation, non-faradaic charge transfer takes place when the net charge of the electrode varies and, accordingly, the charge in the solution is redistributed. If the polarity of stimulation is reversed, so it is the charge

distribution. Thus, the charge injected from the electrode into the electrolyte may be recovered [15]. This behavior is modeled by the double layer capacitance C_{dl}.

Besides, charge may also be injected from the electrode to the electrolyte (extracellular fluid) by faradaic processes such as reduction or oxidation. Contrary to the aforementioned capacitive behavior, faradaic charge injection is characterised by the formation of products in the solution that might not be recovered by reversing the polarity during stimulation. This behavior is electrically modeled by the resistor R_f. These irreversible faradaic reactions lead to changes in the chemical environment that can damage the tissue or the electrode. Thus, when designing an electrical neurostimulator it is mandatory to establish mechanisms for reducing irreversible faradaic reactions.

1.2.2 Electrochemical reversal

If irreversible Faradaic reactions wants to be avoided, biphasic stimulation schemes must be used. Biphasic stimulation is at least formed by two phases: anodic phase and cathodic phase. During anodic phase, electrons are transferred to the electrode –the electrode is a *current source*– whereas in cathodic phase, electrons are transferred from the electrode to the electrolyte –the electrode is a *current sink*–. With a two-electrodes scheme, there is always one electrode sinking current and one electrode sourcing current. Thus, the anodic and cathodic phases are defined by looking at what happens in the vicinity of one electrode of interest –the working electrode (WE)–.

During the *active* phase of biphasic stimulation, electrochemical processes occur. The *reversal* phase is applied in order to invert the direction of those processes, minimizing unrecoverable charge. The final goal is to perform charge transfer through non-faradaic or reversible-faradaic processes, avoiding the injection of toxic materials into the tissue [18].

1.3 Efficacious and safety of electrical neural stimulation

Stimulation charge per phase and pulse-width thresholds vary according to the application and the species in which stimulation is delivered. In this regard, Table 1.1 summarizes charge/phase and pulse-width requirements for different neural prosthesis, depending on the application and species

[19].

Reference	Application	Species	Placement	Charge/phase (nC)	Pulse width (µs)
[20]	Vision	Human	Epi-retinal	6-1120	1000
[21]	Vision	Human	Epi-retinal	24-100	2000
[22]	Vision	Human	Optic nerve	7-124	25-400
[23]	Vision	Human	Introacortical	0.4-4.6	200
[23]	Vision	Human	Cortical	200000	200
[24], [25]	Hearing	Cat	VCN	0.75-1.5	40-150
[26], [27]	Hearing	Human	AB	10-200	300
[28]	Micturition	Cat	Intraspinal	9	100
[29]	DBS	Human	STN	135-400	60-200
[30]	Motor	Cat	Intrafascicular	4	50
[31]	Motor	Cat	Sciatic nerve	5	200
[31]	Motor	Cat	Sciatic nerve	46	200

Table 1.1: Charge/phase threshold and pulse width required for different neural prostheses. Reproduced from [19].

If electrode corrosion or tissue damage wants to be avoided, perfectly charge-balanced biphasic stimulation should be applied [18]. However, one concern is that the *reversal* phase do not only reverses electrochemical reactions induced during the *active* phase, but also suppresses AP that were trying to be evoked. In this regard, an interphase delay can be introduced [32]. However, during the interphase delay, the electrode potential remains relatively negative and non-desirable faradaic reactions can occur. A delay of 100 µs has proven to be enough for overcome the suppressing effect of the reversal phase without causing potential damage to the electrode or the tissue.

In order to assure safety stimulation, active and/or passive methods for charge balancing must be added to the neurostimulator. Two scenarios could lead to a drift in electrode potential after biphasic stimulation: (1) biphasic stimulation could be slightly charge-unbalanced *i.e.* there might a mismatch between anodic/cathodic stimulation current or pulse-width and (2) different amounts of charge could be lost in irreversible faradaic reactions during each stimulation phase. Both factors are related: a slightly charge-imbalanced biphasic stimulation could lead to an accumulation of charge in the ETI thus causing an unsafe increase in the electrode potential that can trigger irreversible faradaic reactions.

There are two main approaches to improve charge balancing in biphasic stimulation: passive charge balancing and active charge balancing [33]. The most common charge-balancing method is electrode shorting, in which the WE to the CE are shorted during a discharge period T_{dis}. In order to successfully discharge the WE, T_{dis} must be larger than the time constant of the ETI impedance and the discharge impedance. Designers usually establish a worst-case scenario with the largest expected ETI impedance and set a discharge period long enough. This technique might not be feasible for compensating highly charge-imbalanced neurostimulators, so it is commonly used to discharge any residual charge generated by precise biphasic current stimulators.

1.4 Optogenetic stimulation

Stimulation of excitable tissue with light is possible thanks to the photosensitization of neuron cells with optogenetic tools. Optogenetic tools comprises the combination of genetic and optical methods that allow to control a number of cellular functions, including: stimulation/inhibition of cells, gene activation, intracellular signaling, and migration [34]–[36]. Specifically, optical stimulation of neural tissue allows to activate or inhibit neural cells with high temporal and spatial resolution. Photosensitization of neurons is achieved by means of *opsins*. *Opsins* are membrane-bound proteins that are activated with light which can be genetically targeted to specific cells [36]. The catalog of opsins have increasing during the last decade [37] but the most widely used in state-of-the-art optical neurostimulators is *Channelrhodopsin-2* (ChR2) [38]. Both DBS and ECS can be performed by means of optogenetic tools [39], [40].

1.4.1 Opsins used in optogenetic neural stimulation

Opsins are light-activated proteins which are found in organisms such as microbes or primates [36]. They can be used for cell activation (depolarization of the neuronal membrane) or inhibition (hyperpolarization of the neuronal membrane). Activation (inhibition) is achieved by the creation of cation (anion) channels in the membrane of opsin-expressing neurons.

Channelrhodopsins

As it was aforementioned, ChR2 is a blue-light gated cation channel that, when activated, depolarizes the neuronal membrane. Millisecond-width

pulses of blue light can induce single Action Potential (AP) in neurons expressing ChR2. Besides, neural spiking activity can be light-driven with high precision at frequencies up to 30 spikes per second.

Opsins with faster temporal kinetics have been developed for applications in which the goal is the extremely fast control of neural activity at high firing rates. Examples of these opsins are ChETA and ChEF/ChIEF [41], [42].

Spectrally shifted opsins

Great effort has been put into the development of opsins with an excitation spectra different from blue. With such opsins, independent optical control of different populations of neurons can be achieved. Red-light activated opsins are particularly interesting because 1) the red wavelength interval (635 nm-700 nm) does not overlap with the blue wavelength interval (450 nm-490 nm) and 2) red electromagnetic radiation enables deeper penetration into the tissue with reduced scattering than blue electromagnetic radiation. Thus, different opsins with red-shifted activation wavelength have been proposed [43], [44].

Opsins for inhibition of neural activity

Inhibition of neural activity comprises the hyperpolarization of neuronal membrane in order to suppress AP. *NpHR* is a widely used halorhodopsin – light-gated ion pump– that hyperpolarize the neuronal membrane by pumping ions into the cell [45]. A series of revision were made in order to improve the performance of this opsin, leading to the development of eNpHR3.0 [46]. eNpHR3.0 has its maximum excitation at 590 nm and it thus can be driven by green, yellow or red light sources.

However, there are two limitations when using light-gated pumps for inhibiting neural activity. First, these pumps are less efficient than excitatory channel opsins. In other words, the rate of ions per absorbed photon flowing through the channel is much higher in excitatory opsins than in the inhibitory ones [36]. Second, techniques used to increase the light sensitivity cannot be used in pumps in an efficient manner.

1.4.2 Light interaction in cerebral cortex

There is another concern to think about when delivering light to the tissue: *irradiance*. Light *irradiance* is defined as the optical power or flux per unit area striking a surface. In this regard, there is a threshold that have to

be overcome in order to successfully evoke AP. In the case of ChR2, the irradiance threshold is $\approx 1\,\mathrm{mW\,mm^{-2}}$ [47].

When the light radiation strikes the neural tissue, a number of light-medium interactions occur. Thus, light intensity and propagation direction might change [48]. Among these interactions one can find reflection, refraction, absorption, and scattering. Even though the analysis of such interactions is outside the scope of this thesis, it is worth noting that absorption –the conversion of light into heat in the tissue– can lead to an increase in the neural tissue temperature. Since many physiological processes are sensitive to temperature, the amount of irradiance delivered has to be carefully set in order not to unwillingly alter brain function [49].

Chapter 2

Literature Review of Neural Stimulators

This chapter introduces some fundamental concepts of neural stimulator from an electrical perspective and presents an analysis of state-of-the-art neural stimulators.

2.1 An introduction to neural stimulators from an electrical perspective

In this section, neural stimulators are analysed from an electrical point of view. First, the major approaches for implementing neurostimulators are compared. Second, the importance of compliance voltage is highlighted. Third, particularities of optical neurostimulators are remarked.

2.1.1 Types of neural stimulators

Fig. 2.1(a-c) show the three major approaches used for implementing neural stimulators: Voltage-Controlled Stimulator (VCS), Switched-Capacitor Stimulator (SCS), and Current-Controlled Stimulator (CCS). It also shows the load current, I_{load}, and load voltage, V_{load}, waveforms obtained during stimulation.

In VCS, a stimulation voltage is directly applied to the neural tissue during a certain period of time. Alternatively, in SCS a previously charged capacitor

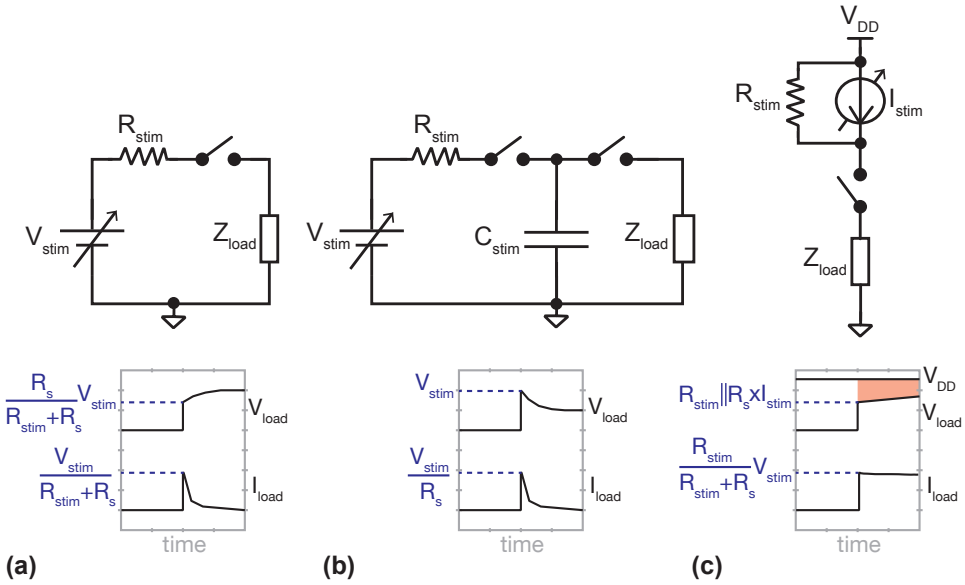


Figure 2.1: Conceptual electrical schemes for the major approaches for neural stimulators. (a) Voltage-Controlled Stimulator (VCS), (b) Switched-Capacitor Stimulator (SCS), and (c) Current-Controlled Stimulator (CCS).

is discharged through the neural tissue. Last, in CCS the current source draws a certain level of current from the supply voltage to the neural tissue.

These approaches can be compared in terms of energy efficiency and precision at charge delivering. For that purpose, efficiency is defined as defined as the power delivered to the load, P_{load}, divided by the power drawn from the stimulator's power source, P_{stim}

$$\eta = \frac{P_{load}}{P_{stim}}. \tag{2.1}$$

Besides, precision at charge delivering can be obtained from the definition of charge

$$Q_{load} = \int_0^{T_{stim}} I_{load}(t)dt, \tag{2.2}$$

where T_{stim} corresponds to the stimulation time and $I_{load}(t)$ is the instantaneous current delivered to the neural tissue. Next, (2.1) and (2.2) are particularized for the three types of electrical stimulators by modelling both the neural tissue and ETI with its electrical equivalent –shown in Fig. 1.1–,

but considering that $R_f \to \infty$ for simplicity.

The expression of efficiency of VCS is

$$\eta_{VCS} = 1 - \frac{1}{2}\frac{R_{stim}}{R_{stim}+R_s}\frac{1 - exp\left(-2\frac{T_{stim}}{(R_{stim}+R_s)C_{dl}}\right)}{1 - exp\left(-\frac{T_{stim}}{(R_{stim}+R_s)C_{dl}}\right)} \approx \frac{R_s}{R_s+R_{stim}}, \quad (2.3)$$

where R_s and C_{dl} are the extracellular fluid resistance and the double-layer capacitance, as shown in Fig. 1.1. The approximation is valid for $T_{stim} << (R_{stim} + R_s)C_{dl}$. Since R_s is usually in the range of some kilo-ohms, efficiencies above 90% can be obtained for moderate values of R_{stim}.

In the case of SCS, power efficiency is maximum when C_{stim} is discharged to the load. However, the efficiency when charging C_{stim} to V_{stim} is

$$\eta_{SCS} = 1 - \frac{1}{2}\frac{1 - exp\left(-2\frac{T_c}{R_{stim}C_{stim}}\right)}{1 - exp\left(-\frac{T_c}{R_{stim}C_{stim}}\right)} \approx 0.5, \quad (2.4)$$

where T_c is the charging time and the approximation holds for $T_c >> R_{stim}C_{stim}$.

Regarding CCS, power efficiency was calculated assuming $R_{stim} \to \infty$ for simplicity

$$\eta_{CCS} = \frac{I_{stim}T_{stim}}{V_{DD}}\left(R_s + \frac{T_{stim}}{2C_{dl}}\right). \quad (2.5)$$

Power efficiency in CCS depends on how close V_{DD} is to V_{load} because the larger that voltage difference the larger the power losses at I_{stim} –as depicted by the shaded region in Fig. 2.1(c)–. It is thus desirable to have a programmable voltage supply, V_{DD}, in order to maximize power efficiency.

The charge delivered by a VCS is

$$Q_{stim,VCS} = V_{stim}C_{dl}\left[1 - \exp\left(-\frac{T_{stim}}{(R_{stim}+R_s)C_{dl}}\right)\right] \approx \frac{V_{stim}T_{stim}}{R_{stim}+R_s}, \quad (2.6)$$

where the approximation holds if $T_{stim} << (R_{stim} + R_s)C_{dl}$. Charge delivered is strongly dependent on R_s.

The charge delivered by an SCS is

$$Q_{stim,SCS} = V_{stim}\frac{\tau_{SCS}}{R_s}\left[1 - \exp\left(-\frac{T_{stim}}{\tau_{SCS}}\right)\right], \quad (2.7)$$

where $\tau_{SCS} = R_s{\cdot}C_{stim}{\cdot}C_{dl}/(C_{stim} + C_{dl})$. The expression can be further simplified by assuming that $T_{stim} << \tau_{SCS}$

$$Q_{stim,SCS} \approx \frac{V_{stim}T_{stim}}{R_s}, \tag{2.8}$$

which shows that stimulation charge is also highly dependent on R_s. Finally, the stimulation charge in CCS is

$$Q_{stim,CCS} = R_{stim}C_{dl}\left[1 - \exp\left(-\frac{T_{stim}}{\tau_{CCS}}\right)\right], \tag{2.9}$$

where $\tau_{CCS} = (R_s + R_{stim}){\cdot}C_{dl}$. Assuming that $T_{stim} << \tau_{CCS}$

$$Q_{stim,CCS} = \frac{R_{stim}}{R_{stim} + R_s}I_{stim}T_{stim}, \tag{2.10}$$

which shows that, even with moderate values of R_{stim}, stimulation charge is highly controlled in CCS.

The analysis of these three approaches for electrical stimulation is summarized in Table 2.1. VCS achieves the best power efficiency but charge delivered is load-dependent. SCS has a 50% efficiency but the charge delivered is also load-dependent. Finally, CCS achieves load-independent charge delivery at the cost of a power efficiency which depends on the load, the stimulation current, and the supply voltage. Given these characteristics, most of the neural stimulators found in the literature implement CCS topologies in which most design effort is put into maximizing power efficiency. This thesis intends to make a contribution in this endeavour.

2.1.2 Optical Neural Stimulators

Optical neurostimulation is carried out by driving a Light-Emitting Diode (LED) or a laser diode in order to deliver light to neural tissue. In either way, the neurostimulator must deliver a precise and constant light irradiance to

Type	Efficiency	Precision at charge delivering	Fully integrable
VCS	>90%	Load-dependent	Yes
SCS	50%	Load-dependent	No
CCS	Load-dependent	Load-independent	Yes

Table 2.1: Qualitative comparison of different electrical neurostimulation approaches.

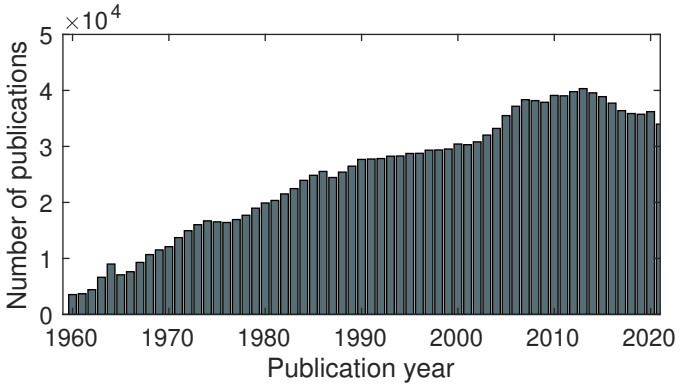


Figure 2.2: Evolution of results appearing in PubMed's search engine when aggregating results for "neural stimulation" and "neuromodulation".

neural tissue. Thus, they are usually implemented with the CCS approach, as shown in Fig. 2.1(c).

Optical stimulation pulses are also delivered at frequencies below 1 kHz, and pulse widths can be well below 100 µs. However, in Optical Neural Stimulators (ONSs) charge balancing is not an issue anymore. Thus, the setting time constraints are less restrictive than in Electrical Neural Stimulators (ENSs).

The neural stimulator here presented was designed to comply with electrical stimulation specifications, but it can also be used as an optical neural stimulator.

2.2 Literature review

In the last decades, a vast amount of scientific literature related to neuromodulation has been published –see Fig. 2.2–. There is thus a need of implantable devices that health researchers can use for exploring and modulating the brain activity. Mixed-signal ASIC designers have been working on offering solutions for the design and development of integrated circuits that meet this need. In this regard, challenges in the design of cutting edge neural stimulators are:

- Charge balance. Biphasic stimulation demands that the charge delivered during both stimulation phases is the same so as to have zero net charge stored at the ETI after a stimulation round [15].

- Compliance voltage. The ETI depends on the geometry and materials of the electrodes; the physiological parameters of the tissue; and the degree of electrical contact at the stimulation zone [15]. Further, the interface is not stationary in nature and the impedance changes throughout the life cycle of the implant. These factors make that the voltage compliance of the neural stimulator front-end varies from a few volts up to over 10 V.

- WPDT. Wired transmission of power and data should be avoided in order to maximize the safety of the implant. The design of highly-efficient fully-implantable WPDT systems is a challenging topic which is experiencing a great development in the last decade [7], [50]–[57].

- Power efficiency. Power dissipation in the form of heat should be minimized for long-term safety of the implant. Besides, a wirelessly-powered implant should demand as little power as possible in order to relax the specifications of the wireless power supply and expand the autonomy of the implant. Both things depend on increasing neural stimulator's power efficiency as much as possible.

Neural stimulators with programmable power supply have been widely studied in the literature. In the case of CCS, they are usually implemented either with single or dual current sources, as shown in Fig. 2.3. Fundamental parts of these stimulator topology are: the current-steering Digital-to-Analog Converter (DAC), current mirror, switches, and DC-DC converter for generating V_{DDH}.

In [58], a CCS with on-chip voltage generator was proposed. It uses a single current source for delivering asymmetrical biphasic pulses. The circuit achieves a 11.5 V compliance voltage, but it was implemented in a 180 nm HV CMOS process. Besides, the DC-DC converter has limited programmability and lacks a regulation loop. A high-voltage-tolerant neurostimulator with an on-chip regulated 5-stages charge pump was proposed in [59]. Implemented in a 180 nm 1.8V/3.3V CMOS process, the compliance voltage reaches 10 V. Nonetheless, power efficiency of the solution was not discussed. Besides, the stimulation current is fixed at 30 µA and charge balancing was not tackled.

Another CCS with programmable power supply was presented in [60]. Implemented in a standard CMOS process, an on-chip voltage generator provides an adjustable voltage supply from 6.7 V up to 12.3 V. A dynamic gate biasing circuit that controls the state of some stacked transistors is proposed for having a compliance voltage up to $3 \times V_{DD}$. Nonetheless, the different

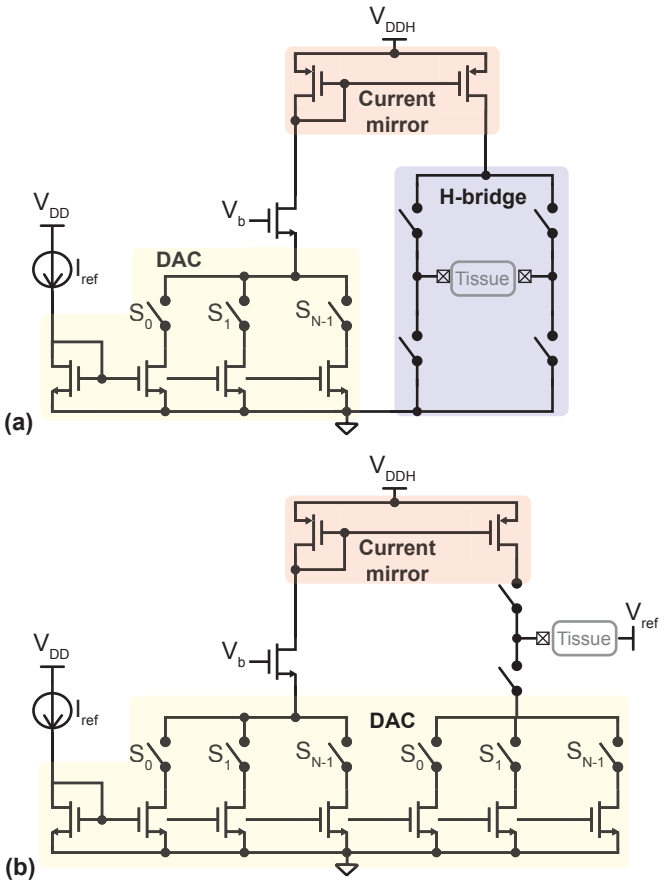


Figure 2.3: Current-Controlled Stimulator (CCS). (a) Single current source. (b) Dual current sources.

power supplies needed for biasing the H-bridge do not adapt to V_{DDH}. Thus, it is expected that the H-bridge shows a non-negligible on-resistance in situations with small V_{DDH}, leading to lower power efficiency.

A slightly different approach was followed in [61], where a Dickson ladder DC-DC converter was implemented to dynamically supply the neural stimulator front-end. The adiabatic solution permits charge recycling but no programmability for disabling unused stages of the Dickson ladder were devised. Besides, there is no regulation loop for locking the output voltage of the DC-DC converter to some reference value. It implements a single current source topology in which a discharging phase can be triggered to

remove any residual charge. However, no experimental results on this were reported.

A CCS implementing the topology shown in Fig. 2.3(b) is discussed in [62]. It was implemented in a standard CMOS process and it delivers up to 3 mA of current and uses an on-chip ±6 V voltage generator. A maximum current mismatch between anodic and cathodic phases of 1.94% is reported. Thus, a discharging phase lasting 2 ms has to be applied after some stimulation rounds in order to limit the charge stored at the ETI.

SCSs have also been addressed in the literature [63], [64]. Even though good efficiencies are generally reported, they all rely on off-chip capacitors. Besides, load-dependent charge delivery and charge mismatch are intrinsic disadvantages of this topology.

VCSs have received less attention because charge delivery is highly load-dependent. In [65], a $3 \times V_{DD}$ compliant neural stimulator is shown. However, no on-chip voltage generator was reported. In [66], a stimulator delivering 1.5-4.5 V pulses with on-chip voltage generator is presented. Nonetheless, power efficiency is low and residual charge is not discussed.

A VCS based on a buck-boost converter is presented in [67]. The system was implemented in a 180 nm HV CMOS process and uses a 22 µH inductor as the only off-chip component. It shows efficiencies around 40% for average output powers above 5 mW. Though, power efficiency rapidly drops at lower output power values. Besides, an external 20 V supply is needed and residual charges left at the ETI after biphasic stimulation rounds were not discussed.

As it was pointed out, most of this thesis is devoted to the design of a fully integrated CCS with high compliance voltage in a standard CMOS process. Thus, it builds on the knowledge reported in previous works such as [59]–[62]. Both discussed and additional references are listed in Table 2.2 and Table 2.3.

Ref.	Year	Process	Type	Ranges	Supply	Charge balancing	Area/ch (mm^2)
[58]	2013	0.18 µm (HV)	Biphasic CCS	0.5 mA (6 bits)	3,6,9,12 V (unregulated)	No	0.35
[59]	2014	0.18 nm (LV)	Biphasic CCS	30 µA	4.5-10 V	No	-
[61]	2015	65 nm (LV)	Biphasic CCS	0.9 mA (6 bits)	1.3-9.1 V	Electrode shorting	0.068
[63]	2015	0.35 µm (LV)	Biphasic SCS	5 bits	2 V	Charge calculation	-
[65]	2015	0.18 µm (LV)	VCS	Up to 9.9 V	9.9 V	No	0.10
[66]	2016	0.18 µm (LV)	Biphasic VCS	1.5-4.5 V (5 bits)	1 V	No	-
[67]	2016	0.18 µm (HV)	Biphasic VCS	<20 mA	20 V	Pulse insertion	-
[68]	2017	0.18 µm (LV)	Biphasic CCS	0.25 mA (8 bits)	3.3 V	Charge calculation	0.078
[64]	2017	0.18 µm (HV)	Biphasic SCS	190 nC	5 V	Pulse insertion	0.035
[69]	2017	0.13 µm (LV)	Arbitrary CCS	1.35 mA (8 bits)	3.3 V	Electrode shorting	0.130
[70]	2018	0.18 µm (HV)	Biphasic CCS	5 mA (8 bits)	15 V	Electrode shorting	-
[71]	2018	0.6 µm (HV)	Chopped CCS	1 mA (8 bits)	12 V	Charge calculation	-
[60]	2018	0.18 µm (LV)	Biphasic CCS	3 mA (4 bits)	6.7-12.3 V	Electrode shorting	-
[72]	2018	0.18 µm (HV)	Biphasic CCS	5.1 mA (7 bits)	5 V (prog)	Electrode shorting	-
[73]	2018	0.18 µm (HV)	Biphasic CCS	3.15 mA (6 bits)	30 V	Charge calculation	0.260
[74]	2019	0.18 µm (SOI)	Biphasic CCS	145 µA (5 bits)	1-3.9 V	Electrode shorting	0.220

Table 2.2: Performance comparison of neural stimulators reported in the literature.

Ref.	Year	Process	Type	Ranges	Supply	Charge balancing	Area/ch (mm^2)
[75]	2019	0.18 µm (HV)	Biphasic CCS	21.7 mA (10 bits)	5-24 V	No	-
[76]	2019	0.13 µm (LV)	Biphasic CCS	1.86 mA (5 bits)	2 V	Electrode shorting	-
[77]	2019	0.18 µm (LV)	Biphasic CCS	0.3 mA (4 bits)	3.3 V	Electrode shorting	-
[78]	2020	65 nm (LV)	Biphasic CCS	2 mA (8 bits)	X-11 V	Electrode shorting	0.360
[79]	2020	0.25 µm (HV)	Biphasic CCS/VCS	5 mA/10 V (6 bits)	20 V	Electrode shorting	0.220
[62]	2021	0.18 µm (LV)	Biphasic CCS	3.2 mA (7 bits)	6 V	Electrode shorting	0.080

Table 2.3: Performance comparison of neural stimulators reported in the literature (cont).

Chapter 3

Wireless Power and Data Transfer

In this chapter, the wireless transfer of power and data from an external unit to/from the neural implant is tackled. On the one hand, a CMOS photovoltaic cell was designed and fabricated in a standard 180 nm CMOS process –see shown in Fig. 1(a)– to experimentally check the feasibility of performing light harvesting for powering the implant [6]. This work was done with the supervision of Prof. Juan Antonio Leñero Bardallo –whose research focuses on the design of CMOS image sensors– and the help of Ph.D. candidate Rubén Gómez Merchán. On the other hand, a topology of inductive WPDT system over a single pair of coils was studied and proposed as the main power source of the implant [7]. This work was carried out at the Swiss Federal Institute of Technology Lausanne (EPFL) with the supervision of Prof. Alexandre Schmid.

3.1 CMOS photovoltaic cell

This section is organised as follows. First, an introduction to CMOS photovoltaic cells is given. Second, the operation of the photodiodes used in the CMOS cell is devised. Third, experimental results are shown and discussed.

3.1.1 Introduction

Diodes implemented in standard CMOS processes can be used as photodiodes if they are biased in the photovoltaic region. This can lead to self-

powered image sensors or to implantable systems that can eventually use solar energy to reduce power drawn from batteries. Different stacked diodes can be implemented using Deep N-type Well (DNW) in standard CMOS processes [80], [81]. Hence, there are many combinations possible which should be investigated for improving the performance of classic light detectors based on single isolated diodes. For instance, several authors have already implemented sensors that can concurrently sense light and harvest energy simultaneously [82]–[84]. Moreover, different diode configurations to harvest energy more efficiently have been proposed [85], [86].

3.1.2 Photodiode operation

Figs. 3.1(a-c) show (a) a single diode's voltage-current curve, (b) the photovoltaic region, and (c) its electrical model, where I_{ph} is the photocurrent generated by the electron-hole pairs captured near the diode depletion region and C_{pd} models the diffusion and junction capacitances. According to this model, the DC current flowing through a single-photodiode configuration, I_{pd}, is given by

$$I_{pd} = I_{ph} - I_D = I_{ph} - I_s \left(e^{\frac{V_{pd}}{n_D U_T}} - 1 \right), \tag{3.1}$$

where I_s is the specific current, n_D is the emission coefficient, $V_{pd} = V_D$ is the forward voltage of the diode, and I_D is the current flowing through the diode with no illumination.

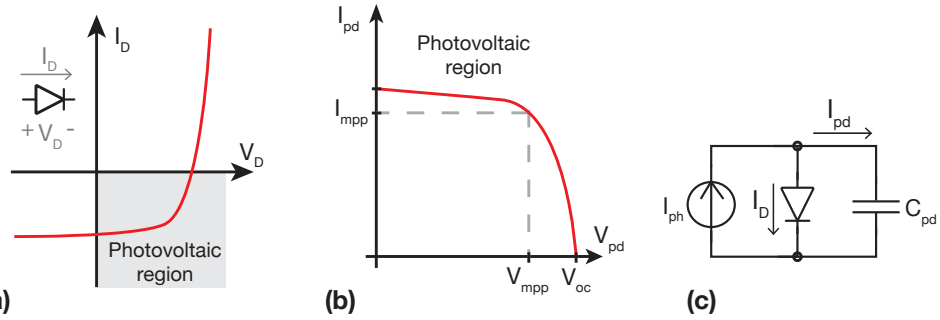


Figure 3.1: (a) Diode I-V curve, (b) photovoltaic region, and (c) circuit model for the diode in the photovoltaic region. The optimum operating point, (I_{mpp}, V_{mpp}), provides the highest power than can be harvested. [6]

The open-circuit voltage, V_{oc}, is defined as the voltage at which no current

flows through the photodiode

$$V_{oc} = V_{pd}(I_{pd} = 0) = nU_T \ln\left(\frac{I_{ph}}{I_s} + 1\right). \tag{3.2}$$

To increase photodiodes' performance, two parameters have to be maximized: the current generated, I_{pd}, and the open circuit voltage, V_{oc}. The last amounts typically between 100 mV and 450 mV under usual illumination conditions in standard CMOS technologies. It is thus important to choose diode configurations that can provide the highest open-circuit voltage to maximize the operation range at which the harvested energy can be directly used to power circuits with minimum previous DC-DC conversion.

Fig. 3.2(a-b) show the two diode configurations under study. The first configuration, shown in Fig. 3.2(a), is a diode based on the P-type Well (PW)-DNW junction. The second configuration, shown in Fig. 3.2(b), adds another diode, implemented with the N-type Diffusion (ND)-PW junction, in parallel to the previous one. Another possibility based on the isolated P-type Substrate (PS)-ND junction photodiode has been discarded because its quantum efficiency is much lower than in the other cases [80].

For the double diode configuration, the contribution of each diode has to be taken into account in the current expression

$$\begin{aligned} I_{pd,double} &= I_{ph_1} - I_{D_1} + I_{ph_2} - I_{D_2} \\ &= I_{ph_1} - I_{s_1}\left(e^{\frac{V_{pd}}{nU_T}} - 1\right) \\ &+ I_{ph_2} - I_{s_2}\left(e^{\frac{V_{pd}}{nU_T}} - 1\right) \end{aligned} \tag{3.3}$$

where it has been assumed that $n_1 = n_2 = n$. Whenever $I_{pd,double} = 0$, the double diode configuration's open circuit voltage, $V_{oc,double}$, is reached.

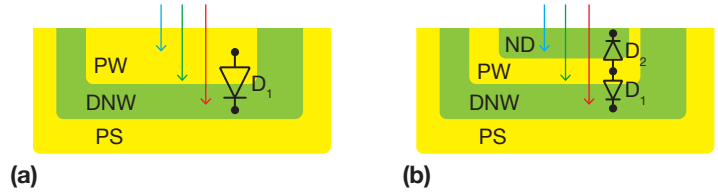


Figure 3.2: Photodiode configurations under study. (a) Isolated PW-DNW junction diode. (b) PW-DNW and ND-PW diodes connected in parallel. [6]

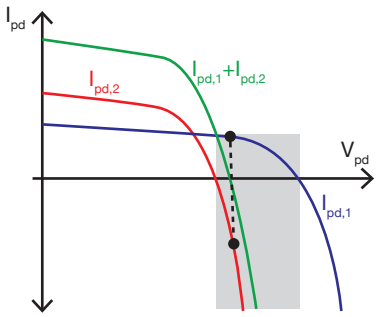


Figure 3.3: Current-voltage curves of two parallel diodes operating simultaneously. [6]

Operating with (3.3), it is easy to deduce that

$$V_{oc,double} = nU_T \ln\left(\frac{I_{ph_1}}{I_{s_1}}\frac{1+\frac{I_{ph_2}}{I_{ph_1}}}{1+\frac{I_{s_2}}{I_{s_1}}}+1\right). \tag{3.4}$$

Comparing (3.2) and (3.4), it is deduced that $V_{oc,double} > V_{oc,single}$ when the ratio between diodes' photocurrents and specific currents satisfies

$$V_{oc,double} > V_{oc,single} \iff \frac{I_{ph_1}}{I_{ph_2}} < \frac{I_{s_1}}{I_{s_2}} \tag{3.5}$$

The specific current value in an abrupt PN junction is given by this expression [87]

$$I_s = qWL\left(\frac{D_p p_n}{L_p}+\frac{D_n n_p}{L_n}\right), \tag{3.6}$$

where W and L are the diode dimensions; D_p and D_n are the holes and electrons diffusion coefficients, respectively; L_p and L_n are the holes and electrons diffusion lengths, respectively; and p_n and n_p and the minority carriers concentration in the P- and the N-regions, respectively. Doping profiles were not disclosed by the foundry.

The ratio between the specific currents can be considered constant in the photovoltaic region. Assuming similar doping profiles for the two PN-junctions, $I_{s_1} > I_{s_2}$, because D_1 is larger than D_2. Finally, it must remarked that diodes photocurrent values in (3.4) depend on the incident light wavelength: while D_2 is more sensitive to shorter wavelengths, D_1 has a sensitivity peak at higher wavelengths [81], [88], [89]. Overall, if technological

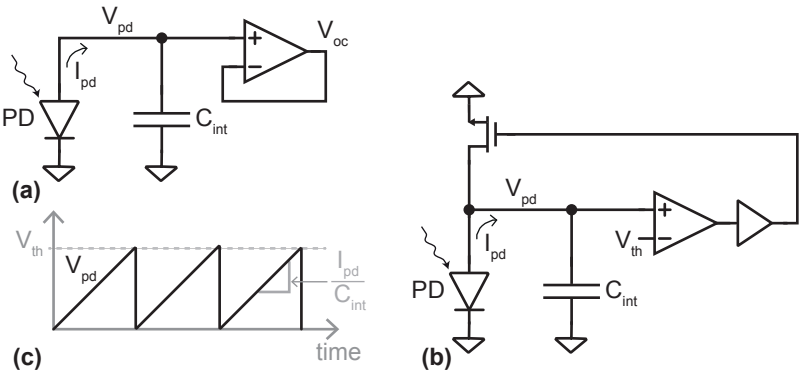


Figure 3.4: Integrated test circuits to compare the two diode configurations performance. (a) Test circuit devised to gauge open circuit voltages (V_{oc}). (b-c) Astable oscillator to compare the relative photocurrents values of each diode. [6]

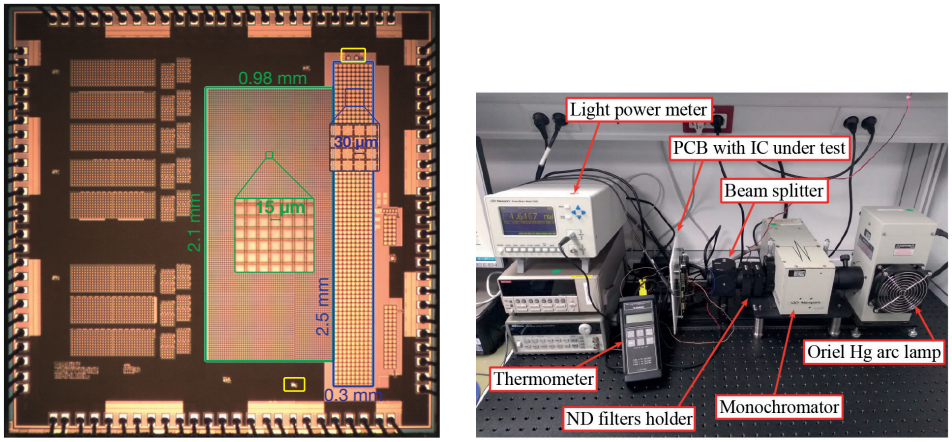
parameters are unknown, it is not direct to guess which diode configuration offers higher V_{oc} without a previous experimental characterization.

When the two diodes operate simultaneously in the photovoltaic region, the configuration shown in Fig. 3.2(b) is more efficient in terms of current generation. However, there may be situations in which one diode can be forward biased outside the photovoltaic region while the other one still operates in photovoltaic region. Fig. 3.3 shows this case, where the green line represents the total current of two parallel diodes with different I-V curves (blue and red lines). Note that, at V_{oc}, the first diode generates the forward current of the second one. Thus, they can compete between them degrading the performance. Hence, the resultant V_{oc} voltage has to be measured and analyzed to decide which diode configuration performs better.

Two circuits were implemented to characterise both photodiode configurations. Fig. 3.4(a) shows a circuit to measure V_{oc}, in which a buffer architecture with low offset, rail-to-rail operation and large current driving capability was chosen [90]. Fig. 3.4(b) shows an astable oscillator that pulses with a frequency proportional, f_{osc}, to illumination [80]

$$f_{osc} \approx \frac{I_{pd}}{C_{int} \cdot V_{th}}, \tag{3.7}$$

where $C_{int} = C_{pd} + C_{par}$ accounts for all the parasitic capacitances at the input node of the comparator. Hence, if the two diode configurations gener-



(a) (b)

Figure 3.5: (a) Chip microphotograph. The array of 7800 photodiodes with dimension of 15 µmx15 µm is highlighted in green. The array of 684 Metal-Insulator-Metal (MIM) capacitors with dimension of 30 µmx30 µm is highlighted in blue color. Test circuits depicted in Fig. 3.4 are surrounded by yellow lines. (b) Experimental setup devised to characterize both diode configurations. [6]

ate pulses with the same frequency, the double diode is generating a higher current.

3.1.3 Experimental results

Fig. 3.5(a) shows a micro-photograph of the test chip implemented in a standard 180 nm 1.8V/3.3V CMOS process. It contains (1) an array of 7800 photodiodes –with the configuration shown in Fig. 3.2– with dimensions of 15 µmx15 µm and connected to an array of 684 MIM capacitors with dimensions of 30 µmx30 µm; and (2) test circuits shown in Fig. 3.4(a-b) for characterizing both diode configurations. Fig. 3.5(b) depicts the experimental setup used for the extensive characterization of both photodiode configurations.

Fig. 3.6 shows both photodiode configurations' open-circuit voltage for different illumination levels. For the two diode configurations, V_{oc} depend logarithmically on I_{ph}. Besides, V_{oc} is always higher in the double diode configuration. It can thus be assumed that, for some wavelengths towards blue and green, the ND-PW top diode contributes positively with current

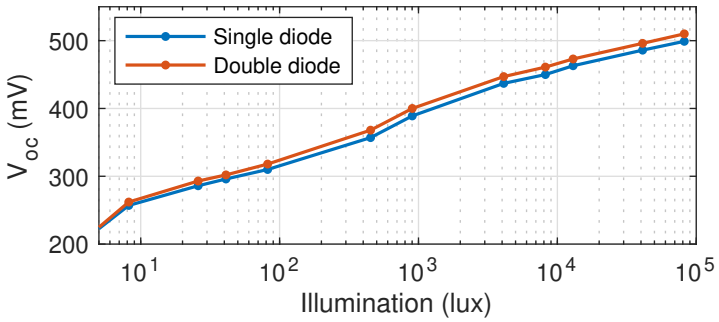


Figure 3.6: Open-circuit voltage, V_{oc}, versus illumination. [6]

values that decrease the current ratio I_{ph_1}/I_{ph_2}, satisfying the condition of (3.5) to achieve a higher V_{oc}. This spectral response is consistent with prior results reported by several authors that have already studied the spectral sensitivity of these diodes separately [81], [88]. Under typical illumination values in indoor environments, V_{oc} ranges between 300 mV and 400 mV. In outdoor environments on sunny days, $V_{oc} \in [410, 500]$ mV. For low illumination values, V_{oc} tends to zero.

Fig. 3.7 depicts current measurements performed. Since the light source was close to the chip, their temperature could affect the measurements. To avoid that, temperature was monitored with a thermometer and kept constant at 35,°C during the experiment. Illuminance on sunny days ranges roughly between 30 klux and 100 klux, thus the 18 µW mm^{-2} harvested at 79 klux serve as a reference value of the amount of power that can be harvested in a standard CMOS process. Given these results, a 20 mm^2 CMOS solar cell mounted on the external unit of the neural interface might be enough for powering the implanted side when it not in stimulation mode.

3.2 Inductive Wireless Power and Data Transfer (WPDT) system

This section is organised as follows. First, an introduction to inductive WPDT is given along with the main limitations of topologies with a single pair of coils. Second, the proposed topology of WPDT system is described. Third, simulation results of an electrical model are shown and discussed.

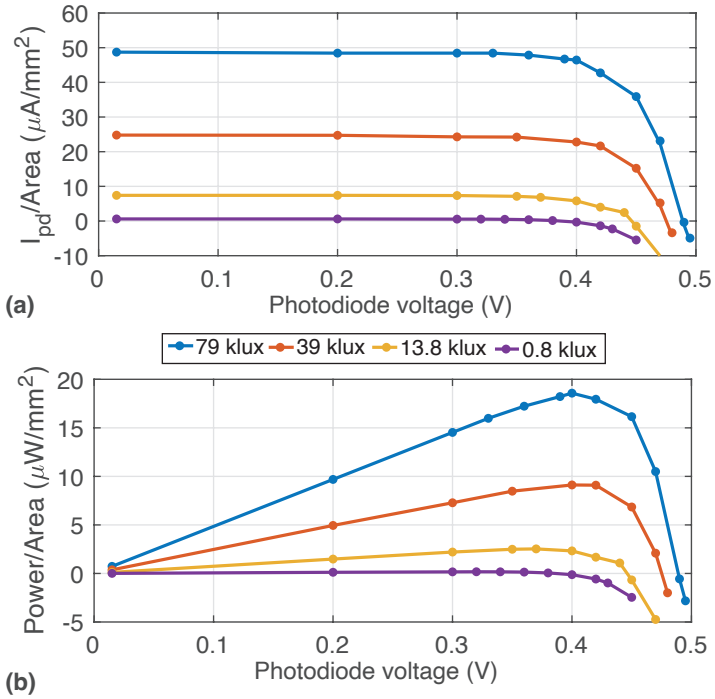


Figure 3.7: Measurements on the photodiode array for different illumination values. (a) Current-voltage curves. (b) Power-voltage curves. [6]

3.2.1 Introduction

WPDT systems are widely used in many applications such as Near-Field Communication (NFC) systems and Implanted Medical Devices (IMD) [91]–[93]. In the latter, the WPDT subsystem allows the implant to be powered and programmed without the need of wires, thus minimizing the risk of infection.

In electrical neuro-modulators, currents from a few hundreds of microamperes up to some milliamperes must be delivered in multiple stimulation sites. Thus, the power demand of the system can range from under 1 mW up to tens of milliwatts. Besides, real time monitoring of neural activity requires sending data from the electrical neuro-modulator to the external unit at rates –i.e. UDT– above 1 Mbps.

To illustrate how WPDT can be performed over a single inductive link, a simplified system is shown in Fig. 3.8. For the sake of simplicity, the

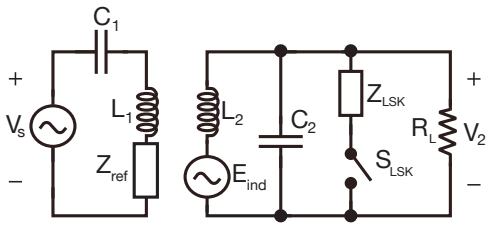


Figure 3.8: Simplified schematic of a resonant inductive WPDT system. Downlink data transfer is performed with ASK by changing the amplitude of V_s. Uplink data transfer is performed with LSK. [7]

impedance seen by the secondary side of the inductive link is modelled as a resistance, R_L. In such a system, power is transferred from the power source at a frequency f_c; UDT is performed with Amplitude-Shift Keying (ASK) by changing the amplitude of V_s; and UDT is performed with LSK. This latter is commonly implemented by switching on and off either a capacitor or a resistor that is placed in parallel to the secondary coil. Finally, it is worth noting that, when implementing WPDT subsystems in IMDs, near-field electromagnetic induction –or inductive coupling– is preferred over far-field electromagnetic induction because living tissue's specific absorption rate increases with the frequency of the electromagnetic wave [94]. In such an arrangement, the voltage gain magnitude is

$$\left|\frac{V_2}{V_s}\right| = \frac{R_L}{\omega_c L_1}\frac{1}{k^2}\frac{Q_L^2}{Q_L^2+1}, \tag{3.8}$$

where k is the coupling factor and Q_L is the quality factor of the series association of L_2 and R_L. It has been assumed that resonant inductors are tuned at ω_c –i.e. $\omega_c^{-1} = \sqrt{C_1 L_1} = \sqrt{C_2 L_2}$ – and that inductors are have no resistive losses –i.e. quality factor tends to infinity–.

In LSK, the impedance seen by the inductive link's secondary side is modified to change the value of the reflected impedance, Z_{ref}, –modeled as a resistor R_{ref} and a capacitor C_{ref}– at the primary side. This change in the reflected impedance is sensed and uplink data is demodulated. However, since the WPDT system is expected to continuously power an electrical neuro-modulator, the reflected impedance is also affected by the amount of power being demanded.

To illustrate this effect, the reflected impedance is calculated both for $Z_{LSK} = R_{LSK}$ and for $Z_{LSK} = (s{\cdot}k_2{\cdot}C_2)^{-1}$. In the first case, the reflected impedance

is

$$R_{ref} = k^2 \frac{L_1}{L_2}(R_L||R_{LSK}) \tag{3.9}$$

$$C_{ref} = \frac{1}{\omega_c k^2 L_1}, \tag{3.10}$$

This way, from Eq. 3.9 and as illustrated in Fig. 3.9a, the reflected resistance equally depends on R_L and R_{LSK}. Thus, the only way to perform reliable LSK is by keeping R_{LSK} smaller than the smallest expected load resistance, thus negatively affecting power delivery. In the second case, the reflected impedance is

$$R_{ref} = k^2 \omega_c L_1 \frac{Q_L(Q_L^2 + k_2^2)}{Q_L^2 + (Q_L^2 + k_2(k_2 - 1))^2} \tag{3.11}$$

$$C_{ref} = \frac{1}{(k\omega_c)^2 L_1} \frac{Q_L^2 + (Q_L^2 + k_2(k_2 - 1))^2}{(Q_L^2 + k_2^2)^2 - k_2(Q_L^2 + k_2^2)}, \tag{3.12}$$

Again, as depicted in Fig. 3.9b, reliable UDT would only be achieved by doing k_2 large, thus heavily detuning the resonant inductive link and affecting power delivery.

The transmission of power to a variable load while simultaneously operating reliable UDT has been previously tackled in the literature. A WPDT system that transmits power and data over a single pair of coils was proposed in [54]. Even though power transferred reaches 10 mW, the UDT rate is just 33.3 kbps. Another proposed solution reports a power transmission of 111 µW and a UDT rate of 1 Mbps [95]. However, the system relies on a complex arrangement of five coils. In [92], a WPDT system that self-regulates against load variations is proposed. It achieves up to 94 mW of power delivered and up 5 Mbps UDT rate. However, the system needs two bulky 40 µH inductors and a LSK demodulator that consumes 6.8 mW.

The electrical model of a WPDT system that allows simultaneous power and data transmission to a wide range of loads over a single pair of coils is presented in the next section.

3.2.2 Proposed WPDT system

A simplified block diagram of the proposed WPDT system is shown in Fig. 3.10(a), including: a programmable step-down DC-DC converter performing ASK modulation, class-E power amplifier, LSK demodulator, resonant two-coils inductive link, LSK modulator, ASK demodulator, rectifier

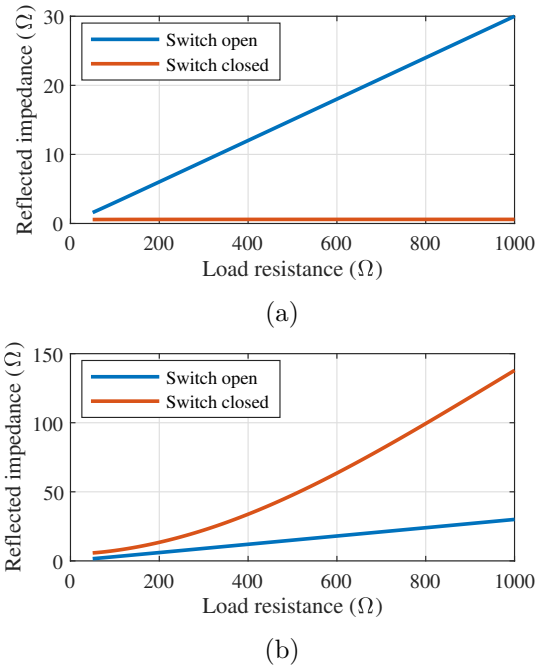


Figure 3.9: Reflected impedance magnitude variation under different load resistances with/without LSK. Parameters: L_1=600 nH, C_1=229.6 pF, L_2=200 nH, C_2=688.9 pF, k=0.1, and f_c=13.56 MHz. (a) Resistive LSK (R_x=500 Ω). (b) Capacitive LSK (k_2=0.1). [7]

and load adapter. Besides, a more detailed schematic of the load adapter block is presented in Fig. 3.10b. In this solution, the issue described in Section I is alleviated by implementing a Power Transfer Phase (PTP) followed by a Data Transfer Phase (DTP), according to the timing diagram depicted in Fig. 3.11.

In the proposed load adapter block, capacitors C_A and C_B store energy. During PTP, one capacitor is charged up at a constant current rate, I_{rect}, which is directly sunk from the rectifier whereas during PTP no current is drawn from the inductive link. The load, I_L, is always being powered by either one capacitor or another. There is no significant power transfer during DTP and, thus, data transmission can be done without affecting power delivery to the load nor consuming much power. The system takes advantage of the fact that microfarad capacitors with sub-mm footprints are commercially available, allowing mW-power and Mbps-data transmission

using only a single pair of coils.

The constant current charging the capacitors must be larger than the maximum current expected to be drawn by the load. With this constraint, the capacitors are sized taking into account 1) the difference between the voltage at which a capacitor is considered to be charged, V_{c1}, and the voltage at which a capacitor is considered to be depleted, V_{c2}, and 2) the duration of PTP, T_{PTP}. The expressions of T_{PTP} and T_{DTP} are

$$T_{PTP} = C_{A,B}\frac{V_{c1} - V_{c2}}{I_{rect}} \tag{3.13}$$

$$T_{DTP} = C_{A,B}(V_{c1} - V_{c2})\left(\frac{1}{I_L} - \frac{1}{I_{rect}}\right), \tag{3.14}$$

In this implementation, the load current ranges from 1 mA up to 15 mA, with an output regulated voltage of 2.5 V. The chosen carrier frequency is 13.56 MHz. The selected storage capacitors have a capacitance of 4.7 µF; the constant current drawn from the rectifier is 25 mA; and the voltage difference in capacitors, $V_{c1} - V_{c2}$, is 0.3 V. Thus, the PTP lasts 26.4 µs or 357.98 periods of the carrier frequency whereas the DTP lasts from 17.6 µs (238.66 periods) to 633.6 µs (8591.6 periods). A longer DTP allows achieving larger bandwidth for data communication. There is thus a trade-off between the power demand and the achievable data transmission bandwidth.

The rest of the system is modeled as follows. Regarding the inductive link, the primary coil is set to 600 nH and the secondary coil to 200 nH. Both coils' quality factors are set to 40. Capacitors are sized to resonate at 13.56 MHz (229.6 pF and 688.9 pF). Besides, we use an electrical model of a Class-E power amplifier (PA) for driving the primary side of the inductive link

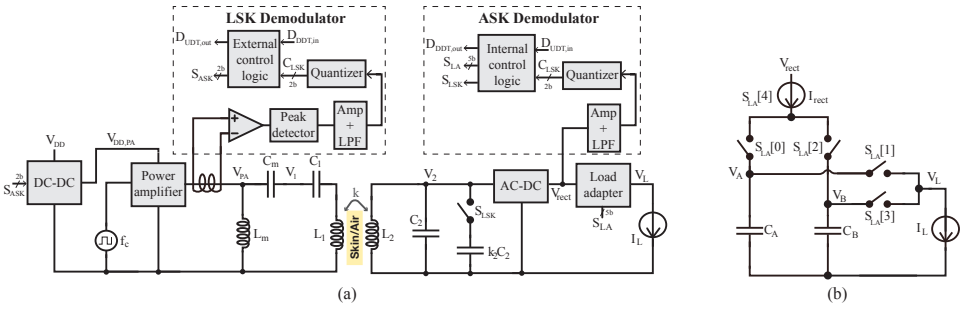


Figure 3.10: (a) Simplified block diagram of the proposed WPDT system. (b) Schematic of the load adapter block. [7]

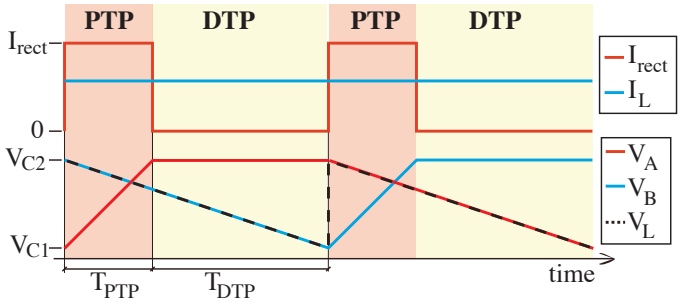


Figure 3.11: Timing diagram of the load adapter block. [7]

[96], [97]. The voltage supply of the PA, $V_{DD,PA}$, originates from a programmable step-down DC-DC converter whose input is 3 V and whose gain is programmed by the external control unit. The values of $V_{DD,PA}$ are 2 V for the PTP and 1 V for the DTP, obtaining a voltage amplitude of around 4.5 V at the secondary side of the link in both phases. The AC-DC converter is modelled as a half-wave rectifier. Finally, uplink demodulator comprises a peak detector, low-pass filter, amplifier and 2-bits quantizer; and downlink demodulator includes a low-pass filter, amplifier and 2-bits quantizer.

3.2.3 Simulation results

We built an electrical model of the proposed WPDT system in MATLAB Simulink, taking advantage of the Simscape Electrical and Stateflow toolboxes for implementing analog and digital blocks, respectively. First, we show power transmission to a 15 mA load current. Results are shown in Fig. 3.12, where power and data transfer phases are highlighted. The WPDT system can deliver around 40 mW of power to a load even when no significant power is drawn from the inductive link. Power consumption of circuitry at the secondary side during DTP was modelled with a 0.5 mA load current.

UDT with LSK modulation was proven by sending two bytes of data at 1 Mbps meanwhile a 15 mA load is powered. Results are depicted in Fig. 3.13. The main limitation for achieving higher data rates are both the carrier frequency and the hold time required by the LSK demodulator, which was modelled at roughly 0.7 µs in this work. Two bytes of data were sent along with start/end of frame delimiters identifying the beginning and end of the data package.

Finally, DDT with ASK modulation was tested by sending two bytes of

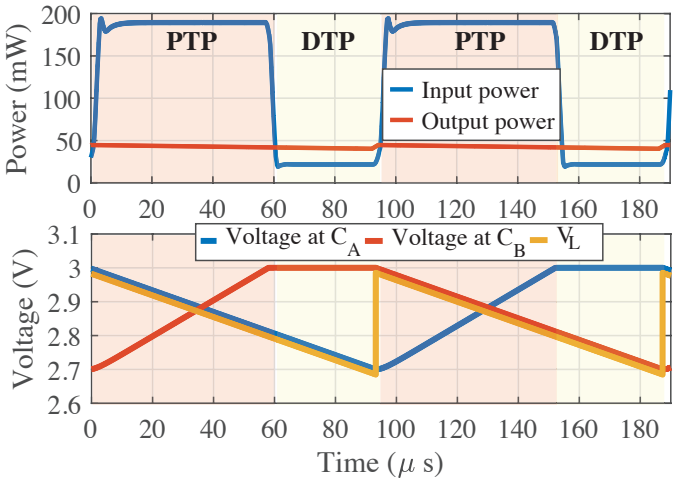


Figure 3.12: Power transmission to a 15 mA load. (Top) Power drawn by the primary side of the inductive link and power delivered to the load. (Bottom) Voltages V_A, V_B and V_L (as shown in Fig. 3.10b). [7]

data at 500 kbps while powering a 5 mA load. Results are shown in Fig. 3.14. It can be seen that ASK modulation is performed by changing the voltage supply of the PA between 1 V and 1.2 V, which induce a change in the voltage at the secondary side. The output voltage is then sensed by the ASK demodulator and converted back to a serial data stream.

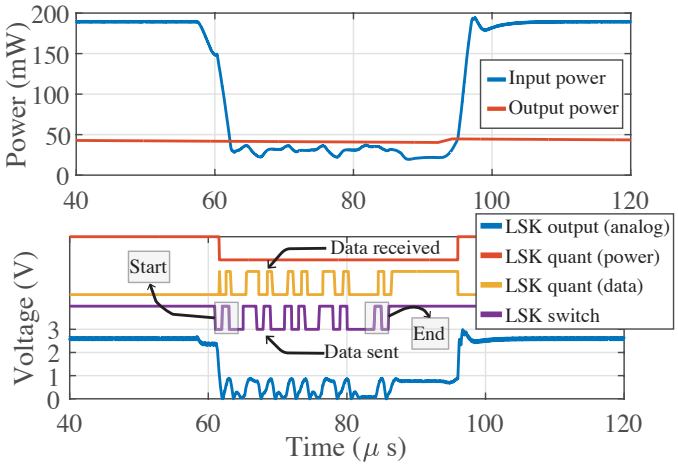


Figure 3.13: Power transmission to a 15 mA load and UDT of two-bytes package. (Top) Power drawn by the primary side and power delivered to the load. (Bottom) Digital signal driving the LSK switch (purple), analog output voltage of the LSK demodulator (blue), LSK demodulator bit for differentiating between PTP and DTP (red) and LSK demodulator bit for received data (yellow). [7]

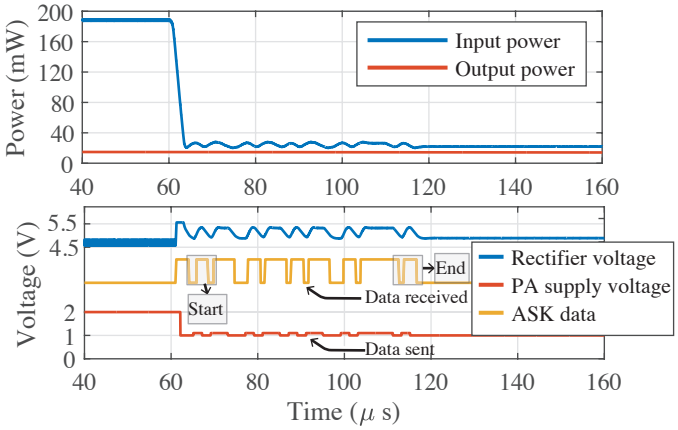


Figure 3.14: Power transmission to a 5 mA load and DDT of two-bytes package. (Top) Power drawn by the primary side and power delivered to the load. (Bottom) output voltage at the rectifier of the secondary side (blue), voltage $V_{DD,PA}$ (red) and ASK demodulator output for received data (yellow). [7]

Chapter 4

High-Voltage Switched-Capacitor DC-DC Converter

In this chapter, the High-Voltage Switched-Capacitor Regulated DC-DC Converter (HV-SCRC) implemented in the neurostimulator shown in Fig. 1(b) is presented. In Section 4.1, an introduction to the circuit is given. Architecture, components, and operation modes are described in Section 4.2. In Section 4.3, experimental results are presented and discussed.

4.1 Introduction

As discussed in Chapter 2, to withstand a broad range of current/voltage values, it is fundamental that the power management unit of the neural implant, on which this chapter focuses, includes a programmable DC-DC converter with adjustable Voltage Conversion Ratio (VCR) to guarantee that the stimulator operates under safety limits without excessive power dissipation [98], particularly, when the ETI equivalent impedance and/or the stimulation currents are large. Additionally, to relax the power transfer specifications of the wireless powering mechanism, the efficiency of the DC-DC converter should reach its peak for large stimulation currents for which the availability of electrical power is more demanding. Last but not least, the DC-DC converter should react rapidly under variations of the load current as occurs in electrical neurostimulation, and use no external component to

reduce the form factor of the implant.

These aspects are addressed in this chapter, where a versatile fully on-chip High-Voltage Switched-Capacitor Regulated DC-DC Converter (HV-SCRC) is presented. Instead of using a HV CMOS node, the converter is implemented in a standard 1.8V/3.3V 0.18 µm CMOS process to allow for a single-chip neural implant integration, along with other elements already designed in this technology [1], [2].

The use of standard processes for the generation of voltages above the nominal supply of the technology demand for circuit solutions that guarantee that voltage drops across devices are safely below the breakdown limits. The approach has been also followed in previous contributions [78], [99]–[104]. However, these solutions present some drawbacks such as the lack of output voltage regulation [100], usage of off-chip capacitors [100], [104], generation of a fixed output voltage [78], [104], low load current driving capability [100], [101], [103], [104], or low VCR [102].

4.2 System architecture and circuit design

Fig. 4.1 shows the proposed HV-SCRC. It consists of three main blocks: (1) an $M \times N$ array of Charge-Pumps (CPs) driven by the input voltage

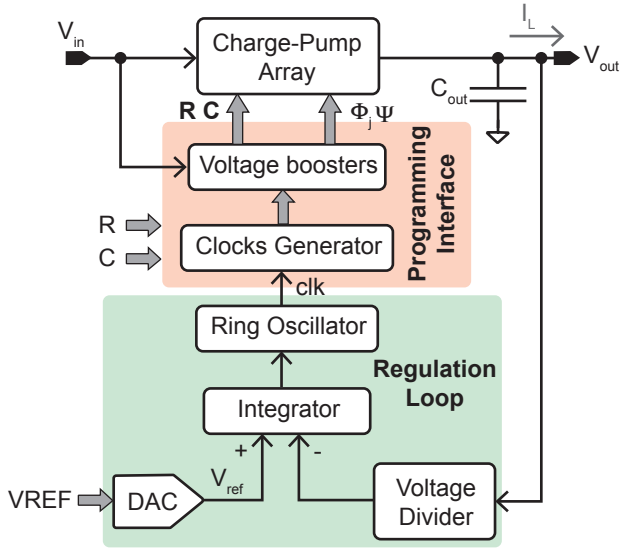


Figure 4.1: Simplified schematic of the proposed HV-SCRC.

V_{in}; (2) a Voltage-Controlled Oscillator (VCO) based feedback loop which regulates the output voltage of the CP array, V_{out}, against variations of the load current I_L by adjusting the pumping clock frequency, f_{clk}; and (3) a programming interface for enabling/disabling rows or columns in the array and for generating a set of clock phases from clk. The output of the array is loaded with a 125 pF Metal-Oxide-Metal (MOM) capacitor, C_{out}, to attenuate voltage ripples. The feedback loop and the programming interface are supplied at $V_{DD} = 1.8\,V$. The logic high of the clocks driven the CP array, $\mathbf{\Phi}_j$ and $\mathbf{\Psi}$, and the row/column cell selection variables, $\mathbf{R}$ and $\mathbf{C}$, are boosted from V_{DD} to V_{in} by means of conventional level shifters based on differential cascode voltage switch logic [105].

4.2.1 Charge-pump array and programming interface

In the proposed implementation, the array comprises 16 structurally identical CPs distributed in a 4×4 architecture ($M = 4$, $N = 4$), as shown in Fig. 4.2. The outputs of all the CPs in the same column are connected together. Active rows and columns are enabled using the $\mathbf{R} = \{R_i\}, i = 1, \ldots, 4$, and $\mathbf{C} = \{C_j\}, j = 1, \ldots, 4$, configuration bits, respectively (see Fig. 4.1). All possible row combinations, 16 in total, are possible. However, a column can only be activated if the previous one is enabled and, therefore,

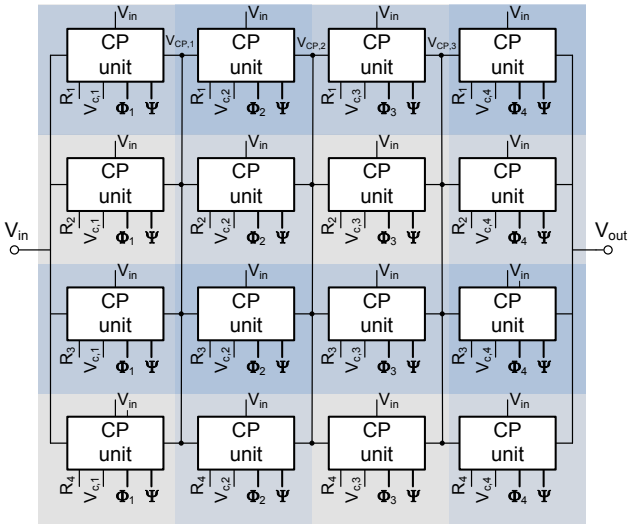


Figure 4.2: Block diagram of the charge-pump array. Signals $V_{c,j}$ are voltage-shifted versions of C_j which are distributed per column in the array.

only 4 combinations are possible. Extensions for different number of rows, M, or columns, N, is straightforward, whenever the breakdown voltages of the CMOS process are not exceeded.

In the selected process, the PN-junctions of PMOS and DNW-NMOS transistors have breakdown voltages above 14 V, and transistors can withstand voltage differences of up to 3.3 V. Consequently, the number of columns in the presented design has been set to $M = 4$ and the maximum input voltage has been set to 3 V, to give some margin against transient spikes during switching.

The voltage levels of **R** and **C** have to be adjusted according to the cell position in the array. Namely, it has to be guaranteed that the transformed variables are comprised between the input $V_{CP,j-1}$, and the output, $V_{CP,j}$ of the cell (by construction, $V_{CP,0} = V_{in}$, i.e., the input voltage of the array). This is done by means of HV-FLS [4], [106]. The schematic and symbol of a HV-FLS are shown in Fig. 4.3. Assuming the control signal EN is comprised between ground and V_{in}, the circuit generates a voltage-shifted

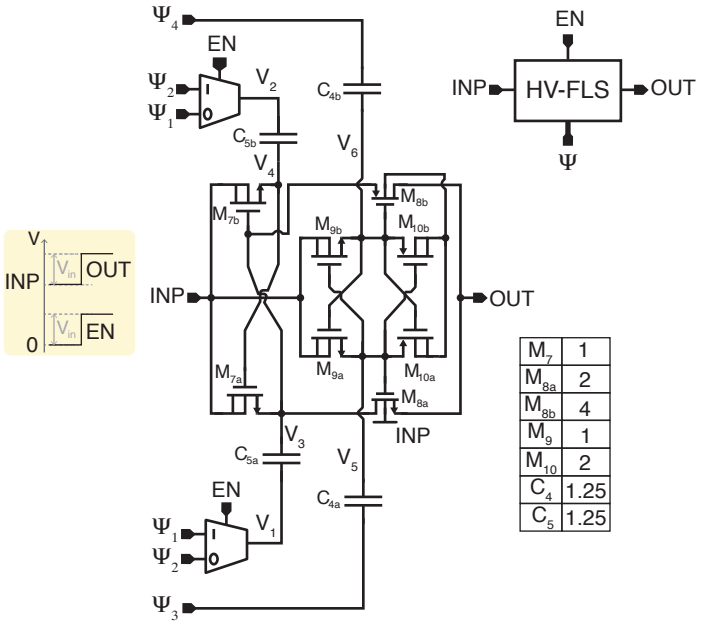


Figure 4.3: Schematic and symbol of the HV-FLS for sliding configuration bits. The dimensions of the transistors and capacitors are given in µm and pF, respectively. All the transistors have a length of 0.35 µm. [4]

version, OUT, which swings from INP to $V_{in} + INP$. As capacitors C_{4x}-C_{5x} (x stands for a or b) are periodically refreshed with $\mathbf{\Psi} = \{\psi_k\}, k = 1, \ldots, 4$, the circuit can tolerate non-periodical EN signals or variations of the shifting voltage, INP. The HV-FLS supports a wide range of INP values, exhibits a propagation delay of only 1.86 ns, and its power consumption is 13.9 µW (for $INP = 9.5$ V and $f_{\mathbf{\Psi}} = 2.5$ MHz).

The circuit consists of three main blocks: (1) a local HV-FLS (C_{5x} and M_{7x}), (2) a basic charge-pump (C_{4x}, M_{9x}, and M_{10x}), and (3) a sample-and-hold

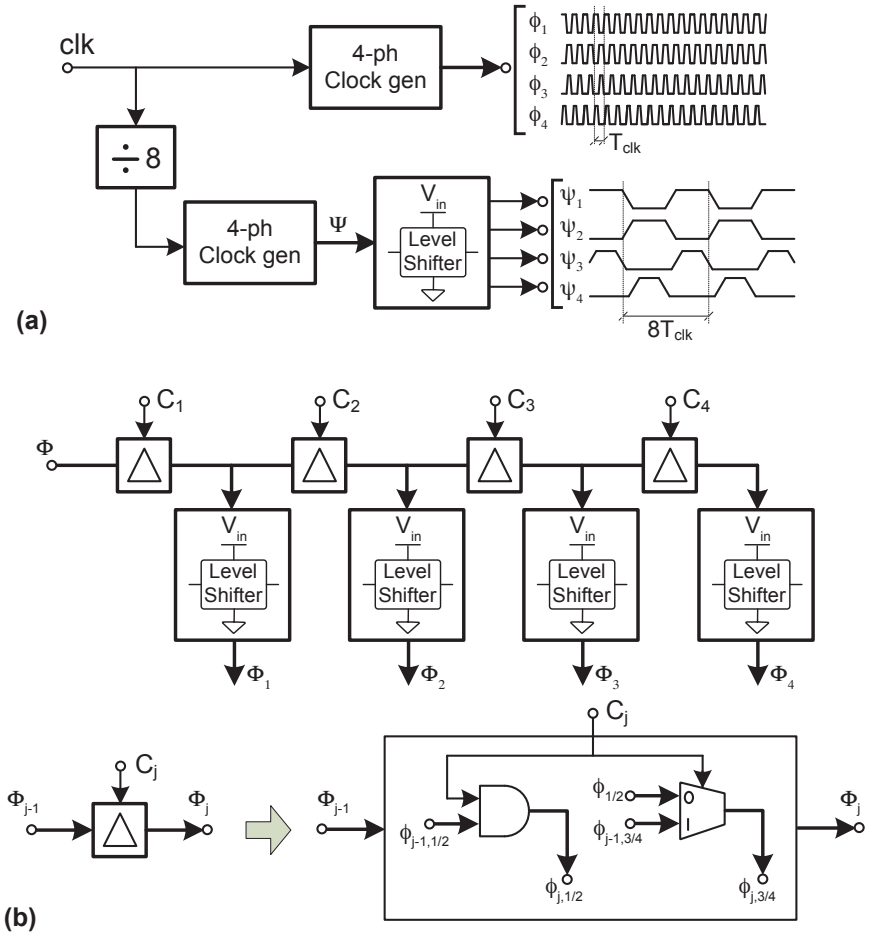
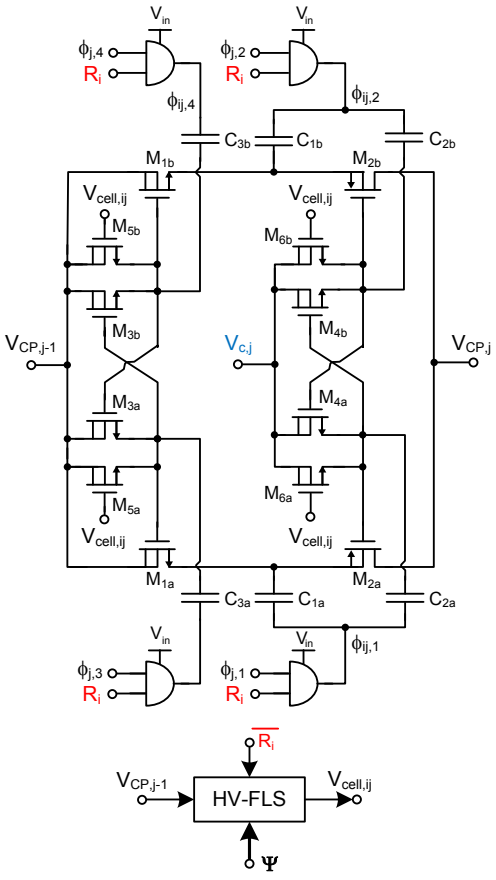


Figure 4.4: Timing diagram of the 4-phase clock signals $\mathbf{\Phi}$, $\mathbf{\Phi}_j$ and $\mathbf{\Psi}$. All the circuit elements are supplied at V_{DD}, excepting the clock drivers that are biased at V_{in}.

(S&H) (transmission gates M_{8x} and load capacitor). Complementary clock signals Ψ_1 and Ψ_2 are in-phase with signals Ψ_3 and Ψ_4, respectively, with non-overlapping time margins at the rising and falling edges, as illustrated in 4.4(a).

The local HV-FLS provides the input voltage, V_3, of the S&H circuit. Signal V_3 is in-phase with Ψ_1 if the FLS input, EN, is in high state; otherwise V_3 is in-phase with Ψ_2. Accordingly, if EN is HIGH, $V_3 \approx V_{in} + INP$ and,



M_1	M_2	M_3	M_4	M_5	M_6	C_1	C_2	C_3
48	96	0.5	0.5	4	8	12.5	0.6	0.6

Figure 4.5: Proposed cross-coupling CP cell with enhanced conduction main transistors. Similar comments as in Fig. 4.3 hold for dimensions and values.

otherwise, if EN is LOW, $V_3 = INP$. The charge pump generates two voltage-shifted versions of the clock signals Ψ_3 and Ψ_4, named V_5 and V_6, that drive the gates of transistors M_{8a} and M_{8b}, respectively. Also, it biases the bulk of M_{8b} and the deep n-wells of DNW-NMOS transistors. When Ψ_3 is HIGH (alt. Ψ_4 is LOW), voltage V_3 is sampled in the load capacitor. Otherwise, if Ψ_3 is LOW (alt. Ψ_4 is HIGH), the charge stored in the load capacitor is held. Note that the non-overlapping margins between Ψ_1 and Ψ_3 (similarly between Ψ_2 and Ψ_4) guarantee that signal sampling only occurs when V_3 is established.

During the sampling phase, if the EN signal state is LOW (alt. HIGH), C_{5a} (alt. C_{5b}) stores the voltage level INP and C_{5b} (alt. C_{5a}) pumps charge to the load capacitor. On the other hand, during the holding phase, if the EN state is LOW (alt. HIGH), C_{5b} (alt. C_{5a}) stores the voltage level INP and C_{5a} (alt. C_{5b}) pumps charge to the load capacitor. Regardless of signal EN level, the capacitor C_{4a} (alt. C_{4b}) stores INP in the hold (alt. sampling) phase and the capacitor C_{4b} (alt. C_{4a}) pumps charge in the hold (alt. sampling) phase. Hence, the capacitors are refreshed at the frequency of the main clock. This allows to track time-varying shifting voltages INP and handle non-periodic input signals EN.

Fig. 4.4(a) shows the timing diagram of clock $\mathbf{\Psi}$, which is generated at the programming interface from the *clk* output of the regulation loop (see Fig. 4.1). Clock $\mathbf{\Psi}$ is made 8× slower than $\mathbf{\Phi}$ by means of a clock divider to save power consumption.

Fig. 4.5 shows the schematics of the CP core. It follows a cross-coupling architecture [107], [108]. Besides the main charge pumping stage (M_{1x}-M_{2x} and C_{1x}), it includes two auxiliary charge-pump circuits (M_{3x}-M_{4x} and C_{2x}-C_{3x}) for boosting the conductivity of the core transistors; one HV-FLS integrated within the CP cell for level-shifting the selection bits R_i and C_j to $V_{cell,ij}$; and switches (M_{5x}-M_{6x}). The flying capacitors (C_{1x}-C_{3x}) nominally have a capacitance of $C_{fly} = 12.5\,\text{pF}$. They are implemented with a single MIM structure in the cells located in the first and second columns of the array; however, the CPs in the third and fourth columns use two series-connected MIM capacitances to support higher voltages. DNW NMOS transistors were employed in the CPs.

Fig. 4.6 shows the cascade circuit used for implementing the voltage-shifted column selection signals $V_{c,j}$ from the configuration bit $C_j, j = 1, \ldots, 4$. The circuit is implemented outside the CP array and employs both HV-FLS and digital buffers. The values of $V_{c,1-4}$ for $N_a = \{1, 2, 3, 4\}$ are shown

Table 4.1: Values of the voltage-shifted column selection signals, depending on the number of stages enabled.

Node	$\mathbf{N_a = 1}$	$\mathbf{N_a = 2}$	$\mathbf{N_a = 3}$	$\mathbf{N_a = 4}$
V_{out}	$V_{in} + V_{pump}$	$V_{in} + 2{\cdot}V_{pump}$	$V_{in} + 3{\cdot}V_{pump}$	$V_{in} + 4{\cdot}V_{pump}$
$V_{c,1}$	V_{in}	V_{in}	V_{in}	V_{in}
$V_{c,2}$	V_{in}	$V_{in} + V_p$	$V_{in} + V_{pump}$	$V_{in} + V_{pump}$
$V_{c,3}$	V_{in}	$V_{in} + V_{pump}$	$V_{in} + 2{\cdot}V_{pump}$	$V_{in} + 2{\cdot}V_{pump}$
$V_{c,4}$	V_{in}	$V_{in} + V_{pump}$	$V_{in} + 2{\cdot}V_{pump}$	$V_{in} + 3{\cdot}V_{pump}$

in Table 4.1, where V_{pump} is the voltage pump introduced by each enabled column.

The clock signals $\mathbf{\Phi}_j = \{\phi_{j,k}\}, k = 1, \ldots, 4$ employed by the CPs are shared by columns. They are derived from the non frequency-divided clock $\mathbf{\Phi}$ represented in Fig. 4.4(a) using the circuit shown in Fig. 4.4(b). Note that the phases $\phi_{j,k}$ depend on the configuration bits C_j. Using the Delta blocks shown in Fig. 4.4(b), the phases $\phi_{j,k}$ are defined as:

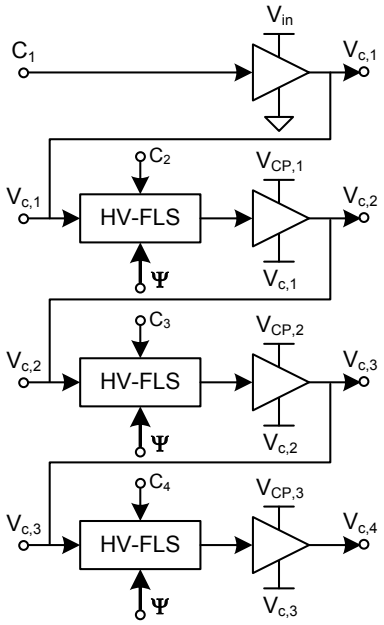


Figure 4.6: HV-FLS based generation of voltage-shifted column selection signals $V_{c,j}$ from the configuration bit $C_j, j = 1, \ldots, 4$.

$$\mathbf{\Phi}_j = \begin{cases} \{\phi_1, \phi_2, \phi_3, \phi_4\} & , C_j = 1 \\ \{0 \ , 0 \ , \phi_1, \phi_2\} & , C_j = 0 \end{cases} \tag{4.1}$$

Also note that because of the cascaded synthesis of the clocks $\mathbf{\Phi}_j, j = 1, \ldots, 4$, they are slightly time delayed each other, regardless of the C_j values. This avoids that flying capacitors are charged at the same time, thus smoothing the current demand of the DC-DC converter [109].

Depending on whether the row and column of the CP cell are enabled or disabled, three different operation modes, denoted as PUMP, BYPASS, or DISABLED, can be defined. They are illustrated in Fig. 4.7 (only core transistors M_{1x}-M_{2x} are shown for clarity).

- **PUMP**. In this mode (see Fig. 4.7(a)), the row and column of the cell are enabled, $V_{cell,ij} = V_{CP,j-1}$ and $V_{c,j} = V_{CP,j-1}$. Hence, the cell operates as a cross-coupled CP in which core transistors (M_{1x}-M_{2x}) are switched on and off as illustrated in the figure, and switches (M_{5x}-M_{6x}) are off. The voltage $V_{pump,j}$ pumped to the following *j-th* column of the array is given by

$$\begin{aligned} V_{pump,j} &= V_{CP,j} - V_{CP,j-1} \\ &= V_{in} - \frac{I_L}{2M_a f_{clk} C_{fly}} \end{aligned} \tag{4.2}$$

  where C_{fly}, M_a, $V_{CP,i-1}$, V_{in}, f_{clk}, and I_L are, respectively, the value of the flying capacitor C_{1x}, the number of active rows, the cell's input voltage, the input voltage of the HV-SCRC, the pumping frequency, and the load current. Since the cells of the CP array are equally sized, the charge pumped from the input voltage source to the load is equally distributed among the flying capacitors, thus resulting in a constant pumping voltage, V_{pump}, across all cells. As V_{pump} decreases, the conduction resistance of M_{2x} increases, thus increasing the charge transfer time constant formed with the flying capacitors. When this time constant is comparable to the pumping clock period, charge is not fully transferred to the next stage, and the output voltage can not be properly regulated. In the proposed design, this performance limit is observable when $V_{pump,j}$ drops below roughly 1 V.

- **BYPASS**. In this mode (see Fig. 4.7(b)), the row of the cell is enabled but the column is disabled. This is done by permanently setting M_{2x} on and by alternatively switching M_{1x} on and off. In this case, $V_{cell,ij} =$

$V_{CP,j-1}$ and $V_{c,j} = V_{c,j-1}$. If the previous stage is in PUMP mode, $V_{c,j} = V_{CP,j-2}$, otherwise, if it is in BYPASS mode, $V_{c,j} = V_{c,j-2}$. Note that the flying capacitors are tied to the cell output node to reduce voltage ripples.

- **DISABLED**. In this mode (see Fig. 4.7(c)), the row of the cell is disabled and, regardless of the C_j value, the cell's input and output voltages are isolated and flying capacitors contribute to reducing the ripple. In this case, $V_{cell,ij} = V_{CP,j-1} + V_{in}$, and if the column is enabled, $V_{c,j} = V_{CP,j-1}$, otherwise $V_{c,j} = V_{c,j-1}$.

Assuming a general $M \times N$ array architecture and neglecting conduction and switching losses in the CPs, the output voltage V_{out} of the HV-SCRC follows a saw-tooth waveform with period $T_h = T_{clk}/2$ given by

$$V_{out}(t) = V_0 - R_{eq} I_L + \left[1 - \left(\frac{t}{T_h} - \left\lfloor \frac{t}{T_h} - 1 \right\rfloor\right)\right] \frac{I_L}{C_{eq}} \tag{4.3}$$

where $\lfloor \cdot \rfloor$ represents the floor function, $V_0 = (N_a + 1)V_{in}$, N_a is the number of active columns in the array, and

$$R_{eq} = \frac{N_a}{2M_a f_{clk} C_{fly}} \tag{4.4}$$

$$C_{eq} = \left[2M(N - N_a + 1) - M_a\right] C_{fly} + C_{out} \tag{4.5}$$

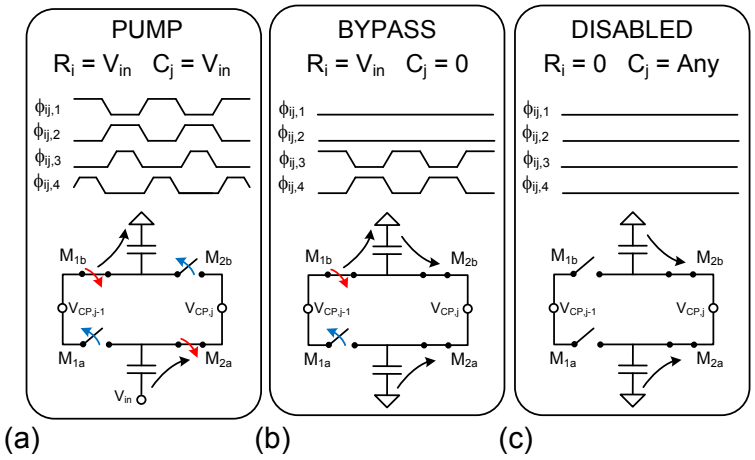


Figure 4.7: Simplified schematic of the proposed CP cell in its different states: (a) PUMP, (b) BYPASS, (c) and DISABLED. Clock phases are also shown.

Note that during the time interval $[0, T_h]$, $V_{out}(t)$ can be interpreted as the voltage drop across an equivalent $R_{eq} - C_{eq}$ series circuit, with the capacitor having an initial voltage V_0, which is discharged by a current load I_L. From (4.3), the average output voltage, $V_{out,avg}$, and the output ripple, ΔV_{out}, of the converter are, respectively, given by

$$V_{out,avg} = V_0 - \left(R_{eq} + \frac{1}{4 f_{clk} C_{eq}} \right) I_L \tag{4.6}$$

$$\Delta V_{out} = \frac{I_L}{2 f_{clk} C_{eq}} \tag{4.7}$$

For a given flying capacitance C_{fly} and output capacitor C_{out}, (4.6) shows that the voltage conversion ratio, $VCR = V_{out}/V_{in}$, is mainly determined by N_a, however, it also depends on M_a and f_{clk}. Similarly, the output voltage ripple also depends on N_a, M_a and f_{clk}, according to (4.7). This reliance on multiple parameters is key to expanding the operating range of the HV-SCRC, as well as allowing different configurations for a given target. This is illustrated in Fig. 4.8 which shows the operation range segments (thick lines) for four different M_a and N_a combinations in the V_{pump} vs. $V_{out}(0)$ plane for an arbitrary case where $V_{in} = 3.0\,\text{V}$ and $I_L = 0.5\,\text{mA}$. The combinations

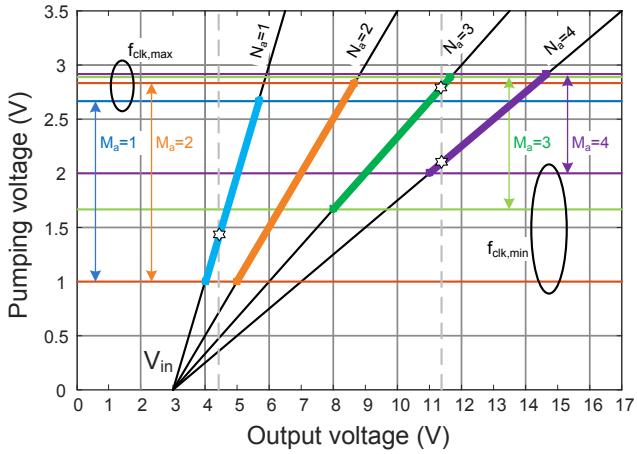


Figure 4.8: Graphical representation of the converter operation range for different row/column configurations, assuming $I_L = 0.5\,\text{mA}$, $V_{in} = 3.0\,\text{V}$. Top (alt. bottom) horizontal colored lines represent the achievable pumping voltage at maximum (alt. minimum) f_{clk} for $M_a = 1, 2, 3, 4$.

are $M_a = N_a = \{1, 2, 3, 4\}$. From (4.2) and (4.3), the segments follow the expression

$$V_{pump} = \frac{V_{out}(0) - V_{in}}{N_a} \tag{4.8}$$

and the upper and bottom boundaries of each are obtained from (4.2) for the maximum and minimum values of the pumping clock frequency f_{clk} generated by the regulation loop. As mentioned, the lower boundaries cannot be decreased below approximately 1 V. Note from Fig. 4.8 that the segments cover different operation ranges, and there are output voltages which can only be accessed with one configuration. For instance, an output voltage of 4.3 V is only achievable if $M_a = N_a = 1$, as shown in the plot. It can also be observed that the segments overlaps for given output voltages. For instance, an output voltage of $V_{out} = 11.3$ V can be generated both with $M_a = N_a = 3$ and $M_a = N_a = 4$. This paves the way to select one configuration or another for a target output voltage based on considerations like power efficiency or voltage ripple.

This is further illustrated in Fig 4.9, which shows the accessible output voltage regions of the converter in terms of the load current and the number of activated rows $M_a = \{1, 2, 3, 4\}$, assuming $N_a = 4$ and $V_{in} = 3$ V. The overlaps between the different regions are clearly observable and it can also be seen that some operation points are only accessible from a single con-

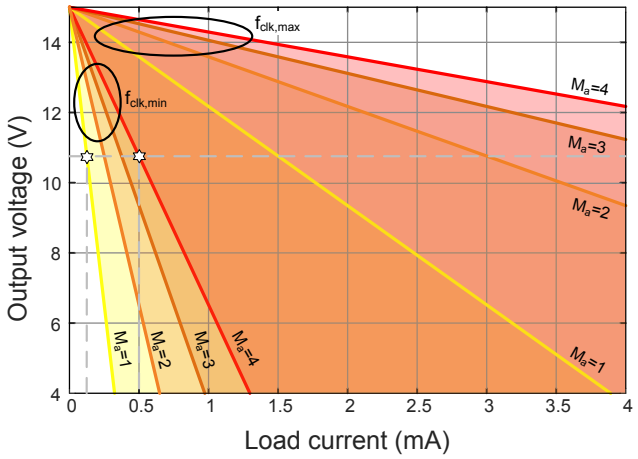


Figure 4.9: Graphical representation of the HV-SCRC's operation range in terms of the load current and the number of activated rows for N_a=4, V_{in}=3 V.

figuration. For instance, $M_a = 1$ is the only possibility for generating a target output voltage $V(0) = 10.5$ for load currents down to 0.1 mA. This illustrates the advantages that row programming offers for extending the operation range of the converter – a non-programmable $M_a = 4$ implementation would have require a load current of 0.5 mA for the same output voltage–.

The power losses of the array, not considered in (4.3), depend on the number of active cells and the $f_{clk} \cdot C_{fly}$ product as [110],

$$P_{loss,tot} = f_{clk} \cdot C_{fly} \cdot (2 \cdot \beta \cdot V_{in}^2 + K_{inv}) \cdot M_a \cdot N_a. \tag{4.9}$$

where the first sum term accounts for the switching-losses due to the parasitic capacitances of the flying capacitors (they are estimated as a fraction β of the C_{fly} nominal value), and the second term represents the short-circuit losses of the flying capacitor drivers. This loss is modeled by parameter K_{inv} which depends on circuit dimensions and increases with the square of the input voltage, V_{in}.

Equation (4.9) reveals that power losses increase with the pumping frequency. However, from (4.4) and (4.7), the equivalent output resistance and the output voltage ripple are both inversely proportional to f_{clk}. Hence, there is a trade-off between power efficiency, achievable output voltage, and voltage ripple. A similar trade-off also holds if the number of active rows increases, i.e., power efficiency lowers but the converter output is smoother. Referring back to the graphical representation in Fig. 4.8, if a given target output voltage can be generated from two or more configurations, the one for which the operating point is closer to the lower limit of its feasibility segment gets a better energy efficiency. On the contrary, the configuration with an operating point closer to the upper limit obtains a better ripple behavior. These trade-offs will be further illustrated in Section III.

4.2.2 Regulation circuit

It consists of a negative feedback loop which generates a clock signal that locks when the difference between a 1/10 scaled version of the HV-SCRC's output and an internal voltage reference cancel out. Voltage scaling is implemented using a string of diode-connected PMOS transistors from the converter output to ground, and the voltage reference is obtained from a 4 bits NMOS-based DAC –shown in Fig. 4.10(b)–. The output of the DAC is comprised within the range from 0.42 mV to 1.32 V at 60 mV steps, and

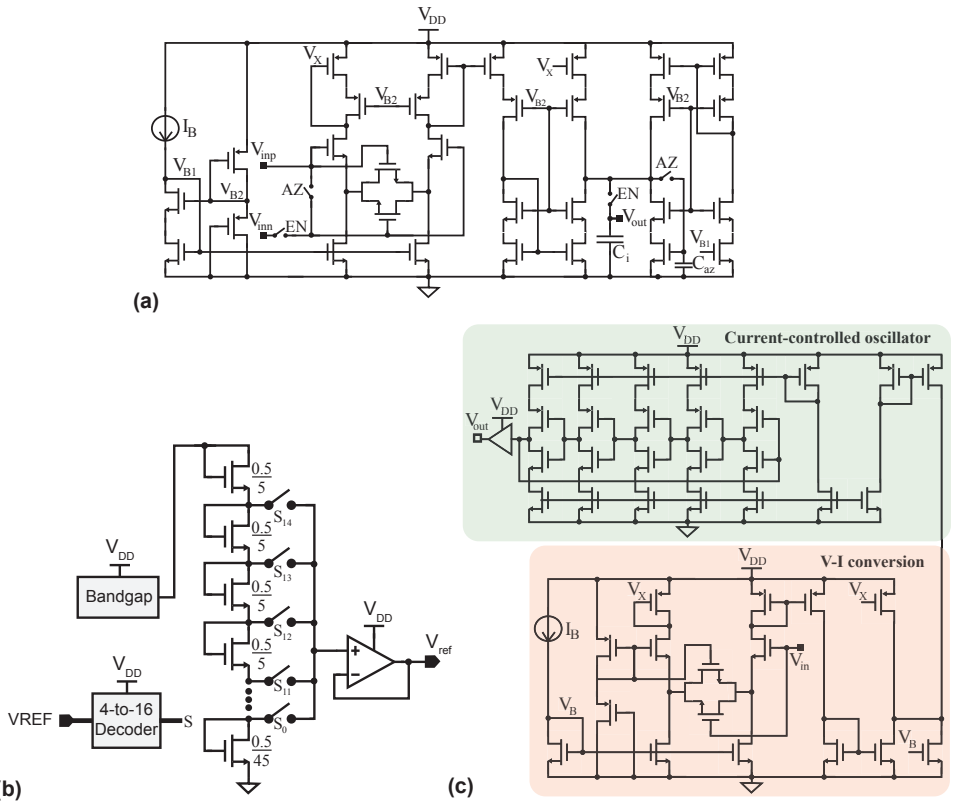


Figure 4.10: Regulation loop circuit. (a) G_m-C integrator with current auto-zeroing circuit for offset-compensation. (b) 4 bits voltage DAC. (c) VCO.

can be selected using the input word *VREF* (see Fig. 4.1). A resistor-less bandgap provides the DAC's reference [111].

Additionally, the feedback loop comprises a G_m-C integrator and a VCO, shown in Figs. 4.10(a,c). Both are powered at 1.8 V and biasing currents are obtained from an integrated self-biased 25 nA current reference [112].

The G_m-C integrator is shown in Fig. 4.10(a). It consists of a single-ended current-mirror transconductor with input source-degeneration for enhancing linearity, and a 110 fF MIM integration capacitor, C_i. The integration time constant is approximately 160 µs. A current auto-zeroing circuit is used for offset-compensation [113]. During auto-zero ($AZ = \text{'}1\text{'}$), the feedback loop is opened, the inputs of the transconductor are shorted together to the DAC output, and the offset current is sampled in a 780 fF MIM capacitor, C_{az}.

In this phase, which lasts 15 µs, the integration capacitor C_i is disconnected from the transconductor and drifts at a rate of roughly 2 mV/ms. This, however, has a negligible impact on the pumping frequency f_{clk} and, hence, on the converter output. When the transconductor is enabled ($AZ = $'0'), C_{az} is disconnected from transconductor output, and the stored offset current is subtracted from the output current. Montecarlo simulations with PVT variations on extracted layout showed that the standard deviation of the transconductor input-referred offset decreased from 38.2 mV down to 61 µV through auto-zero. The storage capacitor C_{az} discharges during the hold phase ($AZ = $ *'0'*) at about 0.2 mV/m and has to be refreshed through auto-zeroing at a minimum frequency of 200 Hz to maintain the transconductor offset below 1 mV. This deviation carries a converter's output decrease of 10 mV, which is deemed acceptable for the intended application.

Fig. 4.10(b) shows the VCO. It uses a source degenerated Operational Transconductance Amplifier (OTA) for voltage-to-current conversion and a current-starved ring-oscillator for current-to-frequency conversion. The negative input of the OTA is set to mid-rail, and the output current range is shifted from $[-I_{out,max},\ I_{out,max}]$ to $[0,\ 2{\cdot}I_{out,max}]$. In this range, the frequency of the VCO output, f_{clk}, approximately sweeps from 5 MHz up to 60 MHz.

4.2.3 Biasing and reference circuitry

Fig. 4.11 shows the on-chip bandgap voltage reference, which outputs 1.33 V at $T = 36\ ^{o}C$. It adds a voltage, V_0, which is Proportional To Absolute Temperature (PTAT) with a negative Temperature Coefficient (TC) to a voltage

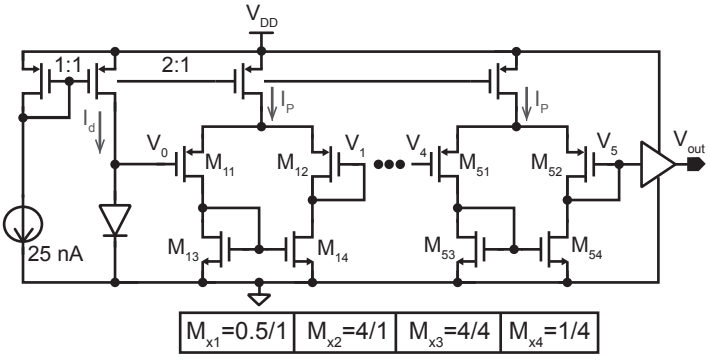


Figure 4.11: On-chip bandgap voltage reference [111]. Transistor dimensions are shown in micrometers.

with positive TC. Voltage V_0 is generated by forcing a current I_d to flow through a diode

$$V_0 = n_D \cdot U_T \cdot ln\left(\frac{I_d}{I_s} + 1\right), \tag{4.10}$$

which, as mentioned, shows a negative TC with temperature [114]. Each of the five subsequent differential pairs is biased in the weak inversion region in order to add a voltage ΔV_P to V_0

$$\Delta V_P = V_i - V_{i-1} = n_P \cdot V_{TH,P} \cdot \ln(K_N K_P), \tag{4.11}$$

where n_P and $V_{TH,P}$ are the subs-threshold slope and threshold voltage of PMOS transistors $M_{x1,x2}$; K_N is the fraction between the aspect ratios of M_{x3} and M_x4; and K_P is the fraction between the aspect ratios of M_{x2} and M_x1. Since $V_{TH,P}$ has a positive TC, so does ΔV_P.

The output voltage, V_{out}, is thus

$$V_{out} = 5 \cdot n_P \cdot V_{TH,P} \cdot \ln(K_N K_P) + n_D \cdot U_T \cdot ln\left(\frac{I_d}{I_s} + 1\right). \tag{4.12}$$

The circuit was designed for a temperature $T = 36\,^oC$, which is approximately the body temperature both in humans and mices. Fig. 4.12 shows the voltage-temperature curve obtained in post-layout simulations.

Fig. 4.13 depicts the implemented self-biased current reference, generating 25 nA at $T = 36\,^oC$ [112]. Transistors M_{3-8} operate in weak inversion, whereas M_{1-2} are biased in moderate inversion. M_{4-7} generate a current which flows through M_1, which is in triode in region. Since the circuit has a stable state in which no current flows through any branch, a start-up circuit was added. Fig. 4.14 shows the current-temperature curve obtained in post-layout simulations.

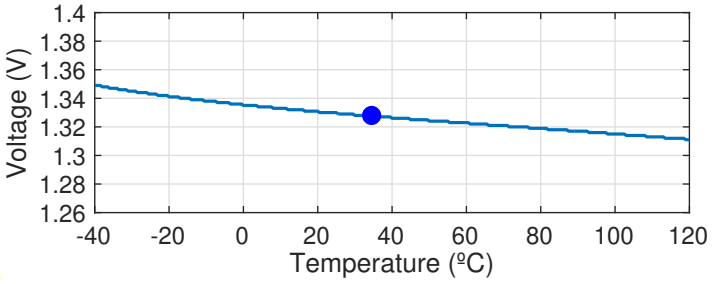
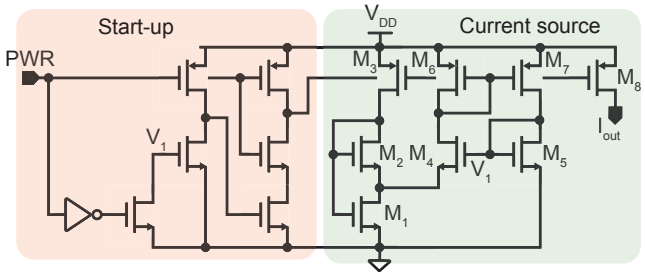


Figure 4.12: Voltage-temperature curve of the bandgap voltage reference, obtained from post-layout simulations.



M_1=0.85/19.9	M_2=1.7/19.9	M_3=2/10	M_4=126/1.4
M_5=42/1.4	M_6=2/10	M_7=8/10	M_8=2/10

Figure 4.13: On-chip self-biased current reference [111]. Start-up circuitry is also shown. Transistor dimensions are shown in micrometers.

4.3 Experimental results

Fig. 4.15 shows a micro-photograph of the proposed HV-SCRC, fabricated in a standard 0.18 µm 1.8V/3.3V CMOS process. The circuit occupies an active area of 2.1 mm^2 and can be programmed though an internal Serial-Peripheral Interface (SPI) module. No external components are needed.

Depending on the experiment, the load current is generated either with an off-chip voltage-controlled current source (for the static characterization of the circuit), or with the on-chip neural stimulator (for evaluating the dynamic behavior of the converter). In the first case, the HV-SCRC is controlled by means of a Digilent Digital Discovery pattern generator. In the latter case, a micro-controller is used for implementing a Look-Up Table (LUT) which automatically maps the 128 combinations of the 16 target

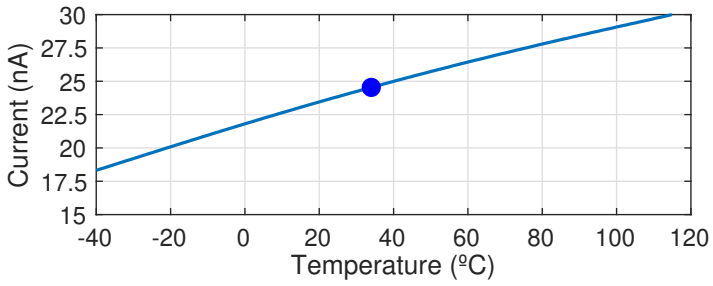


Figure 4.14: Current-temperature curve of the self-biased current reference, obtained from post-layout simulations.

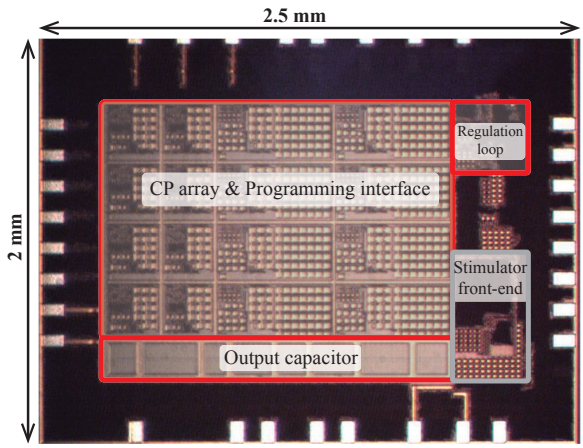


Figure 4.15: Microphotograph of the fabricated chip. The DC-DC converter occupies an active area of 2.1 mm^2.

output voltages and 8 target load currents –0-2 mA range divided into 8 intervals– to the number of active rows and columns. This LUT was generated from the insights given by Fig. 4.8, Fig. 4.9, and (4.3). Given that the micro-controller also shapes the current stimulation pulses, the HV-SCRC can be precisely programmed to adapt the number of active rows and columns to the stimulation current.

4.3.1 Open loop characterization

In this setup, the output of the regulation circuit is disconnected from the programming interface, the pumping clock is provided externally, and the average output voltage and efficiency of the HV-SCRC are measured under different conditions.

Fig. 4.16(a) shows the effect when the load current is swept from 0 to 4 mA for pumping frequencies of 12.5, 25 and 50 MHz. The number of activated rows and columns, M_a and N_a, are 4 and 1, respectively. As described in (4.6), the average output voltage decreases linearly with the load current, and the slope becomes steeper as the clock frequency decreases. Also, the load current for which the power efficiency is maximum increases with the clock frequency. Note that when the output voltage drops below roughly 4 V –i.e. the pumping voltage is below 1 V–, charge is not fully transferred by the CP-cell and the output voltage exhibits a more pronounce decrease with the load current.

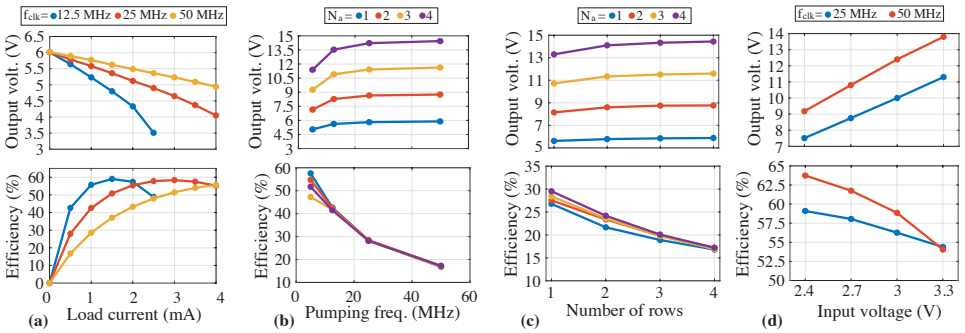


Figure 4.16: Open loop measurements. Parameters: (a) $M_a = 4$, $N_a = 1$, $V_{in} = 3\,\text{V}$; (b) $M_a = 4$, $I_{load} = 0.5\,\text{mA}$, $V_{in} = 3\,\text{V}$; (c) $f_{clk} = 50\,\text{MHz}$, $I_{load} = 0.5\,\text{mA}$, $V_{in} = 3\,\text{V}$; and (d) $M_a = 4$, $N_a = 4$, $I_{load} = 3.5\,\text{mA}$.

Fig. 4.16(b) illustrates the converter behavior when the pumping frequency, f_{clk}, is swept from 2.5 to 50 MHz for different numbers of activated columns N_a. In these plots, the number of activated rows is 4 and the load current I_L is 0.5 mA. Note that the output voltage tends asymptotically to V_0 as the pumping frequency increases, reaching 14.45 V for f_{clk}=50 MHz. Also, in agreement with (4.9), for a given load current, the power efficiency decreases with the pumping frequency from nearly 60% to 15%.

Fig. 4.16(c) shows the converter's performance for different number of activated rows and columns, M_a and N_a. Load current and pumping frequency are 0.5 mA and 50 MHz, respectively. The output voltage increases with the number of activated rows as a result of the decrease in the equivalent output impedance of the HV-SCRC, as shown in (4.4). However, the power efficiency decreases due to the higher number of switching elements, as stated in (4.9).

Fig. 4.16(d) shows the output voltage and efficiency in terms of the input voltage. As shown in (4.6), the output voltage linearly increases with the input voltage; however, the measured efficiency decreases due to the increasing power losses, as stated in (4.9).

Fig. 4.17 shows the operation of the HV-SCRC and the HV-FLSs for different enabled columns. The input voltage is 3 V, $I_L = 3\,\text{mA}$, M_a=4, f_{clk}=50 MHz, and $V_{pump} \approx 2.35\,\text{V}$. The HV-FLS clock frequency is 6.25 MHz. Fig. 4.17(a) shows the output voltage of the multi-stage charge pump, when the number of active stages N_a increases from 1 to 4 at 50 µs intervals. The different voltage levels agree with the values shown in Table 4.1. Similarly, Fig. 4.17(b-d)

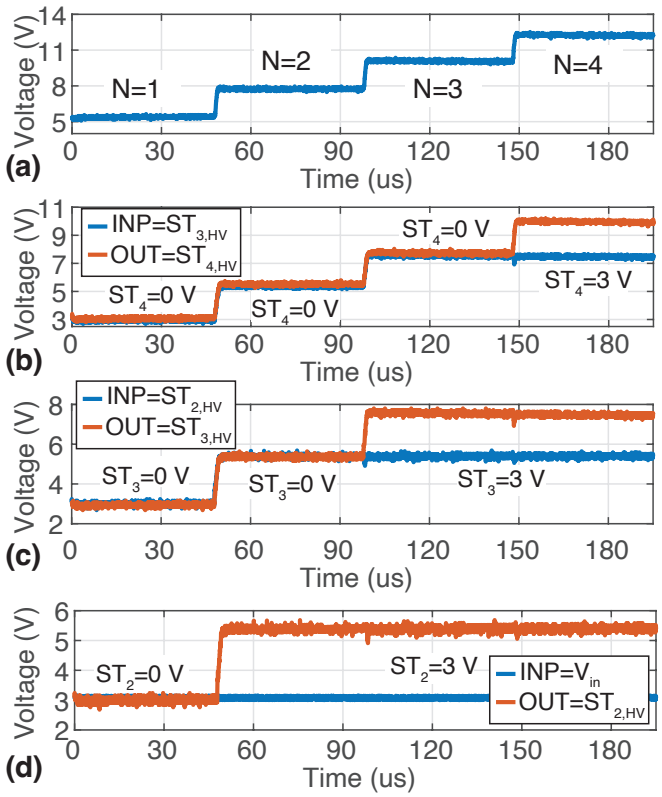


Figure 4.17: Experimental measurements with V_{in}=3 V, f_{clk}=50 MHz, M_a=4, and I_L=3 mA. Columns are successively enabled. (a) Output voltage. (b-d)) Level shifting voltage supply and output voltage of the HV-FLS driving the fourth/third/second columns, respectively.

shows the signals INP and OUT of the HV-FLS driving the fourth, third, and second CP columns, respectively, for the same time sequence of activated cells. Again, the level shifters update their outputs, $V_{c,2-4}$, according to the values previously discussed. When N_a changes, the signals settle after roughly 2 µs. This delay is essentially dominated by the internal dynamics of the charge pumps, which are much slower than the HV-FLS blocks.

Fig. 4.18 shows the response of the HV-SCRC and the HV-FLSs to a varying load current. In this case, M_a=N_a=4, f_{clk}=50 MHz, and the load current changes from 0.5 mA to 4 mA within 50 µs. From top to bottom, the oscilloscope screenshot shows V_{out}, $V_{c,4}$, $V_{c,3}$, and $V_{c,2}$. The voltage difference between adjacent signals is always V_{pump}, as discussed in (4.2). However,

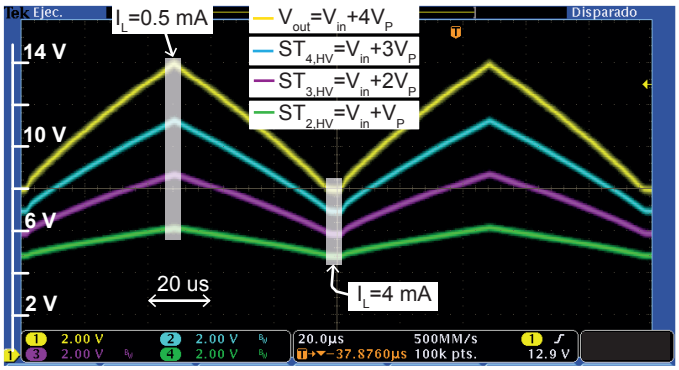


Figure 4.18: Experimental measurements for V_{in}=3 V, M_a=N_a=4, and f_{clk}=50 MHz. The load current is a 10 kHz triangular wave from 0.5 mA to 4 mA.

V_{pump}, and, hence, V_{out} varies with the load current. Namely, V_{out} changes from 13.6 V –for a load current of 0.5 mA– to 8 V –under a load current of 4 mA–. Even though the digital input of the floating level shifters do not change, thanks to the charge-refreshing topology, the HV-FLS successfully maintain their outputs $V_{c,2-4}$ at the correct level.

4.3.2 Closed loop characterization

In this setup, the pumping frequency of the CP array is internally controlled by the regulation loop; and the average output voltage, power efficiency, and output voltage ripple of the DC-DC converter are evaluated for all 16 possible values of *VREF*. Measurements are repeated for every combination of load currents (assuming discrete values of 0.5, 1.5, 3.5, and 4 mA) and input voltages (assuming discrete values of 3.0, 2.7, and 2.4 V).

The surface plot of Fig. 4.19(a) illustrates the circuit behavior for a 3 V input voltage. Row/column configurations have been selected for improving power efficiency. The DC-DC converter can deliver output voltages from 4.2 V up to 13.2 V depending on the load current. For a 4 mA load, the output voltage is 12.1 V and the power efficiency is 65%. For loads larger than 1.5 mA, the efficiency is above 50%. At lower values, the efficiency decreases to 35%. Fig. 4.19(b) illustrates the case for V_{in} = 2.7 V. The output voltage can be adjusted from 4.2 V up to 13 V and, hence, the VCR is comprised in the range 1.6-4.8 V/V. The peak power efficiency is 66%, obtained when the circuit delivers around 40 mW. Finally, Fig. 4.19(c) shows the operation for

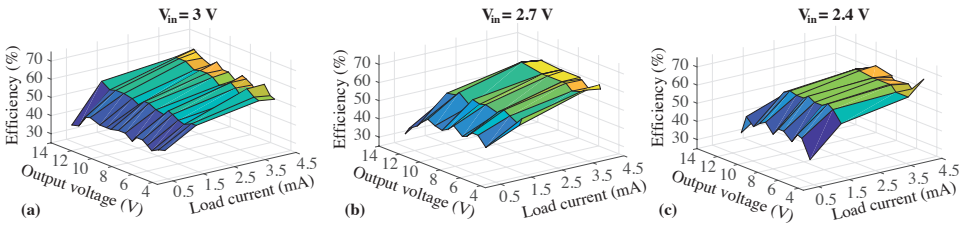


Figure 4.19: Closed loop measurements. Power efficiency for (a) $V_{in} = 3.0\,\mathrm{V}$, (b) $V_{in} = 2.7\,\mathrm{V}$, and (c) $V_{in} = 2.4\,\mathrm{V}$.

$V_{in} = 2.4\,\mathrm{V}$. The DC-DC converter outputs voltages from 4.2 V up to 11.7 V, and the efficiency stays above 40% in most of the operation points, reaching a local maximum of 67%, when driving a 4 mA load current at 8.6 V.

Using the same setup, output voltage ripple is measured rather than power efficiency, and the corresponding surface plots are shown in Fig. 4.20. In the case $V_{in} = 3.0\,\mathrm{V}$, illustrated in Fig. 4.20(a), the peak voltage ripple is measured at 3.5 mA load current and 11.4 V output voltage, where a ratio $\Delta V_{out}/V_{out,avg}$ of 2.4% is obtained. In the case $V_{in} = 2.7\,\mathrm{V}$, shown in Fig. 4.20(b), the peak ratio decreases to 1.4%, obtained at 4 mA load current and 10.4 V output voltage. Finally, when V_{in}=2.4 V (case shown in Fig. 4.20(c)), the peak $\Delta V_{out}/V_{out,avg}$ ratio further decreases to 0.9%, measured for V_{out}=8.6 V and I_L=4 mA. This decrease of the output voltage ripple with the input voltage can be explained through (4.2) and (4.7). Decreasing V_{in} increases the pumping clock frequency needed for reaching the target output voltage and, thus, ripples are smaller.

As discussed in Fig 4.9, the programmability of the charge-pump array extends the low side of the load current operation range. This is experimentally confirmed in Fig 4.21, which shows the output voltage, V_{out}, for different

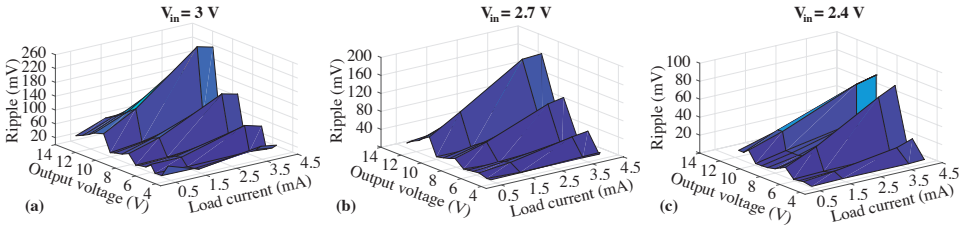


Figure 4.20: Closed loop measurements. Output voltage ripple for (a) $V_{in} = 3.0\,\mathrm{V}$, (b) $V_{in} = 2.7\,\mathrm{V}$, and (c) $V_{in} = 2.4\,\mathrm{V}$.

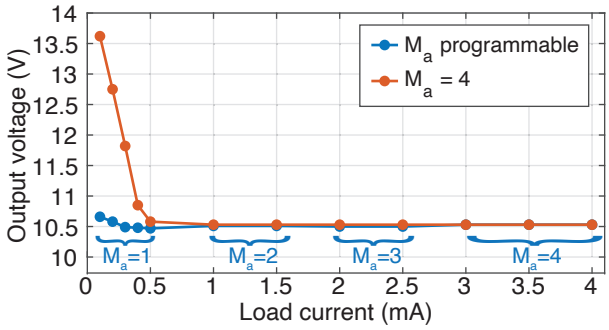


Figure 4.21: Closed loop measurements. Orange line represents the output voltage for M_a=4. Blue line represents the output voltage when M_a is adapted to the load current. $V_{in} = 3.0\,\text{V}$, *VREF = '1010'*, $N_a = 4$.

load currents ranging from 0.1 mA to 4 mA at *VREF = '1010'*. The plot compares a case in which $M_a = 4$ to a case in which the number of activated rows is programmed according to the current load. Note that for currents below 0.5 mA the converter with $M_a = 4$ is not able to regulate the targeted output voltage and large deviations occurs. Contrarily, when M_a is programmable, the circuit tolerates load currents as low as 0.1 mA with an average voltage deviation of 36 mV. This is in agreement with Fig 4.9. Furthermore, as discussed in Sec. II and captured by (4.7), flying capacitors of disabled rows contribute to reducing the voltage ripple by increasing the equivalent capacitance, C_{eq}.

Fig. 4.22(a) illustrates the use of the DC-DC converter together with the on-chip neural stimulator. It shows the output voltage response to a load current I_L that switches from 0.2 mA to 2 mA at a rate of 1 kHz. During the transitions, the configuration of the CP array changes from $M_a = 1$, $N_a = 4$ (for the low current level), to $M_a = 4$, $N_a = 3$ (for the high current level). Note that despite the large load change and the structural reconfiguration of the array, V_{out} variations remain below 0.3 V. Additionally, it can be observed that the regulation loop successfully stabilized the output voltage after around 6 µs.

Finally, Fig. 4.22(b) shows the output voltage transient response to a change in the target output voltage, *VREF*, for a load current of 1.5 mA. Each 40 µs, the target voltage is changed from '0000' to '1111'. The output voltage can reach the target within 5 µs.

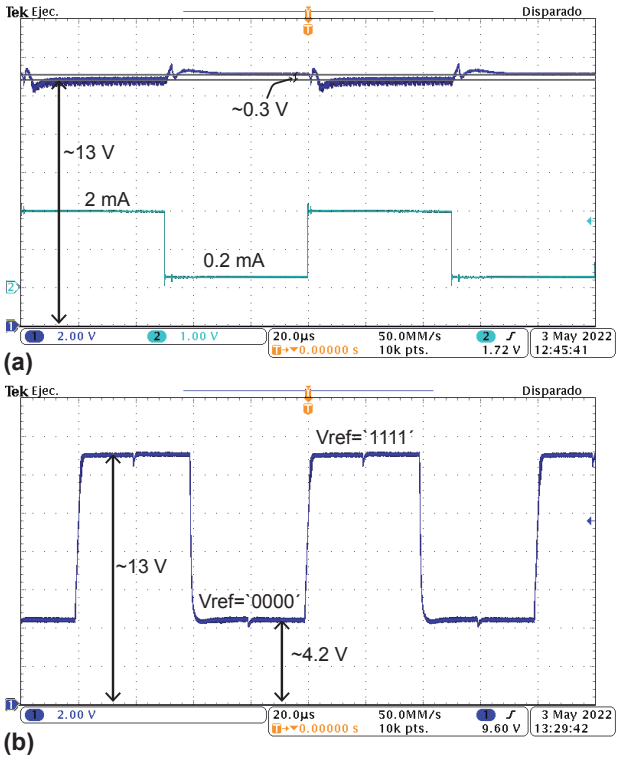


Figure 4.22: (a) Response of V_{out} to a switching I_L. (M_a, N_a) is set to (1, 4) under I_L=0.2 mA and to (4, 3) under I_L=2 mA. V_{in}=3 V, *VREF = '1111'*. (b) Response of V_{out} to a change in *VREF*. (M_a, N_a) is set to (2, 1) for *VREF = '0000'* and to (2, 4) for *VREF = '1111'*. V_{in}=3 V, I_L=1.5 mA.

4.3.3 State-of-the-art comparison

Table 4.2 summarizes the performance of the proposed HV-SCRC, together with other solutions proposed in the literature. Only a few reported HV DC-DC converters implemented LV CMOS processes are fully implemented on-chip [78], [101]–[103]. Compared to them, the proposed circuit can operate for different input voltages $V_{in} \in [2.4, 3.0]$ V, obtains higher output power and the occupied area is smaller than the work achieving similar delivered power [102]. Moreover, the efficiency when delivering maximum power is among the highest of the fully-on-chip solutions. Finally, the output voltage gets regulated under a wide range of load currents and the regulation loop is able to stabilize the output voltage within a few microseconds when the load current switches abruptly.

	[100]	[101]	[103]	[102]	[104]	[78]	**This work**
Process	0.18 µm LV	0.35 µm LV	0.18 µm LV	0.18 µm LV	0.18 µm LV	65 nm LV	0.18 **µm LV**
V_{out} (V_{in})	1.7-11.4 V (1.8 V)	7.5-16 V (2.5 V)	5-19.6 V (3.3 V)	3.3-12.6 V (3.3 V)	12.8 V (2.8 V)	11 V (0.5 V)	**4.2-13.2 V** **4.2-13.0 V** **4.2-11.7 V**
Load current	0.1-1 mA	0.1-25 µA	Up to 150 µA	0.5-3.5 mA	0.01-2 mA	Up to mA	**0.1-4 mA**
Maximum op. point	9.8 V@1 mA	11.5 V@25 µA	17 V@150 µA	10.8 V@3.5 mA	12.8 V@1 mA	11 V@2 mA	**12.1 V@**4 mA **10.2 V@**4 mA **8.6 V@**4 mA
Max. power (mW)	9.8	0.3	2.6	37.9	12.8	22	**48.4** **40.8** **34.4**
Efficiency at max. power	77%	32%	34%	60%	82%	31%	**65%** **66%** **67%**
Area (mm^2)	-	0.07	0.06	2.87	-	0.04	**2.10**
Capacitors	1.2 µF	18 pF	26.4 pF	400 pF	9 µF	-	**400 pF**
Fully on-chip	No	Yes	Yes	Yes	No	Yes	**Yes**
Regulated	No	Yes	Yes	Yes	Yes	Yes	**Yes**

Table 4.2: Performance comparison with previously reported HV DC-DC boost converters in LV CMOS process.

Chapter 5

High-Voltage Neural Stimulator Front-End

Abstract

In this chapter, the High-Voltage Neural Stimulator Front-End (HV-NSFE) shown in Fig. 1(b) is presented. In Section 5.1, the operation of a current-controlled biphasic stimulator is described, with an emphasis on the analysis of the compliance voltage and power efficiency. The architecture, components, and operation modes of the proposed HV-NSFE are described in Section 5.2. In Section 5.3, experimental results are presented and discussed.

5.1 Introduction

Figures 5.1(a-b) show the simplified schematics of a monopolar neuronal stimulator and a bipolar neuronal stimulator, respectively. They essentially work in two alternating phases. First, an anodic phase of T_{an} duration is established to inject charge immediately around the stimulation electrode A. Then, a cathodic phase of T_{ca} duration is set to restore the charge balance in the tissue prior to the stimulation. This is done to prevent charge accumulations that can lead to the generation of toxic chemicals or the corrosion of the electrodes [15]. Hence, if $I_{stim,an}$ and $I_{stim,ca}$ are the currents flowing through the ETI during the anodic and cathodic phases, the charges $Q_{an} = \int_0^{T_{an}} I_{stim,an}\, dt$ and $Q_{ca} = \int_0^{T_{ca}} I_{stim,ca}\, dt$ injected and extracted from the tissue, respectively, should have the same magnitude

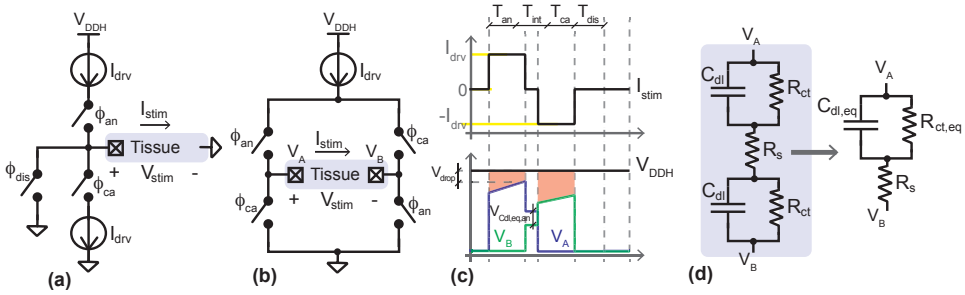


Figure 5.1: (a-b) Simplified schematics of unipolar and bipolar electrical neural stimulators. (c) Electrical model of the ETI and lumped model. (d) Current and voltage stimulation waveforms.

but different sign. Generally, the stimulation currents during the anodic and cathodic phases may have different waveforms and duration as long as $|Q_{an}| = |Q_{ca}|$; however, in this work we consider a typical case in which such currents are pulses of the same duration, $T_{an} = T_{ca}$ and the same magnitude, $|I_{stim,an}| = |I_{stim,ca}| = I_{drv}$.

Fig. 5.1(d) shows a simplified model of the equivalent impedance, Z_L, between the stimulation nodes A and B in the schematics of Fig. 5.1(b) [15], [115]. Such impedance is given by

$$Z_L(s) = R_s + \frac{R_{ct,eq}}{1 + s{\cdot}R_{ct,eq}{\cdot}C_{dl,eq}}, \tag{5.1}$$

where R_s models the spreading resistance of the neural tissue, $C_{dl,eq} = C_{dl}/2$ takes into account the electrical double-layer capacitance at the ETI, and $R_{ct,eq} = 2R_{ct}$ is an equivalent charge transfer resistance that models the faradaic electrochemical reactions at the electrode surface [15]. The voltage between the electrodes A and B, $V_{stim}(t) = |V_A(t) - V_B(t)|$, during the anodic phase (a similar analysis can be done for the cathodic phase) is given by

$$V_{stim}(t) = I_{drv}{\cdot}R_s + V_{C_{dl,eq}}(t), \tag{5.2}$$

where $t \in [0, T_{an}]$ and $V_{C_{dl,eq}}(t)$ is the voltage across the equivalent double-layer capacitance given by,

$$V_{C_{dl,eq}}(t) = I_{drv}{\cdot}R_{ct,eq} - (I_{drv}{\cdot}R_{ct,eq} + V_{C_{dl,eq},0}){\cdot}\exp\left(-\frac{t}{R_{ct,eq}{\cdot}C_{dl,eq}}\right), \tag{5.3}$$

where $V_{C_{dl,eq},0}$ is the $V_{C_{dl}}$ voltage stored at the beginning of the pulse and $\tau = R_{ct,eq}{\cdot}C_{dl,eq}$. Assuming that the time constant of the ETI is much

larger than the duration of the anodic phase, i.e. $T_{an} \ll \tau$ as it occurs in practice, the peak stimulation voltage between the electrodes at the end of the anodic phase ($t = T_{an}$) (preserved during the interphase delay period) can be approximated as,

$$V_{stim,pk} \approx V_{C_{dl,eq},0} + I_{drv}\left(R_s + \frac{T_{an}}{C_{dl,eq}}\right). \tag{5.4}$$

The efficiency η_{stim} of the neural stimulator during the anodic phase can be defined by the ratio between the energy delivered to the tissue and the energy supplied by the biasing voltage, V_{DDH}. Hence, assuming again that $T_{an} \ll \tau$, the following expression is obtained

$$\eta_{stim} = \frac{\int_0^{T_{an}} V_{stim}(t)\cdot I_{drv}\cdot dt}{\int_0^{T_{an}} V_{DDH}\cdot I_{drv}\cdot dt} \approx \frac{I_{drv}}{V_{DDH}}\cdot\left(R_s + \frac{T_{an}}{2\cdot C_{dl,eq}}\right), \tag{5.5}$$

which shows that the efficiency depends on the load impedance and the pulse characteristics. Clearly, the efficiency increases by reducing the supply voltage V_{DDH} up to the limit imposed by the peak stimulation voltage $V_{stim,pk}$ in (5.4). On the other hand, for a given V_{DDH} value, the efficiency and peak of the stimulation voltage decrease both with the amplitude and width of the current pulse and the stimulator may be forced to withstand a large voltage gap between the supply voltage and V_A. These considerations are taken into account in the proposed design.

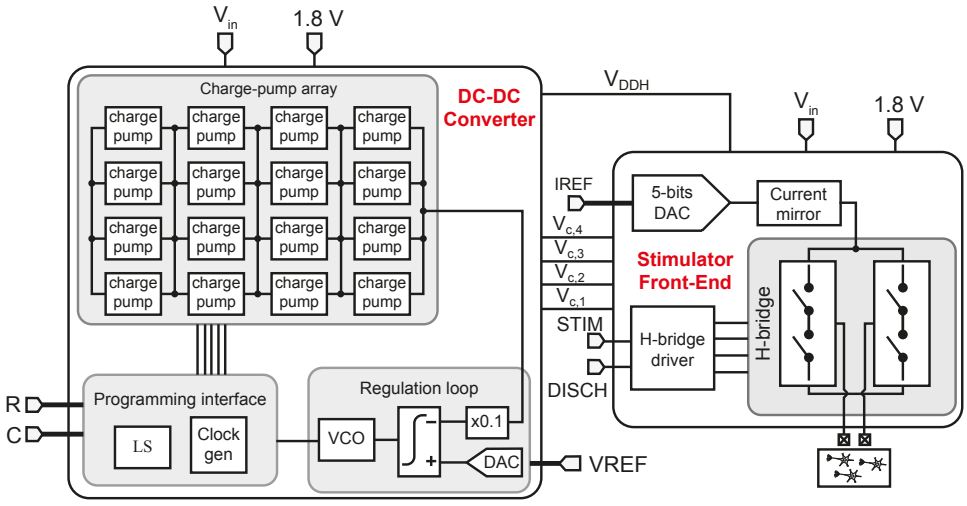


Figure 5.2: Block-level scheme of the proposed HV neural stimulator.

5.2 System architecture and circuit design

Fig. 4.1 shows the proposed HV-ENS, including the front-end stimulator block and the HV-SCRC. The stimulator front-end comprises: (1) a 5 bits current-steering Digital-to-Analog Converter (DAC), (2) a current mirror, (3) a high-voltage-tolerant H-bridge, and (4) an H-bridge driver. The HV-SCRC, presented in Chapter 4, supplies $V_{DDH} \in [4.2, 13.2]$ V and biases the stimulator front-end. The current mirror generates a current $I_{drv} \in [0.07, 2.08]$ mA which is then sourced/sunk to/from the load by the H-bridge in order to generate biphasic pulses. A proposed High Compliance Voltage Cell (HCVC) protects the circuitry from excessive voltage drops between transistor's terminals. As stated in Chapter 4, the biasing and reference generation circuits include a resistorless bandgap [111] and a 25 nA self-biased current reference [112] (not shown in Fig. 5.2 for simplicity).

5.2.1 H-bridge

Fig. 5.3 shows the proposed high-voltage-tolerant H-bridge. Each branch has one PMOS and one NMOS switch (driven by signals S_{Px} and S_{Nx}, respectively) as well as a HCVC. The HCVC consists of eight stacked transistors (shaded in green) and a dynamic gate biasing circuit [116], [117] (shaded in blue). The circuit allows powering the stimulator front-end with a wide range of voltages –up to 4 times the nominal voltage of the technology– while driving a wide range of ETI impedances and without damaging the 3.3 V stacked transistors.

The HCVC is designed to be biased with the voltages internally generated by the DC-DC converter, $V_{c,1-4}$. This way, no additional dynamic biasing circuitry is needed and the voltage operation range is extended compared to other solutions [117].

To describe the operation of the proposed high-voltage-tolerant H-bridge, two simulations were carried out. In both cases the load is purely resistive and $S_{P1} = V_{c,4}$, $S_{P2} = V_{DDH}$, $S_{N1} = 0$, and $S_{N2} = V_{in}$. Thus, the top-left and bottom-right switches are ON, whereas the top-right and bottom-left switches are OFF. In the first simulation, the voltage supply of the neural stimulator front-end is set to 13 V, $I_{drv} = 2$ mA, R_s is swept from 10 Ω to 5 kΩ, and $N_a = 4$ (i.e. $V_{c,1} = 3$ V, $V_{c,2} = 5.5$ V, $V_{c,3} = 8$ V, and $V_{c,4} = 10.5$ V). As shown in Fig 5.4(a), when $V_{stim} < V_{in}$, transistors P_{1-4} are saturated and they equally withstand the voltage across the H-bridge, limiting their maximum drain-to-source voltage to V_{in}. As V_{stim} increases,

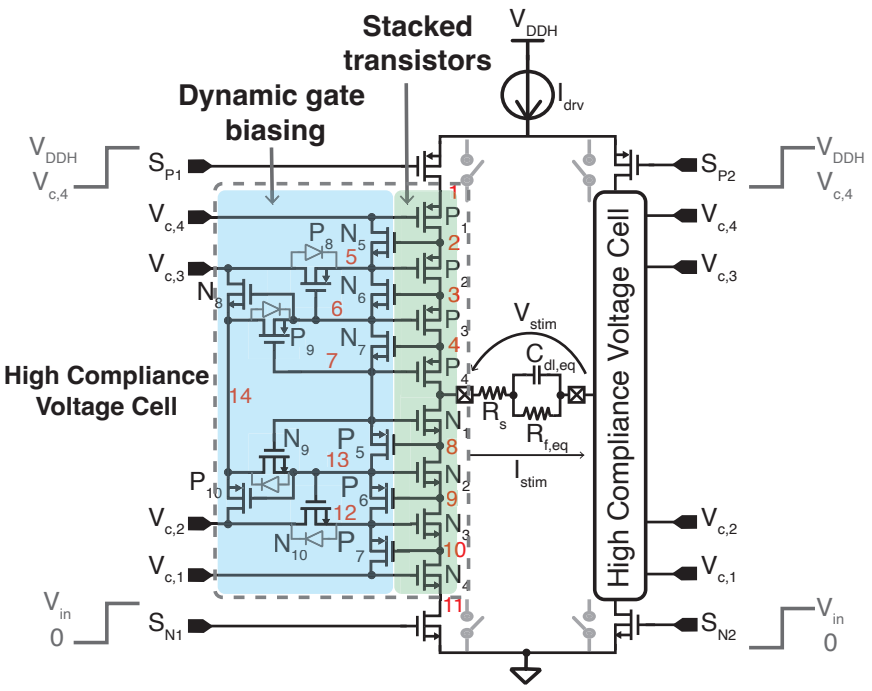


Figure 5.3: Proposed high-voltage-tolerant H-bridge, including the HCVC.

the voltage V_4 also increases, so transistor N_7 turns on, V_7 approaches V_6, and transistor P_4 enters in triode mode. As V_{stim} increases further, this behavior is sequentially repeated for voltage V_3, transistor N_6, voltage V_6, and transistor P_3, respectively; and then for voltage V_2, transistor N_5, voltage V_{B4}, and transistor P_2. Transistors P_8 (resp. P_9) ensure that nodes V_5 (resp. V_6) are gradually connected to $V_{c,3}$. Besides, as V_{stim} increases, transistor N_8 starts to turn on and continuously connects node 14 to $V_{c,3}$.

On the contrary, as shown in Fig 5.4(b), when $V_{out} < V_{in}$, transistors N_{1-4} act as closed switches –i.e. they are biased in the deep triode region– and, thus, $V_{8-11} \approx V_{in}$. As V_{stim} rises, so do V_{8-11}, thus switching P_{5-7} off. At the same time, N_{9-10} progressively make that $V_{12,13}$ approach $V_{c2,14}$, respectively. Thus, N_{1-4} gradually increase their drain-to-source voltage to a maximum drop of roughly V_{in}. Finally, opposite to N_8, transistor P_{10} starts biasing node 14 to $V_{c,2}$ and continuously switches off. The gate voltages of the stacked transistors, which permit proper biasing to adapt the stimulation voltage, is shown in Figure 5.4(c). In the second simulation, the voltage supply of the neural stimulator front-end is set to 7 V, $N_a = 2$.

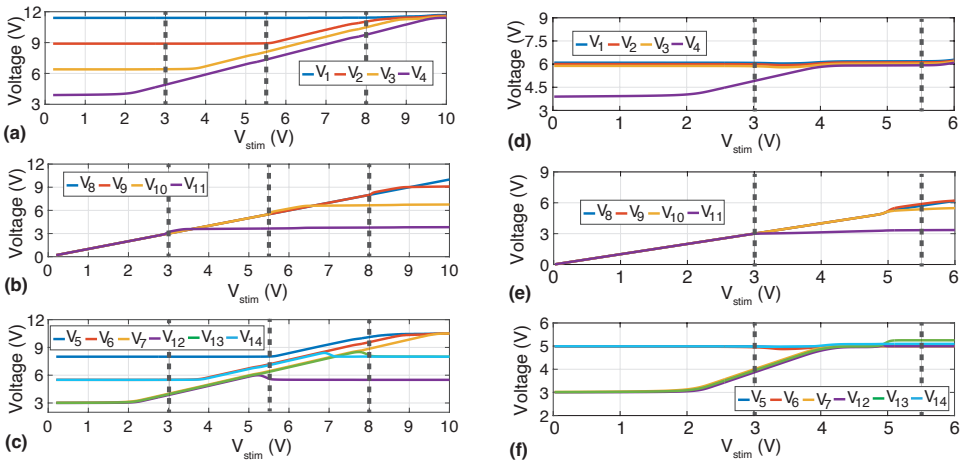


Figure 5.4: Evolution of the voltages at the nodes of the HCVC, as depicted in Fig. 5.3. (a-c) The load resistance, R_s, is swept from 0 to 5 kΩ, V_{DDH}=13 V, and $N_a = 4$. (d-f) The load resistance, R_s, is swept from 0 to 3 kΩ, V_{DDH}=8 V, and $N_a = 2$.

(i.e. $V_{c,1} = 3\,\text{V}$, $V_{c,2} = 5\,\text{V}$, $V_{c,3} = 5\,\text{V}$, and $V_{c,4} = 5\,\text{V}$), and $R_S = [0, 3]\,\text{k}\Omega$. In this case, as shown in Fig 5.4(d), when $V_{stim} < V_{in}$, transistors P_{1-3} are biased in deep triode region, whereas P_4 is saturated. Thus, now the voltage drop in the HCVC is approximately the source-to-drain voltage of P_4, which is around 2 V. As V_{stim} increases, P_4 gradually enters in deep triode region, leading to a voltage drop across the HCVC close to zero. Fig. 5.4(e) shows that transistors N_{1-4} are biased in the deep triode region and they sequentially enter in saturation as V_{stim} rises. As before, Fig 5.4(f) shows the gate voltages of the stacked transistors.

The simulations in Figure 5.4 show that the proposed H-bridge has two fundamental features. First, it withstands up to $4 \times V_{DD}$ voltage differences between input output nodes. Second, it acts as an H-bridge with low on resistance. Both behaviors manifest depending on the stimulation current, the supply voltage V_{DDH}, and the load impedance.

5.2.2 DAC and current mirror

Fig. 5.5 shows a schematic diagram of the 5 bits thermometric current-steering DAC supplied at 1.8 V, a PMOS current mirror with regulated cascode output supplied at V_{DDH}, and two HCVC.

Since the DAC was implemented with a thermometric topology, a mux-based 5-to-32 thermometer encoder [118] was designed for converting the binary input to the thermometric code. Output impedance was enhanced by means of a regulated cascode topology with a current-mirror OTA. The DAC outputs currents up to 15.6 µA with 0.5 µA steps from a 1.8 V power supply.

The floating current mirror has a gain of 128 and it implements a regulated cascode current mirror topology that achieves good output impedance, fast transient response, and uses no operational amplifiers [119]. The output impedance, $r_{out,CM}$, is

$$r_{out,CM} = g_{m3} \cdot r_{out3} \cdot g_{m4} \cdot (r_{out1} || r_{out4}) \cdot r_{out2}, \tag{5.6}$$

where the output impedance of the output transistor, r_{out2}, gets amplified by a factor $g_{m3} \cdot r_{out3} \cdot g_{m4} \cdot (r_{out1} || r_{out4})$. Besides, PMOS capacitors were added to reduce overshoots in the output current when switching. Since it is supplied at V_{DDH}, with no connections to the analog ground, it supports a wide range of V_{DDH}.

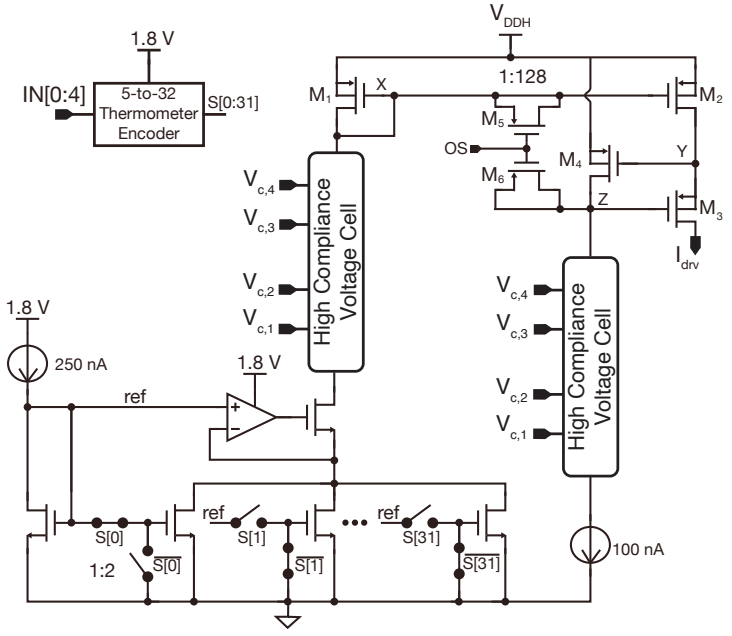


Figure 5.5: Schematic of the 5 bits current-steering DAC, current mirror, and two HCVCs for interfacing LV circuitry with HV circuitry. Biasing currents are copies of the on-chip 25 nA self-biased current source.

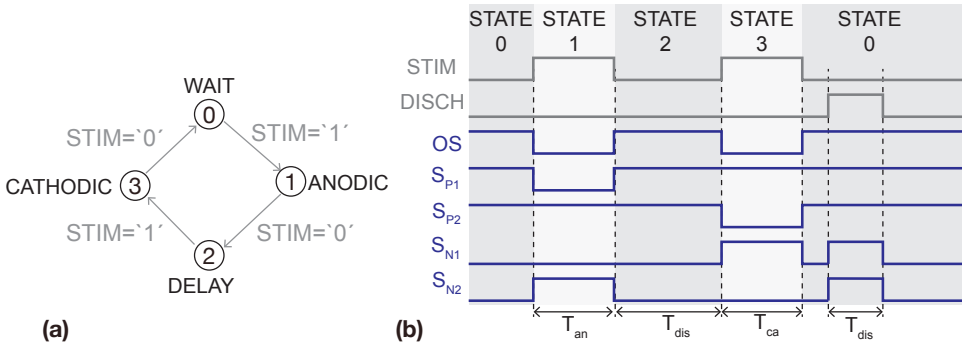


Figure 5.6: (a) Mealy's state machine implemented for driving the H-bridge. (b) Timing diagram of signals generated by the H-bridge driver.

5.2.3 H-bridge driver

The H-bridge driver converts the input signals *STIM* and *DISCH* to the four signals driving the H-bridge, $S_{P,1-2}$ and $S_{N,1-2}$, and to the signal reducing the current overshoot, *OS*. It consists of a Mealy's Finite State Machine –shown in Fig. 5.6(a)– and level shifters for adapting the signals to the adequate voltage level. Fig. 5.6(b) shows a timing diagram of these signals. The level shifters driving the PMOS switches of the H-bridge are implemented as HV-FLS.

5.3 Experimental results

The circuit was fabricated in a standard 0.18 µm 1.8V/3.3V CMOS process. Next, the setup and experimental characterization are detailed.

5.3.1 Setup

Fig. 5.7(a) shows a micro-photograph of the ASIC, fabricated in a standard 0.18 µm 1.8V/3.3V CMOS process. The circuit occupies an active area of 2.34 mm^2 –including the on-chip HV-SCRC (2.1 mm^2), HV-NSFE 0.15 mm^2, internal SPI module for communication, and other test circuitry–. No external components are needed.

Fig. 5.7(b-c) show a photography and a diagram of the testbench. The test board includes a nRF52832 micro-controller which communicates with a custom MATLAB GUI through USB, delivers control signals to the ASIC, and measures some ASIC's analog input/outputs. Electrical characterization

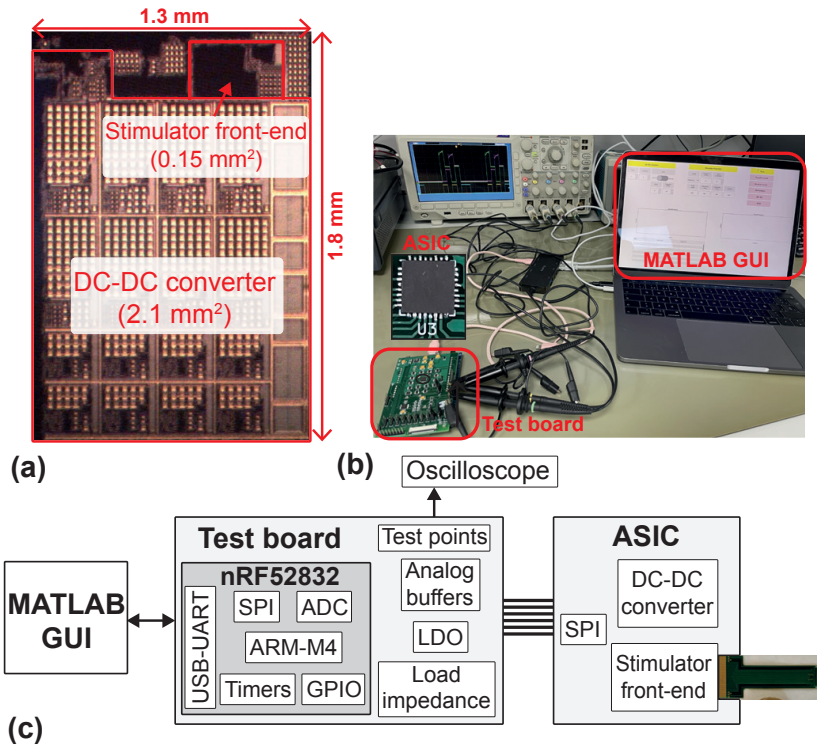


Figure 5.7: (a) Microphotograph of the ASIC with HV-NSFE and HV-SCRC highlighted. (b-c) Photography and block diagram of the testbench for characterization.

was done with a load impedance Z_L mounted on a test PCB (R_s=4.7 kΩ, $C_{dl,eq}$=330 nF, and $R_{ct,eq}$=40 MΩ).

Experimental measurements on a Phosphate-Buffered Saline (PBS) solution were also carried out. For this purpose, we designed two flexible μelectrode and μelectrode/μLED arrays, which are shown in Fig. 5.8. One includes 22 recording μelectrodes and 6 pairs of stimulation μelectrodes, while the other includes 28 recording μelectrodes and 6 μLED footprints. Both arrays were fabricated on a polyimide substrate, having 120 μm-width copper paths with 120 μm-diameter electrodes covered with gold.

5.3.2 Electrical characterization

Fig. 5.9(a,b) show the measured Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) of the neural stimulator. INL was calculated as

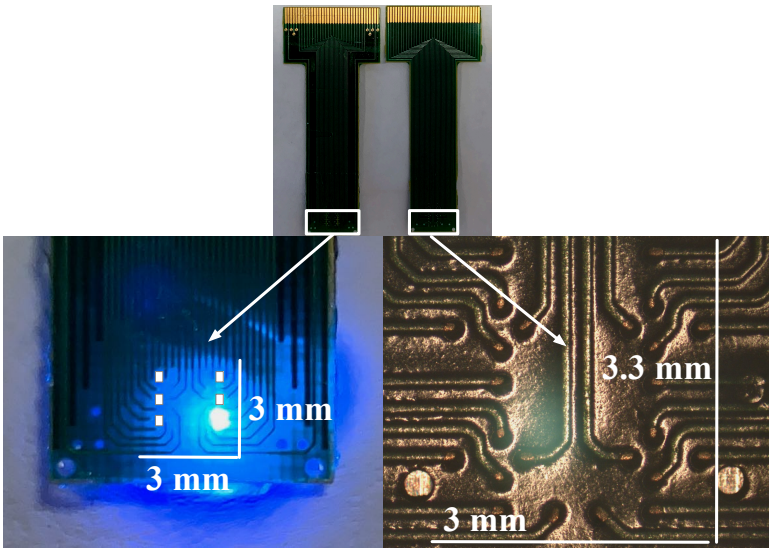


Figure 5.8: Photography of the micro-electrode arrays for cortical optogenetic/electrical stimulation and neural recording. Optical stimulation array with one µLED ON is zoomed, while the electrical stimulation array is displayed in a micro-photography. Active stimulation/recording area occupies an area of roughly 3x3 mm^2.

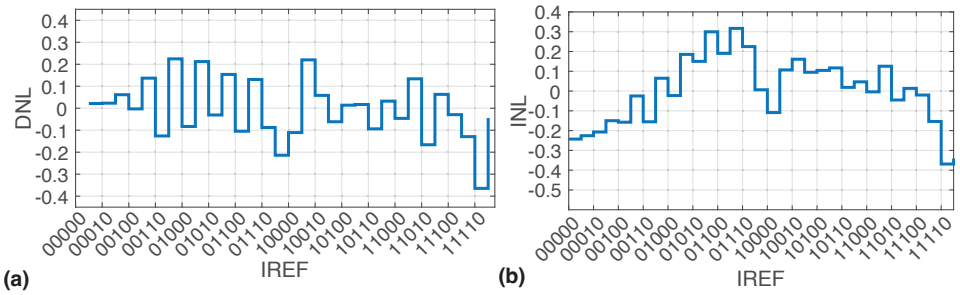


Figure 5.9: Measured stimulation current's DNL, as a fraction of one LSB for a 4.7 kΩ load and V_{DDH}=11 V. Maximum DNL and INL are 0.22 LSB and -0.19 LSB, respectively.

the deviation of the response from the best-fit straight line [120]. It can deliver currents from 69 µA up to 2.08 mA with a Least-Significant Bit (LSB) current of approximately I_{LSB}=65 µA. Given that V_{DDH} reaches 13.2 V, the stimulator can deliver a current of 2.08 mA to resistive loads close to 6.3 kΩ.

Fig. 5.10 depicts the residual voltage and residual charge stored at the double-layer capacitance for different stimulation currents. The residual voltage was measured by delivering 200 biphasic stimulation rounds with anodic/cathodic and interphase phases lasting 200 µs. Voltage at $C_{dl,eq}$ was sampled before the first stimulation round and after the 200-th stimulation round, then it was averaged. No discharging phase was triggered. The residual voltage remains below 1 mV for most of the stimulation current range. Expressed as a percentage of the charge delivered during each stimulation phase, the residual charge is less than 0.1% for most of the stimulation current range.

Fig. 5.11(a-b) illustrates the use of the discharging phase by electrode shorting to remove the residual voltage. A 2 mA current is delivered with $T_{an/ca} = T_{int} = 200\,\mu s$ and V_{DDH}=12 V. On the one hand, Fig. 5.11(a) shows both electrodes' voltage when no discharging phase is triggered. The 2 mA current causes an instant 9.4 V difference between electrodes when flowing through R_s=4.7 kΩ. Besides, the voltage stored at $C_{dl,eq}$=330 nF is 1.2 V, as expected by observing (5.3). Thus, after the anodic phase, both outputs remain halfway between V_{DDH} and ground, with a 1.2 V difference between them. Then, after the biphasic stimulation, both electrodes remain at a voltage around 6 V. In this point, the voltage difference between both outputs is in the range of milli-volts, as shown in Fig. 5.10. Hence, even with the zoomed screenshot, the residual voltage can not be accurately measured. On the other hand, Fig. 5.11(b) shows both electrodes' voltage when a 100 µs electrode shorting phase is triggered, which discharges both electrodes to ground. A

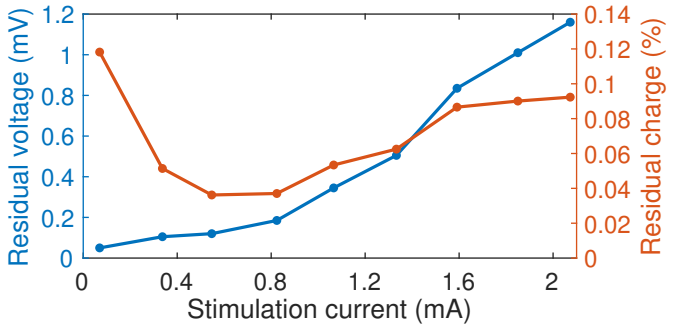


Figure 5.10: Measured residual voltage and residual charge stored at the double-layer capacitance C_{dl} with no discharging phase. $T_{an/ca}$=T_{int}=200 µs.

zoom of the electrode shorting phase is also included. Applying a discharging phase lasting more than 100 µs, the remaining residual voltage was below the LSB of the 12 bits ADC used in the measurements. Fig. 5.11(c-e) depict the electrodes' voltages and HV-SCRC's output voltage, V_{DDH}, in different scenarios. The area of regions shaded in red multiplied by the stimulation current represents energy losses at the stimulator front-end, as discussed in Fig. 5.1. Fig. 5.11(c) shows how the system handles the delivery of a stimulation current of roughly 2 mA to the load, with V_{DDH}=12.5 V. The

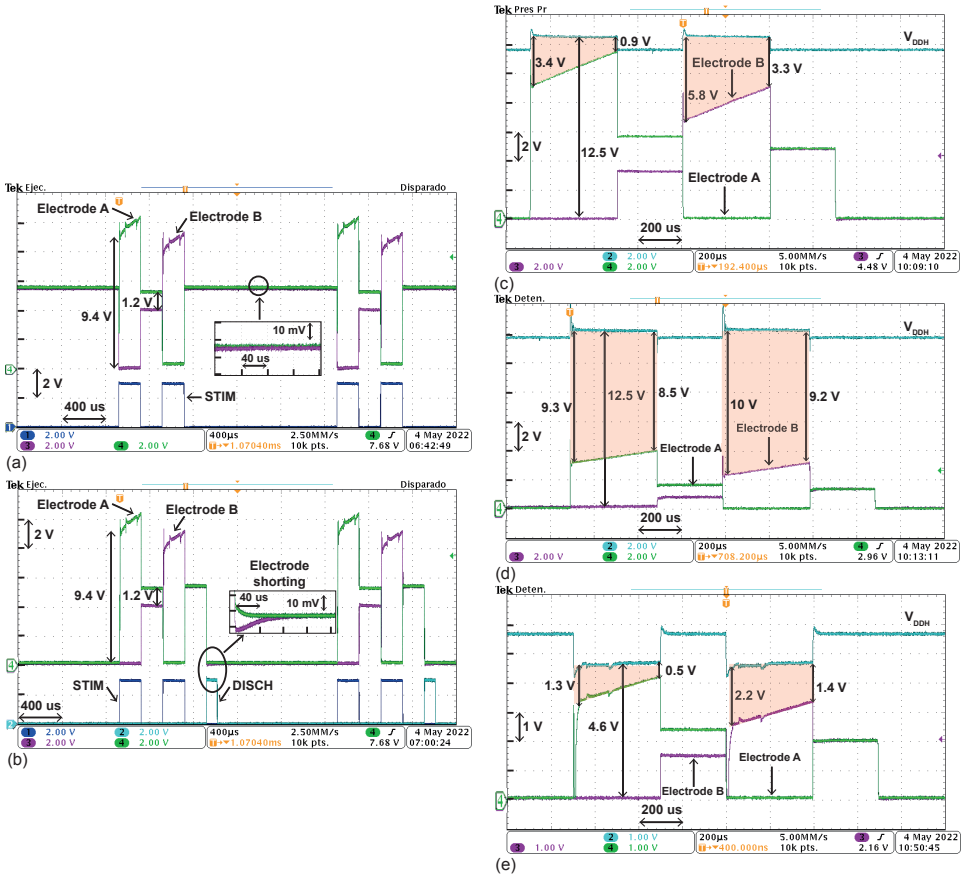


Figure 5.11: (a-b) Electrodes' voltages when a 2 mA stimulation current is delivered with/without electrode shorting phase. $T_{an/ca} = T_{int} = 200$ µs and V_{DDH}=12 V. (c-e) Electrodes' voltages and HV-SCRC's output voltage at different stimulation timing and currents. Voltage drop between V_{DDH} and stimulator's output is shaded in red.

voltage at electrode A goes from 9.1 V to 11.6 V. The stimulator front-end is thus capable of delivering a high stimulation current with a dropout voltage below 1 V while being supplied at a voltage 4 times higher than the nominal voltage supply of the technology.

Fig. 5.11(d) shows how the system handles the delivery of a stimulation current of roughly 0.7 mA to the load, with V_{DDH}=12.5 V. In this case, there is a large voltage drop from V_{DDH} to the electrodes. However, as discussed in Section 5.2 the HCVC maintains the voltage across all devices below 3.3 V.

Fig. 5.11(e) illustrates how the programmability of V_{DDH} improved power efficiency. The response of the system was measured again with I_{drv}=0.7 mA, but V_{DDH} was now set to 4.6 V. With this current level, the neural stimulator can operate with a voltage drop of 0.5 V.

Biphasic stimulation rounds were delivered for all the stimulation current values. Fig. 5.12(a) shows the stimulation voltage at the end of the anodic phase, $V_{stim}(t = T_{an})$ and the HV-SCRC's output voltage. The latter is programmed through the nRF52832 micro-controller. Fig. 5.12(b) depicts overall efficiency. Thus, DC-DC converter's power efficiency in the operation points shown in Fig. 5.11(c-e) is 58%, 46%, and 45%, respectively. This way, measured overall neural stimulator's efficiency, η_{stim}, was 48% at the operation point (V_{DDH}, I_{drv}) equal to (12.5 V, 2 mA); 13% at (12.5 V, 0.7 mA); and 36% at (4.6 V, 0.7 mA).

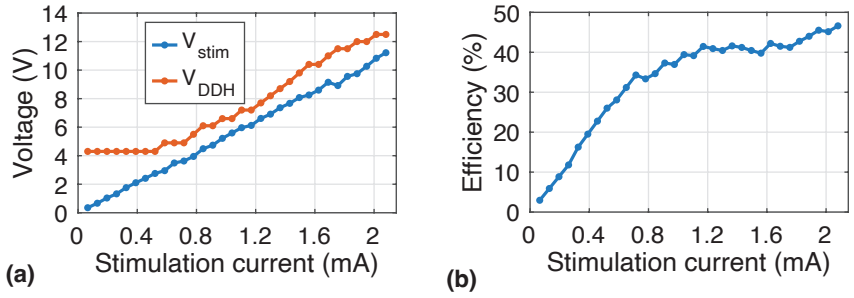


Figure 5.12: Electrical characterization. (a) Measured stimulation voltage at the end of the anodic phase and HV-SCRC's output voltage. (b) Measured overall efficiency.

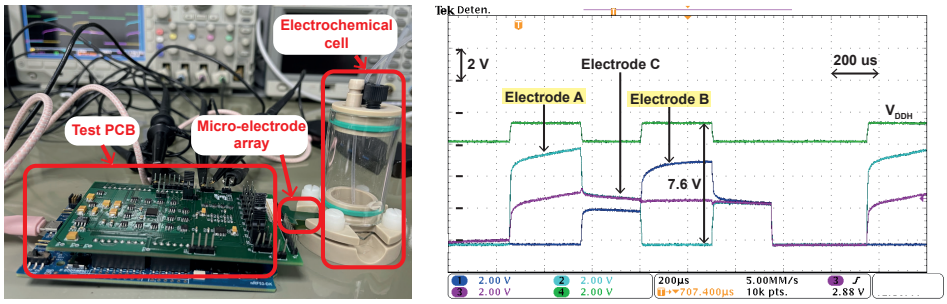


Figure 5.13: Electrodes' voltages when a 2 mA stimulation current is delivered to the Phosphate-Buffered Saline (PBS) solution.

5.3.3 Validation with a PBS solution

The neural stimulator was also characterized by immersing the custom µelectrode array into a PBS solution by means of an electrochemical cell, as depicted in Fig. 5.13(a). Fig. 5.13(b) shows the response when a 2 mA stimulation current is delivered between two electrodes separated roughly 600 µm away in the custom µelectrode array (A and B in the oscilloscope screenshot). Stimulation timing was configured as T_{an}=T_{ca}=300 µs, T_{int}=250 µs, and T_{dis}=200 µs. V_{DDH} is set at 7.6 V during stimulation and decreased to roughly 6.6 V between stimulation phases. From the curves of voltages at electrodes A and B, it can be seen that the response of the electrodes immersed in the PBS solution approaches a series resistance-capacitance circuit with $R_s \approx 2.3\,\text{k}\Omega$ and $C_{dl,eq} \approx 550\,\text{nF}$. Electrode C, also shown in Fig. 5.13, is located in the vicinity of electrodes A and B.

5.3.4 State-of-the-art comparison

Table 5.1 summarizes the performance of the proposed neural stimulator, along with other solutions proposed in the literature. Compared to the reported HV systems implemented in LV CMOS processes, the proposed neural stimulator achieves higher compliance voltage and wider V_{DDH} than any other reported solution. Besides, lower area/channel than [60], [78] was achieved. Finally, when delivering 2 mA of current, similar power efficiency as in [60] was obtained, whereas the 36% power efficiency obtained at 0.7 mA stimulation current outperforms that reported in the mentioned work.

	[60]	[75]	[78]	[79]	[62]	**This work**
CMOS Process	0.18 µm 1.8V/3.3V	0.18 µm 24 V	65 nm LV	0.25 µm 2.5V/5V/12V	0.18 µm 1.8V/3.3V	0.18 µm 1.8V/3.3V
V_{DDH} gen.	6.7-12.3 V (4b)	Up to 22.5 V	11 V	20 V	±6 V	**4.2-13.2 V (4b)**
V_{DDH} gen. area	1.5 mm^2	Off-chip	0.04 mm^2	1.64 mm^2	-	2.1 mm^2
Stim. current	2.48 mA (5b)	48.4 µA (7b) 169.5 µA (7b)	2 mA (8b)	5 mA (6b)	3 mA (4b)	**2.08 mA (5b)**
Area/channel	1.5 mm^2	-	0.36 mm^2	0.22 mm^2	0.08 mm^2	0.15 mm^2
Compliance voltage	11 V	21.3 V	11 V	16.7 V	3.6 V	**12.5 V**
Max. Q_{res}/Q_{stim}	1.7%	0.03%	-	-	1.94%	**0.12%**
Power efficiency	48% (2 mA,10 V) 32% (1 mA,6.7 V)	-	31% (2 mA) 28% (1 mA)	-	-	**48% (2 mA,11.6 V)** **36% (0.7 mA,4.6 V)**

Table 5.1: Performance comparison with previously reported HV neural stimulators.

Chapter 6

Conclusions

In this thesis, the design of a high-voltage neural stimulator with on-chip power management has been presented. Besides, preliminary work regarding the wireless transmission of power and data to/from the neural implant was tackled. In the mixed-signal ASIC design field, novel circuit solutions for the implementation of a high-voltage tolerant circuits in a standard 1.8V/3.3V CMOS process were shown and discussed. Furthermore, the wireless transfer of power and data to/from the neural implant has been investigated.

A remarkable innovation of this work relies in the wide range of voltage supplies that the neural stimulator front-end can handle: from 4.2 V up to 13.2 V. For this purpose, a voltage-adaptive cell based on stacked transistors with dynamic gate biasing has been proposed. This cell can dynamically adjust its impedance in order to withstand large voltages or act as a closed switch, as needed. The generation of the front-end's voltage supply and the biasing of the voltage-adaptive cell is done in an on-chip regulated switched-capacitor DC-DC converter.

The proposed regulated switched-capacitor DC-DC converter can output voltages from 4.2 V up to 13.2 V and deliver currents from 0.1 mA up to 4 mA. Efficiency, load current range, and load regulation were improved by implementing a novel charge-pump array. This topology allows the programming of the equivalent output resistance and equivalent output capacitance of the DC-DC converter with two additional parameters: the number of activated rows and the number of activated columns. This way, the operation range of the DC-DC converter is expanded. Besides, most of the operation points can be reached by either maximizing efficiency or maximizing output

voltage ripple, overall achieving a quite versatile circuit.

At the circuit-level, a charge-pump cell which has three operation modes –PUMP, BYPASS, and DISABLED– has been proposed. This cell allows the implementation of the programmable charge-pump array. Besides, a floating level shifter with charge refreshing has also been proposed. This circuit was implemented in different sub-blocks of the DC-DC converter, as well as in the neural stimulator front-end. Its fundamental features are: high-voltage tolerant operation, tracking of the low-supply rail, and handling of non-periodical input signals.

Implementing a system withstanding voltages 4 times higher than the nominal voltage involved several layout techniques and considerations. Some of them are listed here:

- Distances between same-layer metal paths should be N times larger than the minimum stated in the design rules of the technology, where N is the maximum expected voltage difference between both metal paths divided by the nominal supply of the technology [121].
- Chip pads connected to internal high-voltage nodes shall not be connected to standard ESD I/O cells. Instead, custom high-voltage-tolerant ESD cells should be implemented.
- Both the HV-SCRC and the HV-NSFE run currents over one milliampere. Thus, current densities have to be taken into account when drawing metal paths [122].
- Switched-capacitors implemented as MIM structures which are floating between high-voltage levels should not be placed above MOS devices. This might cause large charge injections to MOS devices.

Concerning the wireless transfer of power and data, preliminary research were conducted in two fields: CMOS photovoltaic solar cells and inductive links. A CMOS photovoltaic solar cell with a novel stacked-diode configuration was designed, fabricated, and experimentally characterised. This work was done under the supervision of Prof. Juan Antonio Leñero and it allowed us to quantify the power that can be extracted from this standard 1.8V/3.3V CMOS process. Besides, the use of the stacked-diode configuration for CMOS image sensor applications was also investigated. In the inductive links field, a system topology for the Mbps-data and mW-power transfer over a single-pair of coils was proposed. This work was carried out at the Swiss Federal Institute of Technology Lausanne (EPFL), under the

supervision of Prof. Alexandre Schmid. This topology has the potential of overcoming the drawbacks of using a single-pair of coils while keeping the main advantage: its reduced size.

6.1 Future works

Neural stimulator front-end's area might be reduced by synthesising the digital control block instead of implementing it as a full-custom circuit. Also, long-term electrical characterization might be performed in order to check the ASIC's temperature when delivering maximum stimulation currents. Finally, for implementing a multi-channel neural stimulator, different circuit-level power saving techniques should be considered to minimize standby power consumption as much as possible.

Besides, a feedback loop which monitor stimulation electrodes' voltages and accordingly program the output voltage of the HV-SCRC for maximizing power efficiency and/or voltage ripple might be designed and implemented on-chip.

Regarding the wireless transfer of power and data, the presented inductive-link system topology shall be implemented in silicon. This endeavour is probably a thesis-length work itself and it will bring circuit-level issues and challenges that should be solved. Besides, implementing a CMOS photo-voltaic cell in a specialised technology might be devised to keep exploring the possibility of performing light harvesting.

Other research opportunities that arise include (1) the implementation of a digital bio-processor for controlling the stimulator front-end and the versatile DC-DC converter, depending on the recorded neural signals and (2) the implementation of these circuits in a bio-compatible millimeter-sized system.

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David Palomeque Mangut

Seville, Spain
dpm0209@icloud.com

Interests Analog/Mixed-Signal ASIC Design — Embedded electronics

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Experience

Axelera AI – ***Mixed-Signal ASIC Designer*** – July 2022 to Present

- Designing mixed-signal circuits for In-Memory Computing solutions.

Seville Institute of Microelectronics (IMSE-CNM); Seville (Spain) – ***PhD Candidate (Analog/Mixed-Signal ASIC Designer)*** – June 2018 to July 2022

- Thesis title: High-Voltage Compliant Neurostimulator With On-Chip Power Management in Standard CMOS Technology.
- Advisors: Dr. Manuel Delgado Restituto and Prof. Ángel Rodríguez Vázquez.

University of Seville; Seville (Spain) – ***Lecturer*** – October 2019 to June 2022

- Lecturer in electronics and engineering subjects in the Faculty of Physics and the Higher Technical School of Engineering of the University of Seville.

Swiss Federal Institute of Technology Lausanne (EPFL); Lausanne (Switzerland) – ***Guest PhD Student*** – September 2021 to December 2021

- Advisor: Prof. Alexandre Schmid.

BioBee Technologies S.L.; Badajoz (Spain) – ***R&D Electronic Engineer*** – January 2018 to March 2018

- Developed Android applications and back-end Python scripts for processing data obtained with the company's electrical bioimpedance-based technology.

University of Extremadura; Badajoz (Spain) – ***Junior Analog ASIC Designer*** – January 2016 to December 2017

- Advisor: José Luis Ausín.

University of Extremadura; Badajoz (Spain) – ***Research Scholar*** – September 2015 to November 2015

- Advisors: Prof. Raquel Pérez-Aloe and Prof. Miguel Ángel Domínguez.

Education

University of Seville; Seville (Spain) – ***PhD in Electronic Physics (Mixed-Signal IC Design)*** — October 2018 - September 2022 (Expected)

University of Extremadura; Badajoz (Spain) – ***MEng in Industrial Engineering Research*** — 2015-2016; 9.4/10 (with honors)

University of Extremadura; Badajoz (Spain) – ***BEng in Electronics and Control Engineering*** — 2011-2015; 8.1/10 (with honors)

Skills

ASIC/FPGA Design

- Mixed-Signal ASIC design: Cadence's Virtuoso Analog Design Environment, Virtuoso Layout Suite and Virtuoso AMS Designer. ASIC verification with Siemens' Calibre Design Solutions. Also strong background with PSPICE, OrCAD, and LTSpice.
- Digital ASIC design, verification and implementation: Cadence's Genus/Innovus/SimVision.
- FPGA design (minor experience): designed a MIPS-based microprocessor and implemented it on a Xilinx FPGA (ISE Design Suite and Vivado). Also worked with a MicroBlaze processor.
- Hardware Description Languages, specially Verilog.
- System-level modeling and simulation with Verilog-AMS and MATLAB Simulink/Simscape.
- Experience with laboratory equipment for testing/characterizing mixed-signal ASICs.
- Some experience in PCB design with KiCAD.

Software/firmware

- Programming/scripting languages: Python, MATLAB, C, R, Assembly, Java.
- Minor experience implementing fuzzy logic algorithms, neural networks, support vector machines, and genetic algorithms with R and MATLAB.
- Experience in the development of firmware for ARM-based MCUs and Microchip's PIC in C and Assembly languages.

Others

- Fluency in English language: Certificate in Advanced English from the University of Cambridge (C1 level CEFR); some scientific papers written; presented works at English-speaking international conferences/symposiums. Learning French.

Publications

Journal article

Palomeque-Mangut D, Rodríguez-Vázquez A, and Delgado-Restituto M. *A 4.2-13.2 V, On-Chip, Regulated, DC-DC Converter in a Standard 1.8V/3.3V CMOS Process.* Sent to AEUE - International Journal of Electronics and Communications, 2022.

Journal article

Palomeque-Mangut D, Rodríguez-Vázquez A, and Delgado-Restituto M. *A Fully Integrated, Power-Efficient, 0.07-2.08 mA, High-Voltage Neural Stimulator in a Standard CMOS Process.* Accepted at Sensors, 2022.

Journal article

Palomeque-Mangut D, Rodríguez-Vázquez A, and Delgado-Restituto M. *A High-Voltage Floating Level Shifter for a Multi-stage Charge-Pump in a Standard 1.8V/3.3V CMOS Process.* Accepted at AEUE - International Journal of Electronics and Communications, 2022.

Congress paper

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Congress paper

Palomeque-Mangut D, Schmid A, Rodríguez-Vázquez A, and Delgado-Restituto M. *Electrical Model of a Wireless mW-Power and Mbps-Data Transfer System Over a Single Pair of Coils.* Int. Conference on PhD Research in Microelectronics and Electronics (PRIME), 2022.

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Journal article
Gómez-Merchán R, Palomeque-Mangut D, Leñero-Bardallo JA, Delgado-Restituto M, and Rodríguez-Vázquez A. *A Comparative Study of Stacked-Diode Configurations Operating in the Photovoltaic Region.* IEEE Sensors Journal, 20 (16), 2020.

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Palomeque-Mangut D, Ausín JL, and Duque-Carrillo F. *Comparative Study of CMOS Lock-In Amplifiers for Wideband Bioelectrical Impedance Measurements.* IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2016.

Awards

PhD Fellowships
Fellowship from the Spanish Government's for funding my research stay at EPFL (2021).
Fellowship from the Spanish Government's FPU program for funding my PhD (2019).
Fellowship from the University of Seville's PhD program for funding my PhD (2018).

Student Award — University of Extremadura, MEng. Sep 2016
Outstanding Graduate Award. Top of the class.
Outstanding Final Project Award.

Student Award — University of Extremadura, BEng. Sep 2015
Outstanding Undergraduate Award. Top of the class.
Outstanding Final Project Award.