±0.25-V Class-AB CMOS Capacitance Multiplier and Precision Rectifiers

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***Abstract*— Reduction of minimum supply requirements is a crucial aspect to decrease the power consumption in VLSI systems. A high-performance capacitance multiplier able to operate with supplies as low as ±0.25 V is presented. It is based on adaptively biased class-AB current mirrors which provide high current efficiency. Measurement results of a factor 11 capacitance multiplier fabricated in 180-nm CMOS technology verify theoretical claims. Moreover, low-voltage precision rectifiers based on the same class-AB current mirrors are designed and fabricated in the same CMOS process. They generate output currents over 100 times larger than the quiescent current. Both proposed circuits have 300-nW static power dissipation when operating with ±0.25-V supplies.**

***Index Terms*— Capacitance multiplier, class-AB current mirror, low supply voltage, precision rectifiers.**

I. Introduction

INCREASING demand for low-voltage/low-power VLSI systems aimed to portable and biomedical devices mandates a reduction of their minimum supply voltage requirements [$V_{supplymin} = (V_{DD} - V_{SS})_{min}$] and low quiescent current. Furthermore, a low-voltage operation is a requirement in modern CMOS technologies that operate with subvolt supplies ($V_{DD} < 1$ V). Current-mode (CM) systems where input–output and intermediate variables are defined as currents [1] are well suited to very low supply voltages. They often require a low-voltage linear operational transconductance amplifier (OTA) for voltage-to-current conversion as an interface between the external input voltage signals and the internal input current signals required by CM systems. Several approaches to implement low-voltage OTAs have been reported [2], [3].

Capacitance multiplication is used frequently to reduce silicon area requirements in VLSI systems [4]–[15]. In capacitance multipliers (Cap-Mlts), an equivalent capacitance

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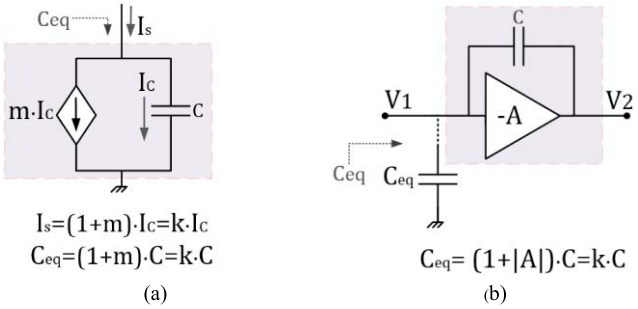


Fig. 1. Capacitance multiplier approaches [5]. (a) Current-mode. (b) Voltage-mode.

$C_{eq} = kC$ is achieved using active devices. Parameter k is the capacitance multiplication factor and C is the base (physical) capacitance. There are two basic approaches for capacitance multiplication: CM [Fig. 1(a)] [4] and voltage mode (VM) [Fig. 1(b)] [5]. In CM capacitance multiplication [Fig. 1(a)], the capacitor current I_c is replicated by a factor m current mirror whose output is connected to the signal terminal driving the capacitor C. This results in a source current $I_s = (1+m)I_c$ corresponding to an equivalent capacitance C_{eq}

$$C_{eq} = (1 + m)C = kC. \tag{1}$$

Fig. 1(b) shows a VM capacitance multiplier based on the Miller effect. It uses an active component (inverting amplifier with gain $|A|$). The resulting equivalent capacitance of Fig. 1(b) is

$$C_{eq} = (1 + |A|)C = kC. \tag{2}$$

Note that the capacitance multiplication factors for CM and VM systems are $k = 1+m$ and $k = 1+|A|$, respectively. CM capacitance multiplier based on current mirrors is preferred over VM capacitance multiplier as they are simpler and can operate with very low supply voltages thanks to the very low swing at their internal nodes. For this reason, their minimum supply voltage corresponds to the supply requirement of the mirror and the current source driving them. They are also very fast since they are feedforward circuits with only low-impedance nodes (high-frequency poles) in the signal path. On the other hand, VM circuits have higher supply requirements since they require at least the voltage signal swing plus the headroom of input differential pair if an op-amp is used to implement the inverting amplifier with gain $|A|$. In addition, in the Miller-based VM capacitance multiplication, since a

small amplitude voltage signal V_1 might result in saturating the output of the amplifier (V_2), the dynamic range is significantly limited by k. In order to avoid distortion caused by the saturation of the output node of the amplifier, the maximum input voltage signal at V_1 is limited by the gain A of the amplifier used as Miller multiplier to a value $V_{1p-pMAX}$ given by

$$V_{1p-pMAX} = \frac{V_{swing}}{|A|} \tag{3}$$

with V_{swing} being the maximum output swing of the amplifier. This implies that large $k = 1 + |A|$ values only allow very small voltage signals at node V_1 of C_{eq}. Another disadvantage of VM capacitance multiplier is that due to feedback the amplifiers' bandwidth (BW) decreases with gain A (consequently k) resulting in a reduction of the effective frequency range of the capacitance multiplication.

As mentioned earlier, CM capacitance multiplier is based on current mirrors [8]–[12] or OTAs [13]–[15]. In both cases, the maximum output current of a class-A circuit is limited by the bias current of the output branch I_{outQ}. This can impose a serious slew rate (SR) and dynamic range limitation on the speed/amplitude of the signals applied to C_{eq} and also on the maximum achievable value of k. Assuming sine-wave voltage signals with peak amplitude A_p and frequency f, the peak current I_{cMAX} applied to a capacitance $C_{eq} = kC$ is given by the following equation:

$$I_{cMAX} = 2\pi f A_p kC = 2\pi f A_p C_{eq}. \tag{4}$$

On the other hand, I_{cMAX} is limited by I_{outQ} in a class-A structure and can impose a severe limitation on any of the parameters A_p, f, or k. For example, for $I_{outQ} = 10$ μA, $f = 100$ kHz, $k = 50$, and $C = 20$ pF ($C_{eq} = 1000$ pF), the maximum amplitude of the voltage signal that can be applied to C_{eq} is only $A_p \approx 16$ mV. Operation at higher frequencies results in lower amplitudes or high distortion due to SR limitation. In order to overcome this limitation, in a class-A circuit, the quiescent current and correspondingly the static power dissipation (P_{diss}) have to be increased. Class-AB circuits allow peak input–output currents which depending on their current efficiency (CE) can be much higher than the bias current. The CE can be defined as the ratio of the maximum output current signal I_{outMAX} to the total supply quiescent current $I_{supplyQ}$

$$CE = \frac{I_{outMAX}}{I_{supplyQ}}. \tag{5}$$

A high CE allows extending the maximum capacitance multiplication factor k for a given input signal amplitude/frequency range without increasing the quiescent power dissipation.

The CM capacitance multiplier circuit in [10] is based on self-biased class-AB current mirrors and has relatively large supply requirements ($V_{supplymin} = 3V_{GS}$) and a poorly controlled quiescent current which is strongly dependent on the supply voltage and temperature variations. Another class-AB CM capacitance multiplier was reported in [11], which uses two independent input stages and two capacitors C which degrade the power/area/CE. In addition, since the output stage is not cascoded, the output resistance (which is in parallel with C_{eq}) is relatively low and decreases significantly for high output currents. This results in a degradation of the quality factor Q of C_{eq} and a narrower operating frequency range over which dominant capacitive behavior is observed (see discussion in Section II). In addition, the lack of cascode transistors results in poor copying accuracy, distortion, and large input dc offset currents which are signal dependent.

Rectification is one of the basic nonlinear functions in analog VLSI systems [16]. It is used in applications such as ac voltmeters, dc converters, peak detectors, piecewise linear function fitting, and CMOS RF demodulation. Especially, low-voltage precision rectifier circuits have a number of applications such as envelope detectors, and biomedical devices. In such systems, precision rectifiers play an important role in converting a received ac signal to a dc signal. Implementations of several precision rectifiers have been reported in the literature mostly based on op-amps and current mirrors [17]–[31]. The limited gain BW and SR of op-amps are their main drawback for their utilization in precision rectifiers. On the other hand, as stated earlier, current mirrors are feedforward systems with only low-impedance nodes, and for this reason, they can have higher BW and provide higher speed if they are used in precision rectifiers [30]. However, if these current mirrors are not cascoded, the accuracy and linearity are seriously affected [19], [30], [31]. On the other hand, cascode transistors increase the minimum supply requirements of the current mirror and limit the maximum output currents.

In this paper, the implementation and experimental validation of a low-voltage CM capacitance multiplier are presented. It is based on a high-performance class-AB current mirror that can operate with very low supplies. In addition, the same mirror is used for the implementation of low-voltage CM precision rectifiers with very high CE.

In Section II, the proposed CMOS class-AB CM capacitance multiplier and precision rectifiers are implemented and discussed. Section III shows the simulation and experimental results of circuits designed and fabricated in 180-nm CMOS technology. Summary and conclusions are given in Section IV.

II. Proposed Schemes

The input–output currents of the conventional class-A current mirror are limited by their bias currents I_{bias}. The circuit shown in Fig. 2 is a class-AB current mirror which overcomes this limitation by generating output currents that can be essentially larger than I_{bias}. It has biasing and cascode voltages V'_{bp}, V'_{cp}, and V'_{cn} that adapt dynamically to the ac input current I_{inp}. This is possible using quasi-floating gate (QFG) techniques [32] based on the inclusion of large time constant RC networks formed by capacitors $C_{1,2,3}$ ($\sim$pFs) and very large resistances R_{QFG}($\sim$10 GΩ) implemented with minimum-size transistors acting as pseudoresistors. Note that 3-dB cutoff frequency $f_{3\text{-}dB}$ of the high-pass circuits formed by $C_{1,2,3}$ and R_{QFG} is in the range of few hertz. This $f_{3\text{-}dB}$ changes due to process/temperature variations of $C_{1,2,3}$ and R_{QFG}, but it is not important as long as the modified $f_{3\text{-}dB}$ is below the lowest frequency of the processed signal [32]. Hence, these variations do not affect significantly the performance of the class-AB circuits.

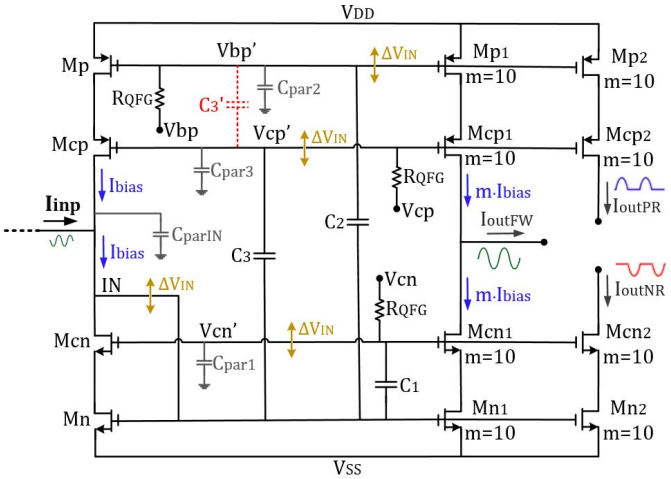


Fig. 2. High-performance power-efficient multiple-output class-AB current mirror.

Under quiescent conditions ($I_{inp} = 0$), voltages $V'_{bp} = V_{bp}$, $V'_{cp} = V_{cp}$, and $V'_{cn} = V_{cn}$ and the PMOS and NMOS transistors have equal currents I_{bias} (transistors with multiplicity m have a quiescent current mI_{bias}). For dynamic operation, capacitors C_1, C_2, and C_3 act as floating batteries that transfer the variations ΔV_{IN} (caused by I_{inp}) in the gate–source voltage of Mn to voltages V'_{cn}, V'_{bp}, and V'_{cp}. Positive (negative) input currents are processed by NMOS (PMOS) transistors as follows. For positive (negative) input current signals, voltage at node IN increases (decreases) and this change is transferred to nodes V'_{cn}, V'_{bp}, and V'_{cp} through the capacitors $C_{1,2,3}$. The change decreases (increases) the current in PMOS (NMOS) transistors and provides more headroom for the drain–source voltage of NMOS (PMOS) mirroring transistors allowing them to handle larger currents.

These currents are not limited by the quiescent current and can have peak values much greater than the bias currents (two decades in the here proposed circuit). Therefore, class-AB operation with very high CE is provided. The dynamic power dissipation of the mirror mainly corresponds to the power associated with the current signal. A small fraction of the dynamic power dissipation is related to the voltage change of the small parasitic capacitances at the gates of QFG transistors.

In Fig. 2, it can be seen that the PMOS section of the circuit performs as a PMOS mirror but it does not add the voltage headroom (V_{SGp}) of a PMOS diode-connected transistor on the input branch to the supply requirements. In practice, since nodes IN and V'_{bp} are ac coupled by C_2, transistor Mp performs as a diode-connected transistor for signals. The minimum supply voltage requirement of the circuit with transistors operating in strong inversion is given by $V_{supplymin} = V_{GS} + 2V_{Dssat} = V_{TH} + 3V_{Dssat}$. It can be under 500 mV for subthreshold operation in fine line technologies as in this case transistors have voltages $V_{GS} < V_{TH}$. For example, in 180-nm bulk CMOS technology, with $I_{bias} =$ 100 nA (or less), transistors can operate in saturation with a value $V_{GS} \sim V_{TH}/2$–230 mV and $V_{DSsat} \sim$ 50–70 mV resulting in $V_{supplymin} \sim V_{TH}/2 + 3V_{Dssat} \sim 440$ mV.

Note that C_3 in Fig. 2 can also be connected as C'_3 (as shown in [33]), however, this reduces the input current range and working frequency because capacitors C_2 and C'_3 form voltage dividers with the parasitic capacitances C_{par2} (at node V'_{bp}) and C_{par3} (at node V'_{cp}) and it leads to cumulative attenuation of two capacitive dividers between nodes IN and V'_{cp}. For large mirror gain m, C_{par2} and C_{par3} are relatively large, requiring larger C_2, and C'_3 to prevent high attenuation between nodes IN and V'_{cp}. Therefore, here, the proposed substitution of C'_3 by C_3 (Fig. 2) prevents the cumulative attenuation of the two capacitive voltage dividers and allows the use of smaller C_1, C_2, and C_3 values.

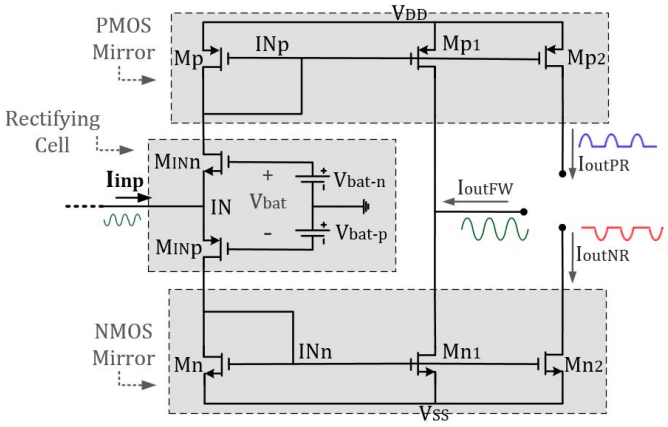


Fig. 3. Conventional class-AB current mirror using PMOS and NMOS mirrors and a rectifying cell [34].

Fig. 3 shows a frequently used class-AB current mirror reported in [34]. It has PMOS and NMOS mirrors in the input branch with $V_{supplymin} = 2V_{GS} + 2V_{DSsat}$ which are almost twice as large as the class-AB mirror of Fig. 2. In addition, if mirrors are not cascoded, the cell has very poor accuracy. Cascode mirrors enhance accuracy at the expense of increasing the supply voltage requirements and limiting the maximum output current.

This is since conventional cascode transistors with constant cascode bias voltages limit the maximum current signals. Improved linearity, lower supply requirements, higher output current range, and power efficiency of the class-AB current mirror of Fig. 2 with respect to other class-AB mirrors, i.e., [18], [19], [30], [31], [34], make it a highly efficient building block for several CM applications such as CM capacitance multipliers and precision rectifiers. In addition, the proposed class-AB mirror can be easily modified to become a gain programmable mirror with digitally adjustable factor m. This can be done by connecting in parallel various output stages with binarily weighted scaled gain factors using switches.

A. Class-AB Capacitance Multiplier

A CM capacitance multiplier with capacitance multiplication factor $k = (1 + m)$ using the class-AB mirror of Fig. 2 is depicted in Fig. 4. As discussed before, the output branch of the current mirror acts as a gain m dependent current source, and the source current I_s is the sum of the capacitance current $I_c = I_{inp}$ and the output current $I_{out} = mI_c$

$$I_s = (1 + m)I_c. \tag{6}$$

In practice, the input resistance R_{in} of the mirror at node IN, which is in series with capacitor C and the output resistance

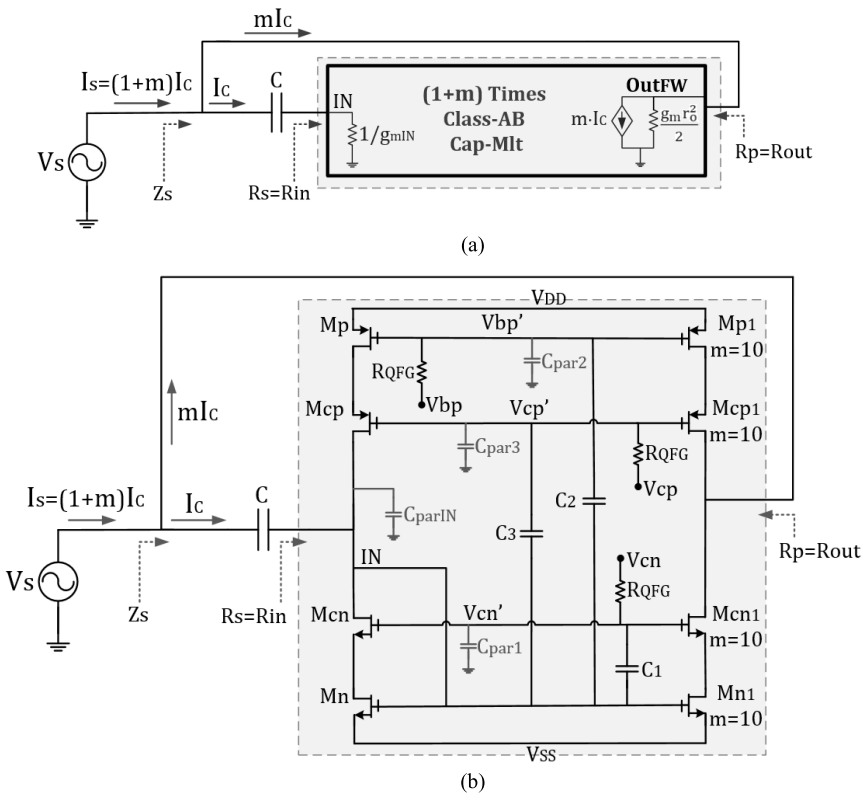


Fig. 4. Configuration of the proposed class-AB capacitance multiplier with $k = (1 + m)$ multiplication factor. (a) Block diagram. (b) Transistor-level implementation.

of the mirror R_{out} which is in parallel with V_s, introduces nonideal effects. Resistances $R_s = R_{in}$ and $R_p = R_{out}$ are the denominated equivalent series resistance and parallel load resistance, respectively. They limit the range of frequencies in which the circuit of Fig. 4 behaves as a high Q capacitor. Since at ac Mp acts also as a diode-connected transistor with resistance $1/g_{mp}$, the resistance R_s is determined by the transconductances of both transistors Mn and Mp (g_{mn} and g_{mp}, respectively)

$$R_s = R_{in} \approx \frac{1}{g_{mn}} \left\| \frac{1}{g_{mp}} = \frac{1}{(g_{mn}+g_{mp})} = \frac{1}{g_{mIN}} \right. \tag{7}$$

where $g_{mIN} = g_{mn} + g_{mp}$ is the transconductance at node IN. On the other hand, the resistance $R_p = R_{out}$ ($\sim$MΩs) is the large output resistance of the cascode mirror $R_{out} \approx (g_m r_0^2)/2$. (Assuming for simplicity that output PMOS and NMOS transistors have the same transconductance gain g_m and output resistance r_0.)

Fig. 5(a) shows the simplified small signal model of the proposed capacitance multiplier of Fig. 4 where the input impedance $Z_s = V_s/I_s$ is given by the following equation:

$$\begin{aligned} Z_s(s) &= \frac{V_s}{I_s} \\ &= \frac{R_p\left(1 + s\frac{C+C_{parIN}}{g_{mIN}}\right)}{1 + s\left((1+m)\,R_pC + \frac{C+C_{parIN}}{g_{mIN}}\right) + s^2\left(\frac{R_pCC_{parIN}}{g_{mIN}}\right)} \\ &= \frac{R_p\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)\left(1+\frac{s}{\omega_{pnd}}\right)} \end{aligned} \tag{8}$$

with C_{parIN} being the total parasitic capacitance at node IN given by the following equation:

$$C_{parIN} \approx C_{gsMn} + C_{gdMcn} + C_{gdMcp} + C_{dbMcn} + C_{dbMcp}. \tag{9}$$

Note that Z_s has a left half-plane zero ω_z, a dominant pole ω_{pd}, and a nondominant pole ω_{pnd}. Assuming that $R_p \gg R_s$ (i.e., $R_{out} \gg 1/g_{mIN}$) and $C \gg C_{parIN}$, the approximate values of ω_z, ω_{pd}, and ω_{pnd} (with $\omega_{pd} \ll \omega_z \ll \omega_{pnd}$) are given by the following equations, respectively,

$$\omega_z \approx \frac{g_{mIN}}{C + C_{parIN}} \approx \frac{g_{mIN}}{C} \approx \frac{1}{R_sC} \tag{10}$$

$$\omega_{pd} \approx \frac{1}{\frac{C+C_{parIN}}{g_{mIN}} + R_p(1+m)C} \approx \frac{1}{R_p(1+m)C} \tag{11}$$

$$\omega_{pnd} \approx \frac{C + C_{parIN} + (1+m)R_pg_{mIN}C}{R_pCC_{parIN}} \approx \frac{(1+m)}{R_sC_{parIN}}. \tag{12}$$

In (8), if the negligible phase shift introduced by $f_{pnd} = \omega_{pnd}/(2\pi)$ is not considered ($C \gg C_{parIN}$), the small signal model of the capacitance multiplier of Fig. 5(a) is simplified to the model depicted in Fig. 5(b) and Z_s reduces to the following equation:

$$\begin{aligned} Z_s(s) &\approx \frac{R_p\left(1+\frac{s}{\omega_z}\right)}{\left(1+\frac{s}{\omega_{pd}}\right)} = \frac{R_p\left(1+s\frac{C}{g_{mIN}}\right)}{1+s\left((1+m)R_pC + \frac{C}{g_{mIN}}\right)} \\ &= \frac{1}{(1+m)}\left(\frac{1}{sC} + R_s\right) \left\| R_p. \right. \end{aligned} \tag{13}$$

Note that in (13), both base capacitor C and resistance R_s are scaled by the same factor $(1 + m)$ [see Fig. 5(c)].

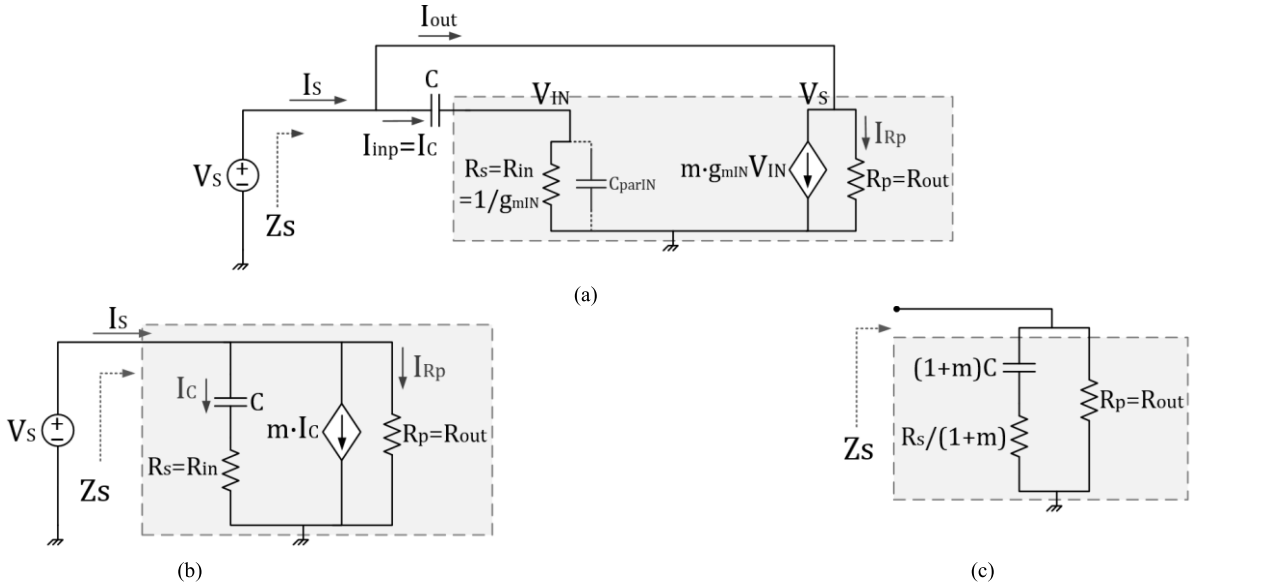


Fig. 5. Simplified small signal models of the capacitance multiplier of Fig. 4. (a) Considering the effect of C_{parIN}. (b) Neglecting the effect of C_{parIN}. (c) Equivalent impedance Z_s (neglecting the effect of C_{parIN}).

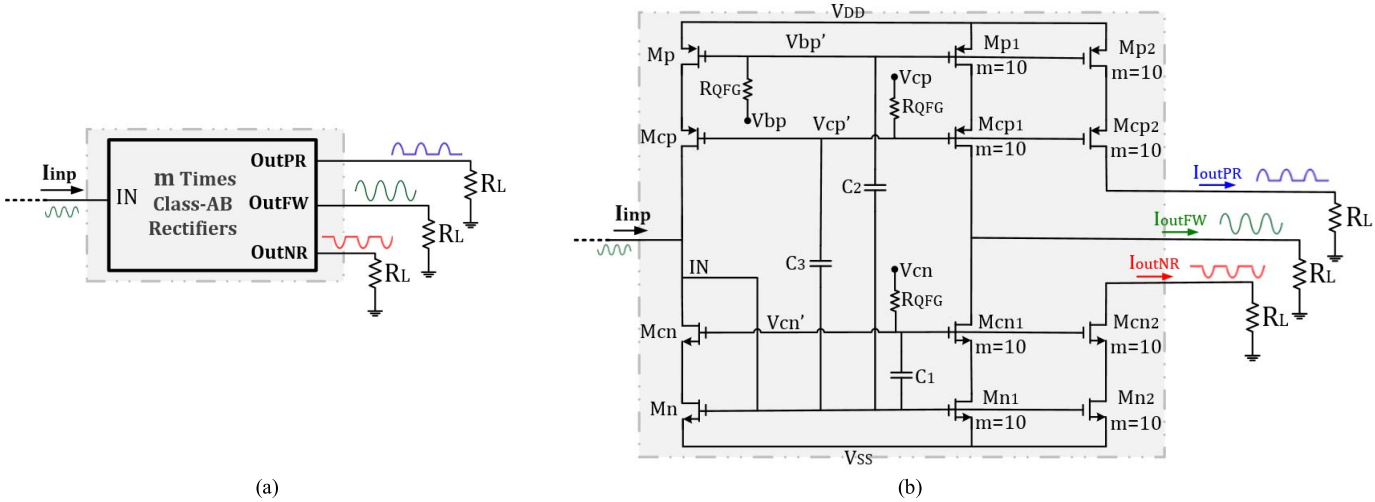


Fig. 6. Configuration of the class-AB half-wave positive (I_{outPR}) and negative (I_{outNR}) rectifiers: (a) Block diagram. (b) Transistor-level implementation.

In Z_s, the reactive (capacitive) component is higher than the resistive component in the frequency range (f_L, f_H) where $f_L = \omega_p/(2\pi)$ and $f_H = \omega_z/(2\pi)$ are the low and high corner (3-dB) frequencies, respectively. For frequencies $f < f_L$, the output resistance of the mirror dominates Z_s, while for $f > f_H$, the input resistance of the mirror dominates Z_s. The frequency-dependent quality factor Q of the equivalent capacitance $C_{eq} = (1 + m)C$ is defined in the following equation:

$$Q(f) = |\tan(\theta)|. \tag{14}$$

Q is considered high in the range (f_1, f_2) with $f_1 \approx 10 f_L$ and $f_2 \approx f_H/10$ where θ is the phase of $Z_s(\theta)$ and very close to $-90°$ ($|Q| > 10$ for $-90° < \theta < -85°$). A dB-wise linear decrease in the magnitude of Z_s in the same range of frequencies (f_1, f_2) should be observed as in the case of a physical capacitor. If required, the effective capacitance multiplication factor can be increased by cascading several current mirrors. The assumption that the mirror introduces negligible phase shift (and consequently negligible Q degradation) in Z_s for frequencies $f \ll f_H$ is justified if $f_{pnd} \gg f_H$. This requires to select a value of C that satisfies the condition $C \gg C_{parIN}$.

B. Class-AB Precision Rectifiers

Another application of the class-AB current mirror of Fig. 2 is the implementation of highly CE low-voltage CM precision rectifiers, as shown in Fig. 6. As explained before, NMOS and PMOS transistors process positive and negative half cycles of the input current signal I_{inp}, respectively. Output branches with only NMOS or PMOS transistors provide I_{outNR} or I_{outPR}, respectively, which are half-wave negative and positive rectified versions of the input current signal.

Resistors R_L (or transresistance amplifiers) can be used, if required, to transform output currents into output voltages (for example, $V_{OutPR} = I_{outPR} R_L$).

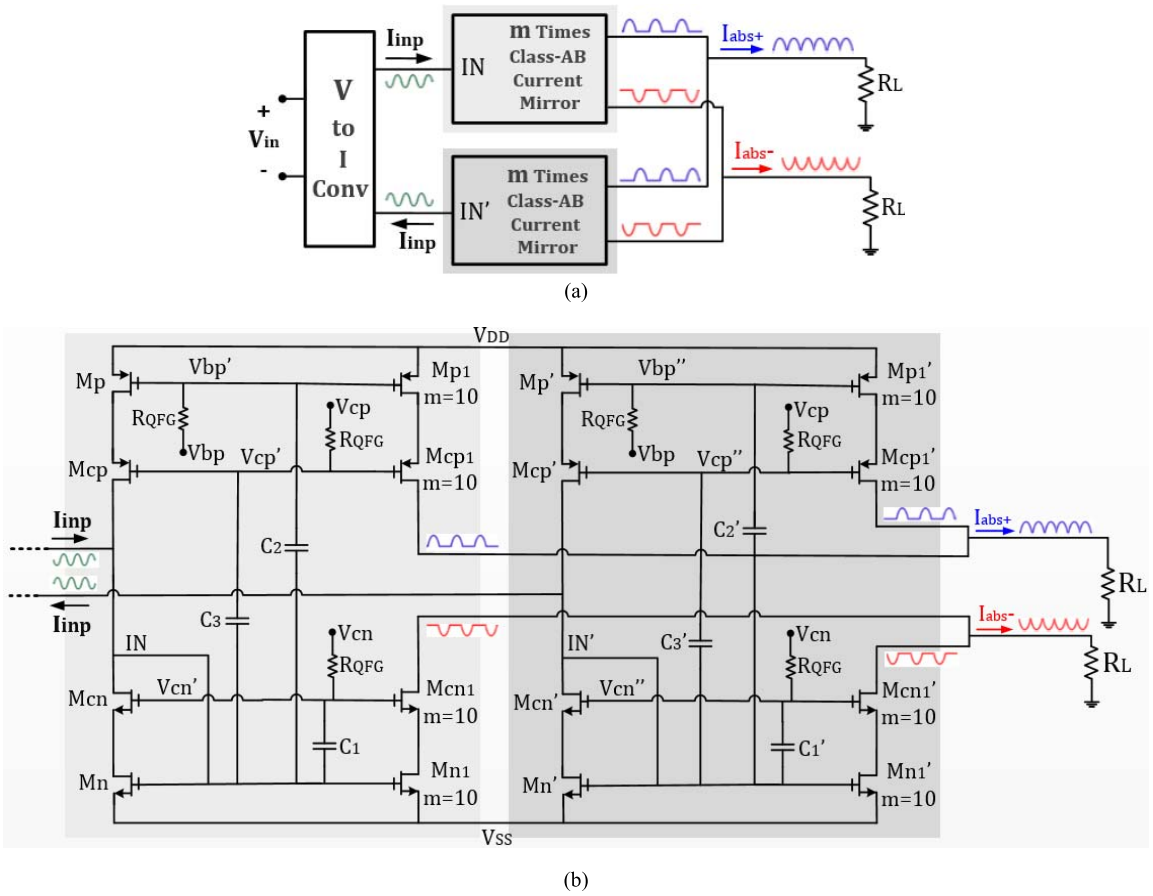


Fig. 7. Proposed class-AB positive (I^+_{abs}) and negative (I^-_{abs}) full-wave rectifiers. (a) Block diagram. (b) Transistor-level implementation.

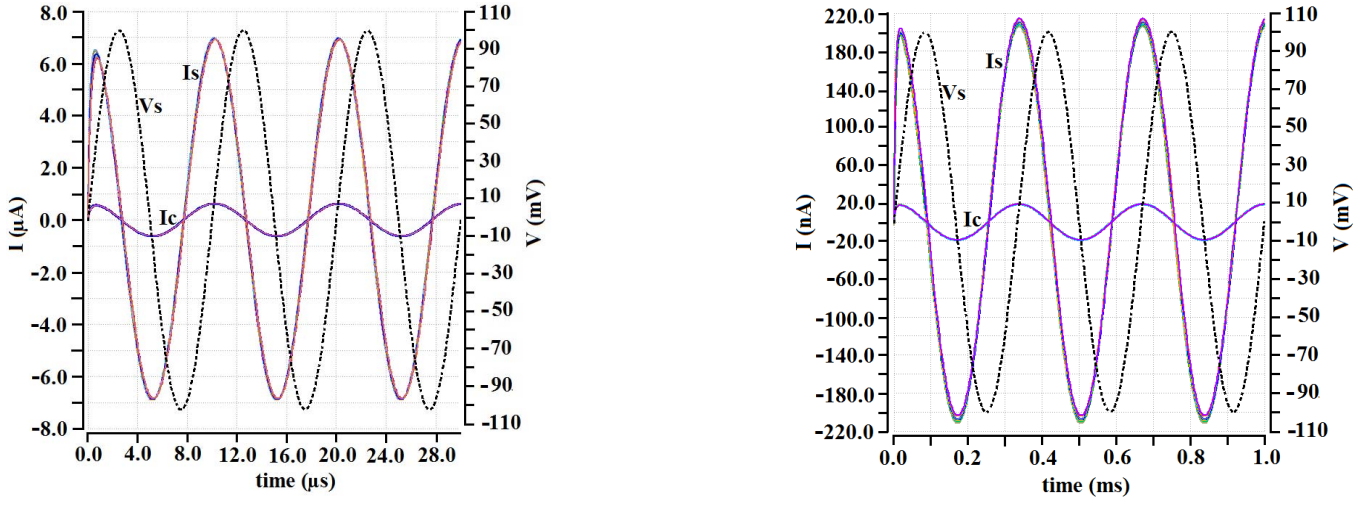


Fig. 8. Simulated waveforms of V_s, I_s, and I_c in the proposed capacitance multiplier of Fig. 4 over 15 process corners (TT, SS, FF, SF, and FS) and temperature variations ($T = -40$ °C, 27 °C, 85 °C). (a) With nominal supplies of ±0.9 V, $I_{outQ} = m \cdot I_{bias} = 12$ μA, and input signal $V_s = 100$ mV at 100 kHz. (b) With low supplies of ±0.25 V, $I_{outQs} = 0.55$ μA, and $V_s = 100$ mV at 3 kHz.

Full-wave rectification requires the addition of the two half-wave rectified signals with one of them inverted. Positive and negative full-wave (absolute value) rectified currents (I^+_{abs} and I^-_{abs}, respectively) can be generated, as shown in Fig. 7. The proposed circuit uses two of the class-AB current mirrors of Fig. 2 with their corresponding two positive and two negative half-wave rectified outputs connected in parallel. These current mirrors have complementary input current signals (I_{inp} and $-I_{inp}$) which are generated by a fully differential linear voltage-to-current converter (V-to-I Conv) used as the interface between input voltage signal and a CM system (Fig. 7). In other reported approaches, i.e., [19] and [30],

TABLE I

SIMULATED PARAMETER VALUES OF THE PROPOSED CIRCUITS OF FIGS. 2, 4, AND 6 FOR NOMINAL AND LOW SUPPLY VOLTAGES

Nominal Dual Supply Voltages V_{DD}=+0.9 V , V_{SS}=-0.9 V , and I_{bias}=1.2 µA										
Transistor	***W/L* (µm/µm)**	**I_D (µA)**	**V_{TH} (V)**	**V_{GS} (V)**	**V_{DS} (V)**	**g_m (µA/V)**	**g_{ds} (µA/V)**	**g_m/I_D (V^{-1})**	**I_f**	**Region of Inversion**
Mn	5/0.4	1.207	0.439	0.373	0.188	29.7	0.312	24.606	0.150	Moderate
Mcn	5/0.4	1.207	0.479	0.416	0.185	30.1	0.320	24.938	0.150	Moderate
Mp	20/0.4	1.207	0.419	0.356	0.251	28.66	0.408	23.745	0.159	Moderate
Mcp	20/0.4	1.207	0.476	0.416	1.176	29.62	0.276	24.540	0.159	Moderate
Mn1	50/0.4	12.08	0.439	0.373	0.191	297.2	3.087	24.603	0.150	Moderate
Mcn1	50/0.4	12.08	0.479	0.413	0.710	307.7	1.347	25.472	0.150	Moderate
Mp1	200/0.4	12.06	0.419	0.356	0.247	286.2	4.112	23.731	0.159	Moderate
Mcp1	200/0.4	12.06	0.479	0.420	0.653	294.1	3.118	24.386	0.159	Moderate
Low Dual Supply Voltages V_{DD}=+0.25 V , V_{SS}=-0.25 V , and I_{bias}=55 nA										
Transistor	***W/L* (µm/µm)**	**I_D (nA)**	**V_{TH} (V)**	**V_{GS} (V)**	**V_{DS} (V)**	**g_m (µA/V)**	**g_{ds} (µA/V)**	**g_m/I_D (V^{-1})**	**I_f**	**Region of Inversion**
Mn	5/0.4	55	0.439	0.257	0.112	1.49	0.034	27.091	0.0068	Weak
Mcn	5/0.4	55	0.463	0.284	0.145	1.51	0.014	27.455	0.0068	Weak
Mp	20/0.4	55	0.419	0.238	0.133	1.46	0.030	26.545	0.0072	Weak
Mcp	20/0.4	55	0.454	0.278	0.110	1.48	0.048	26.909	0.0072	Weak
Mn1	50/0.4	550	0.439	0.257	0.112	14.92	0.345	27.127	0.0068	Weak
Mcn1	50/0.4	550	0.463	0.284	0.145	15.08	0.144	27.418	0.0068	Weak
Mp1	200/0.4	550	0.419	0.238	0.134	14.58	0.301	26.509	0.0072	Weak
Mcp1	200/0.4	550	0.454	0.278	0.110	14.82	0.475	26.945	0.0072	Weak

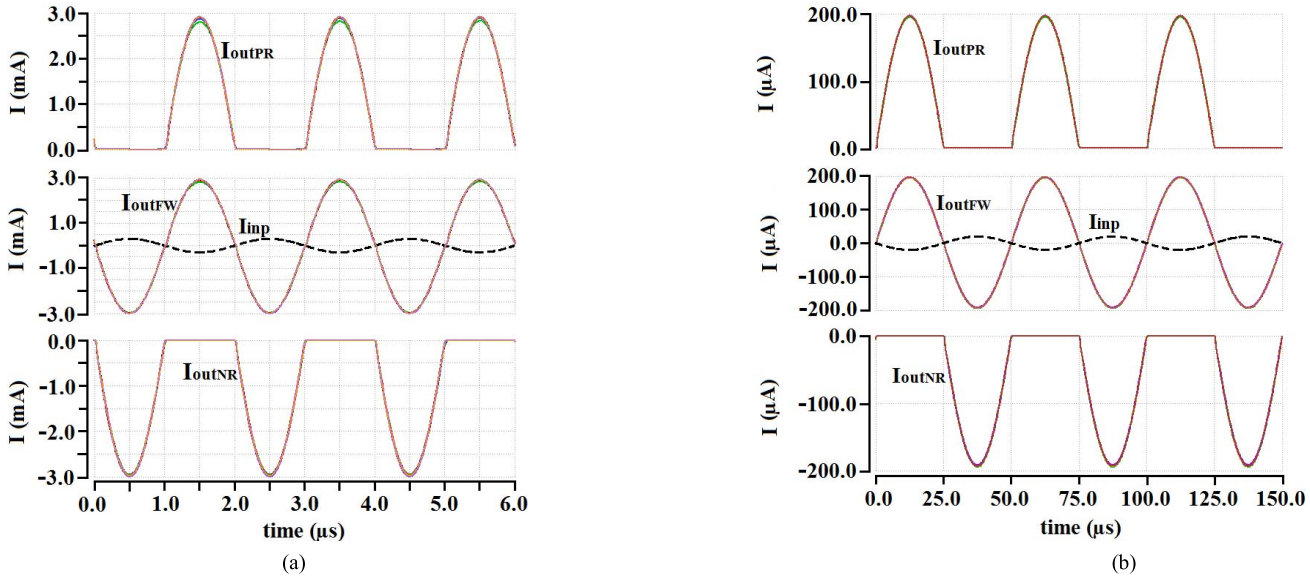


Fig. 9. Simulated waveforms of half-wave rectified currents of Fig. 6 (I_{outPR}, I_{outNR}, and I_{outFW}) over 15 process corners (TT, SS, FF, SF, and FS) and temperature variations (T = −40 °C, 27 °C, and 85 °C). (a) With nominal supplies ±0.9 V, I_{outQ} = 12 μA, and input current signal I_{inp} = 300 μA at 500 kHz. (b) With low supplies of ±0.25 V, I_{outQ} = 0.55 μA, and I_{inp} = 20 μA at 20 kHz.

to implement full-wave precision rectifiers one of the half-wave rectified signal components is inverted by passing it through another current mirror. This component experiences an additional delay which generates crossover distortion in the full-waved rectified output and reduces the maximum operating frequency of the rectifier. Compared to the above-mentioned approaches, the proposed full-wave rectifier of Fig. 7 has the advantage that all half-wave signal components are generated in parallel. Therefore, they experience the same delay which avoids crossover distortion and allows higher operating frequency.

III. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Results

The capacitance multiplier and precision rectifiers (Figs. 4, 6, and 7) were designed and simulated in a 180-nm CMOS technology. The nominal threshold voltages in this

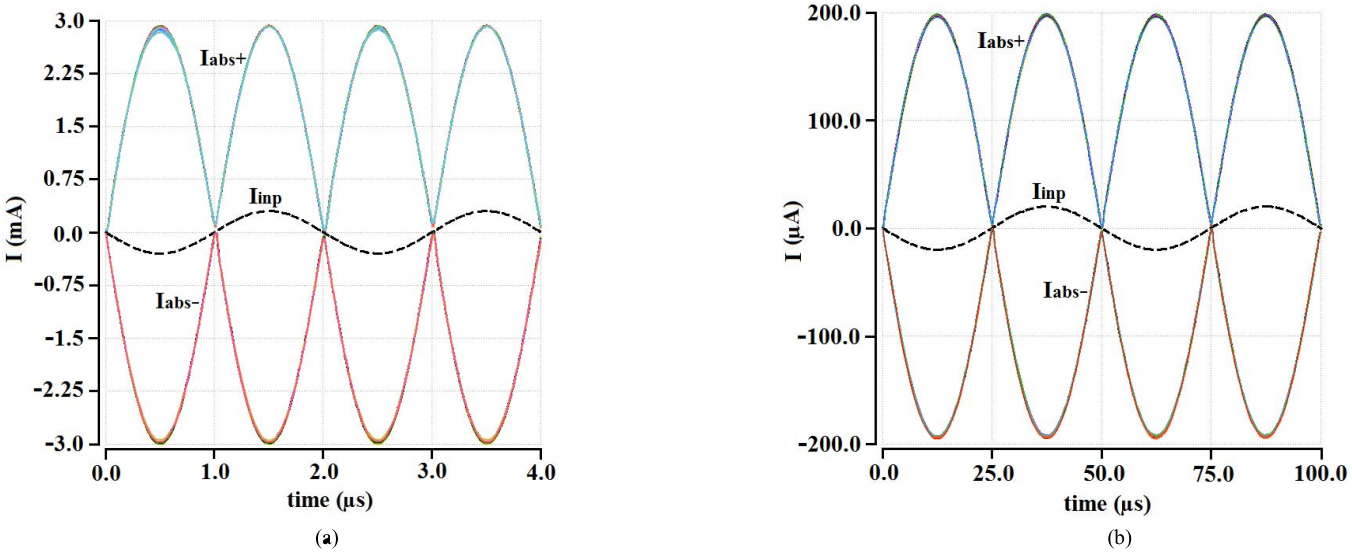


Fig. 10. Simulated full-wave rectified currents of Fig. 7 (I^+_{abs} and I^-_{abs}) over 15 process corners (TT, SS, FF, SF, and FS) and temperature variations ($T = -40$ °C, 27 °C, and 85 °C). (a) With nominal supplies of ±0.9 V, $I_{outQ} = 12$ μA, and $I_{inp} = 300$ μA at 500 kHz. (b) With low supplies of ±0.25 V, $I_{outQ} = 0.55$ μA, and $I_{inp} = 20$ μA at 20 kHz.

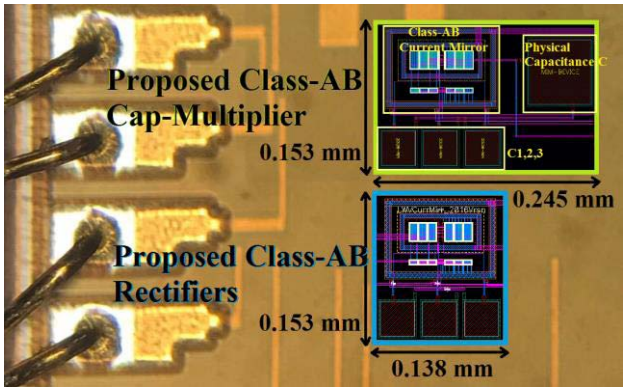


Fig. 11. Microphotograph of the fabricated chip including class-AB capacitance multiplier and half-wave precision rectifiers.

technology are approximately $V_{THn} = |V_{THp}| \approx 0.45$ V and $\mu_n C_{ox} \approx 340$ μA/V^2 for NMOS and $\mu_p C_{ox} \approx 80$ μA/V^2 for PMOS transistors. In addition, the sizes (in μm) of unit NMOS and PMOS transistors were (W/L)n $= (5/0.4)$ and (W/L)p $= (20/0.4)$, respectively. QFG transistors with dimensions (W/L)p$_{QFG} = (0.22/0.22)$ were used to implement R_{QFG}. Capacitances $C_1 = C_2 = C_3 = 3$ pF and base capacitor $C = 10$ pF were used in simulations. Also, the load capacitance was $C_L = 25$ pF. The standard circuitry was used to generate I_{bias} and bias voltages (V_{bn}, V_{cn}, V_{bp}, and V_{cp}) [35]. The proposed circuits were simulated with the following supply voltages and bias currents:

1) nominal dual-supply voltages $V_{DD} = 0.9$ V, $V_{SS} = -0.9$ V, and input branch bias current $I_{bias} = 1.2$ μA (operation in moderate inversion with $V_{GS} \sim V_{TH}$);
2) low-dual-supply voltages $V_{DD} = 0.25$ V, $V_{SS} = -0.25$ V, and $I_{bias} = 55$ nA (operation in weak inversion region: $V_{GS} \sim V_{TH}/2$, see the Appendix).

The simulated parameter values (V_{GS}, V_{DS}, V_{TH}, g_m, $g_{ds} = 1/r_0$, etc.) are shown in Table I verifying the discussion in the Appendix. It can be seen that in each region of operation, the inversion factor I_f for all transistors is almost the same ($I_f \approx 0.15$ for moderate inversion and $I_f \approx 0.007$ for weak inversion). Unit NMOS and PMOS transistors with the same bias current have equal transconductance gain $g_m \approx 30$ μA/V and $g_m \approx 1.5$ μA/V with nominal and low supply voltages, respectively. Furthermore, the g_m of scaled transistors scales proportionally with sizing.

TABLE II
MONTE CARLO ITERATIONS FOR SOME PARAMETERS OF FULL-WAVE RECTIFIERS OPERATING IN WEAK INVERSION

Parameters	Min	Max	Mean	Std Dev
Peak I_{abs}^- (µA)	188.7	212.3	198.1	3.432
Peak I_{abs}^+(µA)	192.9	205.8	198.8	1.907
$I_{supplyQ}$ (µA)	0.792	1.847	1.205	0.169
CE (µA/µA)	105.5	246	167.6	23.47
P_{diss} (µW)	0.475	1.108	0.723	0.101

The robustness of the proposed capacitance multiplier of Fig. 4 and the half and full-wave rectifiers of Figs. 6 and 7 was verified by simulating them over 15 process corners (TT, SS, FF, SF, and FS) and temperature variations ($T = -40$ °C, 27 °C, and 85 °C) in both moderate inversion and weak inversion regions (nominal and low supplies ±0.9 V and ±0.25 V, respectively). Fig. 8 validates that in the proposed capacitance multiplier, the magnitude of the source current I_s and also the close to $-90°$ phase shift between V_s and I_s show relatively small changes over process corners and temperature variations. Similarly, Figs. 9 and 10 verify the robustness of the proposed half- and full-wave rectifiers, respectively, overall process corners and temperature variations.

In addition to corner simulations, the robustness of the proposed circuits operating in weak inversion is verified by performing Monte Carlo iterations with 1000 random samples (considering process and mismatch data) in the full-wave

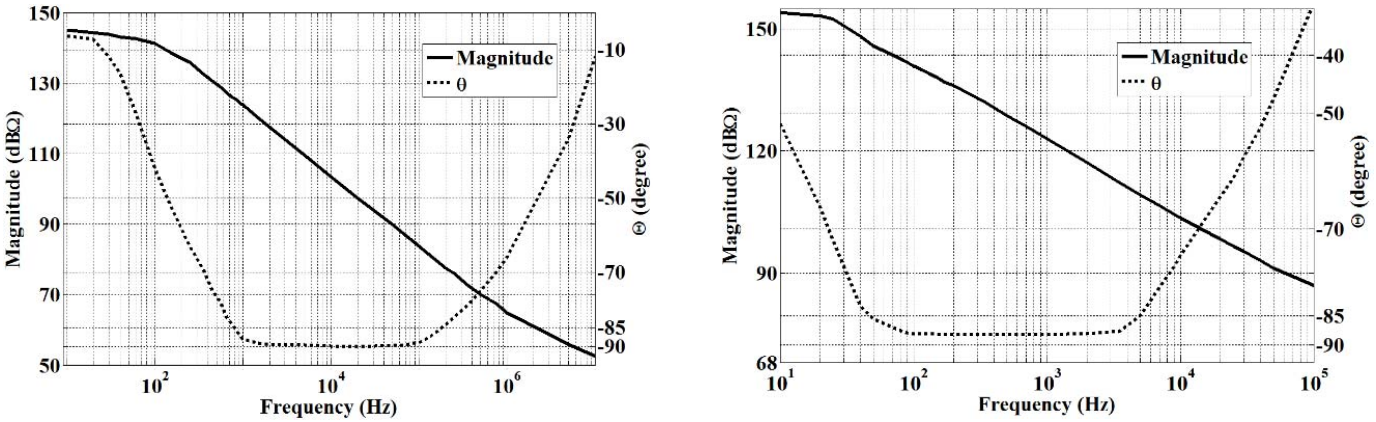


Fig. 12. Experimental measured magnitude and phase of Z_s of capacitance multiplier. (a) With nominal dual supplies of ±0.9 V, $I_{bias} = 1.2\ \mu$A. (b) With low dual supplies of ±0.25 V, $I_{bias} = 55$ nA.

TABLE III
COMPARISON OF EXPERIMENTAL RESULTS WITH OTHER CAPACITANCE MULTIPLIER

Parameters	[6][b]	[10]	[13]	[9]	[14]	[11]	[15]	[8]	[12]	This work Fig. 4	
CMOS Technology (µm)	0.8	0.35	OTAs CA3280E	0.18	0.5	0.5	0.5	0.5	0.065	**0.18**	
Structure[a]	A	AB[c]	A	A	A	AB[d]	A	A	A	**AB**	
Base Capacitance *C* (pF)	1	170	1000	7.95	18	100	10	25	7	**10**	
Supply Voltage (V)	3	2.8	±2.5	1.8	±1.35	3	3	2.2	1.2	**±0.9**	**±0.25**
$I_{supplyQ}$ **(µA)**	20	240	5750	100	650	1760	605	600	-	**13.2**	**0.605**
Power dissipation P_{diss} (µW)	60	672	28750	180	1755	5280	1815	1320	-	**23.76**	**0.302**
Multiplication Factor *k*	7.85	16	22	65	10.1	20	90.3	28	140	**11.4**	**10.88**
C_{eff} **(pF)**	7.85	2720	22000	516.8	182	1004	903	700	980	**114**	**108.8**
f_1 **(kHz)[e]**	4.4	0.7	<1	0.07	1500[b]	1.5	5	1	-	**0.75**	**0.045**
f_2 **(kHz)[e]**	132	40	100	30	10500[b]	100	10	100	-	**200**	**5**
$FOM_{Cap\text{-}Mlt}$ **(kHz/µW)**	16.7	0.94	0.08	10.81	51.79	0.32	0.25	2.1	-	**95.6**	**178.5**
Area (mm^2)	-	-	-	<0.228	0.702	0.053	0.042	0.07	-	**0.037**	

[a] Class-A or Class-AB. [b] Simulated. [c] Cascode starved Class-AB. [d] Non-cascoded class-AB. [e] Where $|Q|$>10: -90°<θ<-85°.

rectifier for some parameters such as I_{abs} and CE. These results are summarized in Table II.

Remarks:

1) It can be seen from Figs. 9(a) and 10(a) that with nominal supply voltages, the proposed class-AB precision rectifiers can have up to 3-mA dynamic output current (I_{outMAX}) with an output quiescent current of only $I_{outQ} = 12\ \mu$A. In addition, with low supplies, they have $I_{outMAX} \approx 200\ \mu$A with only $I_{outQ} = 0.55\ \mu$A [Figs. 9(b) and 10(b)]. In both cases, CE is very high since $I_{outMAX} \gg I_{outQ}$.
2) The maximum operating frequency of rectifiers is considered as the frequency at which the output currents show negligible phase shift (less than 5°) at the crossover points in relation to the input current signal (I_{inp}).
3) Monte Carlo results shown in Table II verify that the performance of the proposed circuits (such as the maximum dynamic output currents) does not change significantly with mismatches.
4) No dynamic power is consumed inside the mirror with exception of the current charging/discharging parasitic capacitances C_{par}. Hence, it can be said that the circuit has close to 100% dynamic power efficiency.

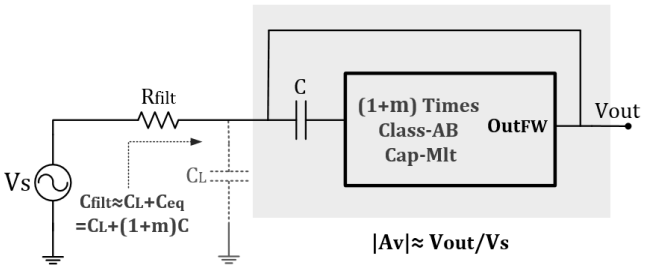


Fig. 13. Implementation of *RC* LPF using capacitance multiplier of Fig. 4.

B. Experimental Results of the Fabricated Test Chip

A test chip prototype with the proposed capacitance multiplier with $k = 11$ was fabricated in 180-nm CMOS technology thanks to MOSIS. The fabricated chip also includes half-wave precision rectifiers. A microphotograph is shown in Fig. 11, where the layouts of the capacitance multiplier of Fig. 4(b)

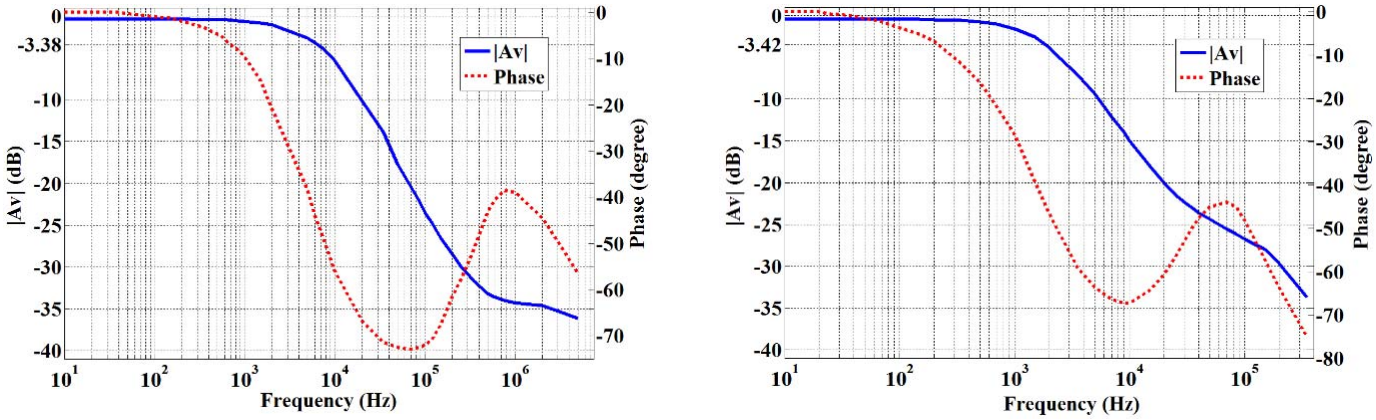


Fig. 14. Experimental measured frequency response of *RC* LPF (gain $|A_V|$ and phase) using the proposed capacitance multiplier ($C_{filt} \approx 140$ pF). (a) With nominal supplies of ±0.9 V, $R_{filt} = 160$ kΩ, and $f_{3\text{-}dB} \approx 7$ kHz. (b) With low supplies of ±0.25 V, $R_{filt} = 600$ kΩ, and $f_{3\text{-}dB} \approx 1.9$ kHz.

and precision rectifiers of Fig. 6(b) are superimposed since the active devices are hidden in the fabricated die by the opaque passivation. The sizes of unit NMOS and PMOS transistors were the same as in Section III-A. The capacitance multiplier and half-wave precision rectifiers occupy silicon areas of 0.037 mm^2 (243 μm × 153 μm) and 0.021 mm^2 (138 μm × 153 μm), respectively. A physical (base) on-chip capacitor with value $C = 10$ pF was used in the capacitance multiplier with a scaling factor $m = 10$, resulting in a nominal equivalent capacitance $C_{eq} = (1 + m)C = 110$ pF. Capacitances $C_{1,2,3}$ ($C_1 = C_2 = C_3 = 3$ pF) and C were laid out with two higher level metals in 180-nm CMOS technology. With the transistor dimensions indicated earlier and $C_{ox} = 8.78$ fF/μm^2 in 0.18-μm CMOS technology, the parasitic capacitance $C_{parIN} \approx 1$ pF [see (9)] and the condition $C \gg C_{parIN}$ are satisfied.

Fig. 12 shows the measured magnitude (in dBΩ) and phase (θ) of Z_s for the nominal and low supply biasing conditions mentioned in Section III-A.

The measured capacitance had a value $C_{eq} \approx 114$ pF for nominal supplies (±0.9 V) and $C_{eq} \approx 108.8$ pF for low supplies (±0.25 V). C_{eq} shows slight deviation w.r.t. the expected nominal value $C_{eq} = 11\ C = 110$ pF, due to process tolerances on the value of $C = 10$ pF. With both nominal and low supplies, dominant capacitive behavior ($|Q| > 10 : -90° < \theta < -85°$) is observed over two decades of frequency ($f_1 = 750$ Hz to $f_2 = 200$ kHz in Fig. 12(a), and $f_1 = 45$ Hz to $f_2 = 5$ kHz in Fig. 12(b), respectively). These results are in good agreement with the theoretical discussion in Section II-B.

The main measured parameters are summarized in Table III, including results for other reported capacitance multipliers. To ease comparison, a capacitance multiplier figure of merit $\text{FOM}_{Cap\text{-}Mlt}$ can be defined as follows:

$$FOM_{Cap\text{-}Mlt} = \frac{kBW}{P_{diss}} = \frac{k(f_2 - f_1)}{P_{diss}} \tag{15}$$

with $P_{diss} = (V_{DD} - V_{SS})I_{supplyQ}$ being the total quiescent power dissipation of the circuit and BW $= f_2 - f_1$ being the BW over which the quality factor of the capacitor has a value $|Q| > 10$. Note that the capacitance multiplier in this paper shows the highest $\text{FOM}_{Cap\text{-}Mlt}$.

In order to verify the value of C_{eq}, the proposed class-AB capacitance multiplier was tested in the first-order low-pass filter (LPF), as shown in Fig. 13. It is made of an off-chip resistance R_{filt} and a capacitor C_{filt} implemented using C_{eq}. This is applicable as long as the LPF cutoff frequency $f_{3\text{-}dB}$ is in the range (f_1, f_2) where Z_s has dominant capacitive behavior

$$f_{3\text{-}dB} = \frac{1}{2\pi\, R_{filt}C_{filt}} \approx \frac{1}{2\pi\, R_{filt}C_{filt}}. \tag{16}$$

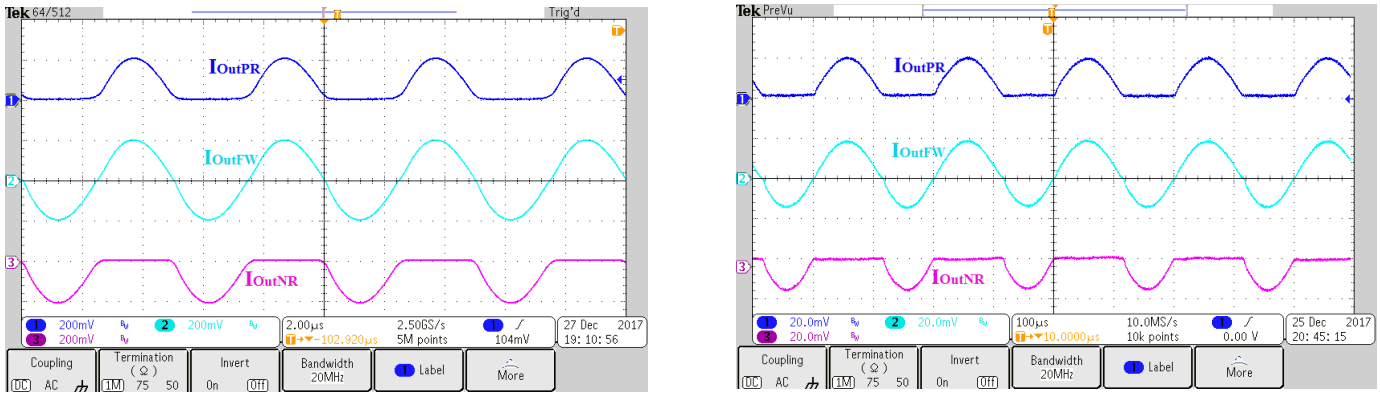
Due to the parasitic capacitance of the test board, input pad and test probe, a load capacitor with an estimated value $C_L = 25$ pF appears at the input of the capacitance multiplier, as shown in Fig. 13. This C_L must be taken into account to determine the effective capacitance $C_{filt} \approx 140$ pF of the LPF

$$C_{filt} \approx C_L + C_{eq}. \tag{17}$$

The measured frequency response of the LPF (gain $|A_V|$ and phase) is shown in Fig. 14(a) (nominal supply voltages) and Fig. 14(b) (low supply voltages). Off-chip resistors with values $R_{filt} = 160$ kΩ and $R_{filt} = 600$ kΩ are used for the results of Fig. 14(a) and (b), respectively. The higher value of R_{filt} employed for lower supply voltages is due to the fact that the frequency range over which the proposed circuit performs as a high-Q capacitor is scaled to lower frequencies in this case [$f_1 = 45$ Hz to $f_2 = 5$ kHz in Fig. 12(b)].

The dc gain $|A_{Vdc}|$ observed in Fig. 14(a) and (b) is lower than 0 dB. This is due to the fact that the capacitor C_{eq} has a resistance $R_p = R_{out}$ in parallel. At dc, the resistance R_{out} forms a voltage divider with resistance R_{filt}. This leads to a slight attenuation. The measured dc gain $|A_{Vdc}|$ has values of −0.38 and −0.42 dB for nominal and low supplies, respectively. The measured cutoff frequencies of the LPF $f_{3\text{-}dB} \approx 7$ kHz [Fig. 14(a)] and LPF $f_{3\text{-}dB} \approx 1.9$ kHz [Fig. 14(b)] are in good agreement with the ideal values calculated from (16).

Concerning the fabricated rectifier circuits, Fig. 15 shows the measured positive and negative rectified (I_{OutPR} and



(a) (b)

Fig. 15. Experimental output voltage waveforms of Fig. 6 using $R_L = 150\ \Omega$. (a) With supply voltages of ±0.9 V, $I_{bias} = 1.2\ \mu$A, $I_{outQ} = 12\ \mu$A, and $f = 200$ kHz. (b) With supply voltages of ±0.25 V, $I_{bias} = 55$ nA, $I_{outQ} = 0.55\ \mu$A, and $f = 5$ kHz.

TABLE IV
EXPERIMENTAL RESULTS OF THE PROPOSED PRECISION RECTIFIERS AND COMPARISON TO RECENT REFERENCES

Parameters	**[21]**	**[22]**	**[23]**	**[20]**		**This work, Fig. 7 (Full-wave) I_{abs}^+ & I_{abs}^-**		**This work, Fig. 6 (Half-wave) I_{outPR} & I_{outNR}**	
Experimental (Exp) or Simulation (Sim)	Sim	Exp	Sim	Sim[a]	Exp (Discrete elements)	Sim (Integrated)		Exp (Integrated)	
CMOS Technology (µm)	-	1.2	0.5	0.25	LM13700 and 1N4148	0.18		0.18	
Mode of Operation	VM	CM	VM	CM	CM	CM		CM	
Class-A or Class-AB	-	Class-AB	Class-A	Class-A	Class-A	Class-AB		Class-AB	
Full-wave or Half-wave	Half-wave	Full-wave	Full-wave	Full-wave	Full-wave	Full-wave		Half-wave	
C_L (pF)	0.5	-	-	-	-	25		25	
Supply Voltage (V)	±2.5	±0.6	±5	±1.5	±15	±0.9	±0.25	±0.9	±0.25
I_{bias} (µA)	-	10	120	60	1000	1.2	0.055	1.2	0.055
I_{outQ} (µA)	-	-	60	120	500	12.08	0.55	12	0.55
$I_{supplyQ}$ (µA)	380	-	420	300	3000	26.65	1.21	13.2	0.605
P_{diss} (µW)	1900	-	4200	900	90000	47.97	0.605	23.76	0.302
R_L (Ω)	-	1500	3000	1000	1000	1	1	150	150
f_{MAX} (kHz)	5000	3000	50000	<100	<100	500[b]	20[b]	200[b]	5[b]
I_{outMAX} (µA)	-	300	40	100[c]	250[c]	2918	194.5	1333.33[d]	106.67
CE (µA/µA)	-	-	0.1	0.33	0.083	109.5	160.74	101[d]	176.31
FOM_{Rect} (µA·kHz/µW)	-	-	476.2	<11.11	0.28	30415	6430	11223[d]	1766
Area (mm²)	-	-	-	-	-	-		0.021	

[a] Not fully integrated implementation: it combines CMOS technology with discrete diodes 1N4148.
[b] Unlike some other references listed in Table IV, the output of this work at maximum operating frequency shows negligible phase shift at the cross-over points (less than 5°).
[c] I_{outMAX}=V_{outMAX}/R_L [20].
[d] With nominal supply voltages of ±0.9 V, the circuit can have I_{outMAX} up to 3000 µA resulting in about 3-times higher CE, and FOM_{Rec}.

I_{OutNR}) as well as the unrectified (I_{OutFW}) output waveforms corresponding to the scheme of Fig. 6 for the nominal supplies of ±0.9 V, $I_{bias} = 1.2\ \mu$A, $I_{outQ} = 12\ \mu$A, $R_L = 150\ \Omega$, and $f = 200$ kHz [Fig. 15(a)] and also for low supplies of ±0.25 V, $I_{bias} = 55$ nA, $I_{outQ} = 0.55\ \mu$A, $R_L = 150\ \Omega$, and $f = 5$ kHz [Fig. 15(b)].

A linearized commercial bipolar OTA IC (CA3280E) was used to generate the input current source (I_{inp}) of the proposed precision rectifiers. Fig. 15(a) shows the experimental output currents (I_{OutPR}, I_{OutNR}, and I_{OutFW}) that have peak values of 1.33 mA at frequency 200 kHz. These peak values are more than 100 times larger than the output branch bias current $I_{outQ} = 12\ \mu$A. This corresponds to the very high CE and also two decades output current enhancement (C_{Enhc}) of the proposed circuit. Output current enhancement is defined as the ratio of the maximum output signal current I_{outMAX} to the quiescent current of the output branch (I_{outQ})

$$C_{Enhc} = \frac{I_{outMAX}}{I_{outQ}}. \tag{18}$$

By reducing I_{bias} from 1.2 μA to 55 nA, half-wave precision rectifiers were functional with dual-supply voltages as low as ±0.25 V, showing output currents over two orders of magnitude larger than the output branch bias currents [Fig. 15(b)].

Table IV summarizes the measured performance of the proposed rectifiers and results from other previous works. To ease comparison, a figure of merit FOM_{Rect} can be defined

for precision rectifiers

$$FOM_{Rect} = \frac{I_{outMAX} \cdot f_{MAX}}{P_{diss}}. \quad (19)$$

Note that the precision rectifiers proposed in this paper show the highest FOM_{Rect}. In addition, most references of precision rectifiers report simulation results or experimental results with discrete elements.

IV. Conclusion

Low-voltage/low-power CM capacitance multiplier and precision rectifiers using a highly power-efficient class-AB current mirror are presented. In the example of the capacitance multiplier, the emulated capacitor C_{eq} acts as a grounded capacitance which is $k = 11$ times larger than the on-chip base capacitor C. It has the highest $\text{FOM}_{Cap\text{-}Mlt}$ and operates with the lowest supply voltages of all reported capacitance multipliers. In addition, the proposed precision rectifiers generate output currents which are over 100 times larger than their quiescent output current. The performance of the proposed circuits is validated through simulation and experimental results of a fabricated chip in 180-nm CMOS technology.

Appendix
Low-Power Design

Designs with transistors operating in moderate inversion or in weak inversion regions are desirable for low-voltage/low-power applications, i.e., biomedical. This is because, in these regions, the transistors operate with gate–source voltages lower than their threshold voltages $V_{GS} < V_{TH}$ and the drain–source voltage V_{DS} can be very low ($V_{DS} < 100$ mV). This reduces essentially the minimum supply requirements and power dissipation of the circuit. Transistors are considered to operate in strong, moderate, or weak inversion depending on the value of the inversion factor I_f [36]–[38]. It can be calculated as

$$I_f = \frac{I_D \kappa}{2\mu C_{ox}} \cdot \left(\frac{q}{kT}\right)^2 \cdot \frac{L}{W} = \frac{I_D}{2\beta\zeta U_T^2} \quad (20)$$

where I_D, μ, C_{ox}, and $\beta = \mu C_{ox} W/L$ are the drain current, the carrier mobility, the oxide capacitance per unit gate area, and the transistor gain factor, respectively. Furthermore, k, T, and q are the Boltzmann's constant ($1.38064853 \times 10^{-23}$ JK^{-1}), absolute temperature (K), and the electric charge on the electron ($1.6021766209 \times 10^{-19}$ C), respectively, and the thermal voltage ($U_T \approx 26$ mV at $T = 300$ K) is defined as $U_T = kT/q$. The subthreshold slope factor $\zeta = n = 1/\kappa \approx 1.4$ is the reciprocal of the channel divider factor $\kappa \approx 0.7$. The transistor is considered to operate in weak inversion if $I_f < 0.1$, in moderate inversion if $0.1 < I_f < 10$, and in strong inversion if $I_f > 10$. Based on the EKV model [39], there is a general expression for the gate transconductance g_m in all regions of operation

$$g_m \approx \frac{4I_f \cdot \beta \cdot U_T}{(1+\sqrt{1+4I_f})} = \frac{2I_D}{\zeta U_T (1+\sqrt{1+4I_f})}. \quad (21)$$

For transistors working in weak inversion or in moderate inversion with low I_f, their g_m can be expressed as

$$g_m \approx \frac{I_D}{\zeta U_T}. \quad (22)$$

This leads to the highest transconductance to current ratio g_m/I_D that can be achieved by MOS transistors, and also results in a high BW to I_D factor since BW is proportional to g_m and consequently to I_D. Operation of the proposed circuits in both moderate inversion and weak inversion region is discussed in Section III.

References

[1] J. Ramírez-Angulo, M. Róbinson, and E. Sánchez-Sinecio, "Current-mode continuous-time filters: Two design approaches," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 39, no. 6, pp. 337–341, Jun. 1992.
[2] F. Khateb, M. Kumngern, T. Kulej, and V. Kledrowetz, "Low-voltage fully differential difference transconductance amplifier," *IET Circuits, Devices Syst.*, vol. 12, no. 1, pp. 73–81, Jan. 2018.
[3] J. Ramírez-Angulo, A. Torralba, R. G. Carvajal, and J. Tombs, "Low-voltage CMOS operational amplifiers with wide input-output swing based on a novel scheme," *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, vol. 47, no. 5, pp. 772–774, May 2000.
[4] G. Di Cataldo, G. Ferri, and S. Pennisi, "Active capacitance multipliers using current conveyors," in *Proc. IEEE Int. Symp. Circuits Syst.*, vol. 2, May/Jun. 1998, pp. 343–346.
[5] G. A. Rincon-Mora, "Active capacitor multiplier in Miller-compensated circuits," *IEEE J. Solid-State Circuits*, vol. 35, no. 1, pp. 26–32, Jan. 2000.
[6] S. Pennisi, "CMOS multiplier for grounded capacitors," *Electron. Lett.*, vol. 38, no. 15, pp. 765–766, Jul. 2002.
[7] Y. Tang, M. Ismail, and S. Bibyk, "Adaptive Miller capacitor multiplier for compact on-chip PLL filter," *Electron. Lett.*, vol. 39, no. 1, pp. 43–45, Jan. 2003.
[8] I. Padilla-Cantoya and P. M. Furth, "Enhanced grounded capacitor multiplier and its floating implementation for analog filters," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 62, no. 10, pp. 962–966, Oct. 2015.
[9] J. Choi, J. Park, W. Kim, K. Lim, and J. Laskar, "High multiplication factor capacitor multiplier for an on-chip PLL loop filter," *Electron. Lett.*, vol. 45, no. 5, pp. 239–240, Feb. 2009.
[10] L.-C. Hwang, "Area-efficient and self-biased capacitor multiplier for on-chip loop filter," *Electron. Lett.*, vol. 42, no. 24, pp. 1392–1393, Nov. 2006.
[11] I. Padilla-Cantoya, "Low-power high parallel load resistance current-mode grounded and floating capacitor multiplier," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 60, no. 1, pp. 16–20, Jan. 2013.
[12] W. Germanovix, E. Bonizzoni, and F. Maloberti, "Capacitance super multiplier for sub-hertz low-pass integrated filters," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 65, no. 3, pp. 301–305, Mar. 2018.
[13] J. Aguado-Ruiz, J. Hernandez-Alvidrez, A. J. López-Martín, R. G. Carvajal, and J. Ramírez-Angulo, "Programmable capacitance scaling scheme based on operational transconductance amplifiers," *Electron. Lett.*, vol. 45, no. 3, pp. 159–161, Jan. 2009.
[14] J. Aguado-Ruiz, A. J. López-Martín, and J. Ramírez-Angulo, "Three novel improved CMOS C-multipliers," *Int. J. Circuit Theory Appl.*, vol. 40, no. 6, pp. 607–616, Jun. 2012.
[15] I. Padilla-Cantoya, "Capacitor multiplier with wide dynamic range and large multiplication factor for filter applications," *IEEE Trans. Circuits Syst., II, Exp. Briefs*, vol. 60, no. 3, pp. 152–156, Mar. 2013.
[16] A. S. Sedra, G. W. Roberts, and F. Gohh, "The current conveyor: History, progress and new results," *IEE Proc. G-Circuits, Devices Syst.*, vol. 137, no. 2, pp. 78–87, Apr. 1990.
[17] J. Ramírez-Angulo, "High frequency low voltage CMOS diode," *Electron. Lett.*, vol. 28, no. 3, pp. 298–300, Jan. 1992.
[18] S. Pennisi, "A low-voltage design approach for class AB current-mode circuits," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 4, pp. 273–279, Apr. 2002.
[19] M. Kumngern, "New versatile precision rectifier Montree Kumngern," *IET Circuits, Devices Syst.*, vol. 8, no. 2, pp. 141–151, Mar. 2014.
[20] M. Sagbas, S. Minaei, and U. E. Ayten, "Component reduced current-mode full-wave rectifier circuits using single active component," *IET Circuits, Devices Syst.*, vol. 10, no. 1, pp. 1–11, Jan. 2016.

[21] H. Chaoui, "CMOS high-frequency rectifier with unity voltage gain," *Electron. Lett.*, vol. 31, no. 9, pp. 717–718, Apr. 1995.
[22] J. Ramírez-Angulo, R. G. Carvajal, J. Tombs, and A. Torralba, "Very low-voltage class AB CMOS and bipolar precision current rectifiers," *Electron. Lett.*, vol. 35, no. 22, pp. 1904–1905, Oct. 1999.
[23] N. Minhaj, "OTA-based non-inverting and inverting precision full-wave rectifier circuits without diodes," *Int. J. Recent Trends Eng.*, vol. 1, no. 3, pp. 72–75, May 2009.
[24] P. P. Sahu, M. Singh, and A. Baishya, "A novel versatile precision full-wave rectifier," *IEEE Trans. Instrum. Meas.*, vol. 59, no. 10, pp. 2742–2746, Oct. 2010.
[25] J.-P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. J. Declercq, "A model for μ-power rectifier analysis and design," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2771–2779, Dec. 2005.
[26] R. Amirtharaj and P. Wright. *Energy Harvesting for Biomedical Devices and Health Care Intelligent Infrastructure*. [Online]. Available: http://www.citris-uc.org/research/projects/energy_harvesting_for_bio medical_devices_and_health_care_intelligent_infrastructure
[27] A. J. Cardoso, M. C. Schneider, and C. G. Montoro, "Design of very low voltage CMOS rectifier circuits," in *Proc. IEEE Circuits Syst. Med. Environ. Appl. Workshop (CASME)*, Dec. 2010, pp. 1–4.
[28] S. S. Hashemi, M. Sawan, and Y. Savaria, "A high-efficiency low-voltage CMOS rectifier for harvesting energy in implantable devices," *IEEE Trans. Biomed. Circuits Syst.*, vol. 6, no. 4, pp. 326–335, Aug. 2012.
[29] A. J. Cardoso, C. G. Montoro, and M. C. Schneider, "CMOS rectifier design for energy harvesting based on vibrations," in *Proc. XV Wokshop IBERCHIP*, Iguacu Falls, Brazil, 2010, pp. 241–245.
[30] J. Ramírez-Angulo, E. Sánchez-Sinencio, and A. Rodriguez-Vazquez, "A piecewise-linear function approximation using current mode circuits," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, vol. 4, May 1992, pp. 2025–2028.
[31] K. C. Smith and A. S. Sedra, *Microelectronic Circuits*. New York, NY, USA: Oxford Univ. Press, 2004.
[32] J. Ramírez-Angulo, A. J. López-Martín, R. G. Carvajal, and F. M. Chavero, "Very low-voltage analog signal processing based on quasi-floating gate transistors," *IEEE J. Solid-State Circuits*, vol. 39, no. 3, pp. 434–442, Mar. 2004.
[33] F. Esparza-Alfaro, A. J. López-Martín, J. Ramírez-Angulo, and G. R. Carvajal, "Low-voltage highly-linear class AB current mirror with dynamic cascode biasing," *Electron. Lett.*, vol. 48, no. 21, pp. 1336–1338, Oct. 2012.
[34] A. S. Sedra, "The current conveyor: History and progress," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 1989, pp. 1567–1571.
[35] R. J. Baker, *CMOS, Circuit Design, Layout, and Simulation*, 3rd ed. Hoboken, NJ, USA: Wiley, 2010.
[36] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications," *IEEE J. Solid-State Circuits*, vol. 38, no. 6, pp. 958–965, Jun. 2003.
[37] A. J. López-Martín, J. Ramírez-Angulo, C. Durbha, and R. G. Carvajal, "A CMOS transconductor with multidecade tuning using balanced current scaling in moderate inversion," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1078–1083, May 2005.
[38] Y. Tsividis, *Operation and Modeling of the MOS Transistor*, 2nd ed. Boston, MA, USA: McGraw-Hill, 1998.
[39] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical MOS transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, Jul. 1995.

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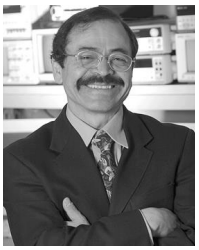

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