This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2018.2808236, IEEE Transactions on Circuits and Systems II: Express Briefs

An Op-amp Approach for Bandpass VGAs with Constant Bandwidth

Shirin Pourashraf, *Member, IEEE*, Jaime Ramirez-Angulo, *Fellow, IEEE*, Antonio J. Lopez-Martin, Ramon González-Carvajal, *Senior Member, IEEE*, and Jose Maria Algueta-Miguel, *Member, IEEE*.

***Abstract*—Two approaches to implement variable gain amplifiers based on Miller op-amps are discussed. One has true constant bandwidth while the other has essentially reduced bandwidth variations with varying gain. Servo-loops and AC coupling techniques with quasi floating gate transistors are used to provide a bandpass response with very low cutoff frequency in the range of Hz. In practice, one of the schemes is shown to have bandwidth variations close to a factor two while the second one has true constant bandwidth over the gain tuning range. Experimental results of test chip prototypes in 180 nm CMOS technology verify the theoretical claims.**

***Index Terms*—Constant bandwidth, VGA, Servo-loop, AC coupled amplifiers, QFG transistors.**

I. Introduction

SEVERAL approaches to implement Variable Gain Amplifiers (VGAs) with constant bandwidth based on Current Conveyors (CC) [1]-[2], Current Feedback (Transresistance) Amplifiers (CFA) [3]-[5], OTAs with tunable transconductance gain and constant load [6] and Cherry-Hooper amplifiers (OTA op-amp combination) [7]-[9], have been reported. In all cases, constant bandwidth is achieved by adjusting the gain G with resistor R_1 as depicted in Figs. 1a-c. For high gains, resistor R_1 is required to have small values relative to R_2. In the case of CC and CFA this requires very low impedance at input terminal X ($R_X << R_1 << R_2$), which is difficult to achieve at high frequencies. In Cherry-Hooper amplifiers, the OTA has typically a transconductance gain $G_m=1/R_1$ related to a resistor R_1 which is also required to have a small value. In both cases (very low R_X, and high G_m) increased power dissipation is required. Amplifiers based on conventional op-amps in inverting and non-inverting configurations have a bandwidth $BW=GB/(1+R_2/R_1)=\beta GB$ which decreases with the gain (Fig. 1(d)), where β is the feedback factor given by $\beta=1/(1+R_2/R_1)$ and GB is gain bandwidth product given by $GB=g_{mDP}/C_c$ in Miller (two-stage) op-amps and by $GB=g_{mDP}/C_L$ in one stage op-amps (OTAs). Further, g_{mDP} is the transconductance gain of the transistors in the differential input stage, C_L is the load capacitance and C_c is the compensation capacitance in Miller op-amps (typically a value $C_c=C_L$ is selected to achieve unity gain stability). A technique to achieve constant bandwidth has been proposed by scaling g_{mDP} with the gain [10]. This requires digitally programmable arrays of transistors and current sources for the input differential pair and it is limited to relatively narrow gain tuning ranges.

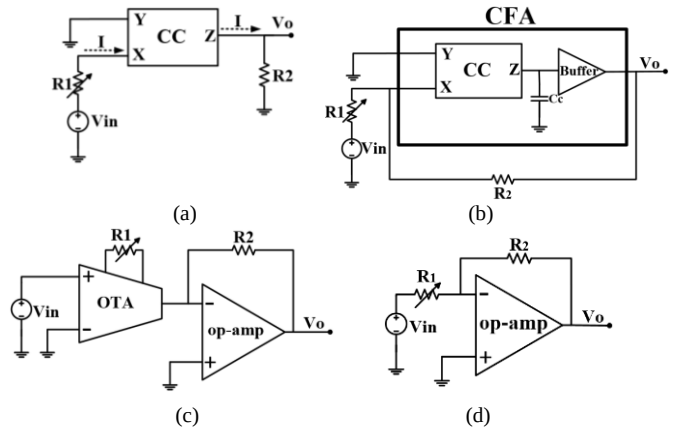


Fig. 1. (a) Current Conveyor amplifier CCA, (b) Current Feedback Amplifier CFA, (c) Cherry-Hooper amplifier, and (d) Conventional inverting amplifier.

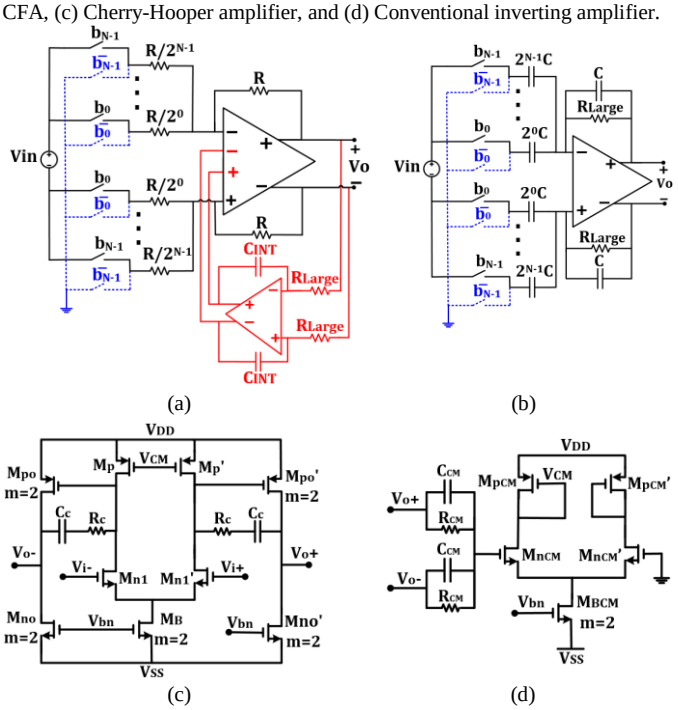


Fig. 2. Bandpass VGA implementations: (a) Servo-loop. (b) AC coupled. (c) Fully differential (FD) two-stage Miller op-amp used in VGAs. (d) Common mode feedback network.

In this paper, two simple approaches for the implementation of bandpass VGAs based on two-stage Miller op-amps (Fig. 2) are compared. They both have low cutoff frequencies in the range of Hz. One of them is shown to have greatly reduced BW variations with respect to the Conventional Approach while the other has true constant bandwidth with varying gain. Bandpass

S. Pourashraf and J. Ramirez-Angulo are with the VLSI Laboratory, Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM, 88003, USA (e-mail: shirin_p@nmsu.edu; and jairamir@nmsu.edu).

A. J. Lopez-Martin and J. M. Algueta-Miguel are with the Institute of Smart Cities, Public University of Navarra, E-31006 Pamplona, Spain (e-mail: antonio.lopez@unavarra.es; and josemaria.algueta@unavarra.es).

R. Carvajal is with the Departamento de Ingeniería Electrónica, Escuela Superior de Ingenieros, Universidad de Sevilla, E-41092, Spain (e-mail: carvajal@gte.esi.us.es).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2018.2808236, IEEE Transactions on Circuits and Systems II: Express Briefs

response is achieved using the two methods described in Sections I-A and I-B, respectively.

A. Servo-loop (shown in red in Fig. 2a)

This method uses an integrator in a negative feedback loop to achieve attenuation in the low frequency band. The op-amp has an additional differential pair (differential difference amplifier (DDA)) to inject the feedback signal from an integrator with unity gain frequency $\omega_o=1/(R_{Large}C_{INT})$. In this case, the open loop response of the op-amp can be approximated by a bandpass response with two real poles $A_{OL}(s)=A_{OLDC}[s/(s+\omega_L)][1/(s+\omega_H)]$ (see Fig. 3a). Further, A_{OLDC} is the op-amps DC open loop gain, $\omega_L=\omega_oA_{OLDC}$ and $\omega_H=GB/A_{OLDC}$. Note that $A_{OL}(s)$ neglects the op-amp high frequency pole ω_{pH}, the finite attenuation at DC, where $A_{OL}(0)=1/A_{OL\text{-}INT}$, and a very low frequency zero $\omega_Z=\omega_o/A_{OL\text{-}INT}$ caused by the finite DC open loop gain of the integrator $A_{OL\text{-}INT}$. Notice that the unity gain frequency ω_o of the integrator becomes the unity gain frequency of the bandpass amplifier in the low frequency band. Straightforward analysis assuming $\omega_H>>\omega_L$ and $\beta A_{OLDC}>>1$ shows that the closed loop response $G(s)$ given by $G(s)=A_{OL}(s)/[1+\beta A_{OL}(s)]$ can be approximated by a bandpass response $G(s)=G[s/(s+\omega_L')][1/(s+\omega_H')]$ with real poles ω_L', ω_H'. Further, $G=-R_2/R_1$ is the mid-band gain and the relation $\omega_L\omega_H=\omega_L'\omega_H'=\omega_oGB$ applies. In the Conventional Approach the switches shown in blue and controlled by b_i low are not included. In this approach, the high -3 dB frequency is given by $\omega_H'=\beta GB$ while the low -3 dB frequency is given by $\omega_L'=\omega_o/\beta=\omega_o(1+|G|)$.

B. AC Coupled Amplifier (see Fig. 2b)

In this method an AC coupled amplifier is used, and ω_H' is also given by $\omega_H'=\beta GB$ while ω_L' is constant and given by $\omega_L'=1/(R_{Large}C)$ (see Fig. 3b) i.e. [11].

The remainder of this paper is organized as follows. In Section II, two approaches for constant bandwidth are discussed. Simulation and experimental results of two test chip prototypes are presented in Section III. Conclusions are drawn in Section IV.

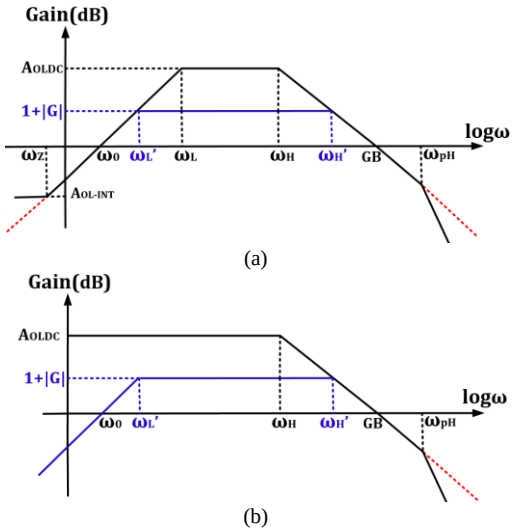


Fig. 3. Frequency response in open and closed loop (shown in black and blue, respectively): (a) Servo-loop. (b) AC coupled.

II. Approaches

A. Approach I

In this approach, the compensation capacitor has a value C_{ceff} that is dependent on G. It is scaled down with the gain $G=-R_2/R_1$ according to $C_{ceff}=C_c/|G|$ which leads to $\omega_H'=\beta[g_{mDP}/C_{ceff}]=\beta|G|[g_{mDP}/C_c]$. In turn ω_H' can be expressed as $\omega_H'=(GB|G|)/(1+|G|)$ and has a moderate gain dependent variation. For gain values $|G|>>1$, ω_H' remains approximately constant with a value $\omega_H'\approx GB$; whereas, for $|G|=1$ it attains the minimum value $\omega_{HMIN}'=GB/2$. Fig. 4 shows a very simple implementation of a digitally scaling approach for C_c applied to an inverting amplifier with digitally programmable gain $|G|=(2^0b_0+\cdots+2^{N-1}b_{N-1})$ (see Fig. 2a and 2b without switches shown in blue and controlled by b_i low). The gain programmable compensation capacitor is simply implemented as the series combination of binarily weighted capacitors (see Fig. 4), therefore $C_{ceff}=C_c/(2^0b_0+\cdots+2^{N-1}b_{N-1})=C_c/|G|$ as required. The concept of scaling down C_c with the gain to maintain constant GB has been addressed in [12]-[13] using active methods based on Miller multiplication that adapt the compensation capacitance to the gain. They were applied in [13] to a buffered single stage OTA using an additional high bandwidth VGA as Miller multiplier.

Remarks:

1. The total capacitance required to implement the digitally programmable capacitor array is $C_{tot}\approx 2C_c$, this is twice the capacitance C_c required in the conventional amplifier.
2. Bottom and top plate capacitances and MOS parasitic capacitances (especially C_{gdOUT} of the output transistor), as well as switch on resistances, lead to larger than expected variations in ω_H'. In practice, the effective compensation capacitance can be approximated by $C_{ceff}=(C_c/|G|)+C_{gdOUT}+kC_{par}$ (k is a coefficient that depends on gain $|G|$) and high -3dB frequency by $\omega_H'=[g_{mDP}/(C_c+|G|(C_{gdOUT}+kC_{par}))][|G|/(1+|G|)]$. For gains $|G|>>1$, ω_H' can be approximated as $\omega_H'=[g_{mDP}/(C_c+|G|(C_{gdOUT}+kC_{par}))]$. This shows that ω_H' decreases with gain; in order to reduce this effect, values of $C_c >> (|G_{MAX}|C_{gdOUT})$ should be used.
3. This approach can also be used in single stage op-amps (OTAs) by using a buffer at the output of the OTA i.e. [14]-[15]. In this case, higher bandwidths could be achieved since GB_{MAX} is limited by high frequency internal poles.
4. The switch on resistances can lead to changes in the phase margin and op-amps unity gain frequency.

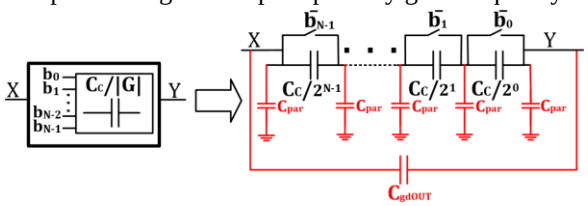


Fig. 4. Implementation of digitally programmable C_c in Approach I.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2018.2808236, IEEE Transactions on Circuits and Systems II: Express Briefs

5. In both the Conventional Approach and Approach I, the low -3 dB frequency ω_L' does not remain constant when a Servo-loop is used to achieve bandpass response. Instead, it increases with $|G|$ according to $\omega_L'=\omega_o(1+|G|)$. Implementation of C_{INT} as a digitally programmable array of binarily weighted capacitors in parallel with value $C_{INTeff}=C_{INT}|G|$ would lead to a constant ω_L', however it is not efficient in terms of area, since requires a large total capacitance $G_{MAX}C_{INT}$.

B. Approach II

In this approach (Fig. 2 including the switches shown in blue and controlled by b_i low), the capacitance C_c (and therefore GB) is constant. True constant bandwidth and phase margin is achieved by connecting the active input terminals that determine G (with b_i high) to the input signal source V_{in}, while connecting the remaining passive input terminals to ground (this approach includes the switches shown in blue and controlled by with b_i low in Fig. 2a and 2b). This leads to a constant feedback factor $\beta=1/(1+|G_{MAX}|)$ and as a consequence, to a constant value $\omega_H'=\beta GB=GB/(1+|G_{MAX}|)=g_m/[(1+|G_{MAX}|)C_c]$. The phase margin also remains constant since the unity gain frequency of the loop gain ($\omega_{uLG}=\omega_H'$) does not change with $|G|$, which is, in turn, set by the active input terminals connected to V_{in}.

Remarks:

1. Implementation of bandpass VGAs can be done according to the two schemes shown in Fig. 2 including the switches shown in blue and controlled by b_i low. In both, ω_L' is constant. For the amplifier with Servo-loop $\omega_L'=\omega_o/\beta=\omega_o(1+|G_{MAX}|)$ and for the AC coupled amplifier $\omega_L'=1/(R_{Large}C)$.
2. Conventional VGAs have the lowest phase margin for $|G|=1$. For stability it is typically required that $\omega_{pH}>2GB$ in order to achieve a phase margin greater than 60° (ω_{pH} is the high frequency pole of the op-amp open loop response). The unity gain frequency of the loop gain ω_{uLG} decreases with G according to $\omega_{uLG}=\omega_H'=GB/(1+|G|)$. This causes the phase margin to increase with $|G|$. In Approach II, the unity gain frequency of the loop gain is constant and given by $\omega_{uLG}=\omega_H'=GB/(1+|G_{MAX}|)$. The stability condition requires $2GB/(1+|G_{MAX}|)<\omega_{pH}$ instead of $2GB<\omega_{pH}$. This can be satisfied even with values $\omega_{pH}<GB$, since $\omega_{uLG}=GB/(1+|G_{MAX}|)$ is constant and has the lowest possible value (Fig. 5). Given that ω_{uLG} and ω_{pH} are constant, the phase margin does not change with gain.

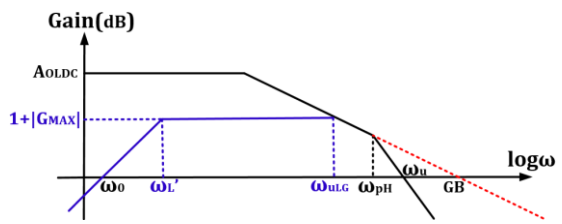


Fig. 5. Frequency response in open and closed loop Approach II.

3. Selecting $C_c=C_L$ is a common choice to achieve unity gain stability in conventional VGAs based on Miller op-amps. Approach II allows the designer to select a smaller value $C_c=C_L/(1+|G_{MAX}|)$ to achieve stable behaviour for all gains. For $[C_L/(1+|G_{MAX}|)]<C_{gdOUT}$, no compensation capacitance is required. This leads to the maximum possible bandwidth. The BW factor can be programmed digitally using an array of digitally programmable capacitors. In practice, the minimum value for C_c is determined by noise considerations.
4. The rms input noise in this Approach is constant and proportional to $1/[(1+|G_{MAX}|)C_c]^{1/2}$. It is lower by the factor $\cdot[(1+|G|)/(1+|G_{MAX}|)]^{1/2}$ than the Conventional Approach and by factor $[(1+|G|)/(|G|(1+|G_{MAX}|))]^{1/2}$ than Approach I. As indicated above, if required, noise can be reduced by increasing C_c; however, there is a bandwidth penalty for higher C_c. If C_c is increased and the bandwidth needs to be maintained then g_{mDP} needs to be increased by the same factor as C_c, which also has impact on power dissipation.

III. Simulation and Experimental Results

A. Simulation Results

In order to compare the Conventional Approach and Approach I (Fig. 2a without switches in blue) to Approach II (Fig. 2a including switches in blue) discussed above, fully differential bandpass VGAs using Miller op-amps with servo-loops were simulated in 180 nm CMOS technology. Transistor sizes (in µm) were $(W/L)_N$=20/0.5, $(W/L)_P$=120/0.5, and switches $(W/L)_{SW}$=1/0.22. Capacitors and resistors with values C_{INT}=5 pF, C_{CM}=1 pF, C_c=15 pF, C_L=22 pF, R_c=1 kΩ, R_{CM}=100 kΩ, and R=100 kΩ were used. The amplifier was designed with six-bit programmable gain N=6 [G_{MIN}=1 (0 dB) and G_{MAX}=63 (36 dB)]. Dual supplies V_{DD}=0.9 V, V_{SS}=-0.9 V, and bias currents I_{bias}=25 µA were used. The op-amp had a DC open loop gain A_{OLDC}=60 dB and GB=4.8 MHz. For the purpose of achieving a value f_L' in the Hz range, R_{Large} was implemented using minimum sized Quasi Floating Gate transistors (QFGs) [16] that have equivalent resistance values R_{Large}~50 GΩ. Figs. 6 and 7 show plots of f_L' and f_H' as a function of G, respectively. Fig. 6 shows the values of f_L' as a function of the gain $|G|$ in the Conventional Approach and in Approach I (curves a, and b, respectively) and with C_c=15 pF and without C_c in Approach II (curves c and d, respectively). In the first two cases, as expected, f_L' increases with gain according to $f_L'=f_o(1+|G|)$. Fig. 7 shows the values of f_H' as a function of G. In the Conventional Approach, as expected, f_H' decreases according to $f_H'=GB/(1+|G|)$ in the range from 77.7 kHz<f_H'<3.44 MHz (note that for low $|G|$ values the high frequency pole introduces an error in the value of f_H'). In Approach I f_H' shows variations with increasing $|G|$ in the range from 3.44 MHz to 5.1 MHz and then decreases monotonically to 2.61 MHz. The changes in f_H' are consistent with the values of f_H' calculated using the effective compensation capacitance C_{ceff} with C_c=15 pF, 1<$|G|$<63 (0 dB<$|G|$<36 dB), and C_{gdOUT}=0.3 pF. Approach II was simulated with and without C_c (curves c, and d, respectively, in Figs. 6 and 7).

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TCSII.2018.2808236, IEEE Transactions on Circuits and Systems II: Express Briefs

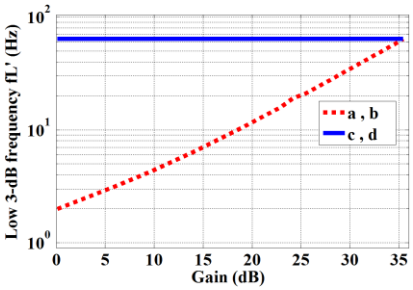


Fig. 6. Low -3 dB frequency f_L' vs $|G|$ in FD-VGAs: (a) Conventional Approach with C_c=15 pF. (b) Approach I with (C_c=15/$|G|$) pF. (c) Approach II with C_c=15 pF. (d) Approach II with no C_c.

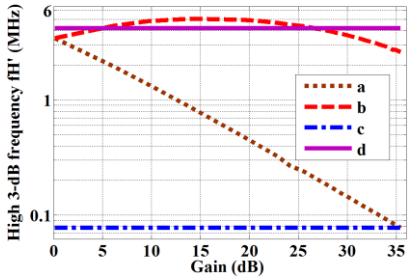
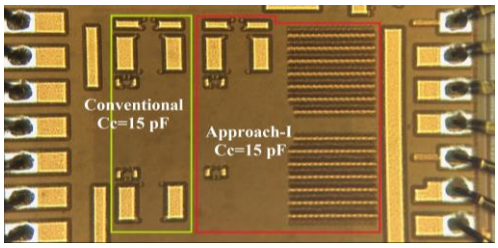


Fig. 7. High -3 dB frequency f_H' vs $|G|$ in FD-VGAs: (a) Conventional Approach with C_c=15 pF. (b) Approach I with (C_c=15/$|G|$) pF. (c) Approach II with C_c=15 pF. (d) Approach II with no C_c.

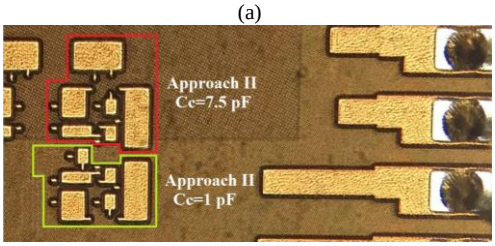
In the case where no C_c was used, the drain-gate capacitance of the output PMOS transistor C_{gdOUTP}~0.3 pF acts as a compensation capacitor and the amplifier is stable for all gains; this is due to the small value β=1/(1+$|G_{MAX}|$)=1/64 that causes the unity gain frequency of the loop gain to be constant and lower than the high frequency output pole of the op-amp given by f_{pH}=g_{moutP}/(2πC_L). In this case (with C_L=22 pF), f_{pH}'~7 MHz. The (constant) values for f_H' with and without compensation capacitance are 77.7 kHz and 4.2 MHz, respectively. It can be seen that Approach II, as expected, provides true constant values for f_H' and f_L' independent of G. The phase margin of the circuit of Approach II also remains constant (not plotted due to space constraints). It has a value of 92° with C_c and 53° without C_c. Another possible way to achieve higher bandwidth without removing/reducing C_c is to utilize power efficient g_m boosting techniques. This also increases the open loop gain and consequently reduces the nonlinearity associated to the attenuation introduced by utilization of a constant minimum β factor in as seen in Approach II.

B. Experimental Results

Fig. 8a shows a test chip prototype including two servo-loop bandpass FD-VGAs (Fig. 2a without switches in blue and controlled by b_i low). One with the Conventional Approach (fixed C_c) and the other using Approach I (digitally programmable C_c, Fig. 4). For tests, they had the same parameters (W/L, C_c, etc.) specified in the simulation section. Fig. 8b shows another test chip prototype with two single ended (SE) AC coupled VGAs (SE of Fig. 2b including switches in blue and controlled by b_i low) and G_{MAX}=15 (23.5 dB) fabricated to verify Approach II. One of the VGAs had C_c=7.5 pF and the other C_c=1 pF. In this case, transistor dimensions (in µm) were $(W/L)_N$=5/0.7 and $(W/L)_P$=25/0.7, and the feedback capacitor had a value C=1 pF.



(a)



(b)

Fig. 8. Micrograph of fabricated test chips in 180 nm CMOS Technology including: (a) servo-loop bandpass FD-VGAs with Conventional Approach (Fig. 2a) and Approach I (Fig. 4). (b) two SE AC coupled VGAs using Approach II (SE of Fig. 2b), one with C_c=7.5 pF and another with C_c=1 pF.

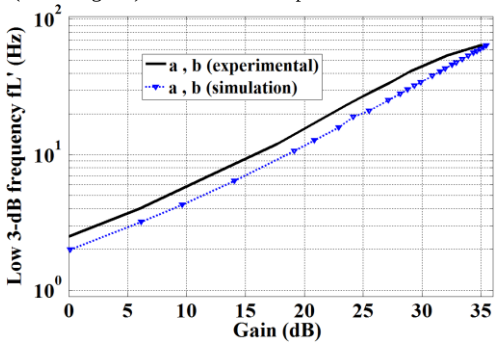


Fig. 9. Experimental and simulated f_L' vs $|G|$ in FD-VGAs using servo-loop: (a) Conventional Approach with C_c=15 pF. (b) Approach I with (C_c=15/$|G|$) pF.

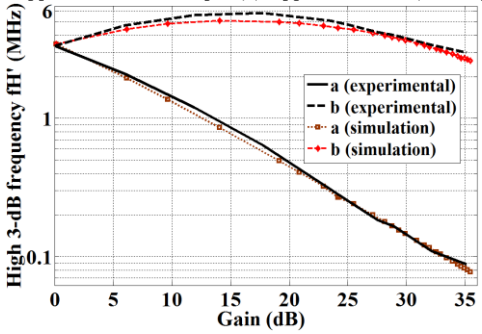


Fig. 10. Experimental and simulated f_H' vs $|G|$ in FD-VGAs using Servo-loop: (a) Conventional Approach with C_c=15 pF. (b) Approach I with (C_c=15/$|G|$) pF.

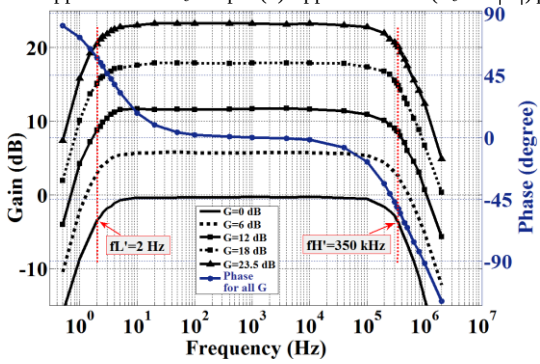


Fig. 11. Experimental frequency response of AC-coupled VGA with Approach II (Fig. 2b including switches in blue, C_c=7.5 pF) showing constant passband 2 Hz to 350 kHz. Simulated phase response shown in blue which remains the same for all gain settings.

Both chips were fabricated in 180 nm CMOS technology and tested with V_{DD}=0.9 V, V_{SS}=-0.9 V, and I_{bias}=25 µA. Note that FD or SE implementations do not affect the *BW* characteristics of any of the approaches. Figs. 9, and 10 show changes in f_L' and f_H' versus |*G*| for the Conventional Approach and Approach I which are seen to be consistent with the theory discussed in Section II and also with simulation results. Fig. 11 shows the experimental gain and simulated phase response validating the constant passband from f_L'=2 Hz to f_H'=350 kHz and constant phase for all gains using Approach II (Fig. 2b, C_c=7.5 pF). It can be seen that, as expected, from the discussion in Section II, Approach I has close to a factor 2 bandwidth variation while Approach II has true constant bandwidth, less area, and power dissipation than the other two approaches. Table I summarizes the results of the experimental characterization which are in good agreement with theory assuming C_{gdOUT}~0.3 pF. Linearity is characterized in the Table I in terms of Total Harmonic Distortion *THD* and Output Intercept Point OIP_3 with a 20 mV_{p-p} and 1 kHz input signal for G_{MAX}. The higher *THD* (lower OIP_3) values for Approach II are attributed to the SE implementations.

IV. Conclusion

Two approaches to essentially reduce bandwidth variations in bandpass VGAs based on Miller op-amps were compared. In practice, Approach I has bandwidth variations by approximately a factor two while the second approach has true constant bandwidth/phase margin over the entire gain tuning range. Innovative features of the circuits are the simplicity of Approach I to digitally scale C_c with the reciprocal of the gain and the simple implementation of Approach II that achieves true constant bandwidth. Both approaches have a bandpass response starting from very low cut-off frequencies (~Hz), this prevents amplification of the op-amps offset and blocks the DC components of the input signals. Another advantage of Approach II over Approach I is that the very low cut off frequency f_L' remains constant with gain. Simulation and experimental results from two test chips verified theoretical predictions.

References

[1] A. Sedra, and K. C. Smith, "A Second Generation Current Conveyor and its Applications." *IEEE Trans. Circ. theory*, vol. *17*, pp. 132–134, 1970.

[2] C. Bai, J. Wu, X. Deng, and C. Chen, "A 35-dBm OIP3 CMOS Constant Bandwidth PGA with Extended Input Range and Improved Common-mode Rejection." *IEEE Trans. Circuits and Systems-II (TCAS-II): Express Briefs*, vol. *64*, no. 8, pp. 922 - 926, Aug. 2017.

[3] F. Esparza-Alfaro, S. Pennisi, G. Palumbo, and A. J. Lopez-Martin, "Low-Power Class-AB CMOS Voltage Feedback Current Operational Amplifier with Tunable Gain and Bandwidth." *IEEE Transactions on Circuits and Systems II*, vol. *61*, no. 8, pp. 574-578, Aug. 2014.

[4] S.-C. Tsou, C.-F. Li, and P.-C. Huang, "A Low-Power CMOS Linear-in-Decibel Variable Gain Amplifier with Programmable Bandwidth and Stable Group Delay," *IEEE TCAS- II*, vol. *53*, no. 12, pp. 1436-1440, 2006.

[5] S. D'Amico, M. De Blasi, M. De Matteis, and A. Baschirotto, "A 255 MHz Programmable Gain Amplifier and Low-Pass Filter for Ultra Low Power Impulse-Radio UWB Receivers." *IEEE Transaction of Circuits and Systems-I*, vol. *59*, no. 2, pp. 337-345, Feb. 2012.

[6] T. Sánchez-Rodríguez, J. A. Galán, M. Pedro, A. J. López-Martín, R. G. Carvajal, and J. Ramírez-Angulo, "Low-power CMOS variable gain amplifier based on a novel tunable transconductor." *IET Circuits, Devices & Systems*, vol. *9*, no.2, pp.105-110, 2015.

[7] L. Acosta, R. G. Carvajal, J. Ramirez-Angulo, and A. J. Lopez-Martin, "A Simple Approach for the Implementation of CMOS Amplifiers with Constant Bandwidth Independent of Gain." *IEEE International Symposium on Circuits and Systems*, 2008, pp. 292-295.

[8] E. M. Cherry, and D. E. Hooper, "The design of wide-band transistor feedback amplifiers." *Proceedings of the Institution of Electrical Engineers*, vol. *110*, no. 2, pp. 375-389, Feb. 1963.

[9] C. Garcia-Alberdi, J. Aguado-Ruiz, A. J. Lopez-Martin, and J. Ramirez-Angulo., "Micropower Class-AB VGA with Gain-Independent Bandwidth." *IEEE TCAS-II*, vol. *60*, no. 7, pp. 397-401, July. 2013.

[10] X. Tian, and J. Wu, "Constant bandwidth gain-linear programmable gain amplifier." *IEEE Conference (ICSICT)*, 2014, pp. 1-3.

[11] S. Pourashraf, J. Ramírez-Angulo, A. J. Lopez-Martin, R. G. Carvajal, and A. Diaz-Sanchez, "±0.18 V Supply Gate Driven PGA with 0.7 Hz to 2 kHz Constant Bandwidth and 0.15 µW Power Dissipation." *International Journal of Circuit Theory and Applications*, May. 2017.

[12] S. Pennisi, S. Giuseppe, and A. Trifiletti, "Avoiding the Gain-Bandwidth Trade Off in Feedback Amplifiers." *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. *58*, no. 9, pp. 2108-2113. Sep. 2011.

[13] S. Pennisi, G. Scotti, and A. Trifiletti, "Constant and Maximum Bandwidth Feedback Amplifier with Adaptive Frequency Compensation." *IEEE International Symposium on Circuits and Systems*, 2012, pp. 436-439.

[14] S. Pourashraf, J. Ramirez-Angulo, A. J. Lopez-Martin, and R. G. Carvajal "Super Class AB OTA without open-loop gain degradation based on dynamic cascode biasing." *International Journal of Circuit Theory and Applications*, vol. 45, no. 5, pp. 2111-2118, May, 2017.

[15] S. Pourashraf, J. Ramírez-Angulo, A. Roman-Loera, A. J. Lopez-Martin, A. Diaz-Sanchez, and R. G. Carvajal, "High current efficiency class-AB OTA with high open loop gain and enhanced bandwidth." *IEICE Letters, Electronics Express*, vol. 14, no. 17, Aug. 2017.

[16] J. Ramírez-Angulo, A. J. López-Martín, R. G. Carvajal, C. Lackey, "Very low voltage rail-to-rail programmable-gain CMOS amplifier." *Analog Integrated Circuits Signal Processing*, vol. 37, no. 3, pp. 269-273, 2003.

TABLE I
EXPERIMENTAL RESULTS OF DIFFERENT APPROACHES FOR CONSTANT BANDWIDTH

Parameters	[4] 2006	[7] 2008[a]	[5] 2012	[9] 2013	[3] 2014	[6] 2015	[2] 2017	Conv. App.[b] (C_c=15pF)	App. I[b] (C_c=15pF)	App. II[b] (C_c=7.5 pF)	App. II[b] (C_c=1 pF)
CMOS Tech. (nm)	180	500	90	500	500	130	180	180	180	180	180
Supply (V)	1.8	±3.3	1.2	±1.65	3.3	1.2	1.8	±0.9	±0.9	±0.9	±0.9
Config.	FD	FD	FD	FD	SE	FD	FD	FD	FD	SE	SE
C_L (pF)	-	15	-	-	-	-	2	22	22	22	22
f_L' (Hz)	N.A.	N.A.	6000000	N.A.	-	-	N.A.	2.5~65	2.5~65	2	2
f_H' (MHz)	30	30[a, c]	255	1.4	1.9~2.9[c]	2.8	30	0.088~3.35[d]	3~5.8[e]	0.35	2.6
G (dB)	-10~20	0~42[a]	0~40	5~20	0~23.6	0~20	0~14	0~36	0~36	0~23.52	0~23.52
THD (dB)	-	-	-	-	-87.5	-55	-50.5	-52	-56	-47	-47
OIP_3[f] (dBm)	29.2	-	14	30.5	36.2	-	-	33.2	34	24	24
Input Noise (nV/√Hz)	11.2	-	12.5	3	0.54[a]	62	56	21.5[a]	21.5[a]	18[a]	18[a]
Area (mm^2)	0.3	-	0.062	0.25	0.127	0.025	0.052	0.144	0.39	0.028	0.013
P_{diss} (mW)	2.43	1.98[a]	1.56~2.28	0.5	0.28	0.22~0.395	1.044	0.816	0.816	0.172	0.172
FOM[g] (MHz·pF/mW)	N.A.[h]	227.3[a]	N.A.[h]	N.A.[h]	N.A.[h]	N.A.[h]	57.47	2.37~90.32	8.88~156.37	44.77	332.56

[a] Simulated. [b] Conv. App.: Conventional Approach (Fig. 2a without switches shown in blue and controlled with b_i low), App. I: Approach I (Fig. 4 implemented in Fig. 2a without switches shown in blue and controlled with b_i low) and App. II: Approach II (Fig. 2b including switches in blue and controlled with b_i low).
[c] Approximately constant bandwidth. [d] f_H' decreases from 3.35 MHz to 0.088 MHz when gain increases from G_{MIN} to G_{MAX}
[e] f_H' increases from 3.35 MHz (at G_{MIN}) to 5.8 MHz, then for |*G*|>>1, f_H' decreases to 3 MHz (at G_{MAX}) [as discussed in section II-A, remark 3 and section III-A].
[f] $OIP_3=P_0+HD_3/2=P_0-(P_0-P_3)/2$ where P_0 and P_3 (in dBm) are power of fundamental and power of third harmonic respectively.
[g] Figure of Merit $FOM=BW\cdot C_L/P_{diss}$ (MHz·pF/mW) which *BW*, and P_{diss} are the bandwidth and power consumption of bandpass VGA respectively. [h] N.A. since C_L is not given.