Super class AB RFC OTA using nonlinear current mirrors

M. P. Garde, A. J. Lopez-Martin, R. G. Carvajal, J.A. Galan and J. Ramirez-Angulo

An alternative approach to the design of super class AB recycling folded cascode operational transconductance amplifiers is proposed. Instead of using local common-mode feedback for boosting dynamic currents, simple current mirrors with input transistors entering triode region for large currents are employed. Measurement results from a 0.5 µm CMOS test chip validate the proposal.

Introduction: Super Class AB Operational Transconductance Amplifiers (OTAs) are a very attractive solution when power efficiency is required. They feature both very low quiescent current consumption and very high dynamic current boosting, with output currents ideally proportional to V_{id}^4 (with V_{id} the differential input voltage). This is achieved by the use of single-stage topologies where dynamic current boosting is carried out both at the adaptive biasing and active load of the differential pair [1]. Recently super class AB operation has been applied to the Recycling Folded Cascode (RFC) OTA [2], [3]. However, reported super class AB RFC OTAs require additional local common-mode feedback (LCMFB) loops at the active load of the differential pair, either using passive [2] or active [3] matched resistors.

In this Letter we propose an alternative implementation of a super class AB RFC OTA which does not modify the active load. Dynamic current boosting at the active load is achieved just varying the bias point of such load. This approach was formerly applied by the authors to the current mirror OTA in [4] and it is thus extended here to the RFC OTA.

Circuit Description: The conventional Folded Cascode (FC) OTA and RFC OTA [5] are shown in Fig. 1*a* and 1*b*, respectively. Transistors in the differential pair and NMOS current sources have been split in Fig. 1*a* to simplify comparison with Fig. 1*b*. The gain-bandwidth product (GBW) and slew rate (SR) of the FC OTA are

$$GBW_{FC} = \frac{2g_{m1A}}{2\pi C_L} \tag{1}$$

$$SR_{FC} = \frac{2I_B}{C_L} \tag{2}$$

where g_{mi} is the transconductance of transistor M_i. The RFC OTA improves GBW by a factor 1+*K* and SR by a factor *K*, where *K* is the current gain of the NMOS current mirrors in the RFC OTA that replace the NMOS current sources of the FC OTA. However, in practice *K* is not higher than 4 to prevent too much phase margin (PM) degradation [5], so the improvement is limited. Moreover, SR is still proportional to I_B and power efficiency is limited since factor *K* scales both static and dynamic currents. These issues are overcome by the super class AB RFC OTAs in [2], [3], but they require not only an adaptive bias current source but also rearranging transistors M_{3B}-M_{4B} and including two extra local feedback loops that employ two matched resistors. A simpler way to overcome these drawbacks without altering the arrangement of M_{3B}-M_{4B} is proposed here and is shown in Fig. 1*c*.

The adaptive bias current source is the same as in [1]-[3]. It is formed by two cross-coupled Flipped Voltage Followers (FVFs) [1] (M_{1C}-M_{2C} and M_{1D}-M_{2D}) that allow in M_{1A}, M_{1B}, M_{2A} and M_{2B} a well-controlled quiescent current $I_B/2$ and dynamic current not limited by I_B. This adaptive bias is the only topological change in Fig. 1*c* versus the RFC OTA of Fig. 1*b*. The extra dynamic current boosting at the active load of the differential pair is achieved by changing the bias voltage of the cascode transistors M_{3C}-M_{4C}. This new bias voltage V_{BIAS} is chosen so that in quiescent conditions (i.e. with current $I_B/2$ flowing through M_{3B}-M_{3C} and M_{4B}-M_{4C}) transistors M_{3B} and M_{4B} operate in saturation, but close to the ohmic region (with V_{DS} slightly larger than $V_{DS,sat}=V_{GS}-V_{TH}$). Hence, in quiescent and small-signal conditions M_{3A}-M_{3B} and M_{4A}-M_{4B} act as linear current mirrors. However, when $V_{id} > 0$, current I_{2B} in M_{2B} increases, which increases $V_{GS,3C}$. This way, $V_{DS,3B}$ decreases, driving M_{3B} into triode region. As a result the gate voltage of M_{3A}-M_{3B} increases notably, yielding a large current in transistor M_{3A} (which is in saturation region) that is conveyed to the output by M_5 and M_7-M_{10}.

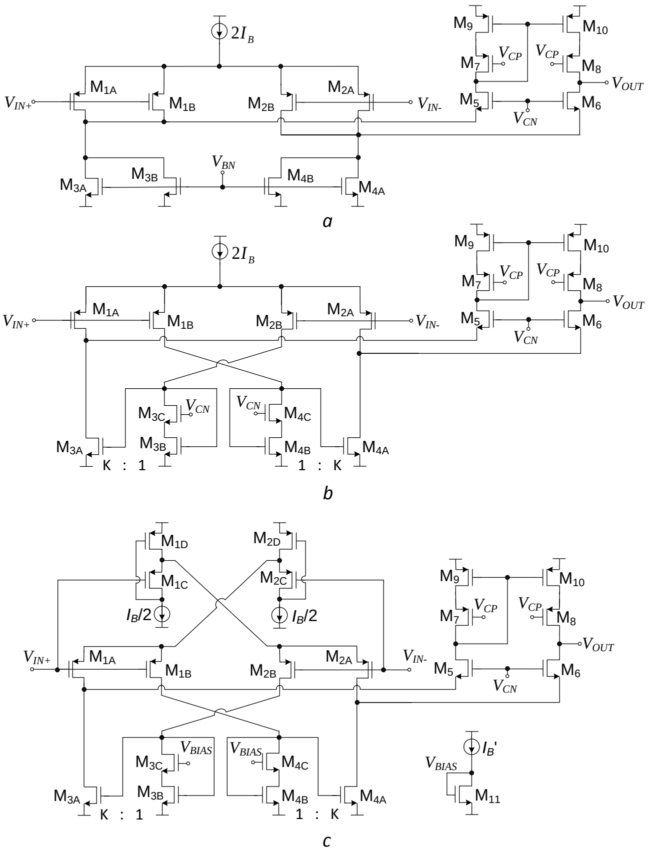

Fig. 1 *Single-stage folded cascode OTAs*
a Conventional class A FC OTA
b RFC OTA
c Proposed super class AB RFC OTA

An approximate analytical expression for the output current I_{out} when $V_{id} > 0$ can be obtained using the simple square-law MOS model for strong inversion and saturation region and the expression for ohmic region and low V_{DS} given by $I_D = \beta\cdot(V_{GS} - V_{TH})\cdot V_{DS}$. The resulting current in M_{3A} is

$$I_{3A} = \frac{\beta_{3A}}{2}\left(\frac{I_{2B}}{\beta_{3B}V_{DS,3B}}\right)^2 \tag{3}$$

where $\beta_i=\mu C_{ox}(W/L)_i$ and $V_{DS,3B} = V_{BIAS} - \sqrt{2I_{2B}/\beta_{3C}} - V_{TH}$. Expressing I_{2B} as a function of V_{id}, current I_{3A} becomes

$$I_{3A} = \frac{\beta_{3A}}{2}\left[\frac{\beta_{2B}}{2\beta_{3B}V_{DS,3B}}\left(\sqrt{\frac{I_B}{\beta_{1B}}} + V_{id}\right)^2\right]^2 \quad . \tag{4}$$

For a large positive differential input step of *A* Volts current in M_{1A} and M_{4A} is very low and M_{2A} enters deep triode region, so $I_{out} \approx I_{3A}$ and

$$SR_{+} \approx \frac{\beta_{3A}}{2C_L}\left[\frac{\beta_{2B}}{2\beta_{3B}V_{DS,3B}}A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{2B}^2}{\beta_{3B}V_{DS,3B}^2}A^4 \quad . \tag{5}$$

Analogously, if $V_{id} < 0$:

$$I_{4A} = \frac{\beta_{4A}}{2}\left[\frac{\beta_{1B}}{2\beta_{4B}V_{DS,4B}}\left(\sqrt{\frac{I_B}{\beta_{2B}}} - V_{id}\right)^2\right]^2 \tag{6}$$

and for a large negative differential input step of -*A* Volts, $I_{out} \approx -I_{4A}$ and

$$SR_{-} \approx \frac{\beta_{4A}}{2C_L}\left[\frac{\beta_{1B}}{2\beta_{4B}V_{DS,4B}}A^2\right]^2 \approx \frac{K}{8C_L}\frac{\beta_{1B}^2}{\beta_{4B}V_{DS,4B}^2}A^4 \quad . \tag{7}$$

In practice SR is lower due to second-order effects not considered in the analysis and since transistors operating in saturation may leave this region for large inputs. Note however that a large SR compatible with low static power is achieved as SR is not proportional to I_B.

A simple and robust way to generate V_{BIAS} is shown in Fig. 1*c*. Choosing I_B' and the *W/L* of M_{11} correctly, $V_{DS3B,4B}$ can be set slightly above $V_{DS,sat}$ regardless of process, temperature or supply voltage variations as V_{BIAS} is set by the V_{GS} of a scaled replica of M_{3B}-M_{4B}.

The adaptive bias current source employed also improves GBW, as the full differential input signal is applied to each input transistor [1].

Measurement Results: The three OTAs of Fig. 1 were included on a 0.5 µm CMOS chip prototype. Transistors M_{1A}, M_{1B}, M_{1C}, M_{2A}, M_{2B}, M_{2C} have an aspect ratio (in µm/µm) of 190/0.6, that of M_{1D}, M_{2D}, M_{3B}, M_{3C}, M_{4B}, M_{4C} is 60/0.6, M_{3A}, M_{4A} have 180/0.6, that of M_5, M_6 is 120/0.6, that of M_7, M_8, M_9, M_{10} is 200/0.6 and that of M_{11} is 15/0.6. Fig. 2 shows a microphotograph of the OTAs in Fig. 1. Supply voltage was set to ±1 V, $I_B = I_B' = 10\ \mu A$, $V_{CP} = -0.5$ V and $V_{CN} = 0.3$ V.

The measured transient response in voltage follower configuration of the three OTAs is shown in Fig. 3. An external load capacitor of 47 pF was connected. However, including the capacitance of the test setup (pad, board and test probe), the overall load capacitance is $C_L \approx 70$ pF. The input signal was a 1 MHz 0.5 V periodic square wave, whose DC level was -0.6 V. Table 1 summarizes the main measured performance parameters. Note an improved SR by a factor of 28 versus the FC OTA.

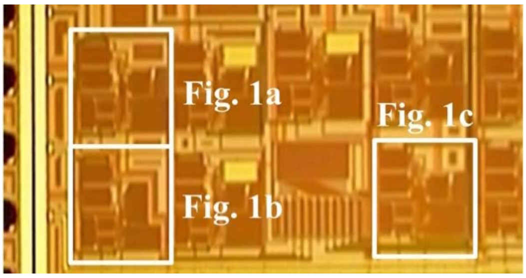

Fig. 2 *Microphotograph of the OTAs of Fig. 1*

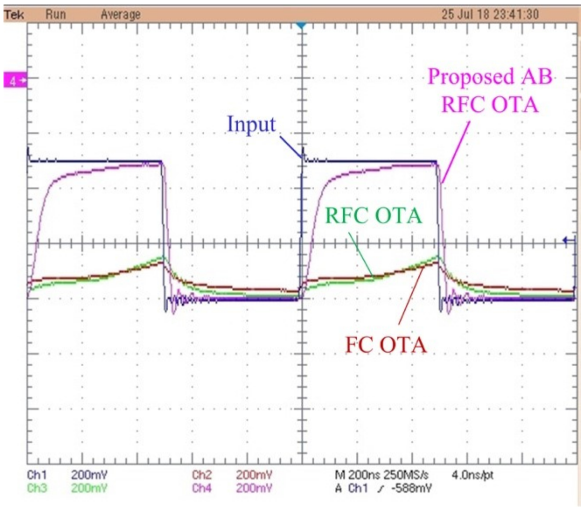

Fig. 3 *Measured transient response of the OTAs of Fig. 1*

Table 1: Measured performance summary ($C_L = 70$ pF)

Parameter	Fig. 1a	Fig. 1b	Fig. 1c
SR+	0.26 V/µs	0.48 V/µs	7.27 V/µs
SR-	-0.86 V/µs	-1.5 V/µs	-18.8 V/µs
THD @25kHz, 0.5V_{pp}	-37.81 dB	-44.54 dB	-47.85 dB
DC gain (*)	60.26 dB	68.37 dB	75.06 dB
PM (*)	89º	86.62º	76.34º
GBW	480 kHz	950 kHz	3.4 MHz
CMRR @ DC	97 dB	111 dB	112 dB
PSRR+ @ DC	73 dB	82 dB	89 dB
PSRR- @ DC	93 dB	104 dB	105 dB
Eq. input noise @1MHz	49 nV/√Hz	35 nV/√Hz	22 nV/√Hz
Power	80 µW	80 µW	100 µW
Area	0.020 mm^2	0.024 mm^2	0.026 mm^2

(*) Simulation

In order to compare with other class AB amplifiers, two conventional figures of merit (FoM) are used: $FoM_L = SR \cdot C_L / I_{supply} = I_{maxL}/I_{supply}$, where I_{supply} is the total static current consumption, and $FoM_S = GBW \cdot C_L / I_{supply}$ (MHz·pF/mA). Note that the proposed OTA shows competitive small-signal and large-signal performance.

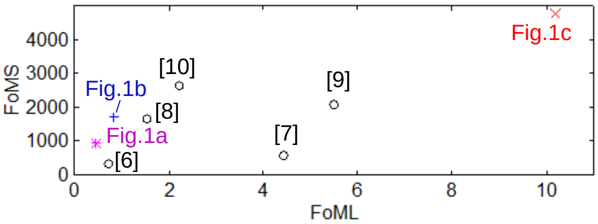

Fig. 5 *Performance comparison*

Conclusion: Proper biasing of the differential pair active load in the RFC OTA can provide dynamic current boosting in a simple way. Together with an adaptive biasing current source, efficient super class AB operation can be achieved.

Acknowledgments: This work was funded by the Spanish Ministerio de Economía y Competitividad (grant TEC2016-80396-C2-1-R)

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