Sustainable Energy, Grids and Networks 32 (2022) 100911

Contents lists available at ScienceDirect

Sustainable Energy, Grids and Networks

journal homepage: www.elsevier.com/locate/segan

Energy management in Converter-Interfaced Renewable Energy Sources through ultracapacitors for provision of ancillary services

Andrei Mihai Gross [a], Kyriaki-Nefeli Malamaki [b], Manuel Barragán-Villarejo [a,*], Georgios C. Kryonidis [b], Francisco Jesús Matas-Díaz [a], Spyros I. Gkavanoudis [b], Juan Manuel Mauricio [a], José María Maza-Ortega [a], Charis S. Demoulias [b]

[a] Department of Electrical Engineering, Universidad de Sevilla, Sevilla, Spain
[b] Department of Electrical and Computer Engineering, Aristotle University of Thessaloniki, Thessaloniki, Greece

ARTICLE INFO

Article history:
Received 23 March 2022
Received in revised form 24 July 2022
Accepted 9 August 2022
Available online 20 August 2022

Keywords:
Ancillary services
Energy storage systems
Renewable energy source
Renewable generation
Ultracapacitors
Voltage source converters

ABSTRACT

The ever-growing penetration of Converter-Interfaced Renewable Energy Sources (CI-RES) and the gradual decommission of synchronous generators (SGs) are posing several challenges to guarantee the stability and robustness of the electric power system. A possible solution to overcome the foreseen problems is to enable the provision of ancillary services (AS) by advanced CI-RES emulating the SG performance. However, given the fact that most of the CI-RES operate at maximum power point, it will be required to rely on energy storage systems (ESS) to deal with active power related ASs. The ESS integration can be done in a straightforward manner within the CI-RES DC bus by means of a DC/DC converter. It is required, however, an adequate DC energy management to properly control the DC bus voltage, the ESS energy and the power delivered to the grid by the primary power source. This is a major challenge which must be solved to unlock the AS provision by means of CI-RES. With this regard, the main contribution of the paper is the design of an energy management system to simultaneously regulate the CI-RES DC bus voltage using the UC and also maintain the UC voltage within their safety limits while a given AS is provided. The control strategy is validated experimentally using a prototype with results that reveal a reliable and stable operation.

© 2022 The Author(s). Published by Elsevier Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

1. Introduction

During the past two decades, the new advances in Renewable Energy Sources (RES) have initiated a major shift towards a decentralized, decarbonized non-synchronous generation. This shift is further encouraged by the European Union with proposals concerning the 2030 Climate & Energy Package, aiming to achieve an increase of 32% of RES penetration and a reduction of 40% in greenhouse gas emissions, both with respect 1990, until 2030 [1]. As the level of the Converter-Interfaced RES (CI-RES) increases displacing conventional synchronous generation units, several serious problems are revealed related to the dynamic performance and stability of the power system. These problems stem from the intermittent nature of the primary energy source, wind and sun mainly, as well as the power electronic interface with the grid which significantly differs from a conventional synchronous generator. It is worth noting that CI-RES are operated to extract the maximum possible power from the primary energy source and, therefore, without any reserve to provide an extra power if required. In addition, Voltage Source Converters (VSCs) are static devices which do not provide any inherent inertia. On the bright side, the VSCs have an important control capability which can be used for solving these problems. Recently, several VSC control algorithms have been proposed in the technical literature with the aim of mimicking the performance of a synchronous generator. In this way, these new CI-RES controllers enable the provision of ASs to the network such as: primary frequency regulation (PFR), i.e. operation with *P-f* droop [2,3]; ramp-rate limitation (RRL), also referred as power smoothing (PS) [4,5]; fault-ride through (FRT) capability [6]; and virtual inertia (VI) [7–10] which will help the operation and stability of the future CI-RES dominated power system.

ASs involving active power injection deserve special consideration since CI-RES are usually operated at its maximum power point (MPP). Therefore, two alternatives are possible: operation below the MPP or integration of an energy storage systems (ESS). Evidently the choice depends on technical and economic decisions. From a technical point of view, the operation below the MPP prevents the AS provision in case of no RES power, e.g. PV plants during the nights. Evidently, the operation below the MPP reduces the incomes of the CI-RES owner but the ESS integration

* Corresponding author.
E-mail address: manuelbarragan@us.es (M. Barragán-Villarejo).

https://doi.org/10.1016/j.segan.2022.100911
2352-4677/© 2022 The Author(s). Published by Elsevier Ltd. This is an open access article under the CC BY license (http://creativecommons.org/licenses/by/4.0/).

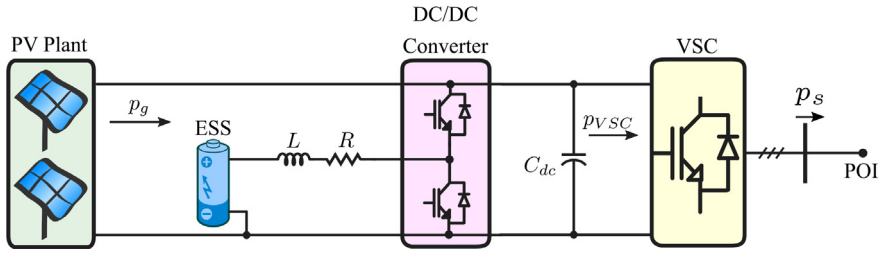

Fig. 1. CI-DRES comprising an ESS interfaced with a DC/DC converter.

requires an additional initial investment. The best option considering this economic point of view is difficult to assess, since the markets related to most of the ASs previously described do not exist nowadays. It has to be considered, however, that the extra active power required for AS provision is estimated about 10% of the CI-RES rated power [11], which certainly limits the additional investment [12]. This fact, in addition to the availability of providing the AS irrespective of the RES power, makes the use ESS a competitive option. The most suitable ESS technology depends on the type of AS to be provided. For fast-response ASs, such as VI or RRL, a short-term ESS like an ultracapacitor (UC) is appropriate. On the contrary, electrochemical batteries (BESS) are preferred for slow-response ASs which may require higher energy amounts, such as PFR.

An efficient way to integrate the ESS into a CI-RES, like the PV inverter shown in Fig. 1, is to use a DC/DC converter [13]. This setup, however, will require an adequate Energy Management System (EMS) in charge of controlling the power balance in the DC bus to guarantee a constant DC voltage while operating the ESS in a safely and reliable manner.

Two possible alternatives can be adopted taking into account that the EMS may set the power references of the VSC and the DC/DC converter. The first option relies on controlling the DC bus voltage with the VSC by setting an adequate active power reference while the DC/DC converter is controlled to provide the required AS [14]. Communications latency is critical in this proposal since the additional active power required for the AS provision must be commanded to the DC/DC converter interfacing the ESS. This is especially relevant in fast ASs like VI, where a high performance is achieved only if the reaction time is in the order of milliseconds [15]. Therefore, the main drawback of this control scheme is that it lacks a full controllability of the Point of Interconnection (POI) active power, preventing a precise synchronous generator emulation. To overcome this shortcoming, the second option is based on controlling the DC bus voltage with the ESS, thus, providing a total VSC controllability [6,16]. In this strategy, the extra energy required for the AS provision is naturally provided by the ESS without no fast communication requirements. Moreover, this strategy has a significant advantage over the first option. Any CI-RES with a VSC control strategy emulating a VSG, which may provide active power ASs, may integrate in a straightforward manner without modifying the VSC control. This is because most of these VSG strategies assume a voltage source [17–19] or a large ESS [20] connected to the DC bus, which maintain the DC bus voltage and provides the required active power. Therefore, no changes are required in the VSC control since the UC maintains de DC voltage. Nevertheless, this proposal has certain limitations since the DC bus voltage regulation depends on an ESS which may have a limited storage energy. In this case, the EMS has to control the state of charge (SoC) of the ESS to avoid any operation out of the technical limits which may jeopardize the CI-RES safe operation.

Previous works have dealt with EMS applications to BESS and UC. However, the EMS for a grid-connected CI-RES with a ESS providing ASs has not been properly addressed in the existing literature. In [21], the authors propose voltage and frequency regulation by means of a virtual excitation. A power management system is applied to coordinate the current sharing between the grid and the ESS but the VI is not integrated with the EMS and just simulation results are presented. A BESS SoC recovery after a PFR event has been addressed for grid-connected applications [22] and islanded microgrids [23]. The BESS performance in case of providing RRL has been analyzed in [14] including some SoC control methods aimed to return to a 50% SoC after this AS provision. These studies, however, focus mainly on the RRL provision rather than on the BESS SoC restoration. On the contrary, little attention has been paid on the UC SoC control, in spite of being a crucial issue given the limited storage energy related to this ESS technology. In [24], a control scheme for the UC SoC control is proposed to return the SoC within the 45%–55% after providing a RRL service. Similarly, a proportional controller is proposed in [6] to restore the UC SoC to 50% after performing RRL or FRT service. A hierarchical three-layer controller to manage the UC storage energy within a safe operating zone has been presented in [25]. However, this strategy does not consider the converter power losses and some crucial practical issues such as the required control actions to protect the UC in the case of the operational limits are reached. A most complete EMS with ASs provision can be found in [15] particularized for a BESS. In this work, a variable proportional gain is proposed as a function of the battery SoC, which is variable over the entire battery operating range. The main disadvantage of this approach is that the EMS and ASs provision performance is highly dependent on the communications between the DC/DC and DC/AC converter. Therefore, to the authors' best knowledge, there is a gap in the current state of the art addressing a control algorithm to provide a nearly ideal AS while maintaining the UC SoC throughout its operation range.

The main contribution of this paper is to propose an efficient EMS for a CI-RES comprising an UC that emulates a synchronous generator with capability of providing AS. The EMS is designed to give almost ideal ASs, operating the UC within their technical limits and, after the AS event, return the UC to its reference SoC as soon as possible. In addition, the proposed strategy guarantees stable control of the common DC bus through the UC. Due to the UC energy limitations, the EMS is in charge of controlling the UC SoC but this just require a low-latency communication channel to command the DC/DC controller adequate control actions. Finally, it is important to highlight that this paper has the following contributions with respect to [26]:

- A detailed description of the three-level hierarchical EMS including all the controllers and the main variables involved in the UC SoC control.
- A new energy control scheme for the UC EMS based on the UC voltage. More specifically, three areas of operation are defined depending on the UC voltage: safe area, warning area and unsafe area. The required UC energy to provide an AS is released or restricted depending on the UC voltage

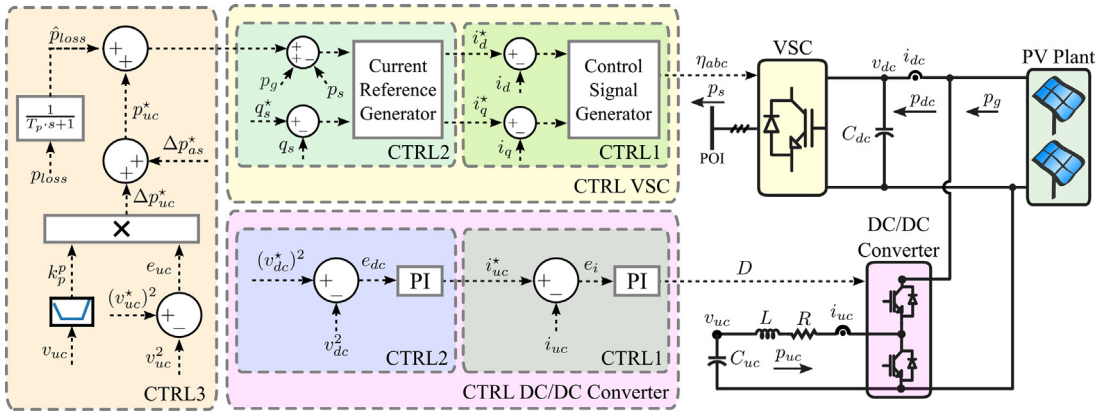

Fig. 2. EMS hierarchical control scheme.

in order to maintain the CI-RES controllability. With this new approach, a more robust performance is ensured compared to the control scheme of [26], being the safety limits conveniently respected.

- New experimental results aiming to validate the new energy management of the UC voltage.

The rest of the paper is organized as follows. Section 2 presents the EMS control structure. Section 3 describes the prototype used for the experimental validation of the control strategy and discusses the EMS performance via the obtained results. Finally, Section 4 closes the paper with the main conclusions.

2. EMS control strategy

The EMS is composed of a hierarchical three-level control structure as depicted in Fig. 2. The inner control layers, CTRL 1 and CTRL2, are tailored for the VSC and the DC/DC converter while the outer one, CTRL3, manages the DC bus power balance.

Regarding the VSC, CTRL1 and CTRL2 follow a traditional control structure: CTRL1 is a conventional current control loop in charge of tracking the current reference generated by CTRL2 from the active and reactive power references. For this work, a virtual synchronous generator as presented in [27] is implemented in CTRL2.

In the case of the DC/DC converter, CTRL1 and CTRL2 are used to control the VSC DC bus voltage through a classic cascade control: CTRL1 regulates the UC current considering the current reference provided by CTRL2 in order to regulate the DC bus voltage. Meanwhile, the third control loop aims to maintain the UC voltage and, therefore, its SoC, within the technical limits recommended by the manufacturer. For this purpose, three operational areas depending on the UC voltage have been defined, where the controller priority to provide the AS is adjusted in order to maintain a reliable and safe operation.

The following subsections are devoted to give the details of the controllers affecting the UC operation.

2.1. UC current control loop (CTRL1)

This layer corresponds to the inner control loop of the UC cascade controller. Its aim is to generate the duty ratio of the DC/DC converter, D, to properly control the UC current according to its reference value, $i^{\star}_{uc}$, computed by CTRL2. The implemented control law is a proportional and integral (PI) controller which is designed considering the average model of the DC/DC converter:

$$v_{uc} = R \cdot i_{uc} + L \cdot \frac{di_{uc}}{dt} + v_{dc} \cdot D, \tag{1}$$

where v_{uc} and i_{uc} are the UC voltage and current respectively, v_{dc} is the VSC DC bus voltage and L, R are the inductance and the internal resistance of the DC filter respectively. Therefore, the duty ratio of the DC/DC converter can be computed as:

$$D = \frac{v_{uc} - k^i_p \left(i^{\star}_{uc} - i_{uc}\right) - k^i_i \int \left(i^{\star}_{uc} - i_{uc}\right) dt}{v_{dc}}, \tag{2}$$

where k^i_p and k^i_i are the proportional and the integral gains of the PI controller respectively. These are designed by defining a desired closed-loop time constant τ_i as: $k^i_p = L/\tau_i$ and $k^i_i = R/\tau_i$ [28]. This approach provides a first-order closed-loop response of the controller with a time constant τ_i as long as L and R match their actual physical values. Due to the uncertainty of these model parameters, these theoretical PI gains are a starting point for tuning the controller of the experimental setup, further details provided in Section 3.2.1.

2.2. DC bus voltage control loop (CTRL2)

This layer corresponds to the outer control loop of the cascade controller being in charge of the DC bus voltage regulation. The controller design relies on the DC bus power balance which, according to the references shown in Fig. 2, can be formulated as:

$$p_{uc} + p_g = p_c + p_s + p_{loss} \tag{3}$$

where p_{uc} is the injected UC power, p_g is the power of the primary energy source, p_c is the power of the DC bus capacitor, p_s is the POI active power and p_{loss} groups all the system power losses (DC/DC converter, VSC and coupling filters of the UC and VSC).

Note that p_c and p_{uc} can be formulated as a function of the corresponding voltages and currents as:

$$i_{uc} \cdot v_{uc} + p_g = \frac{C_{dc}}{2} \frac{dv^2_{dc}}{dt} + p_s + p_{loss} \tag{4}$$

This equation relates the UC current with the DC voltage and, therefore, it can be considered as the CTRL2 plant. As a result, the following PI controller can be applied to compute the required reference current $i^{\star}_{uc}$ for CTRL1:

$$i^{\star}_{uc} = \frac{k^v_p \left(v^{\star 2}_{dc} - v^2_{dc}\right) + k^v_i \int \left(v^{\star 2}_{dc} - v^2_{dc}\right) dt}{v_{uc}}, \tag{5}$$

where k^v_p and k^v_i are the proportional and the integral gains respectively and $v^{\star}_{dc}$ is the DC bus reference voltage. Note that the terms p_g, p_s and p_{loss} are considered system perturbations and, therefore, their dynamics are ignored in (5). Nevertheless, it should be possible to include them as feed-forward signals to improve the dynamic performance of the DC bus voltage if

required. In this way, the capacitor $C_{dc}/2$ is the only element with dynamics in (4). The control gains k_p^v and k_i^v are set to achieve a first-order closed-loop response of CTRL2 with a time constant τ_v: $k_p^v = C_{dc}/(2 \cdot \tau_v)$ and $k_i^v = 0$. These theoretical values are adjusted in the experimental testing using the procedure explained in 3.2.1.

2.3. UC voltage control loop (CTRL3)

This control level must satisfy two counterpart objectives simultaneously: (i) provide an adequate UC energy release according to the required AS and (ii) maintain the UC SoC, i.e. the UC voltage, within its technical limits. As a result, the UC power reference, $p_{uc}^\star$, can be formulated as:

$$p_{uc}^\star = p_{as}^\star + \Delta p_{uc}^\star \tag{6}$$

where $p_{as}^\star$ and $\Delta p_{uc}^\star$ corresponds to each of the aforementioned objectives respectively. As discussed in the introduction, this paper focuses on the UC energy management rather than on the AS provision. For this reason, it is considered that the term $p_{as}^\star$ will be provided by a suitable algorithm depending on the considered AS [4,5,10,29]. In addition, it is worth noting that both power terms are counterpart since the AS provision will require an UC energy which will lead to its voltage variation. This means that the UC voltage control algorithm should be flexible enough to provide the energy required by the AS provision but, at the same time, achieve a safe UC operation within its technical limits. As a result, it is proposed to apply a proportional controller:

$$\Delta p_{uc}^\star = k_p^p \cdot \left(v_{uc}^2 - v_{uc}^{\star 2}\right) \tag{7}$$

where the proportional gain k_p^p depends on the UC voltage. Particularly, three operational areas has been defined as a function of the UC voltage:

- Safe operation area: $[v_{uc}^l, v_{uc}^h]$.
- Warning operation area: $[v_{uc}^{min}, v_{uc}^l]$ and $[v_{uc}^h, v_{uc}^{max}]$.
- Unsafe operation area: $[0, v_{uc}^l]$ and $[v_{uc}^{max}, -]$.

The values v_{uc}^l, v_{uc}^h, v_{uc}^{min} and v_{uc}^{max} are selected according to the manufacturer's technical and operational restrictions. The priority within the safe operation zone is to provide the AS as close as possible to the reference one. For this reason, considering that the UC voltage is under control, the proportional gain should be as reduced as possible. On the contrary, within the warning operation area the AS provision is sidelined since the priority is to restore the UC voltage within the safe zone. As a result, the proportional gain should be incremented depending on the voltage deviation. Finally, in the case of the control actions are not enough to maintain the UC operation within the safe and warning areas, the system is disconnected to avoid any damage on the involved power components. Therefore, the proposed proportional gain can be formulated as a piece-wise linear function of the UC voltage as shown in Fig. 3 :

$$k_p^p = \begin{cases} k_{p0}^p + m_{pl}^p(v_{uc}^l - v_{uc}) & v_{uc} \in [v_{uc}^{min}, v_{uc}^l] \\ k_{p0}^p & v_{uc} \in [v_{uc}^l, v_{uc}^h] \\ k_{p0}^p + m_{ph}^p(v_{uc} - v_{uc}^h) & v_{uc} \in [v_{uc}^h, v_{uc}^{max}] \end{cases} \tag{8}$$

where the parameters k_{p0}^p, m_{pl}^p and m_{ph}^p can be adjusted according to the application requirements. The value of proportional gain k_{p0}^p is calculated as: $k_p^{p0} = C_{uc}/(2 \cdot \tau_{uc})$, where τ_{uc} is the closed-loop time constant of this control level. The computation of this gain is obtained by relating the UC power and its voltage:

$$p_{uc} = i_{uc} \cdot v_{uc} = \frac{C_{uc}}{2}\frac{dv_{uc}^2}{dt}, \tag{9}$$

and establishing a first-order closed-loop response of the controller with the desired time constant τ_{uc}. This theoretical value is readjusted in the experimental setup according to the procedure outlined in Section 3.2.1. The rest of the parameters, m_{pl}^p and m_{ph}^p, are defined considering that the term $\Delta p_{uc}^\star$ is able to compensate the maximum AS power demand $p_{as}^{\star max}$ at the limits of the warning area, i.e. v_{uc}^{min} and v_{uc}^{max}. In this manner, the proportional gain at these UC voltages can be computed as:

$$k_p^p(v_{uc}^{min}) = \frac{p_{as}^{\star max}}{{v_{uc}^\star}^2 - v_{uc}^{min2}} \qquad k_p^p(v_{uc}^{max}) = \frac{p_{as}^{\star max}}{v_{uc}^{max2} - {v_{uc}^\star}^2} \tag{10}$$

Therefore, the parameters m_{ph}^p and m_{pl}^p are derived considering the proportional gain within the safe area, k_{p0}^p, as:

$$m_{pl} = \frac{k_p^p(v_{uc}^{min}) - k_{p0}^p}{v_{uc}^l - v_{uc}^{min}} \qquad m_{ph} = \frac{k_p^p(v_{uc}^{max}) - k_{p0}^p}{v_{uc}^{max} - v_{uc}^h} \tag{11}$$

Finally, and once the UC energy recovery power term has been defined, it is possible to set the VSC active power reference as:

$$p_s^\star = p_g + p_{as}^\star + \Delta p_{uc}^\star - \hat{p}_{loss}. \tag{12}$$

where $\hat{p}_{loss}$ is an estimation of the CI-RES steady-state power losses, which can be computed applying a low-pass filter to the power balance Eq. (3):

$$\hat{p}_{loss} = \frac{1}{T_p s + 1} p_{loss} = \frac{1}{T_p s + 1}(p_{uc} + p_g - p_s). \tag{13}$$

where T_p is the filter time constant. In this way, the VSC takes care of the steady-state power losses releasing the UC of this task. Note, however, that the compensation refers just to the steady-state power losses due to the application of the low-pass filter. This means that during the provision of a fast AS the actual power losses are compensated by the UC and, therefore, it will be possible to provide accurate ASs. Eq. (12) allows to establish the POI active power considering simultaneously the AS provision while maintaining a reliable and safe UC operation.

3. Experimental validation

3.1. Experimental setup

The hierarchical control structure of the EMS presented in the previous section has been tested in the experimental setup depicted in Fig. 4. This setup is composed of the following components:

- A three-phase three-wire VSC with the AC side coupled through a LCL filter to an AC controllable voltage source. This power converter is in charge of setting the power $p_s^\star$ and its control strategy is based on a virtual synchronous generator [27]. Therefore, it has the capacity of reacting under frequency events injecting/absorbing an extra power term, $p_{as}^\star$, in (6) to provide, among others, VI.
- An UC connected to the VSC DC bus through an inductive filter and the corresponding DC/DC converter.
- A controllable DC current source connected to the VSC DC bus which is responsible of emulating the RES power.

The VSC and the DC/DC converter are integrated in a common power electronic stack (four-leg VSC) to achieve a compact design. This enables the use of a single control board for both devices where all the analog measurements and the corresponding IGBT switching signals are centralized. This facilitates the data exchange between the different control layers since all of them are integrated within the same microcontroller, a TMS320F28335 Delfino provided by Texas Instruments with a sampling frequency

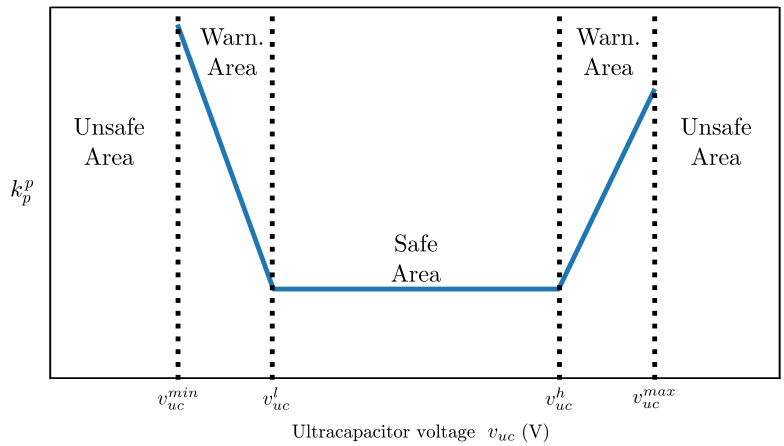

Fig. 3. Proportional gain k_p^p of the UC voltage controller as a function of the UC voltage.

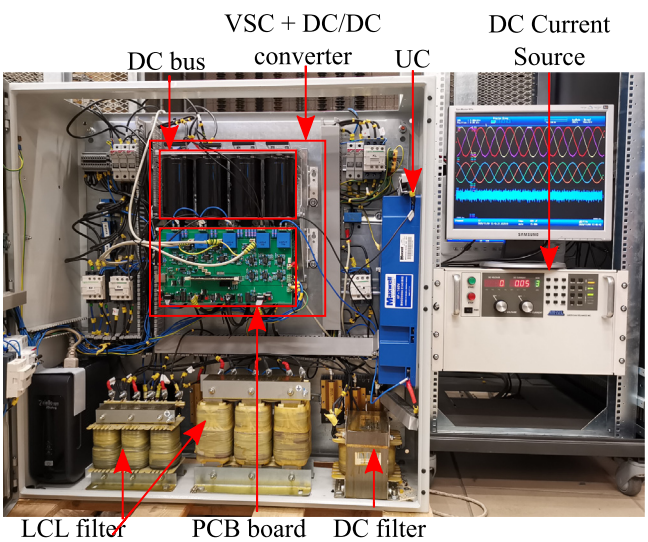

Fig. 4. Laboratory experimental testbed.

Table 1
Parameters of the experimental setup.

Parameter	Value
DC bus voltage (v_{dc}^{hv})	750 V
RMS AC VSC rated voltage	400 V
VSC rated power	20 kVA
VSC and DC/DC converter switching frequency	10 kHz
VSC side AC filter inductance	1.25 mH
Grid side AC filter inductance	1.25 mH
AC filter capacitance (C)	4 μF
DC/DC converter rated power	10 kW
DC/DC converter filter inductance (L_{dc})	3 mH
DC bus capacitor (C_{dc})	2200 μF
DC UC rated voltage	160 V
UC capacitance	6 F
Controllable DC source rated power	30 kW

of 20 kHz. The rated values of all the hardware components of this experimental testbed are summarized in Table 1. The influence of the proportional gain k_p^p within CTRL3 will be analyzed in the discussion of the experimental results.

3.2. Experimental results

This section is devoted to provide the results of two types of tests:

Table 2
Comparison of the theoretical and experimental gains of each control layer.

Gains	Theoretical value	Experimental value	Relative error (%)
τ_i	1 ms	0.907 ms	9.3%
k_p^i	3	3	0%
k_i^i	94.2478	120	27%
τ_v	25 ms	27.92 ms	8%
k_p^v	0.0878	0.0878	0%
k_i^v	0	0.1829	–
τ_{uc}	40 s	37.5 s	7.14%
k_p^{p0}	0.075	0.075	0%

- Experimental validation of each control level. For this purpose, each control layer is tested by executing a step change of its corresponding setpoint. This allows to evaluate the dynamic performance and steady-state error of each controller.
- Analysis of the proposed EMS within the safe and warning operation areas in case of a frequency variation in the AC source. This event causes an UC energy release to provide VI. In this way, it is possible to assess the impact that the UC SoC may have in the AS provision.

3.2.1. Experimental validation of each control level

The dynamic response of each control level is evaluated in the experimental prototype by means of a step change of their corresponding setpoints. These tests are performed from the inner to the outer control loops, considering the controller gains computed according Section 2 and collected in Table 2. This table also shows the final values of the controller gains in the experimental prototype which have been tuned online to achieve the desired dynamic response. The results obtained for each control layer is summarized as follows:

CTRL1 (UC current control loop). The hardware setup consists just on the DC/DC converter which couples the UC with a high voltage DC bus. The UC is precharged to $v_{uc} = 130$ V and the DC bus voltage is set to $v_{dc} = 740$ V during the test. A reference step change from -5 to 0 A is applied to the reference current $i_{uc}^{\star}$ at $t = 0.025$ ms with the results shown in Fig. 5. The UC current, i_{uc}, follows a first-order dynamic response with a good tracking of its reference, $i_{uc}^{\star}$, and a null steady-state error. Moreover, the current time constant in the experimental prototype is $\tau_i = 0.907$ ms, which is very close to the theoretical value. According to Table 2, the integral gain presents the larger discrepancy between its

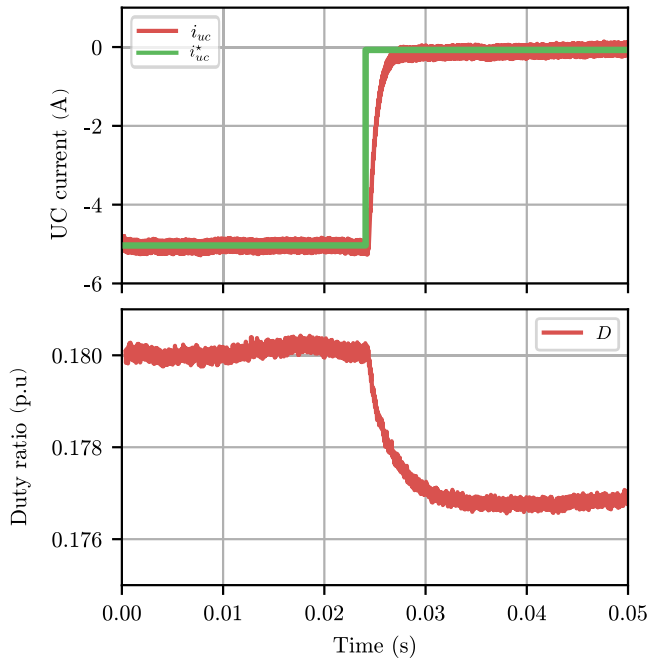

Fig. 5. CTRL1 dynamic response with a reference step change of $i^{\star}_{uc}$ from −5 to 0. Top plot: UC current i_{uc}. Bottom plot: DC/DC converter duty ratio D.

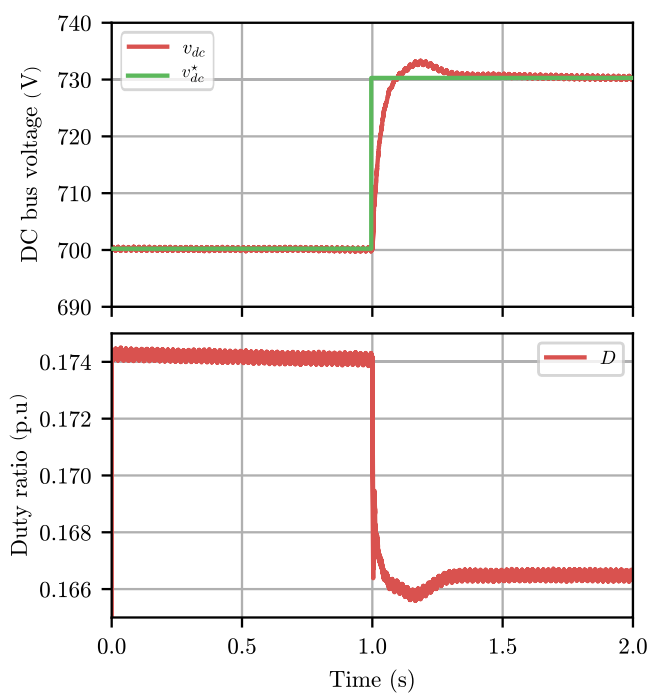

Fig. 6. CTRL2 dynamic response with a reference step change of $v^{\star}_{dc}$ from 730 to 700. Top plot: DC voltage v_{dc}. Bottom plot: DC/DC converter duty ratio D.

theoretical and experimental value. This is due to the uncertainty on the value of the coupling filter resistor, which is quite low and depends on installation factors and other variables like the temperature. In any case, theoretical and experimental values of the integral gain are within the same order of magnitude. The evolution of the duty ratio, D, during this test is depicted in the bottom plot of Fig. 5, which evolves as expected following a first-order dynamic response.

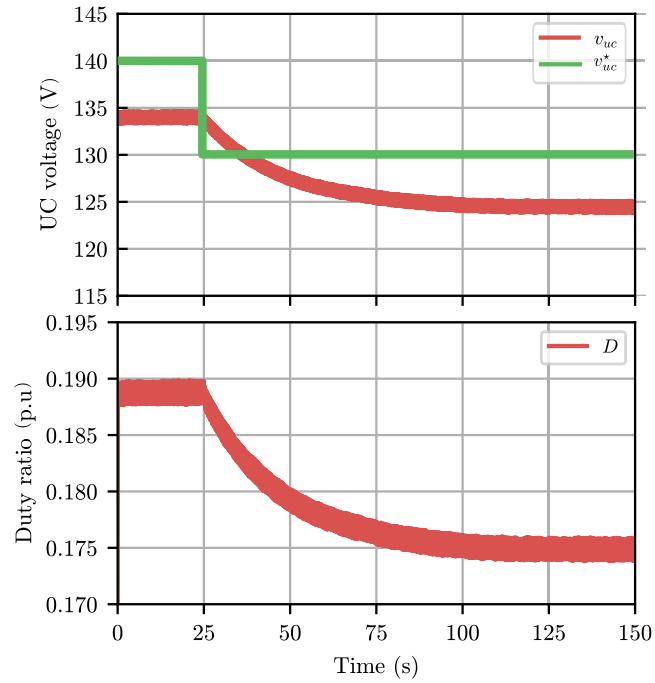

Fig. 7. CTRL3 dynamic response with a reference step change of $v^{\star}_{uc}$ from 140 to 130. Top plot: UC voltage v_{uc}. Bottom plot: DC/DC converter duty ratio D.

CTRL2 (DC bus voltage control loop) . The hardware setup in this test is exactly the same than the previous one but removing the DC voltage source in charge of maintaining the DC bus voltage. A reference step change of $v^{\star}_{dc}$ from 700 V to 730 V is applied to CTRL2 at $t = 1$ s with the results shown in the top plot of Fig. 6. Note that the response corresponds to a second-order system rather than the theoretical first-order dynamics imposed in the CTRL2 design. This is due to inaccuracies of the plant model which is not able to reproduce all the dynamics within the actual plant. It has to be considered, however, that a smooth dynamic response is achieved with an overshoot less than 10%, a damping ratio higher than 30% and a settling time of 2% in 310 ms. In addition, the time to achieve the 63.2% of the steady-state value is 27.92 ms which is very close to the time constant τ_v in the theoretical computation. Again, the integral gain presents the larger discrepancy between the theoretical and experimental values. Particularly, its value has been tuner to achieve a zero steady-state error due to the uncertainty in some system parameters as discussed previously. The duty ratio D is shown in the bottom plot of Fig. 6 which follows the same second-order response of the DC bus voltage v_{dc}.

CTRL3 (UC voltage control loop). The experimental setup comprises the DC/DC converter and the VSC which is connected to a three-phase voltage source which maintains 400 V and 50 Hz. The primary energy source is emulated with a DC source and the reference DC bus is set to 730 V. Considering this experimental setup, two tests are performed:

- Reference step change of the UC voltage $v^{\star}_{uc}$ from 140 to 130 V. Fig. 7 shows the dynamic performance of the voltage v_{uc} and the DC/DC converter duty ratio. The controller perfectly fulfills the design criteria since the UC voltage follows a first-order dynamics and a non-null steady-state error. Note that CTRL3 is just based on a proportional gain and, therefore, it is not possible to achieve a null steady-state error. In any case, this error could be reduced by increasing k_p^{p0} at the

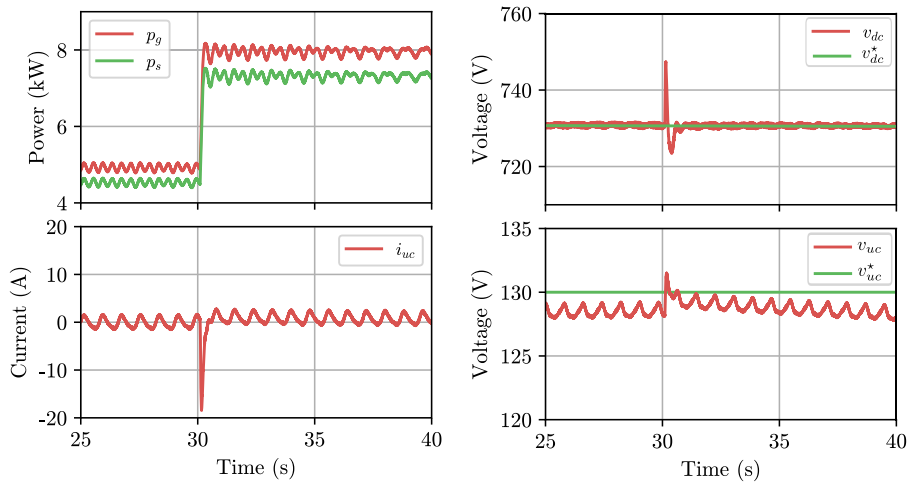

Fig. 8. CTRL3 dynamic response with a large perturbation of the RES power p_g. Left Top plot: RES and POI power p_g and p_s. Left Bottom plot: UC current i_{uc}. Right Top plot: DC bus voltage v_{dc}. Right Bottom plot: UC voltage v_{uc}.

cost of affecting the AS provision, as will be discussed later. Finally, the time constant $\tau_{uc} = 37.5$ s which is very close to its theoretical value.

- Large perturbation on the RES power p_g which increases from 5 kW to 8 kW. Fig. 8 shows the dynamic performance of the different magnitudes. The additional RES power produces almost immediately an increase of the DC bus voltage as shown in the right top plot of Fig. 8. However, CTRL2 acts quickly to return the DC bus voltage to its reference value according to the dynamic response analyzed in Fig. 6. Due to the fast action of CTRL2, the DC voltage increases less than 15 V and returns to its reference value in less than a second. This performance is achieved because the UC absorbs the required power to discharge the DC bus voltage. In fact, the UC current i_{uc} is negative, meaning that the UC is charging as shown in the right bottom plot of Fig. 8. The UC voltage increase is corrected by CTRL3, which progressively discharges the UC to restore its reference voltage as can be noticed from $t = 30$ s onwards. Note that the UC current is positive but not very large because the CTRL3 objective is to return to the UC reference voltage in a smooth manner.

Therefore, the results of these individual tests evidence the adequacy of the controller design process since the controller performance follows the imposed dynamics using controller gains close to the corresponding theoretical values.

3.2.2. Operation within the safe area

These tests consists of studying the influence of the CTRL3 proportional gain k_p^p within the safe operation zone. The time constant of the low-pass filter used for estimating the steady-state power losses has been set to 15 s. Regarding the UC voltage limits, the safe operation area has been set within the interval $[v_{uc}^l, v_{uc}^h] = [115\text{ V}, 145\text{ V}]$ considering that the UC rated voltage is 160 V. In order to avoid continuous transitions between the safe and warning operation zones, a dead-band of $\pm$ 2.5 V has been added.

All the tests have been carried under the same AS provision. This consists on generating a negative frequency variation at the POI with the AC controllable voltage source. In case of implementing a virtual synchronous generator in the VSC controller, this frequency perturbation will lead to an ideal stepped inertial response in $p_{as}^\star$ with an amplitude depending on the rate of change of frequency (RoCoF) and the VI constant. All the tests have considered that the additional power injection, $p_{as}^\star$, due to the frequency variation equals to 2 kW. In addition, all the test have been performed considering a constant RES power injection equal to 6.5 kW.

Fig. 9 represents the active power p_s, p_g and p_{uc} for different values of k_p^p along with the ideal stepped response corresponding to a given frequency perturbation. At the beginning of the test, the system is in steady-state and all the powers for the different proportional gains are similar. It can be observed that p_g is almost identical to p_s and p_{uc} is null because the DC bus voltage and the UC voltage are under control as shown in Fig. 10. The power difference between p_g and p_s corresponds to the converter power losses. Around the time instant $t = 19$ s, the frequency event is activated in the AC controllable voltage source and the power p_s drastically increases from 6 kW to almost 8 kW. It can be observed that the lower k_p^p the closer performance to the ideal response. In fact, as the frequency event advances in time, the power corresponding to the AS provision is progressively reduced with respect to the ideal response, reaching its lowest value at the end of the event around the time instant $t = 23$ s. This is because the term $\Delta p_{uc}^\star$ increases due to the UC voltage deviation with respect to its reference value as shown in Fig. 10. This reduction is greater with high values of k_p^p as expected. Once the frequency event is over, both p_s and p_{uc} tend to return to their previous steady state. Again, a lower value of k_p^p leads to a closer response to the ideal one.

The previous time evolution of p_s and p_{uc} occurs because the UC energy recovery term, $\Delta p_{uc}^\star$, within the UC reference power, $p_{uc}^\star$, directly depends on k_p^p and the quadratic error of the UC voltage. Therefore, the higher k_p^p the higher UC energy recovery term which negatively affects the AS provision since the UC power injection drifts apart from its ideal performance. The evolution of the UC voltage, shown in Fig. 10, is as expected since higher k_p^p leads to a more rigid voltage. In case of large controller gains, lower voltage drops during the AS provision, faster UC voltage recovery after it and lower steady-state errors with respect to the reference ($v_{uc}^\star = 140$ V) are observed. Finally, the DC bus voltage evolution is depicted in the bottom plot of Fig. 10. An adequate tracking of the voltage reference ($v_{dc}^\star = 750$ V) is obtained for any k_p^p even during the AS provision where a slight voltage deviation happens due to the UC active power injection in the DC bus.

In addition to this qualitative comparison, Table 3 collects the mean square error (MSE) of the DC bus and UC voltages with respect to their setpoints for the different values of k_p^p. The table also provides the MSE of the POI and UC powers, p_s and p_{UC}, with respect to their ideal responses. The DC bus voltage MSE is really low in all the cases which indicates the good performance of

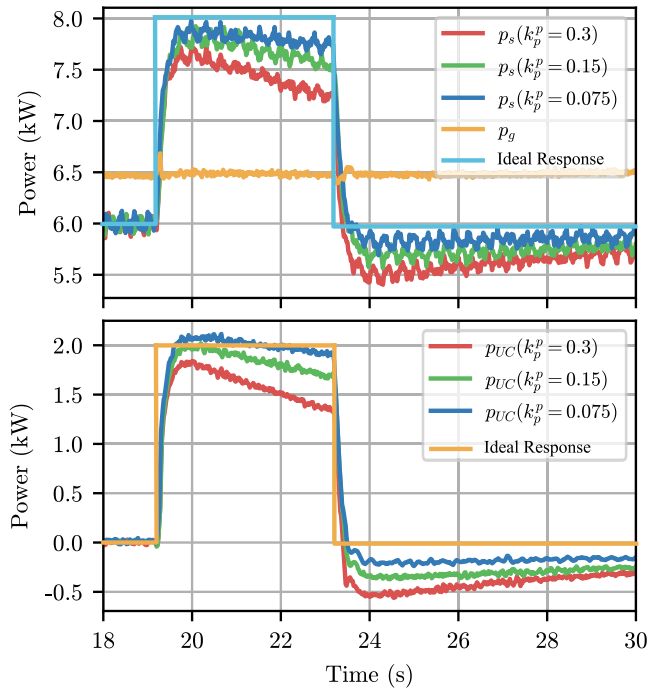

Fig. 9. Operation within the safe area. Influence of the parameter k_p^p with $T_p = 1$ s. Top plot: Primary RES power (p_g) and POI active power (p_s). Bottom plot: UC power (p_{uc}).

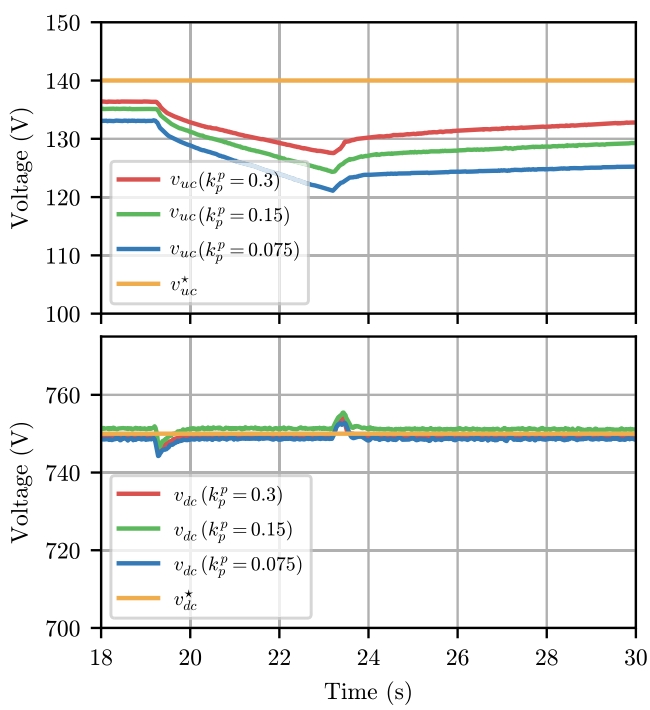

Fig. 10. Operation within the safe area. Influence of the parameter k_p^p with $T_p = 1$ s. Top plot: UC voltage evolution (v_{uc}). Bottom plot: DC bus voltage (v_{dc}).

CTRL2 irrespective of the selected k_p^p. The UC voltage MSE shows a clear trend since it gets lower values with higher k_p^p. Note that a higher k_p^p leads to higher $\Delta p_{uc}^\star$ which maintains the UC voltage. However, this higher k_p^p prevents the UC energy release to provide the required AS power which negatively impacts to the MSE of the POI and UC powers which drifts from their corresponding ideal responses. Finally, it is also interesting to note that the UC voltage MSE are the largest of the evaluated errors since CTRL3 is a proportional controller that does not guarantee a null steady-state error.

Table 3
MSE of different variables with respect to the proportional gain k_p^p.

Value k_p^p	MSE v_{dc}	MSE v_{uc}	MSE p_s	MSE p_{UC}
0.3	0.614	34.451	0.078	0.072
0.15	1.232	74.182	0.046	0.048
0.075	2.244	156.554	0.030	0.029

Table 4
Test within the warning area. Details of the variable proportional gain k_p^p.

Parameter	Value
k_{p0}^p	0.075 W/V^2
v_{uc}^{max}	155 V
v_{uc}^h	145 V
m_{ph}^p	2.9077 W/V^2

3.2.3. Operation within the warning area

This section evaluates the proposed control strategy when the UC operates within the warning area. For this purpose, a positive frequency variation during 5 s is tested departing from a voltage close to v_{uc}^h. It has been assumed that this frequency variation leads to a stepped reduction of 2 kW at the POI and, therefore, to an increase of the UC voltage. The controller parameters used in this test are summarized in Table 4.

The following controllers have been tested in order to evidence the benefits of the proposed EMS:

- C1. Constant proportional gain irrespective of the UC voltage.
- C2. Constant proportional gain but including the AS deactivation if the UC voltage is within the warning area.
- C3. Proposed variable proportional gain depending on the UC voltage.

Fig. 11 shows the evolution of the POI active power, p_s, the UC power p_{uc}, the proportional gain, k_p^p, and the UC voltage, v_{uc}, for comparison purposes. Regarding the active power, it is interesting to note that the evolution of the three tested controllers is almost identical during the first instants of the frequency event. However, significant differences are evident after this initial period. The controller with a constant proportional gain provides an almost ideal AS since the POI active power follows a step waveform. This performance is due to the small proportional gain which leads to a reduced UC energy recovery power term as shown in the bottom right plot of Fig. 11. However, this has a clear impact on the UC voltage which, as shown in the bottom left plot of Fig. 11, has the largest increase of the tested controllers surpassing 150 V and quite close to the voltage limit of $v_{uc}^{max} =$ 155 V.

A simple approach to reduce this UC voltage variation is to apply the second controller which disables the AS provision when the voltage limit is overpassed. The negative counterpart, however, is that the AS is not properly provided as the POI active power injection suddenly returns to its previous value before the frequency event.

The proposed controller is based on an adjustment of the proportional gain within the warning area depending on the voltage deviation. Note that the higher the UC voltage excursion the higher proportional gain, as shown in the top right plot of Fig. 11, in order to restore the UC voltage within the safe area as soon as possible. In fact, the proportional gain mimics the voltage

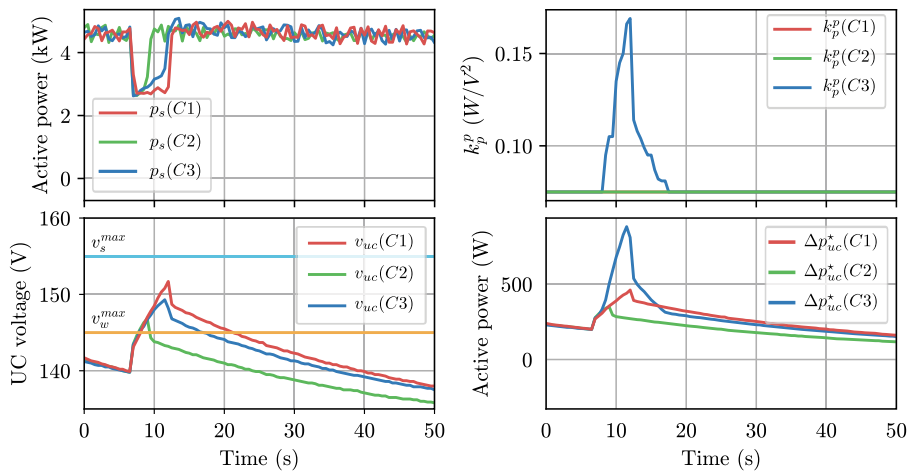

Fig. 11. Operation within the warning area. Comparison of three UC controllers. Top left plot: POI active power (p_s). Bottom left plot: UC voltage (v_{uc}). Top right plot: Proportional gain (k_p^p). Bottom right plot: UC energy recovery power reference ($\Delta p_{uc}^{\star}$).

Table 5
Comparison of UC energy recovery controllers.

Case	AS Energy (kW s)	AS provision (%)	Max. u_{uc} (V)
Ideal response	10	–	–
Constant k_p^p	9.56	93.6	151.7
AS deactivation	5.8	59.8	146.8
Proposed controller	8.66	88.66	149.3

deviation evolution as shown in the top right and the bottom left plots of Fig. 11. The increase of the proportional gain leads to an increase of the UC energy restoration energy, $\Delta p_{uc}^{\star}$, as shown in the bottom left plot of Fig. 11. As a consequence, the AS provision is clearly affected since a linear reduction of the active power p_s is produced. Once the frequency event ends, the original power p_s is restored and the UC voltage smoothly returns to its reference value since the controller gain is progressively reduced.

Finally, Table 5 shows a comparison of the energy provided by each of the controllers during the frequency event with respect to the theoretical step response and the UC maximum voltage. The results clearly evidences the higher performance of the proposed controller both in terms of the AS provision and safe operation of the UC. The energy delivery is close to its theoretical value. Evidently, the constant proportional gain performs better in terms of AS provision but at the expense of a higher voltage deviation which may damage the UC in case of overpassing its maximum voltage. On the contrary, the controller which deactivates the AS provision maintains the UC voltage far from the maximum limits but with the main drawback of providing a poor AS provision. As a conclusion, it can be stated that the proposed controller has a slight impact on the AS provision and, simultaneously, it is able to maintain the UC voltage within the warning zone away from its maximum technical limit.

4. Conclusions

This paper has presented an EMS for a CI-RES comprising an UC for providing ASs to the power grid. The EMS is in charge of providing the adequate control actions to the VSC and the DC/DC converter interfacing the UC with the CI-RES DC bus. The aim of the EMS is three-fold: (i) operate the CI-RES with an almost constant DC voltage, (ii) maintain the UC voltage within its technical limits and (iii) provide accurate ASs, i.e. as close as possible to the corresponding theoretical response. Considering these objectives, it has been decided to regulate the DC bus voltage using the UC by means of adequate control actions to the DC/DC converter. In this way, the VSC active power reference can be defined precisely according to the required AS.

The EMS is based on a hierarchical structure based on three control layers where the two inner ones, CTRL1 and CTRL2, are specifically suited for the VSC and the DC/DC converter while the third one, CTRL3, is in charge of the DC bus power balance. In the case of the VSC, CTRL1 is a classical current control loop which uses the references computed by CTRL2 from the active and reactive power references. On the other hand, the current of the DC/DC converter is controlled by CTRL1 to its reference value which is computed by CTRL2 in order to maintain the DC bus voltage. Finally, CTRL3 is in charge of defining the VSC active power reference to maintain the UC voltage within the limits but, at the same time, with enough flexibility to deliver the power required by any AS. For this reason, the use of a proportional controller with a variable gain has been proposed. This depends on the UC voltage so as to avoid the UC safety limit violations. With this regard, three operation zones have been defined: safe, warning and unsafe areas. In the safe area, the UC voltage is close to its rated operation voltage and, therefore, the proportional gain is as reduced as possible in order to deliver the energy of the required AS. Within the warning operation area, the controller gain is increased linearly with the voltage deviation in order to restore the operation within the safe area. Evidently, this affects the quality of the AS provision but the priority is to restore the UC voltage to the safe operation zone. In addition, CTRL3 incorporates an estimation of the steady-state power losses of the CI-RES in order to release the UC to provide this energy and, therefore, prevent its discharge.

The proposed EMS has been experimentally tested in a laboratory prototype by means of two types of tests. The first group of tests has been carried out to evaluate the dynamic performance and the steady-state error of each one of the control levels of the EMS independently. In addition, these tests have been used to tune the controller gains until the desired dynamic response is obtained. This has allowed to validate the controller design and evidence the reduced differences between the theoretical and experimental controller gains. The second type of tests evidence the influence of the proportional gain on the AS provision and

the UC voltage regulation. Additional tests have compared the performance of the proposed EMS to other alternative approaches within the warning operation area. These tests have revealed that the proposed controller achieves a good balance between the provided AS, which is close to the theoretical one, and the UC voltage, which is maintained far from its technical limits.

CRediT authorship contribution statement

Andrei Mihai Gross: Validation, Software. **Kyriaki-Nefeli Malamaki:** Resources, Writing – original draft. **Manuel Barragán-Villarejo:** Data curation, Investigation, Writing – original draft. **Georgios C. Kryonidis:** Formal analysis. **Francisco Jesús Matas-Díaz:** Validation, Software. **Spyros I. Gkavanoudis:** Formal analysis. **Juan Manuel Mauricio:** Methodology, Conceptualization. **José María Maza-Ortega:** Resources, Investigation, Supervision, Writing – original draft. **Charis S. Demoulias:** Project administration.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Acknowledgments

Funded by the European Union Horizon 2020 under Grant Agreement 764090 (EASY-RES), Spanish Ministry of Economy under grant ENE2017-84813-R and CERVERA Research Programme of CDTI, the Industrial and Technological Development Centre of Spain, under the research Project HySGrid+(CER-20191019).

References

[1] European-Commission, 2030 Climate & energy framework. Available [Online]: https://ec.europa.eu/clima/policies/strategies/2030.

[2] J. Cao, W. Du, H. Wang, M. McCulloch, Optimal sizing and control strategies for hybrid storage system as limited by grid frequency deviations, IEEE Trans. Power Syst. 33 (5) (2018) 5486–5495, http://dx.doi.org/10.1109/TPWRS.2018.2805380.

[3] Q. Yan, Q. Bo, Y. Jingjie, M. Yunfei, G. Bingqing, Frequency control strategy of hybrid energy storage system for microgrid based on frequency hysteretic loop, Energy Procedia 103 (2016) 328–332, http://dx.doi.org/10.1016/j.egypro.2016.11.294, Renewable Energy Integration with Mini/Microgrid – Proceedings of REM2016. URL http://www.sciencedirect.com/science/article/pii/S1876610216315041.

[4] Y. Xiyun, C. Chao, L. Xiangjun, Y. Tingting, Control method of smoothing wind power output using battery energy storage system based on empirical mode decomposition, in: 2015 34th Chinese Control Conference (CCC), 2015, pp. 304–308, http://dx.doi.org/10.1109/ChiCC.2015.7259654.

[5] J. Pegueroles-Queralt, F.D. Bianchi, O. Gomis-Bellmunt, A power smoothing system based on supercapacitors for renewable distributed generation, IEEE Trans. Ind. Electron. 62 (1) (2015) 343–350, http://dx.doi.org/10.1109/TIE.2014.2327554.

[6] S.I. Gkavanoudis, C.S. Demoulias, A combined fault ride-through and power smoothing control method for full-converter wind turbines employing supercapacitor energy storage system, Electr. Power Syst. Res. 106 (2014) 62–72, http://dx.doi.org/10.1016/j.epsr.2013.08.007, URL https://www.sciencedirect.com/science/article/pii/S0378779613002174.

[7] T. Qoria, E. Rokrok, A. Bruyere, B. François, X. Guillaud, A PLL-free grid-forming control with decoupled functionalities for high-power transmission system applications, IEEE Access 8 (2020) 197363–197378, http://dx.doi.org/10.1109/ACCESS.2020.3034149.

[8] V. Natarajan, G. Weiss, Synchronverters with better stability due to virtual inductors, virtual capacitors, and anti-windup, IEEE Trans. Ind. Electron. 64 (7) (2017) 5994–6004, http://dx.doi.org/10.1109/TIE.2017.2674611.

[9] S. Tan, H. Geng, G. Yang, Modeling framework of voltage-source converters based on equivalence with synchronous generator, J. Mod. Power Syst. Clean Energy 6 (2018) 1291–1305, http://dx.doi.org/10.1007/s40565-018-0433-1.

[10] J. Fang, P. Lin, H. Li, Y. Yang, Y. Tang, An improved virtual inertia control for three-phase voltage source converters connected to a weak grid, IEEE Trans. Power Electron. 34 (9) (2019) 8660–8670, http://dx.doi.org/10.1109/TPEL.2018.2885513.

[11] F. Errigo, F. Morel, M.D. Vienne, A submodule with integrated supercapacitors for HVDC-MMC providing fast frequency response, IEEE Trans. Power Deliv. 37 (3) (2022) 1423–1432, http://dx.doi.org/10.1109/TPWRD.2021.3086864.

[12] S.I. Gkavanoudis, D. Tampakis, K.-N.D. Malamaki, G.C. Kryonidis, E.O. Kontis, K.O. Oureilidis, J.M. Maza-Ortega, C.S. Demoulias, Protection philosophy in low short-circuit capacity distribution grids with high penetration of converter-interfaced distributed renewable energy sources, IET Gener. Transm. Distrib. 14 (22) (2020) 4978–4988, http://dx.doi.org/10.1049/iet-gtd.2020.0714, arXiv:https://ietresearch.onlinelibrary.wiley.com/doi/pdf/10.1049/iet-gtd.2020.0714. URL https://ietresearch.onlinelibrary.wiley.com/doi/abs/10.1049/iet-gtd.2020.0714.

[13] M. Chen, D. Zhou, F. Blaabjerg, Modelling, implementation, and assessment of virtual synchronous generator in power systems, J. Mod. Power Syst. Clean Energy 8 (3) (2020) 399–411, http://dx.doi.org/10.35833/mpce.2019.000592.

[14] M.J.E. Alam, K.M. Muttaqi, D. Sutanto, A novel approach for ramp-rate control of solar PV using energy storage to mitigate output fluctuations caused by cloud passing, IEEE Trans. Energy Convers. 29 (2) (2014) 507–518, http://dx.doi.org/10.1109/TEC.2014.2304951.

[15] P.J.d.S. Neto, T.A.d.S. Barros, J.P.C. Silveira, E.R. Filho, J.C. Vasquez, J.M. Guerrero, Power management strategy based on virtual inertia for DC microgrids, IEEE Trans. Power Electron. 35 (11) (2020) 12472–12485, http://dx.doi.org/10.1109/TPEL.2020.2986283.

[16] J. Fang, Y. Tang, H. Li, X. Li, A battery/ultracapacitor hybrid energy storage system for implementing the power management of virtual synchronous generators, IEEE Trans. Power Electron. 33 (4) (2018) 2820–2824, http://dx.doi.org/10.1109/TPEL.2017.2759256, URL http://ieeexplore.ieee.org/document/8059852/.

[17] M. Saleh, Y. Esa, A. Mohamed, Impact of communication latency on the bus voltage of centrally controlled DC microgrids during islanding, IEEE Trans. Sustain. Energy 10 (4) (2019) 1844–1856, http://dx.doi.org/10.1109/TSTE.2018.2873699.

[18] X. Xiong, C. Wu, B. Hu, D. Pan, F. Blaabjerg, Transient damping method for improving the synchronization stability of virtual synchronous generators, IEEE Trans. Power Electron. 36 (7) (2021) 7820–7831, http://dx.doi.org/10.1109/TPEL.2020.3046462.

[19] T. Qoria, C. Li, K. Oue, F. Gruson, F. Colas, X. Guillaud, Direct AC voltage control for grid-forming inverters, J. Power Electron. 20 (1) (2020) 198–211, http://dx.doi.org/10.1007/s43236-019-00015-4.

[20] J. Xiao, Y. Jia, B. Jia, Z. Li, Y. Pan, Y. Wang, An inertial droop control based on comparisons between virtual synchronous generator and droop control in inverter-based distributed generators, Energy Rep. 6 (2020) 104–112, http://dx.doi.org/10.1016/j.egyr.2020.12.003, 2020 The 7th International Conference on Power and Energy Systems Engineering. URL https://www.sciencedirect.com/science/article/pii/S2352484720317042.

[21] K. Shi, H. Ye, W. Song, G. Zhou, Virtual inertia control strategy in microgrid based on virtual synchronous generator technology, IEEE Access 6 (2018) 27949–27957, http://dx.doi.org/10.1109/ACCESS.2018.2839737.

[22] J.W. Shim, G. Verbi, H. Kim, K. Hur, On droop control of energy-constrained battery energy storage systems for grid frequency regulation, IEEE Access 7 (2019) 166353–166364, http://dx.doi.org/10.1109/ACCESS.2019.2953479.

[23] D. Li, Z. Wu, B. Zhao, L. Zhang, An improved droop control for balancing state of charge of battery energy storage systems in AC microgrid, IEEE Access 8 (2020) 71917–71929, http://dx.doi.org/10.1109/ACCESS.2020.2987098.

[24] L.G. González, R. Chacon, B. Delgado, D. Benavides, J. Espinoza, Study of energy compensation techniques in photovoltaic solar systems with the use of supercapacitors in low-voltage networks, Energies 13 (15) (2020) URL https://www.mdpi.com/1996-1073/13/15/3755.

[25] F.J. Matas-Díaz, U. Mushtaq, A.M. Gross, A.R. del Nozal, M. Cvetkovic, K.-N.D. Malamaki, G.C. Kryonidis, J.M. Mauricio, J. María Maza-Ortega, M. Barragán-Villarejo, DC-bus energy management of a converter-interfaced renewable energy source comprising an energy storage system, in: 2021 IEEE Madrid PowerTech, 2021, pp. 1–6, http://dx.doi.org/10.1109/PowerTech46648.2021.9494804.

[26] A.M. Gross, K.-N. Malamaki, M. Barragán-Villarejo, G.C. Kryonidis, F.J. Matas-Díaz, S.I. Gkavanoudis, J.M. Mauricio, J.M. Maza-Ortega, C.S. Demoulias, Energy management in converter-interfaced renewable energy

sources through ultracapacitors for provision of ancillary services, in: 2021 International Conference on Smart Energy Systems and Technologies (SEST), 2021, pp. 1–6, http://dx.doi.org/10.1109/SEST50973.2021.9543130.

[27] G.C. Kryonidis, K.-N.D. Malamaki, J.M. Mauricio, C.S. Demoulias, A new perspective on the synchronverter model, Int. J. Electr. Power Energy Syst. 140 (2022) 108072, http://dx.doi.org/10.1016/j.ijepes.2022.108072, URL https://www.sciencedirect.com/science/article/pii/S0142061522001144.

[28] M. Kermadi, E.M. Berkouk, A. Benachour, Design of discrete pi-based current controller for reversible buck boost converter. Digital implementation using arduino due board, in: 2016 8th International Conference on Modelling, Identification and Control (ICMIC), 2016, pp. 863–866, http://dx.doi.org/10.1109/ICMIC.2016.7804235.

[29] J. Rocabert, A. Luna, F. Blaabjerg, P. Rodríguez, Control of power converters in AC microgrids, IEEE Trans. Power Electron. 27 (11) (2012) 4734–4749, http://dx.doi.org/10.1109/TPEL.2012.2199334, arXiv:arXiv:1011.1669v3.