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# Ready-to-Fabricate RF Circuit Synthesis Using a Layout- and Variability-Aware Optimization-Based Methodology

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**ABSTRACT** In this paper, physical implementations and measurement results are presented for several Voltage Controlled Oscillators that were designed using a fully-automated, layout- and variability-aware optimization-based methodology. The methodology uses a highly accurate model, based on machine-learning techniques, to characterize inductors, and a multi-objective optimization algorithm to achieve a Pareto-optimal front containing optimal circuit designs offering different performance trade-offs. The final outcome of the proposed methodology is a set of design solutions (with their GDSII description available and ready-to-fabricate) that need no further designer intervention. Two key elements of the proposed methodology are the use of an optimization algorithm linked to an off-the-shelf simulator and an inductor model that yield EM-like accuracy but with much shorter evaluation times. Furthermore, the methodology guarantees the same high level of robustness against layout parasitics and variability that an expert designer would achieve with the verification tools at his/her disposal. The methodology is technology-independent and can be used for the design of radio frequency circuits. The results are validated with experimental measurements on a physical prototype.

**INDEX TERMS** Integrated circuit synthesis, electronic design automation and methodology, inductors, metamodeling, radio frequency, voltage-controlled oscillator.

## I. INTRODUCTION

Over the past few years, several optimization-based methodologies for the automated sizing of analog and radio-frequency (RF) integrated circuits (ICs) have been proposed [1]–[9]. These methodologies link an optimization algorithm with a circuit performance evaluator (e.g., the Spectre RF simulator) to evaluate candidate solutions. While doing so, they perform a thorough search through the entire design space, with the objective of finding optimal sizing solutions. However, most of them have not been capable of yielding designs that are sufficiently robust for fabrication, i.e., ready-to-fabricate designs. For instance, most optimization-based design methodologies do not take into account sources of perturbation that affect the circuit performances such as process variability or layout parasitics. Although variability [5], [6] or layout parasitics [7]–[9] have been taken into account in some methodologies, they are always tackled separately during the optimization process. Another downside of previously reported synthesis methodologies pertains to the quality of the modeling used for passive components (e.g., inductors), which, in RF, are extremely important. Most synthesis methodologies use either analytical models, which are typically inaccurate, or electromagnetic (EM) simulations, whose use in optimization-based sizing methodologies is ill-advised due

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to the long computation times that the required large number of simulations involve. Therefore, in order to develop an optimization-based methodology capable of outputting ready-to-fabricate designs, (1) sources of perturbation must be taken into account during the optimization (i.e., parasitics and variability) and (2) passive components must be modeled in such a way that their evaluation is accurate while time-efficient.

Furthermore, reported approaches have rarely been demonstrated with fabricated designs and characterized in the lab. The resulting lack of confidence may be at the roots of the scarce adoption of synthesis methodologies in industrial environments. The work presented in this paper confronts this lack of trust by presenting silicon measurement results of devices and circuits as provided by an automated design methodology, whose main advantages (when compared to former design methodologies) are the following. First, it uses multi-objective optimization algorithms to obtain a Pareto-optimal front (POF), i.e., a set of fully sized optimized designs where all sources of perturbation are taken into account conjointly (layout parasitics and process variability). The POF represents the best trade-offs between the circuit performances being optimized and contains the solutions that the designer can ultimately choose from according to his/her preferences. These fronts are obtained at both the device and the circuit levels, the latter being built by hierarchically composing information from lower-level fronts. Second, the methodology features an extremely accurate and efficient technique, based on machine learning [10], to model inductors; this modeling approach successfully alleviates the need for EM simulations during the optimization while maintaining a very good accuracy.

The methodology has been experimentally validated through several Voltage Controlled Oscillators (VCOs) that were designed automatically, then fabricated, and, finally, measured in the lab. Moreover, the inductor model used in this work is also validated against standalone inductors (the same used in the fabricated VCOs). A brief explanation of the inductor modeling technique is given in Section II, whereas the synthesis methodology is outlined in Section III. Section IV presents and discusses the experimental results. Last, in Section V, conclusions are drawn.

## II. INDUCTOR MODELING USING MACHINE LEARNING TECHNIQUES

Accurate passive component models are still one of the most important requirements in the design of RF circuits/systems. While foundries usually provide sufficiently accurate models for transistors, capacitors and resistors, the modeling of inductors and transformers is still a bottleneck. In this work, a machine-learning technique that employs surrogate models has been used to tackle inductor modeling [10].

As any machine-learning technique, surrogate-based models learn the behavior of a system from a set of training samples to then predict the behavior of new samples [11]. Surrogate models are used to map some input variables, in this case the inductor geometric parameters (number of turns $N$, inner diameter $D_{IN}$ and turn width $w$) to some output variables, e.g., the inductor performance parameters: inductance L and quality factor Q. A highly accurate mapping of $N$, $D_{IN}$, $w$ and frequency $f$ to L and Q was reported in [10], where less than 1% error between the model and actual EM simulations was achieved. Nevertheless, L and Q cannot be easily mapped into a model that yields accurate circuit simulation results. Therefore, in this work, instead of directly modeling these inductor performance parameters, the inductor geometric parameters are mapped to the space of S-parameters. In this way, the performance description of the inductor can be easily and accurately included in circuit-level simulations by using RF circuit simulators.

The surrogate model used in this work resorts to Gaussian-Process techniques. Trying to arrive at a single inductor model that is general, valid and accurate for the widest design variable ranges, frequency span, and topological differences, can be an incredibly complex task, if it can ever be solved at all. Therefore, some modeling strategies have been developed to tackle the problem more efficiently. The complexity of Gaussian process surrogate modeling techniques increases exponentially with the number of dimensions, and so does the number of training samples to reach a given accuracy. The applied strategies reduce the modeling complexity by breaking down the problem into simpler modeling problems that altogether constitute an accurate modeling solution [10]. A first strategy is to create different models for inductors with different number of turns (e.g., one model for inductors with 2 turns and another for inductors with 3 turns) and for each frequency point required. In order to further increase the accuracy, the strategy proposed is to create these models for a specific working frequency (WF) using a filtering strategy in the selection of the inductors used to create the model from those available from the training set. Then, only inductors with a self-resonance frequency (SRF) above the WF are selected for model creation (e.g., if a model is being created for 2.4 GHz, a filtering operation in the training set is performed and only inductors with SRF$<$3 GHz are selected for the model creation). These strategies have demonstrated to accurately model the inductors [10] and the only additional effort is the development of the surrogate model to evaluate the SRF of the inductors, which can be easily done from the training set provided to create the S-parameter models. As a result, the designer would have a model for evaluating the inductor SRF and other models to evaluate the inductor S-parameters. Furthermore, the modeling strategy presented here is completely technology- and topology-independent. The model developed in this work was built with 800 EM simulated training inductors selected using the Quasi-Monte Carlo technique. Total EM simulation time was approximately 12 hours. The model achieves less than 1% error and takes around 0.3 milliseconds to evaluate each inductor, which compared to the several minutes that EM simulations usually takes, it is a clear efficiency improvement. This efficiency improvement is one of the key factors enabling

the optimization-based methodology proposed in this work.

## III. OPTIMIZATION-BASED DESIGN METHODOLOGY

A preliminary version of this methodology was presented in [12], where, through the synthesis of an LNA, it is demonstrated that, in order to obtain ready-to-fabricate designs, it is essential to consider both layout parasitics and variability. A common roadblock to the adoption of new design methodologies is their validation via fabrication and characterization of physical prototypes. The present paper is the first one, to the best of the authors' knowledge, that experimentally validates an optimization-based methodology where layout parasitics and variability are considered during the optimization providing ready-to-fabricate RF circuits. In this paper, the methodology is applied to a VCO.

To attain a set of optimal designs with different trade-offs among their performances, this work uses a multi-objective optimization algorithm, which can be mathematically formulated as:

$$\begin{aligned} &\textit{minimize } f\,(x)\,; \quad f\,(x) \in R^m \\ &\textit{subject to } g\,(x) \leq 0; \quad g\,(x) \in R^k \\ &x \in \Omega \end{aligned}$$

where $f(x)$ is a vector with $m$ objective functions (where $m$>1), g($x$) is a vector with $k$ constraints and $x$ is a vector with $n$ design variables on the search space Ω.

In constrained multi-objective optimization, a solution $a$ is said to dominate solution $b$ if and only if $a$ has a smaller constraint violation than $b$, or, if all constraints are met, $f_i(a) \leq f_i(b)$, for every $i \in \{1, \ldots, m\}$ and $f_j(a) < f_j(b)$ for at least an index $j \in \{1, \ldots, m\}$. A point $y \in \Omega$ is Pareto-optimal if it is not dominated by any other point in Ω. The set of all Pareto-optimal points in the search space is known as the Pareto set and the corresponding points in the objective space is the Pareto-optimal front (POF).

The work presented here resorts to the Non-dominated Sorting Genetic Algorithm (NSGA-II) [13], a multi-objective optimization algorithm based on the evolution of a set of solutions (i.e., individuals) over a certain number of iterations (i.e., generations). The RF circuit design methodology considered in this paper does not exploit any specific characteristic of NSGA-II and, therefore, this algorithm could be replaced by any other multi-objective optimization algorithm.

### A. FIRST STEP: DEVICE-LEVEL OPTIMIZATION

The methodology follows a two-step optimization process [8]. The main idea is that inductors are optimized *a priori* using a multi-objective optimization algorithm in order to obtain an inductor POF. This POF can be considered as a database containing the best inductor designs (with their corresponding GDSII and S-parameter descriptions) for the adopted technology and operation frequency. Afterwards, during the RF circuit optimization, the inductors can be directly selected from this optimal database instead of concurrently searching over the entire inductor design space.

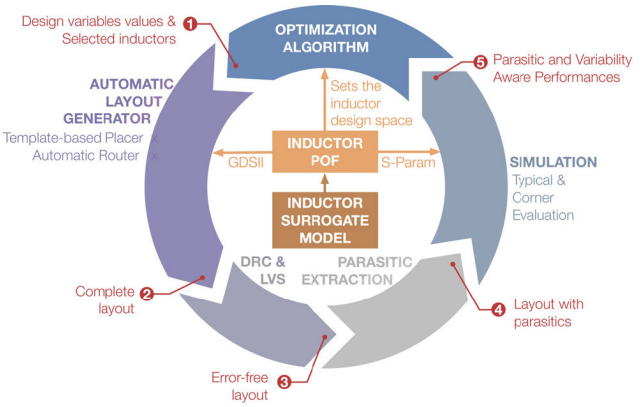


**FIGURE 1. Design methodology flow of the proposed layout-variability-aware methodology.**

### B. SECOND STEP: CIRCUIT-LEVEL OPTIMIZATION

The actual circuit optimization is an iterative process with five consecutive phases (see Fig. 1). In the first phase, the optimizer generates a new set of circuit candidate solutions, using the defined design variables and the inductors from the previously generated database (the inductor POF). In phase two, using the information passed on by the optimizer, the layout of each individual is generated automatically using a template-based placer and a fully-automatic router, as well as the GDSII description of the inductors from the inductor POF previously generated [8]. In the template-based placer, the designer is responsible for providing simple high-level XML forms encoding a technology- and specification-independent floorplan description. From here, all packing procedures are performed automatically given any set of devices. These devices are provided either by correct-by-construction RF module generators or DRC-proven GDSII descriptions. Therefore, in order to ensure the DRC validity of the floorplan it is only necessary to keep minimum allowed distances in all directions of each device's layout. A three-step router is then used to optimize this part of the layout. First, a deterministic wiring planner sets the optimal terminal-to-terminal connectivity from the netlist and cells' positions in the layout. Second, a deterministic path-finding algorithm within a sparse grid transforms the wiring topologies into rectilinear paths. And finally, an optimization-based detailed routing process is carried, where the sparse grid is reduced to the manufacturing grid. The result is a rapid and automated generation of the layout views for every candidate solution. Afterwards, in phases three and four, the layout views of all the individuals are checked for LVS and DRC and all the resistive and capacitive parasitics are extracted using an off-the-shelf tool. In phase five, the simulation phase, all individuals undergo a thorough evaluation of their performances, those defined as objectives and those defined as constraints, taking into account both the typical case

performances and the worst-case corner scenarios. In this approach, the corners that were taken into consideration are: the worst-case power condition (WP); the worst-case speed condition (WS); the worst-case one (WO), which considers fast NMOS and slow PMOS; and, the worst-case zero (WZ), with slow NMOS and fast PMOS. Nevertheless, the approach is valid for any desirable corner combination or any other variability impact evaluation. In each simulation, the inductors' S-parameter description is selected from the previously obtained database for an accurate performance evaluation. Once the simulation results are available (typical and corner performances), the worst-case performance of each individual is passed on to the optimizer in order to guarantee that the constraints are met even in the worst-case scenario. The optimization algorithm generates new solutions by applying crossover, mutation and selection operators to the best solutions simulated in step five, i.e., those with better objective (circuit performances) values, that comply (or better comply) with the constraints imposed. Then, these new solutions undergo a new cycle of layout (phase 2), DRC & LVS (phase 3), extraction (phase 4) and simulation (phase 5). This iterative process is carried out until the stopping criteria are met. Then, the optimizer returns the best solutions found. In this way, the final output of the methodology is a set of circuits (i.e., a POF) with the best trade-offs among the performances selected as objectives and that meet the constraints, along with their GDSII files.

## IV. EXPERIMENTAL RESULTS

The adopted technology for the validation of the methodology is a 0.35-$\mu$m CMOS technology. Note that all technology-dependent electrical simulations and parasitic extractions are performed using commercial off-the-shelf tools, with the technology files provided by the foundry in their Process Design Kit. Therefore, the validity and accuracy of the methodology itself is completely independent of the technology adopted (depending only on the simulators, tools and extraction files used). The use of the 0.35-$\mu$m CMOS technology is only motivated by the fact that a description of the technology layer stack was available at the time, thus allowing accurate EM simulations for the inductor model creation [10].

### A. OPTIMIZATION RESULTS

The design of a cross-coupled double differential VCO using a symmetrical octagonal inductor is used as a case study (see Fig. 2). As a way of easing experimental characterization, the output of the VCO was connected to a source-follower buffer with an input capacitive voltage divider of 1/10 factor to drive the 50 Ω of the spectrum analyzer. The VCO is supplied with $V_{DD} = 2.5$ V and biased with a variable tuning voltage $V_{TUNE}$. The buffers are biased using $V_{BIAS} = 2$ V.

As explained before, the first step consists in the generation of the inductor POF. The search space for the inductor optimization is presented in Table 1. The optimization, performed with NSGA-II, had three design objectives: maximization of

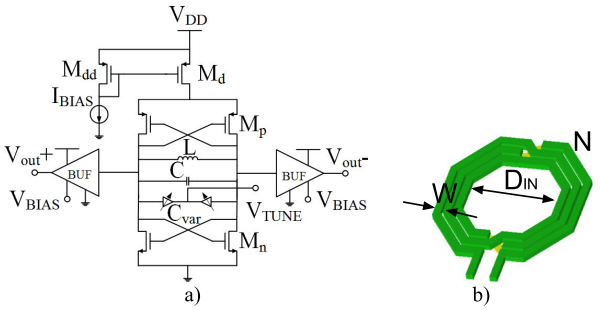


**FIGURE 2.** a) Cross-coupled double differential VCO topology. b) Symmetrical inductor topology used in the optimization, with its geometrical parameters.

**TABLE 1.** Design variables for the inductors.

| $N$ | | | $D_{in}$ (µm) | | | $W$ (µm) | | |
|---|---|---|---|---|---|---|---|---|
| Min. | Max. | Grid | Min. | Max. | Grid | Min. | Max. | Grid |
| 1 | 8 | 1 | 10 | 300 | 0.05 | 5 | 25 | 0.05 |

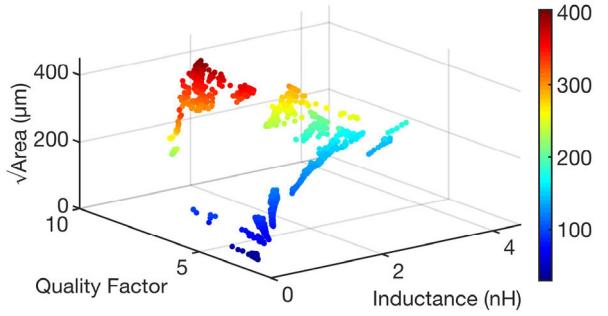


**FIGURE 3.** POF of the inductor octagonal symmetric topology containing 1000 fully-sized inductors. The color bar represents the area objective.

the quality factor, Q, maximization of inductance, L, and minimization of the area. The optimization was performed with 1000 individuals and 80 generations and several constraints were imposed to guarantee the proper behavior of inductors at the WF, i.e., the inductance value is approximately constant in the operating frequency range and equal to the DC value, and the SRF is sufficiently above the WF [10]. The obtained POF is shown in Fig. 3, which took around 10 minutes wall-clock time to obtain in an Intel®Core™i7-3770 @ 3.4 GHz workstation with 32 GB of RAM.

After obtaining the inductor POF, the VCO can be optimized. The optimization was performed using 128 individuals and 200 generations, which took two 2 days wall-clock time to execute in the above mentioned workstation. The search space for the VCO optimization is presented in Table 2. The objectives of the optimization, shown in Table 3, were the minimization of: the phase noise (PN) at a frequency offset ($PN_{offset}$) of 1 MHz, the total power consumption ($P_{DC}$) of the circuit (power consumption of the VCO, $P_{VCO}$, and buffers, $P_{BUF}$) and the area. Several constraints were imposed during the optimization in order to ensure that typical VCO specifications were met, as also shown in Table 3.

**TABLE 2.** Design variables for the VCO optimization.

| Variables | Min. | Max. | Step |
|---|---|---|---|
| $w_{Mn}$ (µm) | 10 | 200 | 10 |
| $w_{Mp,Mdd,Md}$ (µm) | 10 | 150 | 10 |
| $l_{Mn,Mp,Mdd,Md}$ | Fixed @ 0.35 µm | | |
| $I_{BIAS}$ (mA) | 0.1 | 5 | 0.1 |
| $w_{Cvar}$ (µm) | Fixed @ 6.6 µm | | |
| $l_{Cvar}$ (µm) | Fixed @ 0.65 µm | | |
| Inductors | Selected from the POF in Fig. 3 | | |
| $Row_{Cvar}$,$Col_{Cvar}$ [(1)] | 4 | 12 | 1 |
| C (pF) | 0.4 | 4 | 0.4 |

[(1)] $Row_{Cvar}$ is the number of fingers per row and $Col_{Cvar}$ is the multiplicity of the varactors.

**TABLE 3.** VCO specifications: objectives and constraints.

| Specs. | Performance | Target | Units | Description |
|---|---|---|---|---|
| Objectives | PN@1MHz | min. | dBc/Hz | Phase Noise@1MHz |
| | $P_{DC}$ ($P_{VCO}$+$P_{BUF}$) | min. | mW | Power Consumption |
| | Area | min. | $mm^2$ | Die core area |
| Constraints | $f_{OSC}$ | ~2.4 | GHz | Oscillation frequency |
| | $\Delta f$ | ≥ 100 | MHz | Tuning range |
| | PN@1MHz | < -110 | dBc/Hz | Phase Noise@1MHz |
| | $V_{OUT}$ | ≥ 0.15 | V | Output swing |
| | $P_{DC}$ ($P_{VCO}$+$P_{BUF}$) | < 40 | mW | Power Consumption |

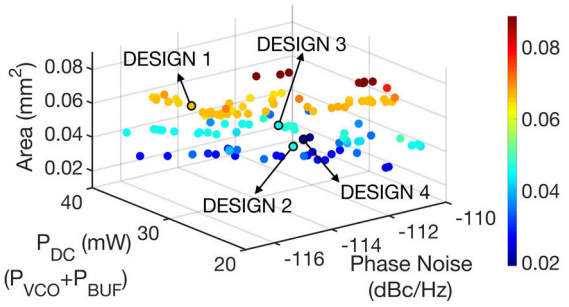


**FIGURE 4.** POF obtained from the optimization containing hundreds of fully-sized VCOs. The worst-case corner performances are depicted, where the colour bar represents the area.

The obtained POF can be seen in Fig. 4, where each plotted dot represents a fully sized VCO (with its GDSII description available). In this POF, the designer would have the best designs for the chosen trade-offs, which comply with the imposed constraints. One main advantage is that now these trade-offs are defined by fully-sized circuits ready to be fabricated. Fig. 5 presents the fabricated chip where 4 different VCOs were selected from the POF (identified in Fig. 4). The output buffer and all the used inductors were also fabricated as individual test structures in order to evaluate their standalone performances.

### B. INDUCTOR MEASUREMENT RESULTS AND DISCUSSION

The inductors were implemented with the top thick metal (with a thickness of 2.8 $\mu$m) and placed over a semiconductor substrate. In the chip implementation, no substrate contacts are placed near the inductor and the metal lines

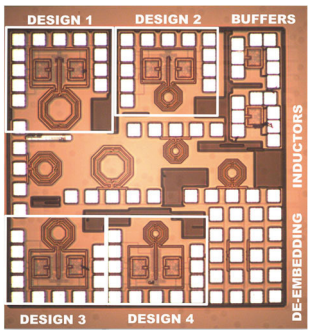


**FIGURE 5.** Chip photograph.

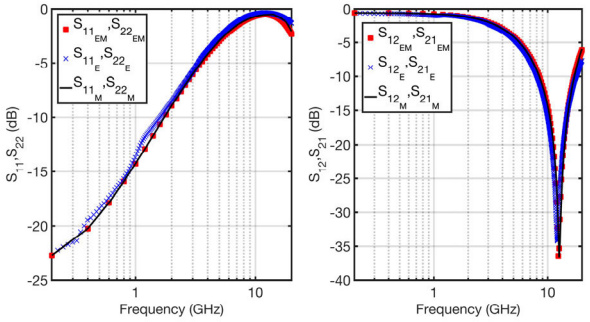


**FIGURE 6.** S-parameter comparison for the inductor used in the VCO denoted by Design 1.

are kept at a relatively safe distance to limit electric and magnetic couplings. On-wafer characterization was carried out using a Cascade Microtech M150 measurement platform and an Agilent N5230A network analyzer. Fig. 6 shows the S-parameter comparison between the full-wave EM simulation ($S_{11EM}$, $S_{12EM}$, $S_{21EM}$ and $S_{22EM}$), the experimental measurements ($S_{11E}$, $S_{12E}$, $S_{21E}$ and $S_{22E}$) and the model predictions ($S_{11M}$, $S_{12M}$, $S_{21M}$ and $S_{22M}$), for the inductor used in the VCO denoted by Design 1. Fig. 7a) shows the inductor performance parameters (inductance and quality factor) comparison between the full-wave EM simulation ($L_{EM}$ and $Q_{EM}$), the experimental ($L_E$ and $Q_E$) and the model predictions ($L_M$ and $Q_M$), for the inductor in Design 1. It is possible to observe that, quality-wise, there is a good matching between measurements and model predictions for the entire measured frequency range (up to 20 GHz), even though the model was created specifically for WF=2.4 GHz (i.e., the model is guaranteed to be accurate only for frequencies up to slightly above the WF). Fig. 7b) shows the performance parameters of the inductor in Design 2, where, again, a very good matching between measurements and the model predictions is achieved. Two other inductors (used in VCO Design 3 and 4, respectively) were measured and their performance comparisons are shown in Fig. 7c) and Fig. 7d), showing a good matching of their performances even above the frequency range for which the model is created.

Table 4 provides a more quantitative analysis of the inductor performances at 2.4 GHz. The fourth, ninth and fourteenth columns represent the error between the full-wave EM

**TABLE 4.** Inductor performances at 2.4 GHz. Experimental (E) results versus full-wave (EM) simulations and model (M) estimation.

| Inductors used in each VCO design and its geometrical parameters | $L_E$ (nH) | $L_{EM}$ (nH) | EM-E (%) | $L_M$ (nH) | M-E (%) | $Q_E$ | $Q_{EM}$ | EM-E (%) | $Q_M$ | M-E (%) | $SRF_E$ (GHz) | $SRF_{EM}$ (GHz) | EM-E (%) | $SRF_M$ (GHz) | M-E (%) |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Design 1 ($N$=3 $D_{IN}$=187 µm $w$=8.8µm) | 2.83 | 2.72 | 3.93 | 2.72 | 3.96 | 7.18 | 7.11 | 0.98 | 7.23 | 0.71 | 12.23 | 11.90 | 2.70 | 11.85 | 3.11 |
| Design 2 ($N$=5 $D_{IN}$ =84 µm $w$=5µm) | 3.52 | 3.40 | 3.34 | 3.41 | 3.00 | 5.65 | 6.21 | 9.89 | 6.25 | 10.73 | 11.41 | 11.70 | 2.54 | 11.68 | 2.37 |
| Design 3 ($N$=4 $D_{IN}$=119 µm $w$=6.95 µm) | 3.15 | 3.01 | 2.88 | 3.05 | 2.10 | 6.50 | 6.67 | 2.67 | 6.49 | 0.04 | 11.56 | 11.50 | 0.52 | 11.53 | 0.26 |
| Design 4 ($N$=5 $D_{IN}$=61 µm $w$=5.05 µm) | 2.53 | 2.47 | 2.22 | 2.52 | 0.19 | 5.46 | 5.53 | 1.28 | 5.50 | 0.70 | 14.75 | 15.10 | 2.38 | 15.10 | 2.37 |

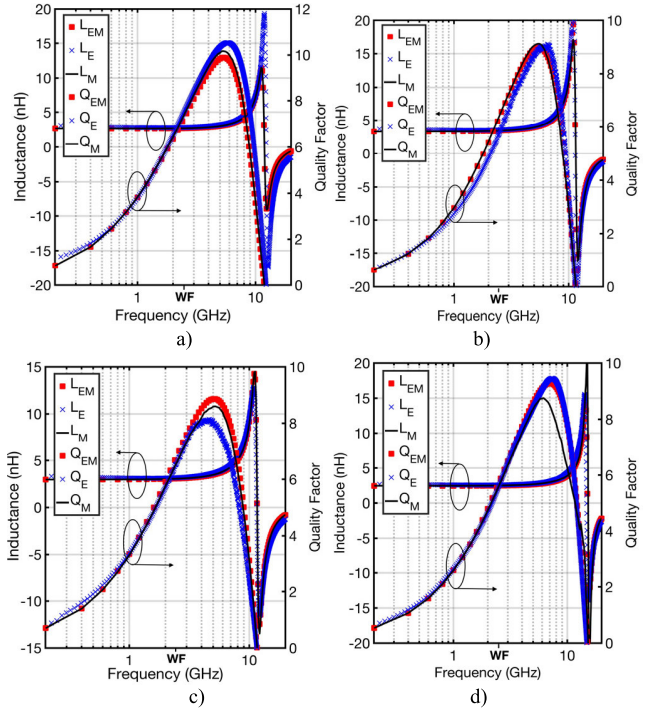


**FIGURE 7.** Performance comparison for the inductors used in different VCO designs. (a) Design 1. (b) Design 2. (c) Design 3. (d) Design 4.

simulation and experimental measurements. The sixth, eleventh and sixteenth columns represent the error between the model and experimental measurements for L, Q and SRF, respectively (columns labelled as "M-E (%)"). In the light of these results, it is reasonable to conclude that the model provides an exceptionally reliable estimation of the inductor performance parameters: the model deviates less than 4% in L, and only one inductor deviates more than 3% in Q (at 2.4 GHz) with respect to physical measurements. The discrepancies attained are almost the same as the errors between full-wave EM simulations and measurements (columns labelled as "EM-E (%)"), suggesting that these small discrepancies are caused more by manufacturing variations than by significant errors in the model. Regarding the SRF model prediction, it is, to the best of the authors' knowledge, the most accurate inductor SRF predictor available in the literature (with less than 3% error when compared to measurements).

### C. VCO MEASUREMENT RESULTS AND DISCUSSION

To measure the VCO, a Keysight E4440A spectrum analyzer was used together with a Keysight B1500A Semiconductor

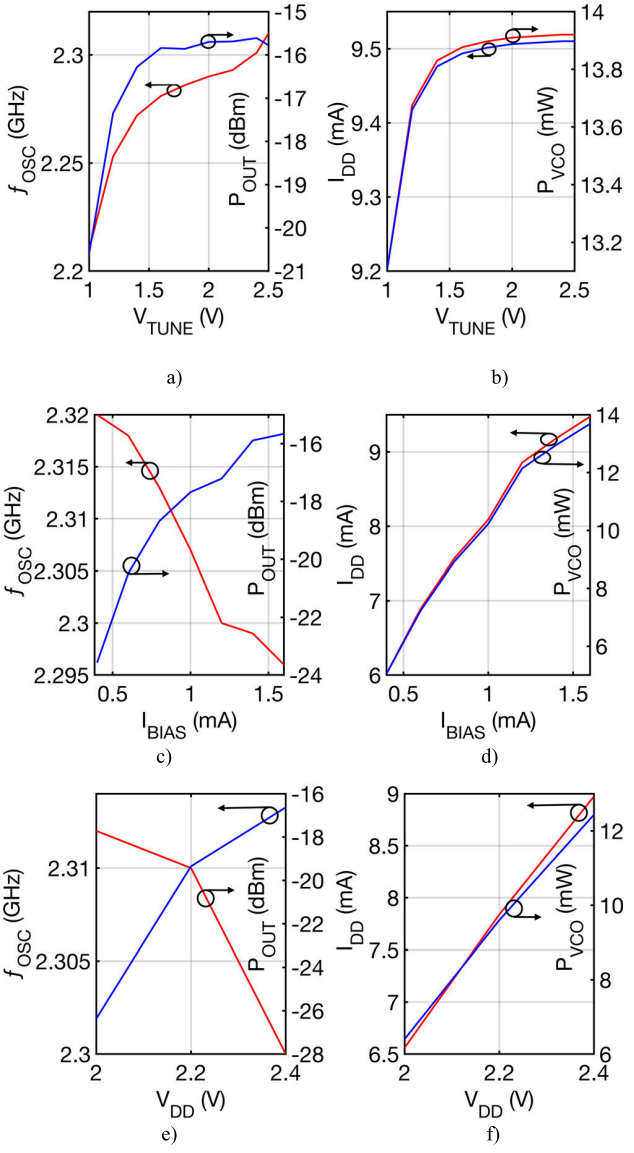


**FIGURE 8.** Measurements for VCO Design 1. a) $f_{OSC}$ and $P_{OUT}$ vs. $V_{TUNE}$; b) $I_{DD}$ and $P_{VCO}$ vs. $V_{TUNE}$; c) $f_{OSC}$ and $P_{OUT}$ vs. $I_{BIAS}$; d) $I_{DD}$ and $P_{VCO}$ vs. $I_{BIAS}$; e) $f_{OSC}$ and $P_{OUT}$ vs. $V_{DD}$; f) $I_{DD}$ and $P_{VCO}$ vs. $V_{DD}$.

Device Parameter Analyzer to bias the circuit. Fig. 8 presents several measurements for Design 1. In Fig. 8a) it is possible to observe how $f_{OSC}$ and the output power ($P_{OUT}$) change with $V_{TUNE}$ (with $I_{BIAS} = 1.7$ mA). Fig. 8b) shows how $I_{DD}$ (the current running through $V_{DD}$) and $P_{VCO}$ change when $V_{TUNE}$ is varied. Fig. 8c) and 8d) show the sensitivity of the

**TABLE 5.** Comparison against reported VCOs in similar technology nodes.

| Work | Technology (µm) | $f_{OSC}$ (GHz) | PN (dBc/Hz) | $PN_{offset}$ (MHz) | $\Delta f$ (MHz) | $P_{VCO}$ (mW) | $V_{DD}$ (V) | Area ($mm^2$) | FOM (dBc/Hz) | $FoM_A$ (dBc/Hz) | $FoM_{AT}$ (dBc/Hz) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Hajimiri [14]** | 0.25 | 1.8 | -121 | 0.6 | x | 6 | 1.5 | x | 163.55 | x | x |
| **Herzel [15]** | 0.25 | 1.9 | -100 | 1 | 250 | 15 | 2.5 | x | 154.55 | x | x |
| **Wong [16]** | 0.35 | 2 | -105 | 1 | 250 | 22.5 | 3 | x | 161.53 | x | x |
| **Lam [17]** | 0.35 | 2.6 | -110 | 0.5 | 320 | 13 | 2.5 | x | 148.30 | x | x |
| **Ranter [7]** | 0.35 | 2.90 | -110 | 1 | 425 | 19.8 | 1.8 | 0.200* | 157.60 | 164.59 | 190.87 |
| **Kao [18]** | 0.35 | 2.6 | -116 | 0.6 | 160 | 22.62 | 3 | 0.976 | 165.91 | 166.02 | 188.06 |
| **Heng [19]** | 0.35 | 1.94 | -121 | 0.5 | 160 | 6.72 | 2.4 | 0.560 | 165.16 | 167.68 | 189.72 |
| **Design 1** | 0.35 | 2.31 | -116.5 | 1 | 98 | 13.66 | 2.5 | 0.169 | 161.49 | 169.21 | 189.12 |
| **Design 2** | 0.35 | 2.29 | -114 | 1 | 100 | 10.5 | 2.5 | 0.085 | 157.81 | 168.52 | 188.52 |
| **Design 3** | 0.35 | 2.28 | -112.4 | 1 | 90 | 12.07 | 2.5 | 0.117 | 156.80 | 166.11 | 185.66 |
| **Design 4** | 0.35 | 2.34 | -110.2 | 1 | 87 | 18 | 2.5 | 0.080 | 156.43 | 167.40 | 186.79 |
| **Design 1+** | 0.35 | 2.31 | -118.6 | 1 | 98 | 13.66 | 2.5 | 0.169 | 163.59 | 171.31 | **191.22** |
| **Design 2+** | 0.35 | 2.29 | -116 | 1 | 100 | 10.5 | 2.5 | 0.085 | 159.81 | 170.52 | **190.52** |
| **Design 3+** | 0.35 | 2.28 | -114.4 | 1 | 90 | 12.07 | 2.5 | 0.117 | 158.80 | 168.11 | **187.66** |
| **Design 4+** | 0.35 | 2.34 | -112.2 | 1 | 87 | 18 | 2.5 | 0.080 | 158.43 | 169.40 | **188.79** |

*Estimated core area.

+Expected phase noise using $I_{BIAS}$.

$$FoM = 10log_{10}\left(\frac{f_{OSC}}{PN_{offset}}\right) + 10log_{10}(P_{VCO}(mW)) - PN \qquad FoM_A = FoM - 10log_{10}(Area(mm^2)) \qquad FoM_{AT} = FoM_A - 10log_{10}\left(\frac{1}{\Delta f}\right)$$

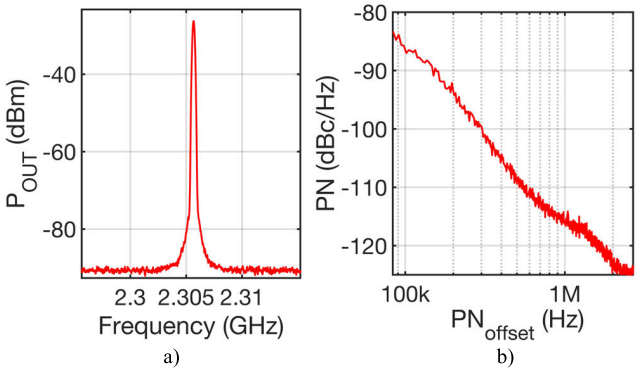


**FIGURE 9.** a) Output spectrum and b) phase noise for Design 1.

same performances when $I_{BIAS}$ shifts (with $V_{TUNE} = 2.5$ V). Fig. 8e) and 8f) show the sensitivity of the VCO performances when $V_{DD}$ shifts (with $V_{TUNE} = 2.5$ V and $I_{BIAS} = 1.7$ mA). In Fig 9a) it is possible to observe the output spectrum of Design 1. The measured $f_{OSC}$ (with $V_{TUNE} = 1.25$ V) deviated 5-6% from the post-layout simulated $f_{OSC}$ (~2.4 GHz). These deviations were consistent over 24 measured VCOs, which indicate that the fabrication process itself was reliable. Since the inductor performances were accurately modeled, the authors attribute these deviations to an underestimation of the tank parasitic capacitances provided by the commercial parasitic extractor. Note that such deviations are not related to the methodology itself and do not hamper its usability. Table 5 lists the measurements results of all four VCO designs compared to other published results. As stated before, the technology selection was determined by the availability of the layer stack information, essential for the implementation of this design methodology. The selection of previously reported results in Table 5, which are relatively old, was therefore motivated by the use of a similar technology node, that could represent a fair comparison for the experimental results reported here. Standalone measurements of the buffer show a $P_{BUF} = 5$ mW which were subtracted from the total $P_{DC}$. Therefore, in Table 5 only the $P_{VCO}$ is considered.

While measuring the phase noise, it was possible to observe that the Keysight B1500A introduced spurs in the VCO output spectrum due to the refresh rate of its screen. Therefore, in order to measure the phase noise, the VCO was powered with a single battery. All biasing voltages where obtained using linear DC regulators and $I_{BIAS}$ was generated using an off-chip variable resistor ($R_{BIAS}$). The measured phase noises using the biasing strategy are given in column 4 of rows 9 to 12 of Table 5 for all designs and in Fig. 9b) for Design 1. The phase noise values shifted slightly from the post-layout simulations because the $R_{BIAS}$ resistor introduced unaccounted noise.

In order to study the difference between the measured and the post-layout simulations, the circuit was re-simulated under the same conditions as measured in the laboratory (using $R_{BIAS}$ instead of the ideal current source $I_{BIAS}$ – see Fig. 2a) emulating therefore a simulation under the actual experimental conditions. The results of such comparisons are shown in Fig. 10. It is possible to observe that the difference between the measured phase noise and the post-layout simulation in the same conditions (with $R_{BIAS}$), is around 2 dBc/Hz. Therefore, it is possible to estimate the phase noise measure, if $I_{BIAS}$ was used, by adding 2 dBc/Hz to the post-layout simulations. The new values for this expected phase noise are given in column 4 of rows 13 to 16 of Table 5 for all designs.

Several figures of merit (FoM) were considered in order to compare the results. FoM takes into account $f_{OSC}$, PN and $P_{DC}$, whereas $FoM_A$, also takes into account the area

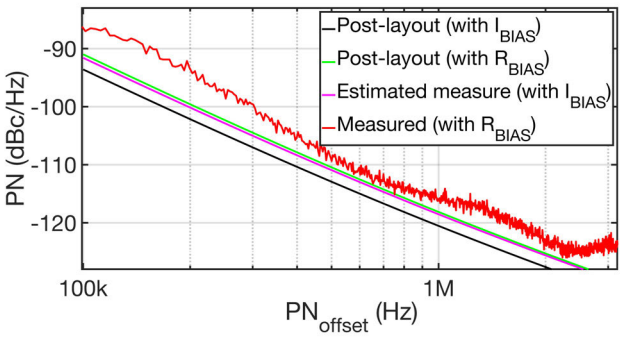


**FIGURE 10.** Phase noise comparisons between measured data and post-layout simulations if a current source ($I_{BIAS}$) or an off-chip resistor ($R_{BIAS}$) is used.

of the VCO core and $FoM_{AT}$ adds the tuning range as a parameter to the FoM. It can be observed that all four circuits designed using this methodology obtain competitive values of all three figures of merit when compared to other works, even when using $R_{BIAS}$. The results obtained in this work prove the strength of the presented automated methodology where more than one hundred fully designed, optimal and ready-to-fabricate VCOs were obtained in only two days of CPU time. Moreover, the obtained designs cover different trade-offs which allow the designer to select the design that best suits his/her needs.

## V. CONCLUSION

This paper reports the experimental validation of a state-of- the-art optimization-based synthesis methodology for RF circuits. Using this methodology, it was possible to obtain a large number of fully-sized, ready-to-fabricate RF circuits. The experimental measurements of several fabricated VCOs suggest that the methodology is fully efficient in attaining competitive designs. Moreover, a Gaussian process machine-learning technique to model integrated inductors was used in the methodology and experimentally validated with silicon implementations. The model can accurately predict the inductors' S-parameters and inductors' SRF while evaluating their performances in milliseconds. By being able to accurately and efficiently predict these S-parameters over the entire design space, the developed model has shown to be extremely useful in the presented circuit synthesis methodology. The methodology developed in this work is valid for any technology node since it uses off-the-shelf circuit simulators, LVS/DRC verification tools and parasitic extractors. Therefore, although in this paper the methodology was tested for a 0.35$\mu$m technology, it would also stand for any modern technology (e.g., 65nm). Furthermore, by applying this methodology to other RF basic circuit blocks, the hierarchical bottom-up approach proposed by the authors in [4] could be additionally used to handle more complex circuits and systems.

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