Feed-forward Modulation Technique for more Accurate Operation of Modular Multilevel Converters

Pablo Montero-Robina, Abraham Marquez, *Member, IEEE,* Mohamed S.A. Dahidah, *Senior Member, IEEE,* Sergio Vazquez, *Fellow, IEEE,* Jose I. Leon, *Fellow, IEEE* Georgios Konstantinou, *Senior Member, IEEE,* and Leopoldo G. Franquelo, *Fellow, IEEE*

***Abstract*—Modular multilevel converters have become the prominent topology for medium and high-voltage applications. The performance of these converters highly depends on the accuracy of the used modulation approach, for which the capacitor voltage of submodules (SM) are usually assumed to be equal. This paper *exhibits* that ignoring the capacitor voltage differences among SMs adversely affects the *system performance.* This becomes more obvious the larger the capacitor voltage differences are. Hence, this paper proposes a more accurate feed-forward modulation approach that takes into account either the instantaneous capacitor voltage value and the real output voltage in the modulation stage. As a result, in applications where larger SM voltage differences are expected, the current distortion and control performance is improved. Particularly, switching-saving approaches benefit from this approach as it enables their operation with reduced switching losses without the downsides of increased distortion due to capacitor voltage differences. The proposed approach is analyzed and compared with the nearest level modulation and with the level-shift PWM (LS-PWM). Simulations and experimental validation are presented to confirm the effectiveness of the proposed technique.**

***Index Terms*—Capacitor voltage balancing, circulating current, feed-forward modulation, modular multilevel converters (MMC), switching-saving algorithm**

I. Introduction

The continuous developments in power electronics have made power converters the game-changer for modernizing power networks. In this regard, high-voltage direct current (HVDC) systems have made great impact on the transmission of electricity and integration of large renewable resources [1], particularly in offshore wind energy conversion systems [2]. However, the required voltage source converters (VSC) necessitate switches that can cope with the high-voltage requirement of such application. Modular multilevel converters (MMC), on the other hand, have shown high potential in this field, alleviating the challenges associated with conventional converters. MMCs demonstrate distinctive features such as modularity, redundancy and scalability, that make them competitive solution for such applications [3].

The MMC is formed by series-connected submodules (SM) with an inductor to limit the output current ripple and harmonic contents. Several SM configurations have been proposed in the literature to address various operational requirement [4], however half-bridge topology was the first one proposed and it has been widely adopted, owing to its simplicity. While managing active and reactive power flows is the main aim of MMC-based systems, capacitor voltage balancing [5], [6] and circulating current regulation [7], [8] can be significant challenges to ensure proper operation, and thus they required to be controlled [3]. The operation of the MMC, that is the commanding of the switching devices, is usually carried out by some well-known modulation techniques [9] such as nearest level modulation (NLM) [10], variable rounding level control (VRLC) [11], or carrier-based pulse width modulation (CB-PWM) [12], [13]. In contrast to PWM-based techniques, NLM switches an integer number of SMs for the whole period of commutation, hence it avoids extra commutations and it is the simplest to implement [14]. However, this leads to a modulation error due to the rounding effect of selecting an integer number of SMs, although this error gets smaller as the number of SMs increases. Alternatively, by using PWM [12], the previous error can be compensated. In this way, level-shift (LS-PWM) [15] and phase-shift (PS-PWM) [16] techniques have been considered. There are papers devoted to the differences and similarities between NLM and PWM-based approaches [9], [13], [17]

Prior to the modulation stage, it is common to carry out a normalization step on the reference voltage either by direct or indirect modulation [18]. While the former is the most straightforward solution that uses the common dc bus voltage, the indirect modulation considers the average capacitor voltage for each arm to achieve a more accurate output voltage. In a similar manner, [19] proposes a controller that considers the average capacitor voltages of each arm separately. Alterna-

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P. Montero-Robina is with the Systems Engineering and Automatic Control Department, Universidad de Sevilla, Sevilla 41092, Spain (e-mail: pmontero1@us.es).

M. Dahidahis with the Electrical Power research group, School of Engineering, Newcastle University, Newcastle upon Tyne, NE1 7RU, United Kingdom (email: mohamed.dahidah@ncl.ac.uk).

G. Konstantinou is with the School of Electrical Engineering and Telecommunications, University of New South Wales, Sydney, NSW 2052,Australia (e-mail: g.konstantinou@unsw.edu.au).

A. Marquez, S. Vazquez, J.I. Leon, L. Franquelo are with the Electronics Department, Universidad de Sevilla, Sevilla 41092, Spain (e-mail: amarquez@ieee.org, sergi@us.es, jileon@us.es, lgfranquelo@us.es).

tively, [20] presents a modification of the NLM by adding a variable offset in the rounding function that reduces the output voltage ripple. The same authors later incorporate a predictive technique with delay compensation [21]. However, none of these methods consider the scenario of different SM capacitor voltage values within the same arm. Indeed, this will introduce an error to the modulated voltage. As a workaround, [22] proposed a PS-PWM approach where there is a voltage command for each SM that is later normalized based on the actual SM capacitor voltage. This solves the modulation error problem, however, every voltage command has to be normalized with regards to the corresponding SM voltage and all SMs are PWM-switched, which both increase the computation burden and the switching losses.

This paper aims to mitigate the above-mentioned modulation errors by a feed-forward modulation technique. The concept of feed-forward modulation for accurate modulation was presented in [23] for space-vector-based modulation in single-phase cascaded H-bridge converters. This paper adapts its implementation for MMC with half-bridge SM using LS-PWM, which results in the proposal of a feed-forward LS-PWM (FF-LS-PWM) technique. For this, the individual measured SM capacitor voltages are stacked until the output reference voltage is reached. Therefore, in contrast to [22], the SM states are determined through simple comparisons, and the only normalization is carried out for the PWM-switched SM in each arm, reducing both the switching losses and the computational burden in comparison with [22]. In this way, each capacitor voltage ripple is considered [24], and a more accurate output voltage is achieved, avoiding any introduced current distortion [25]–[27]. The capacitor voltage ripple control objective can be relaxed, which is particularly beneficial for some applications or algorithms, such as renewable energy integration [28], smaller capacitor systems [29], [30], or switching-saving algorithms (SSA) [31]. However, due to the requirement of measuring the instantaneous capacitor voltage of each SM and the added complexity compared to NLM, this approach would be limited to medium-voltage applications with relatively low number of SMs. It is worth mentioning that some SSAs present a trade-off between the SM switching frequency and SM capacitor voltage ripple; the lower the frequency, the larger the voltage ripple [32]. This paper presents some results with SSAs [24], [25], [31], where the capacitor voltage differences are more noticeable, to illustrate the benefits of the method.

The remainder of the paper is organized as follows. Section II revisits the operation of the MMC system and its modulation approaches. Section III analytically presents and discusses the benefits of the proposed modulation technique when compared to the widely-used LS-PWM and NLM techniques. Some simulation results are exposed and discussed in Sect.IV .Illustrative experimental tests are presented in Section V, validating and confirming the effectiveness of the proposed method. Finally, some conclusions are summarized in Section VI.

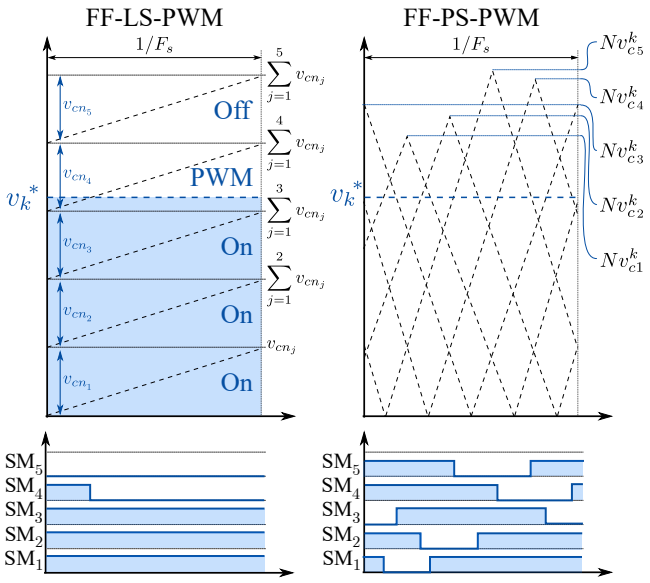

Fig. 1. Feed-forward concept used for LS-PWM and PS-PWM.

II. The MMC System: Operating Principal and Modulation

This section is dedicated to revisit the basic structure of the MMC and its operation. Two well-known modulation approaches (i.e. NLM [10] and LS-PWM [9], [12]) are firstly analyzed to layout the foundation for the proposed technique. The proposed method, which will be referred as feed-forward LS-PWM (FF-LS-PWM), is then presented at the end of this section, which is based on modifying the computation of the duty ratio of the LS-PWM by taking into account the individual instantaneous capacitor voltage. It is worth mentioning that the proposed approach could be extended to other modulation approaches that rely on CB-PWM by modifying the carriers accordingly, as it is shown in Fig. 1, where it is implemented for LS-PWM and PS-PWM.

A. System description

Fig. 2 illustrates the basic structure of one-leg (single-phase) MMC. There are two arms that are built using N half-bridge SMs. Each arm is connected in series with an inductor L_s to limit the current. In the forthcoming analysis, index k denotes the arm, i.e. $k = \{u, l\}$ is the upper and lower arm, respectively; whereas sub-index n refers to the submodule number $n \in [1, N]$

Each SM constitutes of two active switches (S_n^k and its counterpart $\overline{S_n^k}$), and a capacitor whose voltage is denoted as v_{cn}^k. Variable v_n^k denotes the output voltage of SM_n^k. Variables i_u and i_l are the upper and lower arm currents, respectively, whose sum gives the output current that goes through the output inductance L_g. The dc bus voltage, denoted as v_{dc}, is connected in parallel to the two arms whose arm voltage is defined as $v_k = \sum_{n=1}^{N} v_n^k$.

The focus of this work is on improving the modulation stage to ensure a more accurate operation of the converter with enhanced performance when the capacitor voltage differences

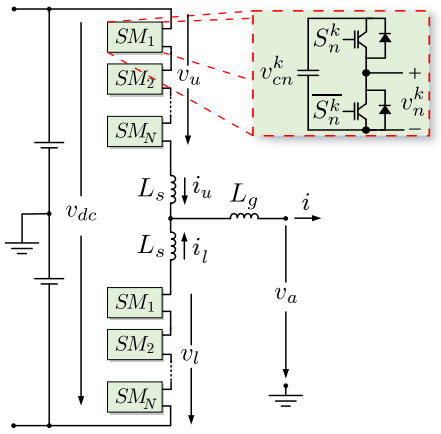

Fig. 2. Layout of a single-phase MMC with half-bridge submodules.

are more noticeable. For this, the arm voltage reference, denoted as $v_k{}^* \in [0, v_{dc}]$—where super-index * denotes the reference value—, for each arm is known and provided by the typical controllers [22].

To facilitate a sensible comparison, indirect modulation is considered from now on, resulting in a normalized arm voltage reference of $v_{k_z}^* \in [0, N]$—where sub-index $_z$ denotes a normalized value.

B. Nearest Level Modulation (NLM)

NLM is considered one of the easiest modulation for MMC that directly computes the switching states of the SM [10]. Due to its familiarity in the field of MMC modulation, NLM is included in the following analysis. With this method, the rounding value of $v_{k_z}^*$ determines the number of switched-on SMs. Letting n_u and n_l be the number of switched-on SMs defined by the sorting algorithm (i.e. $n = 1$ to $n = N$) for each arm, the resulting arm voltage v_k is:

$$\begin{cases} n_u = \text{round}(v_{u_z}^*) \\ n_l = \text{round}(v_{l_z}^*) \end{cases} \quad ; \quad v_k = \sum_{n=1}^{n_k} v_{cn}^k \tag{1}$$

where '*round*' is the rounding function. If the normalization step assumes that the SM capacitor voltages within the arm are equal to their average value—denoted as $\overline{v_c^k}$—, then the desired arm voltage v_k^* is computed as:

$$v_k{}^* = v_{k_z}^* \underbrace{\frac{1}{N}\sum_{n=1}^{N} v_{cn}^k}_{\overline{v_c^k}\text{ : arm } k \text{ average capacitor voltage}} \quad \text{for } k = \{u, l\}. \tag{2}$$

However, the actual arm voltage is the one given by (1). Therefore, a modulation error, denoted as $\widetilde{v_k}$, exists, which can be obtained as follows:

$$\widetilde{v_k} = v_k{}^* - v_k = \left(\frac{v_{k_z}^*}{N} - 1\right)\sum_{n=1}^{n_k} v_{cn}^k + \frac{v_{k_z}^*}{N}\sum_{n=n_k+1}^{N} v_{cn}^k \,. \tag{3}$$

To demonstrate this, an example for one arm is shown in Fig. 3(a), illustrating a capacitor voltage distribution ($v_{cn}^k \in \overline{v_c^k} \pm 5\%$) of one arm for different values of N with same value of v_{dc}. The modulation error described by (3) is depicted in Fig. 3(b) for different values of $v_{k_z}^* \in [0, N]$. **Assuming this particular distribution and that $\overline{v_c^k}$ gets smaller with N**, the larger the N, the smaller the error.

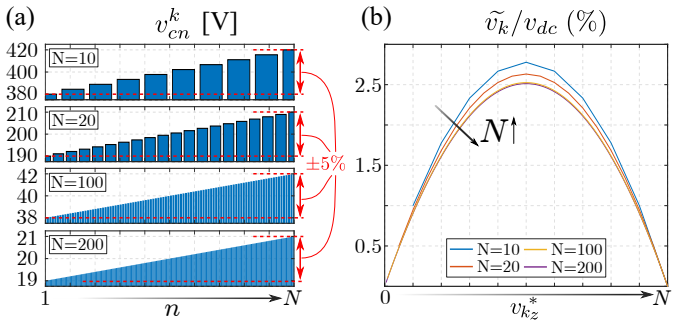

Fig. 3. Example of error made because of equal capacitor voltage assumption in one arm: (a) Capacitor voltage distribution from SM_1 to SM_N with a variation within 5 % of $\overline{v_c^k}$, (b) Voltage arm error as a % of v_{dc}.

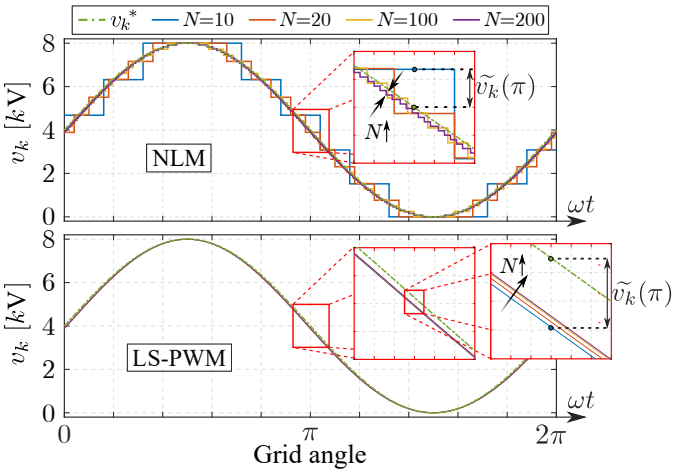

Fig. 4. Example of modulated arm voltage over a grid period using NLM and LS-PWM under different values of N against desired voltage v_k^*.

C. Level-shifted pulse-width modulation (LS-PWM)

LS-PWM technique is one of the well-known and commonly used carrier-based PWM technique. In contrast with NLM, this approach implements the PWM in the SMs. Therefore, the integer part of the $v_{k_z}^*$ is the number of switched-on SMs, while the non-integer part of $v_{k_z}^*$ will be modulated by PWM. It is worth noting that the sorting algorithm prioritizes and orders SMs in accordance with their status, therefore the PWM-modulated SM might change accordingly. As a result of using LS-PWM, the rounding error is corrected, and (1) is modified as follows:

$$\begin{cases} n_u = \text{floor}(v_{u_z}^*) \\ n_l = \text{floor}(v_{l_z}^*) \end{cases} \quad ; \quad v_k = \sum_{n=1}^{n_k} v_{cn}^k + d_{n_k+1}^k v_{cn_k+1}^k \,, \tag{4}$$

where $d_{n_k+1}^k \in [0, 1]$ is the respective duty ratio, i.e. the portion of time that the additional PWM-modulated SM (n_k+1-th SM) is turned on.

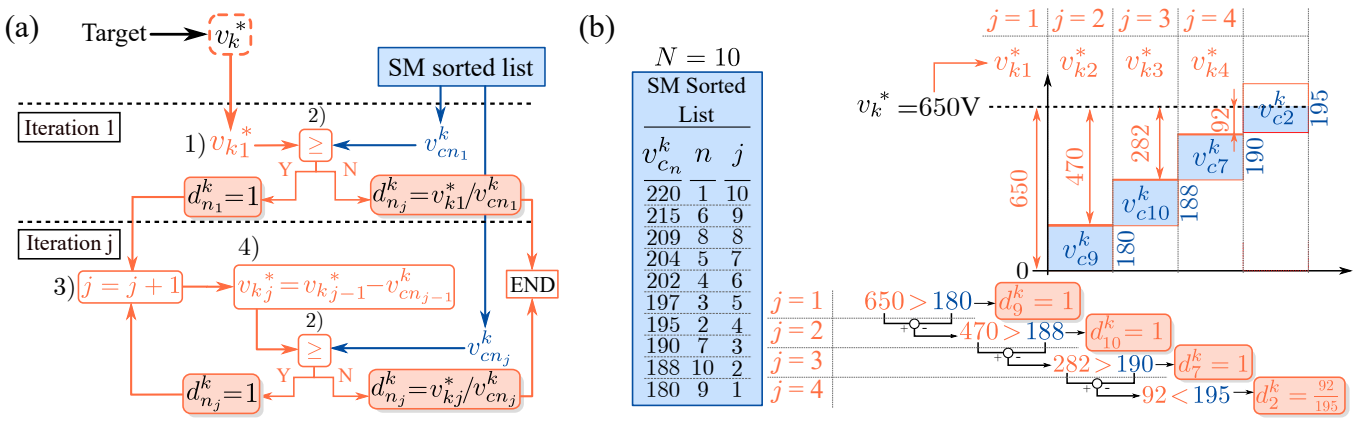

Fig. 5. (a) Flowchart of proposed modulation approach. (b) Example of proposed modulation for $N = 10$, a given sorted list and $v_k^* = 650$ V

Nevertheless, due to the equal voltage assumption, the modulated arm voltage v_k would differ from the desired one as follows:

$$\widetilde{v_k} = \left(\frac{v_{k_z}^*}{N} - 1\right)\sum_{n=1}^{n_k} v_{cn}^k + \frac{v_{k_z}^*}{N}\sum_{n=n_k+1}^{N} v_{cn}^k - d_{n_k+1}^k v_{cn_k+1}^k \,, \quad (5)$$

This is similar to (3) but including the duty ratio term, which complements the rounding function in NLM. Fig. 4 presents a modulated sinusoidal arm voltage (v_k^*) using NLM and LS-PWM for different values of N. The capacitor voltage values follows the same distribution shown in Fig. 3(a). It can be observed that the error, whether it comes from the equal voltage assumption or the rounding effect for NLM, is reduced as N increases, although, for low number of SM, the rounding effect is much larger than the one caused by the normalization. Nevertheless, it is clear that the greater the capacitor voltage differences, the larger the error induced by the normalization.

To provide an example for one arm k, $N = 10$, $\overline{v_c^k} = 200$ V and $v_k^* = 650$ V is considered, along with the capacitor voltage values exhibited in Fig. 5(b). The LS-PWM would yield the following results:

$$v_{k_z}^* = 3.25\left(\frac{650\text{ V}}{200\text{ V}}\right) : 3\text{ SM ON, 1 SM PWM}$$
$$\{d_9^k, d_{10}^k, d_7^k\} = 1\,; \quad d_2^k = 0.25$$
$$v_k = v_{c9}^k + v_{c10}^k + v_{c7}^k + 0.25 v_{c2}^k = 606.75,$$
$$\widetilde{v_k} = 650 - 606.75 = 43.25\text{ V}(6.6\,\%)$$

where a deviation of 6.6% from the desired value is noticed.

D. Feed-forward LS-PWM (FF-LS-PWM) Algorithm

This process is carried out for each arm k, where, the desired arm voltage v_k^* in (2) is considered instead of the normalized one. The SMs are switched-on in accordance to the sorting algorithm. Let j be the index for the sorting algorithm list, then the proposed technique is carried out with the following procedure, which is summarized in the flowchart of Fig. 5(a):

1) Variable v_k^* is saved into variable v_{k1}^*.
2) Starting with $j = 1$, variable v_{kj}^* is compared with the capacitor voltage of the j-th SM in the sorted list (let us denote it as $v_{cn_j}^k$)—which, in the sorted list example of Fig. 5(b), would be v_{c9}^k for $j = 1$, v_{c10}^k for $j = 2, \ldots$. If it is larger, then the respective SM is fully connected ($d_{n_j}^k = 1$) and continues with the next iteration. However, if it is smaller, then the SM is PWM-switched with a duty ratio of $d_{n_j}^k = v_{kj}^*/v_{cn_j}^k$, **the remaining SMs, i.e. SM$_n$ for $n = j+1, \ldots, N$, are disconnected,** and the iteration ends.
3) If the previous considered SM was fully connected ($d_{n_j}^k = 1$), the variable j is updated $j = j + 1$.
4) The remaining arm voltage to be modulated is then updated considering the previous **decision**, that is $v_{kj}^* = v_{kj-1}^* - v_{cn_{j-1}}^k$, and the process is repeated again from point 2).

In any case, the iteration ends when the duty ratio for the PWM-switched SM is computed. In contrast to [22], only one duty ratio is computed per arm while the remaining SMs' state are derived from logical comparisons. For the sake of clarity, the flowchart of the proposed approach is depicted in Fig. 5 with an illustrative example when $v_k{}^* = 650$ V.

III. Analysis and Discussion

To further demonstrate the benefits of the proposed method, a theoretical analysis facilitated with an example is presented. To do so, $N = 20$ is assumed, and the SMs capacitor voltages are normalized ($v_{cn_z}^k$) (with respect to the average $\overline{v_c^k}$) and distributed as depicted in Fig. 6. This example considers a maximum deviation of 30%, i.e. $v_{cn_z}^k \in [0.7, 1.3]$, and that the SMs are already arranged by the sorting algorithm in the proper order, $n = 1 \to 20$. Furthermore, a sinusoidal reference $v_{k_z}^*$ with unity modulation index is assumed. Therefore, one can mathematically express this as follows:

$$v_{cn_z}^u(n) = 1 - 0.3\sin((n-10)\frac{\pi}{20}) \quad (6)$$
$$v_{cn_z}^l(n) = 1 + 0.3\sin((n-10)\frac{\pi}{20}) \quad (7)$$
$$v_{u_z}^* = -10\cos(\omega t) + 10 \quad (8)$$
$$v_{l_z}^* = 10\cos(\omega t) + 10 \quad (9)$$
$$v_z^* = v_{l_z}^* - v_{u_z}^*, \quad (10)$$

where v_z^* is the normalized output voltage reference, **and $v_{cn_z}^k(n)$ refers to the continuous function that expresses the capacitor voltage for arm k.** Now, using the continuous function with the average model of NLM and LS-PWM yields:

$$v_z = v_{lz} - v_{uz} \tag{11}$$

$$\text{NLM: } v_z = \underbrace{\int_0^{\text{round}(v_{lz}^*)} v_{cn_z}^l(n)dn}_{v_{lz}} - \underbrace{\int_0^{\text{round}(v_{uz}^*)} v_{cn_z}^u(n)dn}_{v_{uz}} \tag{12}$$

$$\text{LS-PWM: } v_z = \underbrace{\int_0^{v_{lz}^*} v_{cn_z}^l(n)dn}_{v_{lz}} - \underbrace{\int_0^{v_{uz}^*} v_{cn_z}^u(n)dn}_{v_{uz}}, \tag{13}$$

where v_z is the normalized modulated output voltage.

The output voltage for both NLM and LS-PWM can now be compared using (12) and (13) as portrayed in Fig. 7. As it can be observed, the error produced in the modulation stage, as a result of equal SM voltages assumption, generates dc and low-order harmonics that adversely impacts the performance of the converter. With reference to Fig. 2, one can easily derive the circulating current dynamical equation as follows [27]:

$$v_{dc} = v_u + v_l + L_s\frac{d(i_u - i_l)}{dt} = v_{\text{com}} + 2L_s\frac{di_{\text{circ}}}{dt},$$

where v_{com} is the common component of the upper and lower arm's voltages, i.e. $v_{\text{com}} = v_u + v_l$. Therefore, any modulation error in v_{com} would also affect the circulating current controllability. Once again, under the worst case scenario for i_{circ}, both arms follow the same capacitor voltage distribution, i.e. eq. (7) and $v_{cn_z}^u(n) = v_{cn_z}^l(n)$ are used. Following this assumption, the modulated normalized common voltage ($v_{\text{com}_z} = v_{uz} + v_{lz}$) is shown in Fig. 8. Note that, in this example, the desired normalized common voltage ($v_{\text{com}_z}^* = v_{u_z}^* + v_{l_z}^*$) should be equal to 20 according to (8)-(9). This fact forces the controller to supplement such error, imposing additional restrictions on the controller design, or even generating instabilities as this error can be seen as external disturbances in the closed-loop scheme. This is clearly demonstrated in the experimental result discussed in the following section.

Following on the previous analysis and discussion, there are several practical applications where the proposed modulation would offer better performance and benefits as opposed to NLM and the conventional LS-PWM. Examples include:

- Solutions to medium-voltage applications [5], where the number of SMs is relatively low and the capacitor voltage differences might be more remarkable. In these scenarios, the added complexity is kept low due to the reduced number of measures , while the modulation error compensation achieved with this approach enhances the system performance.
- Integrating renewable energy [13], and energy storage systems [28]. Naturally, these results in unequal steady-state SM capacitor voltages and/or uneven power consumption among SM.
- Application of switching reduction or SSA [33], which are evolving with MMC as an attempt to reduce losses and increase efficiency. **One way to achieve it is by** prolonging the conduction time of SMs, which in turns increases the difference between SMs capacitor voltages. Due to this, SSAs will be considered in the simulation and experimental verification to exhibit one of the potential application of this approach.
- Using smaller capacitors to enable a more compact MMC system [29]. This can be achieved by relaxing the permissible capacitor voltage ripple [34], which would compromise the quality and the performance of the system were the actual capacitor voltage not be taken into account in the modulation stage.

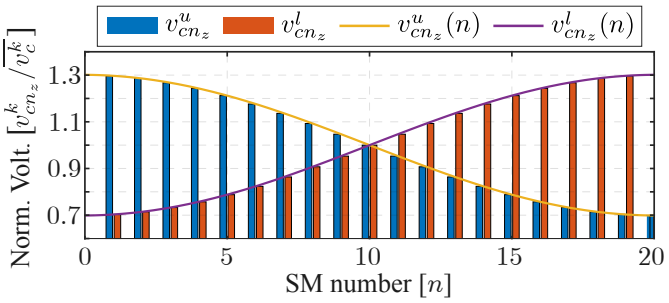

Fig. 6. Example of normalized capacitor voltage distribution, and the continuous function that interpolates them, used for the theoretical analysis with $N = 20$.

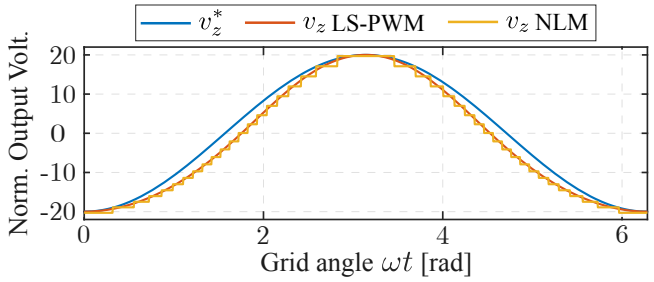

Fig. 7. Normalized output voltages: desired vs modulated by LS-PWM and NLM considering the capacitor voltage distribution of Fig. 6.

IV. Simulation Results

This section presents figures and results of the modulation proposal when compared with LS-PWM. Direct comparison with NLM is skipped given that the literature is plenty of comparisons between LS-PWM and NLM, and that LS-PWM performs better than NLM in terms of accurate modulation.

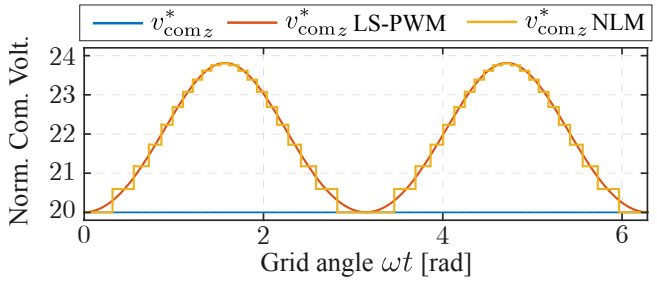

Fig. 8. Normalized common voltage: desired vs modulated by LS-PWM and NLM considering the capacitor voltage distribution given for arm u in Fig. 6 for both arms such that $v_{cn}^l(n) = v_{cn}^u(n)$.

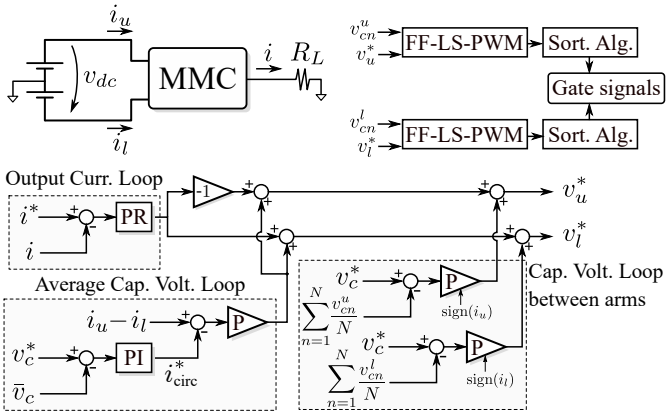

Fig. 9. Block diagram of the used control scheme extracted from [22].

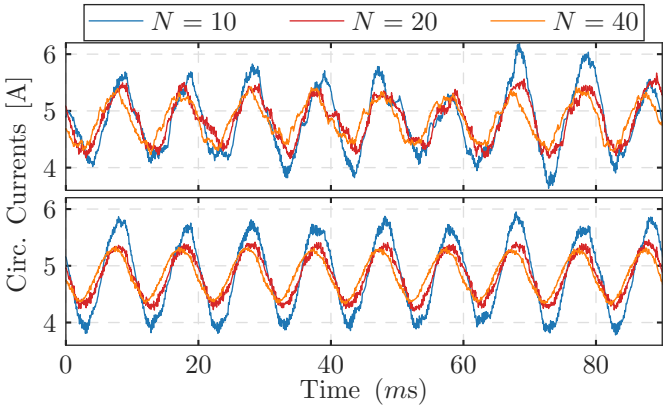

Fig. 10. Circulating current for LS-PWM (top) and FF-LS-PWM (bottom) when a voltage band of 5% is allowed for SSA, for different values of N.

Firstly, an scheme of the employed controller for the simulations is shown in Fig. 9, where two balancing loops and the output current controller are shown. Note that this control scheme is extracted from [22].

To test the improvement of FF-LS-PWM against LS-PWM, a SSA based on a voltage band is used in this section. **The sorting algorithm list for each arm is updated only if a SM voltage deviates away from a defined band. As a consequence, capacitor voltage differences within each arm are generated. For the remaining of this section, the voltage band is set to be 5% of the capacitor voltage reference $\bar{v}_c^* = v_{dc}/N$, which is fixed to 50 V for all tests. Consequently, the dc-link voltage varies accordingly as $v_{dc} = 50N$ V between tests. In order to provide more straight comparisons, the current reference amplitude, load resistor and control parameters are kept constant ($I^* = 32\,A$ and $R = 10\Omega$) between tests.**

The first test shows the circulating current behaviour for LS-PWM and FF-LS-PWM for different number of SMs (N) in Fig. 10. Note how the FF-LS-PWM improves the controllability and smooths the current distortion due to the improved modulation accuracy.

In order to exhibit how these capacitor voltage differences affect the output current distortion, Fig. 11 depicts the output current THD value under different values of N for LS-PWM

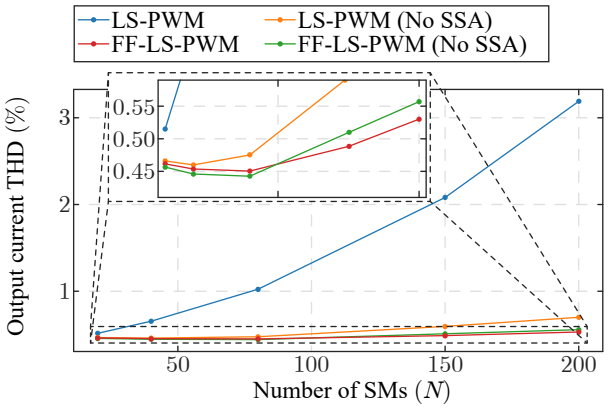

Fig. 11. THD value of the output current for LS-PWM and FF-LS-PWM when the number of SMs are increased.

and FF-LS-PWM with and without the SSA. As it can be seen, considering that $\bar{v}_c^*$ is fixed, the modulation error increases with the number of SMs when a SSA is used, however, FF-LS-PWM is capable of compensating such modulation error, resulting in a minimal change of THD. Besides, the use of SSA while adopting FF-LS-PWM has a negligible effect on the THD value. With a switching and sampling frequency of 5 kHz, the average SM switching frequencies are shown in Table I. Note that both modulations yield similar switching performance, however the distortion performance exhibits some remarkable improvements with FF-LS-PWM.

TABLE I
AVERAGE F_s (kHZ) PER SM OBTAINED FROM SIMULATION

N	LS-PWM	FF-LS-PWM	LS-PWM (SSA)	FF-LS-PWM (SSA)
20	3.05	3.03	0.96	0.95
40	3.82	3.79	0.85	0.85
80	4.28	4.28	0.76	0.76
150	4.40	4.39	0.72	0.72
200	4.47	4.44	0.71	0.71

In summary, FF-LS-PWM with SSA exhibits slightly better distortion performance with considerable reduced commutations when compared with LS-PWM without SSA. LS-PWM with SSA achieves a similar switching reduction at the expenses of largely worsening the distortion performance. It is worth mentioning that PS-PWM in [22] could present an improvement in the current distortion, however, it will be at the cost of PWM-switching every SM, and increasing the computational burden due to the voltage command being normalized for each SM.

V. EXPERIMENTAL VERIFICATION

Fig. 12 shows a 200 W scaled-down single-phase laboratory prototype of an MMC built using 6 modules—3 per arm—to experimentally validate the feasibility of the proposed modulation technique. The parameters of the experimental setrig are tabulated in Table II.

The control system follows the scheme of Fig. 9 [22], which is implemented using a rapid-prototyping SpeedGoat platform as the data acquisition and processing unit. The output current

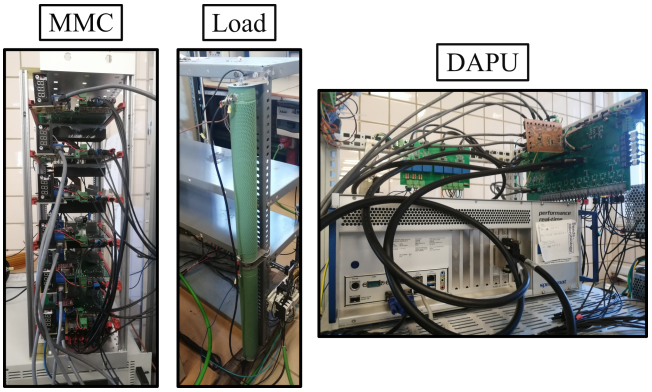

Fig. 12. Single-phase MMC used in experiments along with data acquisition and processing unit (DAPU) and external resistor used as load.

TABLE II
EXPERIMENTAL PARAMETERS

Parameter	Value	Parameter	Value
L_s Arm Inductance	2 mH	L_g Output Inductance	2 mH
C_{SM} SM Capacitance	2 mF	N Number of SM per arm	3
R_L Load Resistance	60 Ω	I^* Load Current reference	1 A
v_{dc} dc-link Voltage	150 V	F_s Sampling Frequency	10 kHz
Output frequency	50 Hz	k_p^{PI} Prop. avg. cap.	0.1
k_i^{PI} Int. avg. cap.	0.05	k_p^{P} Prop. avg. and bal.	1
k_p^{PR} Prop. Out. Curr.	20	k_r^{PR} Res. Out. Curr.	500

control loop tracks a sinusoidal reference with amplitude of I^*. The PR parameters are kept constant at $k_p^{\text{PR}} = 20$ and $k_r^{\text{PR}} = 500$ for all tests conducted in the experimental work. The voltage control loops are implemented considering $v_c^* = v_{dc}/N$ with $k_p^{\text{PI}} = 0.1$, $k_i^{\text{PI}} = 0.05$ and $k_p^{\text{P}} = 1$ for the average control loop, and $k_p^{\text{P}} = 1$ for the balancing between arms. Note that the average capacitor voltage regulation in Fig. 9 involves the circulating current control with a P controller (gain k_p^{P}).

The feasibility of the proposed approach is evaluated using different scenarios of SSA with LS-PWM. **The first one is based on a voltage band as explained in Sect. IV, and the second one uses a time counter [31] which updates the sorting list when a given time has elapsed.** The aim of this is to prolong the conduction time of each SM, hence generating larger voltage ripple and reducing the switching events.

Fig. 13 shows the load currents (i) for the LS-PWM and the FF-LS-PWM along with its low-order harmonic spectrum, with and without employing SSA. Both approaches exhibit similar performance when SSA is not applied. However low-order harmonics appear with LS-PWM when the SSA is implemented. In contrast, with FF-LS-PWM the harmonic profile remains unchanged. In terms of circulating current, the error associated with the use of SSA affects the stability of the current control, causing loss of controllability at some instants. This is clear from Fig. 14, where the circulating currents for LS-PWM and FF-LS-PWM under different switching frequencies are depicted. A similar consequence can be seen in Fig. 15, where the load currents with fundamental frequencies of 100 and 200 Hz, and the circulating currents of FF-LS-PWM and LS-PWM with a SSA with a voltage band of 8 V (16%) are shown. Additionally, Fig. 16 and Fig. 17 demonstrate how the capacitor voltages evolve under both SSAs. Note that FF-LS-PWM achieves a more linear evolution in the capacitor voltages due to the fact that the balancing closed-loop is not affected, in spite of being large differences between SMs—a voltage band of 12 V (24%) in this system can yield one SM to have a voltage around 160% of the smallest capacitor voltage.

Extensive experimental testing were conducted on LS-PWM and FF-LS-PWM, looking into different performance indices as summarized in Table III. These include: total harmonic distortion (THD) of the load current; harmonic distortion of the first 40 harmonics ($\text{HD}_{[0-40]}$) of the load current—to indicate the low-order harmonic presence—; the average switching frequency of all SMs ($\bar{F}_s$)—measured and computed over 70 fundamental periods—, and the standard deviation (σ_{F_s}) of the SM switching frequencies. With this, the benefits of the FF-LS-PWM in achieving overall better THD values and lower low-order harmonic contents over all SSA scenarios considered are exhibited. Moreover, the proposed FF-LS-PWM improves the commutation reduction achieved by the SSA, regardless of the method used. Also note that the value of σ_{F_s} in the FF-LS-PWM, when applying SSA with low values of voltage band or time counter, is lower than the LS-PWM while still achieving a reduction in the number of commutations. This could suggest the feasibility of using FF-LS-PWM with SSA to reduce the switching losses and **to equalize the SM usage as the average switching frequencies tend to be closer in value.**

It is shown how the proposal performs under different capacitor voltage difference profiles using two different techniques of SSA, however, other approaches that required relaxed capacitor voltage difference constraints between SMs within the same arm would be benefited from using FF-LS-PWM.

VI. CONCLUSIONS

This paper presented an accurate approach that addresses the error resulted from the normalization step of typical modulations for MMC.

It has been exhibited that ignoring the capacitor voltage ripple in the modulation stage results in an error that has negative impact on the system performance, especially in applications where the capacitor voltage differences are large. The proposed FF-LS-PWM solves the latter by taking into account the reference voltage and the individual capacitor voltages of each SM. Hence, an accurate arm voltage modulation is achieved.

The FF-LS-PWM is tested experimentally and compared with the standard LS-PWM while using a SSA. The results show that FF-LS-PWM does not increase the THD value of the output current while the capacitor voltage values **can move around a band up to** $\pm 24\%$, at the same time that a 13% of commutation reduction is achieved. **Additionally, LS-PWM suffers from these differences, compromising the performance of the implemented controllers,** which is avoided by the introduction of FF-LS-PWM.

The theoretical analysis, supported by simulation and experimental verification, shows the feasibility and effective-

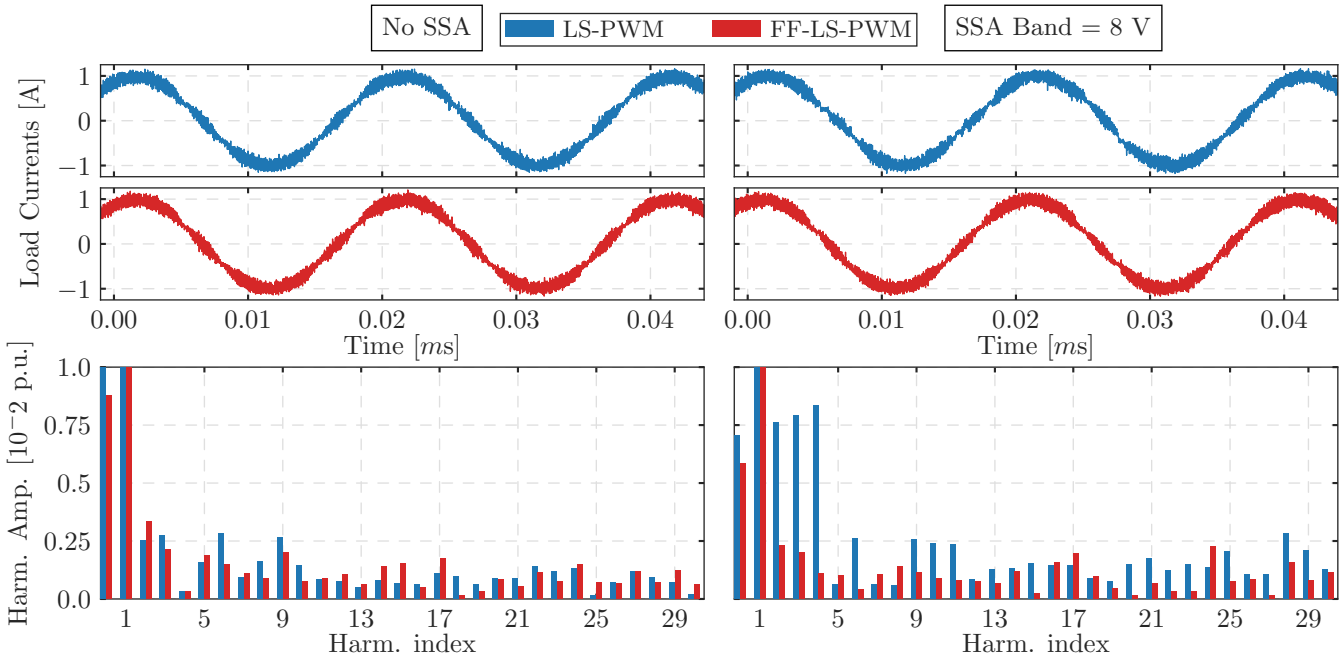

Fig. 13. Experiment results: Load current and its harmonic spectrum for the LS-PWM and the FF-LS-PWM when no SSA and SSA with voltage band of 8 volts are considered.

TABLE III
EXPERIMENTAL RESULTS

SSA	THD [% A/A_1]		$HD_{[0-40]}$ [% A/A_1]		Avg. swt. freq. $\bar{F}_s$ [kHz]		σ_{F_s} [Hz]	
	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM	LS-PWM	FF-LS-PWM
No SSA	11.77	11.87 [+1%]	1.45	1.43 [-1%]	7.705	7.724 [0%]	11.3	11.6 [+3%]
Band 4	12.01	11.87 [-1%]	1.31	1.20 [-8%]	6.815	6.725 [-1.3%]	11.5	9.04 [-21%]
Band 8	12.18	11.42 [-6%]	2.60	1.13 [-56%]	6.996	6.732 [-3.8%]	9.32	21.2 [+127%]
Band 12	13.31	11.64 [-13%]	5.12	1.15 [-78%]	7.047	6.732 [-4.5%]	9.96	26.9 [+170%]
Counter 0.05	11.85	11.96 [+1%]	1.86	1.93 [+4%]	6.763	6.731 [-0.5%]	10.2	5.25 [-49%]
Counter 0.10	11.92	11.79 [-1%]	2.41	1.89 [-22%]	6.852	6.729 [-1.8%]	22.4	14.1 [-37%]
Counter 0.15	12.76	11.72 [-8%]	4.48	1.27 [-72%]	6.917	6.728 [-2.7%]	23.2	27.3 [+18%]

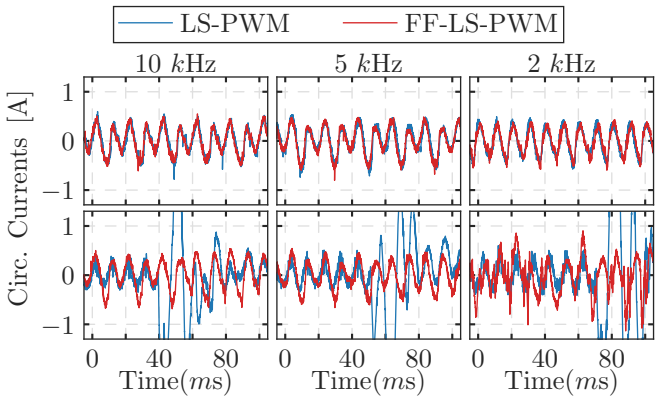

Fig. 14. Circulating current of the LS-PWM and the FF-LS-PWM under different switching frequencies (10, 5 and 2 kHz) when no SSA (Top) and SSA with a voltage band of 8 V (bottom) are considered.

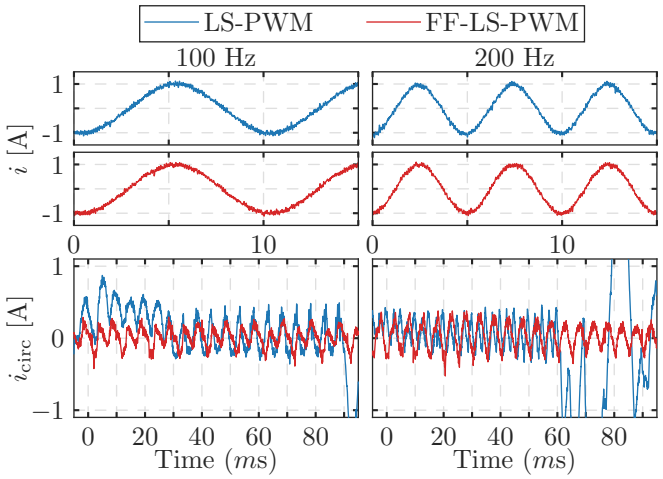

Fig. 15. Load and circulating currents when modulating 100 and 200 Hz output signals for the LS-PWM and the FF-LS-PWM while using a SSA with a voltage band of 8 V.

ness of the proposed approach. Finally, it is worth mentioning that the accuracy achieved comes at the expense of increased computational requirement associated with the instantaneous measurement of the SM capacitors. However, the gained

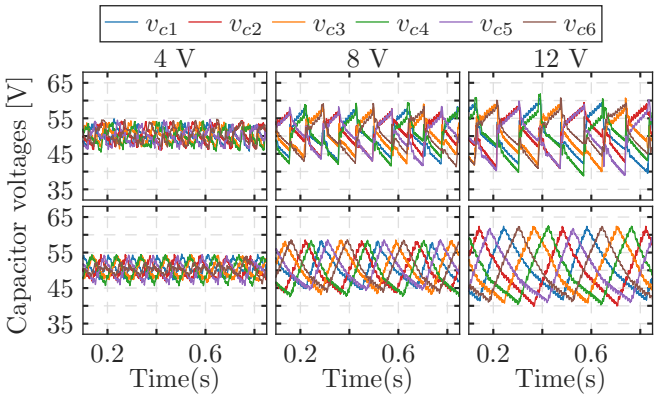

Fig. 16. Capacitor voltage evolution of the SMs for the LS-PWM (top) and the FF-LS-PWM (bottom) when voltage-based SSA is used under different values of the voltage band.

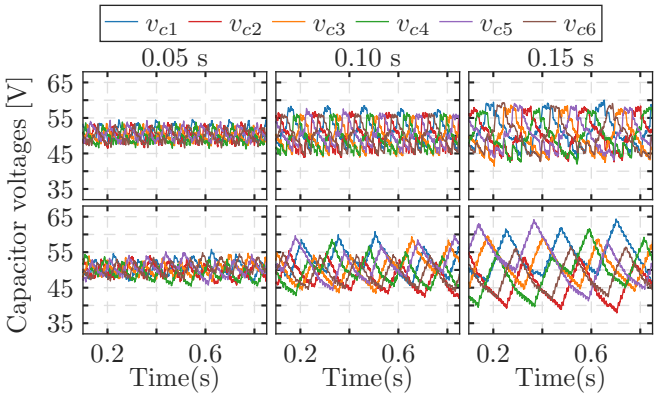

Fig. 17. Capacitor voltage evolution of the SMs for the LS-PWM (top) and the FF-LS-PWM (bottom) when counter-based SSA is used under different values of the time counter.

benefits outweigh these challenges, especially with the advancement in digital processing technologies, where intelligent approaches can be easily incorporated.

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