A 32-Channel Time-Multiplexed Artifact-Aware Neural Recording System

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***Abstract*—This paper presents a low-power, low-noise microsystem for the recording of neural local field potentials or intracranial electroencephalographic signals. It features 32 time-multiplexed channels at the electrode interface and offers the possibility to spatially delta encode data to take advantage of the large correlation of signals captured from nearby channels. The circuit also implements a mixed-signal voltage-triggered auto-ranging algorithm which allows to attenuate large interferers in digital domain while preserving neural information. This effectively increases the system dynamic range and avoids the onset of saturation. A prototype, fabricated in a standard 180 nm CMOS process, has been experimentally verified *in-vitro* with cellular cultures of primary cortical neurons from mice. The system shows an integrated input-referred noise in the 0.5–200 Hz band of 1.4 $\mu\mathrm{V_{rms}}$ for a spot noise of about 85 nV $/\sqrt{\mathrm{Hz}}$. The system draws 1.5 μW per channel from 1.2 V supply and obtains 71 dB + 26 dB dynamic range when the artifact-aware auto-ranging mechanism is enabled, without penalising other critical specifications such as crosstalk between channels or common-mode and power supply rejection ratios.**

***Index Terms*—Artifact-aware, auto-ranging, biomedical electronics, CMOS integrated circuits, correlated double sampling, ECoG, LFP, neural recording, neurophysiology, offset reduction loop, spatial delta encoding, system-on-chip, time multiplexing.**

I. Introduction

THE DESIGN of implanted closed-loop neural prostheses for Brain Machine Interfaces (BMIs) [1], [2] or for the treatment of brain disorders [3], [4] is genuinely compelled to reduce area and power consumptions to minimise the risk of damages to the tissue. However, the trend towards using high-channel count probes or 2D meshes with densely-spaced recording sites for accessing large neuronal populations [5]–[8] or the need for embedding more functional capabilities in brain implants [9], [10] make saving resources difficult. This is particularly challenging at the Analog Front-End (AFE) recording interface where low-noise, low-power performance typically demands for large silicon occupation.

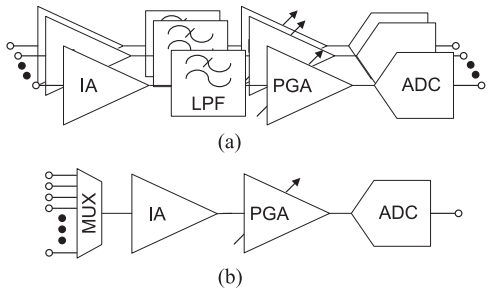

Fig. 1. (a) Conventional neural recording front-ends for multiple channels. (b) Time-multiplexed neural recording front-end for multiple channels.

A promising approach to cope with this problem relies upon trading-off area and operation frequency by using Time-Division Multiplexing (TDM) at the electrode interface. Conventionally there is a one-to-one correspondence between electrodes and AFEs, as shown in Fig. 1(a) [9]–[11]. The alternative is to share a single AFE between different electrodes at different time slots, while keeping the same throughput rate per channel, as shown in Fig. 1(b) [6], [12]–[16]. This approach clearly favours area reduction and essentially eliminates the mismatch problems of multi-channel topologies [17], thus paving the way to delta encode signals recorded from different sites. However, the need for high-bandwidth AFEs may lead to larger in-band noise levels due to aliasing [6], [12].

Another key issue in closed-loop neural prostheses is the implementation of strategies for counteracting the impact of large amplitude artifacts as may arise during electrical stimulation [18]–[20]. Artifacts may not only corrupt the captured neural signals but also lead to the saturation of the recording front-end, thus compromising the performance of the whole implant. Further, the amplitude of the artifacts increases with the proximity between the stimulation and the recording electrodes and, hence, the problem is more acute in dense multi-electrode arrays if both operations, stimulation and recording, are jointly implemented in the probe.

Recent techniques to overcome artifact interferences have been reported in [11], [14], [16], [21]–[24]. In some cases, the

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dynamic range is significantly extended to cope with the unwanted artifacts and avoid the onset of saturation [11], [22], [24]. In others, mechanisms are provided aiming to cancel artifacts. They typically involve the generation of templates which have to be regularly updated, the detection of such templates in the recorded signal, and the use of adaptive filters, e.g., Least Mean Square (LMS) filters, to reconstruct the neural signal [14], [16], [21]. This demands for computationally intensive solutions, which often have to be partially implemented off-chip [14], [16], [21], [23]. Additionally, the approach may suffer from long convergence time and may need prior knowledge of the artifact shape.

This paper addresses the above problems and presents a 32-channel low-noise, high dynamic range recording front-end, fabricated in a 180 nm standard CMOS technology, which mainly focuses on the recording of local field potentials (LFPs) or electrocorticographic (ECoG) signals. This work extends earlier contributions in [25] and [26] with new experimental verifications, including measurements in saline and *in vitro*, and additional theoretical analysis with emphasis in bandwidth and noise issues. Further, the new prototype herein presented integrates a modified version of the converter in [27] and a dedicated digital signal processor not included in [26]. The design follows a TDM recording strategy and uses two digital-feedback loops which provide robustness against large interferences with little impact on power consumption, area occupation or noise behavior. One loop implements a voltage-triggered auto-ranging algorithm which allows to extend the effective dynamic range of the AFE to 71 dB + 26 dB. The other is a DC servo loop for electrode offset cancelling which extends the AFE input range to $300\,\mathrm{mV_{pp}}$. Both loops include modifications with respect to the proposal in [26]. Design considerations to not sacrifice other specifications such as crosstalk between channels, CMRR or input impedance are also presented. Compared to previous TDM front-end proposals with which this work presents similarities (only two to our best of knowledge, [12], [14]–[16]), our circuit uses a closed-loop amplification and filtering approach instead of charge sampling techniques, it offers the possibility of applying both bipolar or monopolar sensing at the input multiplexer and it can delta encode neural signals between channels [28], [29] instead of tracking signal increments per channel. Additionally, our system offers two output modes (in one of them input signals are reconstructed including interferers, no matter their morphology or origin) and exploits the auto-ranging loop for handling differential-mode artifacts instead of adaptive filters [16].

The paper is organised as follows. Section II describes the proposed neural front-end topology and presents the different circuit elements of the design. Section III shows the sensing and coding techniques as well as the signal amplification and filtering stage used. It also discuses scalability issues taking into account noise, area, and power considerations. Section IV focuses on the digital processing section of the chip and explains the feedback loops implemented for artifact compression and DC suppression. Then, Section V presents experimental measurements, Section VI compares this work with prior art, and Section VII concludes the paper.

II. System Overview

Fig. 2 shows the block diagram of the proposed time-multiplexed neural recording system. The main core has been integrated in an Application Specific Integrated Circuit (ASIC) while some functions have been implemented in a microcontroller (μ-C, Rigado BMD-350).

After a switch matrix to multiplex M input neural signals, the ASIC comprises two cascaded fully-differential low-noise instrumentation amplifiers (IA_1 and IA_2) to sample, filter and amplify the signals captured by the electrodes. The multiplexer can be configured in two sensing modes, monopolar or bipolar, depending on whether signals are referred to a common reference or voltage differences between nearby electrodes are measured. Following amplification, a rail-to-rail Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) is used for taking signals into digital-domain. In this work, input signals (not just the ADC) are oversampled by an OSR factor to reduce the AFE Input-Referred Noise (IRN).

Two feedback loops from the ADC memory are combined in a digital adder to drive the input of the first instrumentation amplifier by means of two digital-to-analog converters (DAC), one per differential terminal of the AFE. One loop, denoted as ARL (for Auto-Ranging Loop), is used for the compression of large interferers, such as differential artifacts. The other feedback mechanism is a DC Servo-Loop (DSL) for input offset rejection [30]. This loop is preceded by a decimation stage to filter signals down to baseband. Similar to [16], the ASIC control unit can enable an off-line calibration process to obtain the ADC outputs for all possible DAC input codes.

The ASIC features two output modes. In Mode-1, the decimated signal is transmitted through an SPI port. If monopolar sensing is enabled at the input multiplexer, the system gives the option to transmit increments between consecutive recordings. The purpose is to explore the possibility to losslessly reduce the word length of neuronal data, taking advantage of the large spatial correlation observed in LFP/ECoG signals captured from nearby electrodes. In bipolar sensing, decimated signals are inherently delta compressed and there is no need for further processing. For both sensing methods in Mode-1, output words are 14-b long and the bandwidth of interest is $B_w \approx 200$ Hz. Accordingly, the TDM multiplexing rate, is set to $f_s = 2\,M \cdot OSR \cdot B_w$ to satisfy the Nyquist rate criterion. In this work $M = 32$, the oversampling factor is $OSR = 16$ and the multiplexing rate is about 192 kS/s.

In Mode-2, the output consists of two signals which are transferred through corresponding serial ports. One of the signals is the SAR ADC output (10-b) and the other is the ARL sequence (9-b). Both codes are combined in the μ-C to losslessly reconstruct the input signal, including artifact, with 14-b resolution. Mode-1 and Mode-2 use the same sampling rate f_s; however, the output rate in Mode-2 is $OSR\times$ larger, i.e., $\approx$6 kS/s, because there is no decimation. This rate is smaller than typically used in action potential recorders, but it still enables closed-loop BMI performance equivalent to the use of spike-detection threshold-crossing events [31], [32]. In this work, Mode-2 is essentially used to verifying Mode-1 outcomes; no BMI application is

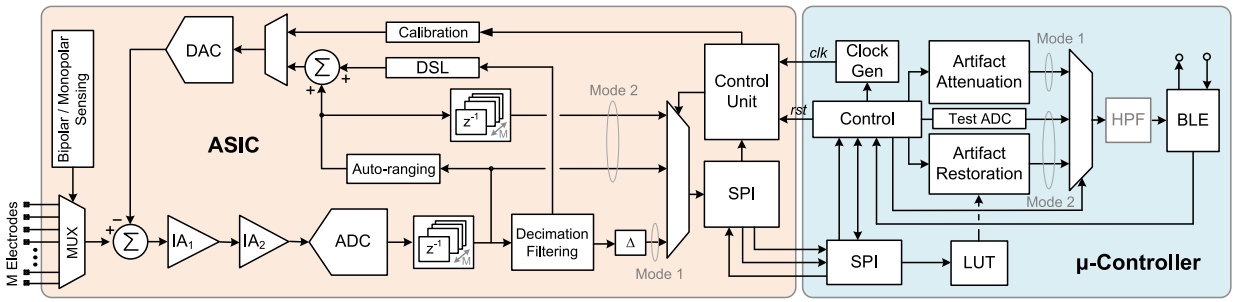

Fig. 2. Block diagram of the proposed neural recording system.

TABLE I
SUMMARY OF FREQUENCY PARAMETERS

Symbol	Description	Equivalent Value
f_m	Master clock frequency	2.5 MHz
f_s	Sampling frequency	$f_m/13 = 2\,M \cdot OSR \cdot B_w$
f_b	Amplifier Bandwidth	$> f_s$
f_c	Sampling frequency per channel	f_s/M
f_{IA}	CDS Bandwidth	$< f_s/2$

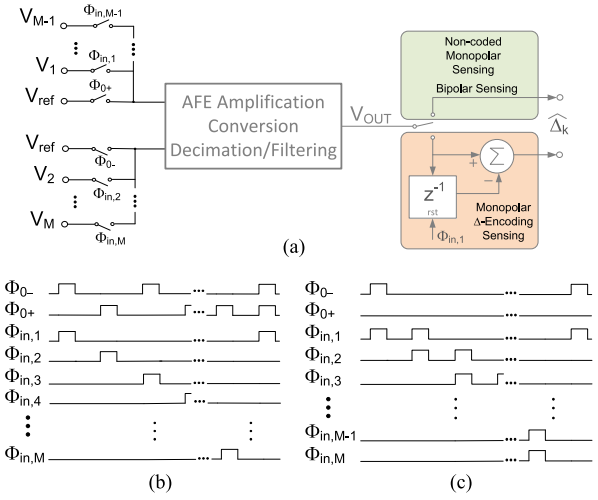

Fig. 3. (a) Input multiplexer and spatial delta coding generation. Timing diagram of the (b) monopolar and (c) bipolar sensing modes.

pursued. For easy reference, Table I summarizes the main system frequencies and their notations. All the time references are extracted from a master clock with frequency, $f_m = 2.5$ MHz.

III. ANALOG FRONT-END

A. Sensing and Coding

Fig. 3(a) shows the schematics of the multiplexer at the interface with the electrodes. It consists of two sets of $M/2+1$ switches each connected to one AFE terminal. The switches are CMOS transmission gates implemented with low leakage thick oxide transistors. Fig. 3(a) also shows the different coding options available after the decimation and filtering stage in the proposed prototype (block Δ in Fig. 2).

As mentioned, the ASIC offers two electrode sensing options, monopolar or bipolar, which differ on how switches are pairwise-combined. Let us denote by $V_{i,j}(k)$ the k-th sample of the voltage difference between the i-th and the j-th nodes, where $i = 1, \ldots, M$, and $k = 1, 2, 3\ldots$ is a time index. Further, let us represent by $\hat{s}$ the amplified, converted, decimated and filtered version of sample s. In the monopolar sensing mode, based on the timing diagram of Fig. 3(b), all the recording sites are referred to the reference electrode. If no delta encoding is selected, output samples are cyclically rendered according to

$$\widehat{\Delta_k} = (-1)^{i-1} \cdot \widehat{V_{i,ref}(k)} \tag{1}$$

where indexes i and k are linked by the expression

$$i = 1 + \mathrm{mod}(k-1, M) \tag{2}$$

Alternatively, a conventional delta encoder, formed by a register and an adder as shown in Fig. 3(a), can be enabled to spatially encode signals in digital domain (only available in Mode-1). In this case, the sequence of coded outputs, $\widehat{\Delta_k}$, is

$$\widehat{\Delta_k} = (-1)^{i-1} \cdot (\widehat{V_{i,ref}(k)} - \widehat{V_{i-1,ref}(k-1)}) \tag{3}$$

where indexes i and k are again related by (2) and it is assumed that $V_{0,ref} = 0$. Note that for $i = 1$, the register of the delta encoder in Fig. 3(a) is cleared and $\widehat{\Delta_k} = \widehat{V_{1,ref}(k)}$.

In the bipolar sensing mode, based on the timing diagram of Fig. 3(c), voltages differences from adjacent recording sites are subsequently amplified. This effectively implements the spatial delta encoding paradigm in analog domain (available both in Mode-1 and Mode-2). In this case the encoded signals are given by,

$$\widehat{\Delta_k} = (-1)^{i-1} \cdot \widehat{V_{i,\,i-1}(k)} \tag{4}$$

where (2) holds again and it is assumed that $V_{1,0}(k) = V_{1,ref}(k)$ for $i = 1$. In this case, there is no need for any extra digital processing and $\widehat{\Delta_k}$'s are readily available after decimation and filtering.

Signals (3) and (4) can be easily decoded at the external hub so they are referred to the common reference electrode. This can be done by reverting the coding operation as

$$V^R_{i,ref}(k) = \sum_{j=m}^{k} (-1)^{i-1} \cdot \widehat{\Delta_j} \tag{5}$$

where $V^R_{i,ref}(k)$ is the decoded signal, $m = 1 + M\lfloor k/M \rfloor$, $\lfloor \cdot \rfloor$ represents the floor function and index i is given by (2).

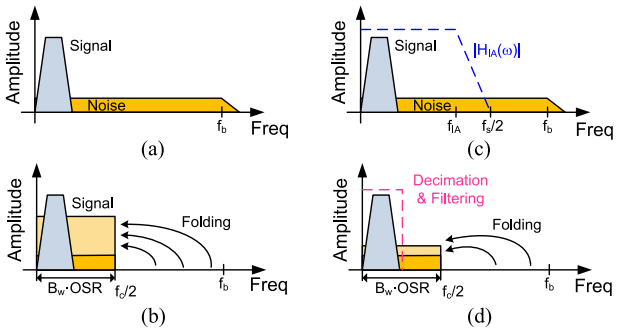

Fig. 4. (a-b) Noise folding problem in multiplexing circuits without input anti-aliasing filtering stage. After sampling, out-of-band noise components are folded back to baseband, increasing the noise floor. (c-d) By filtering during signal sampling, the folding problem can be alleviated. In both scenarios, it has been assumed that signal acquisition is oversampled so that out-of-band folded noise can be filtered out in digital domain.

B. Amplification and Filtering

In an M-channel multiplexed recording system, the sampling frequency f_s has to be $M\times$ faster than when a single channel is addressed to keep the same throughput rate per channel f_c, i.e., $f_s = M\, f_c$. This demands for an equivalent increase in the amplifier bandwidth f_b and, therefore, the AFE in-band noise raises due to spectral folding [6]. As the front-end amplifier typically dominates the noise behaviour of the whole system, noise folding due to multiplexing can indeed compromise the input-referred noise specifications in the bandwidth of interest. This is illustrated in Figs. 4(a-b) where an oversampling ratio OSR has been assumed. To circumvent this problem, a mechanism is needed for reducing the Noise Equivalent Bandwidth of the amplifier, so the IRN specifications are satisfied, while ensuring the appropriate settling accuracy within the time T_s allocated for channel sampling [12]. In this work, we address the problem through the combination of narrow-band Correlated Double-Sampling (CDS) amplification [33] (to reduce flicker noise and counteract the thermal noise excess due to multiplexing) and oversampling (to filter out part of the folded noise generated by the CDS technique itself). As shown in Table I, the sampling frequency per channel, including oversampling, is given by $f_c = 2 \cdot OSR \cdot B_w$.

Fig. 5(a) shows the schematics of the first CDS instrumentation amplifier, IA_1 in Fig. 2 [33]–[35], and the first row of Fig. 5(b) shows the associated timing diagram. In this diagram, numbers indicate the master clock periods, T_m, comprising each phase and arrows indicate charge transfers from one block to another in the main AFE signal path. The circuit operates at a sampling frequency f_s and the pulses in Figs. 3(b-c) are aligned to the clock phase Φ_1. The second amplifier, IA_2, uses the same circuit structure (excluding the positive feedback loop formed by capacitors C_{ib} and the two input DACs) but different phases – see the second row of Fig. 5(b). Given the small bandwidth of neural signals compared to f_s, no continuous-time anti-aliasing filter precedes the ADC.

The positive feedback loop in Fig. 5(a) (only for IA_1) is used for boosting the input impedance of the AFE [36]. In practice,

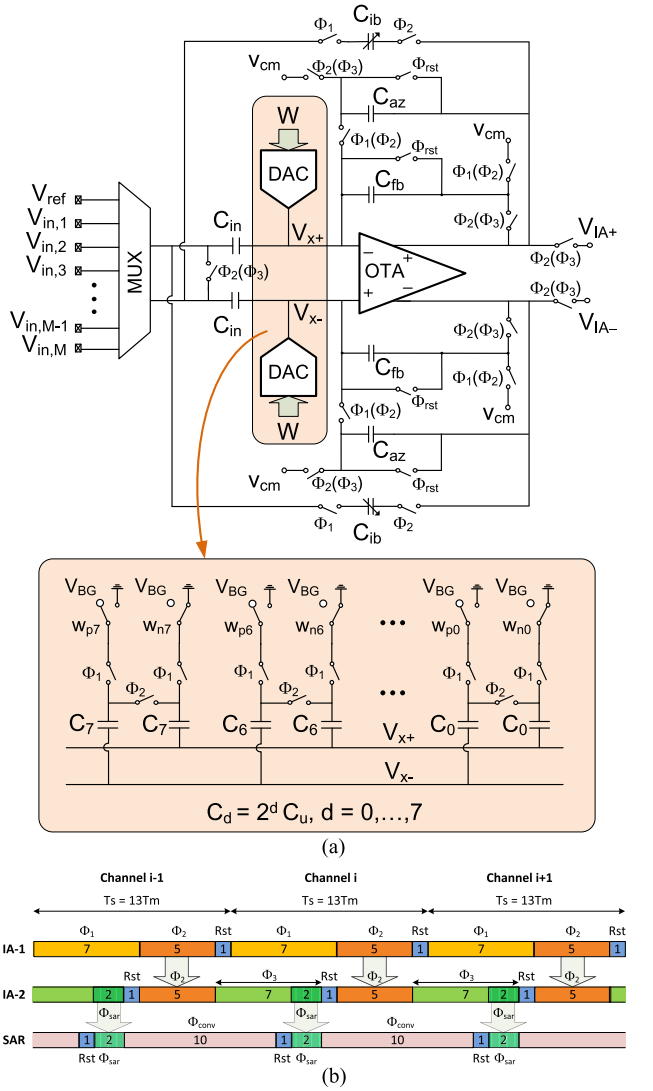

Fig. 5. (a) Instrumentation amplifier IA_1. The inset shows the schematic of the two 8-b DACs used for closing the feedback loops in Fig. 2. Amplifier IA_2 uses the same structure, excluding the input multiplexer, capacitors C_{ib} and DACs. Unparenthesised clock phases hold for IA_1, while parenthesized phases are for IA_2. (b) Timing diagram of the amplifiers and the SAR ADC. All these blocks use a sampling rate f_s.

the capacitors C_{ib} are implemented with 2-b capacitive banks to palliate variations due to mismatch and parasitics.

The DACs in IA_1 are used for closing the digital feedback loops in Fig. 2. Each DAC is implemented with an 8-b binary-weighted capacitive array. Only one DAC injects charge at a time. Accordingly, the programming word W, which combines the ARL and DSL correction codes W_A and W_{DSL}, respectively, consists of 9-b: one for selecting the active branch and the rest for specifying the magnitude (w_p or w_n). Unit capacitors have been sized for an input-referred voltage correction range of ± 150 mV at less than 0.56 mV step. The ratio between the total DAC capacitance per branch C_{DAC} and the input capacitance C_{in}, has been set below $1/4$ to reduce the thermal noise contribution of the DAC to the overall IRN [37]. The reference voltage of the DACs, V_{BG}, obtained from a bandgap circuit, amounts 0.6 V.

TABLE II
SUMMARY OF SAR ADC PERFORMANCE

Sampling rate (kS/s)	192.3
Supply Voltage (V)	1.2/0.6
Power Consumption (μW)	3.46
Area occupation (mm^2)	0.065
SNDR@Nyquist (dB)	58.2
FoM (fJ/conv-step)	27.1

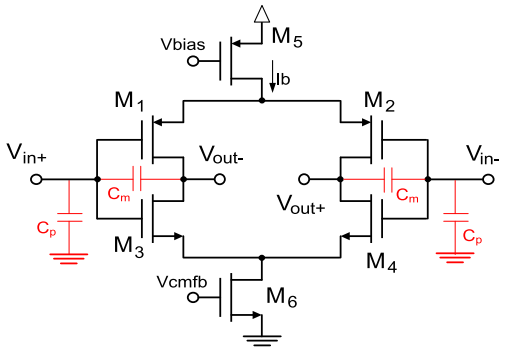

Fig. 6. Current-reuse OTA topology used in the instrumentation amplifiers.

In order to reduce the crosstalk between channels and offer a time-invariant input impedance, a short reset pulse Φ_{rst} after the amplification phases of IA_1 and IA_2 is used for clearing their respective feedback, C_{fb}, and the auto-zero, C_{az}, capacitors – see Fig. 5(b). According to simulations with an electrode-tissue model for a typical Pt electrode [38], the crosstalk decreases quite significantly from -27 dB to -85 dB through the reset of these capacitors. A similar resetting of the input capacitors, C_{in}, reduces crosstalk by 3 dB but at the cost of degrading linearity and noise and, hence, the option was discarded.

In this work, the ADC uses the fully-differential SAR topology in [27] with a rail-to-rail dynamic latched comparator [39] instead of an offset cancelling time-domain comparator. The sampling rate of the ADC both in Mode-1 and Mode-2 operation is f_s, and uses 13 cycles of the master clock with frequency f_m for completing each conversion: 2 cycles are used for signal acquisition, 10 cycles for data conversion and one cycle for discharging internal capacitors, as shown in the third row of Fig. 5(b). The ADC is powered with a 1.2 V supply, excepting the SAR logic which uses 0.6 V. Table II summarizes the performance of the converter.

Both IA_1 and IA_2 employ the same current-reuse topology for the OTAs, shown in Fig. 6. In both cases, input transistors are biased in weak-inversion, however, while in the first amplifier these transistors are large to reduce the flicker noise contribution of the OTA, they are significantly smaller in the second amplifier to reduce parasitics. The OTAs use switched-capacitor CMFB circuits, because of their high linearity and low power consumption. For both amplifiers, the OTA transconductance is large enough so the dynamic settling errors during their respective sampling and amplification phases are lower than 0.1% for 10-bit accuracy. Fig. 7 illustrates the settling behavior at the output of IA_2 during its amplification phase Φ_3. The time scale is expressed in units of the master clock period, T_m. Under large

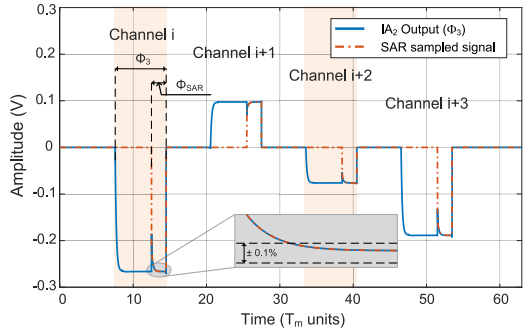

Fig. 7. Illustration of the output of IA_2 along with timing information. Time unit T_m is the period of the master clock. A similar settling behavior is also observed with IA_1, although with smaller voltage excursions.

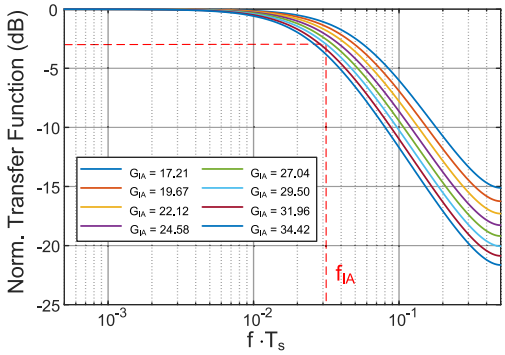

Fig. 8. Normalised transfer function of the CDS instrumentation amplifier for different gain settings. The IA_1 bandwidth is marked in red.

voltage excursions, the circuit is able to drive the SAR ADC within the tolerable accuracy margins, as shown in the inset.

Taking into account parasitics, finite gain and bandwidth effects, as well as the non-negligible gate-to-drain capacitances C_m of the OTA (see Fig. 6), the magnitude of the transfer function, $H_{IA}(\omega)$ for both amplifiers takes the form:

$$|H_{IA}(\omega)| = \sqrt{\frac{N_0^2 + N_1^2 + 2N_0N_1\cos(\omega T_s)}{D_0^2 + D_1^2\cos(\omega T_s) + D_2^2\cos(2\omega T_s)}} \qquad (6)$$

where parameters N_h and D_h, $h = 0, \ldots, 2$ can be expressed in terms of circuit parameters. Equation (6) is represented for different gain settings in Fig. 8. The plots, obtained for IA_1, are normalised with respect to the ideal dc gain, $G_{IA} = C_{in}/C_{fb}$. Only the input capacitance has been varied; the feedback capacitance has been kept fixed. For all the configurations, the circuit complies with the settling requirements of the ADC.

Fig. 8 shows that the amplifier bandwidth, f_{IA}, decreases as G_{IA} increases and it can be made more than one decade smaller than $f_s/2$. In this work, the dc gain of IA_1 has been chosen so that f_{IA} is close to f_c. The gain of IA_2, with much lower impact on noise performance, has been adjusted, taking into account aspects such as the minimum detectable signal or the input range of the AFE. The overall AFE dc gain is $G_{AFE} \approx 200$.

The output-referred noise spectral density of IA_1 (simulation and experimental results show that more than 80% of noise

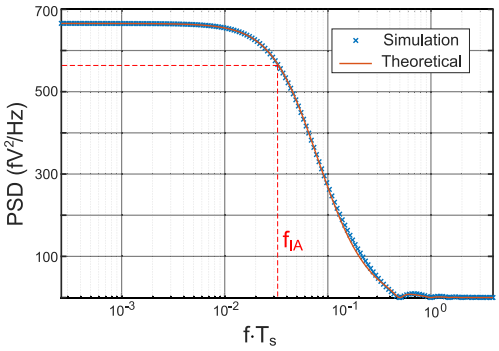

Fig. 9. Output noise spectral density comparison between simulation results and the proposed model.

comes from this stage), considering the white noise contribution of the OTA (this represents more than 94% of the total noise generated by IA_1), can be approximated as [40], [41]:

$$S_{IA}(\omega) = 4\,\mathrm{sinc}^2(\omega T_s/2) \cdot S_{CDS}(\omega) \tag{7}$$

where $\mathrm{sinc}(x) \equiv \sin(x)/x$ and $S_{CDS}(\omega)$ is a spectral density factor which depends on the particular CDS topology (see Appendix for calculation details). This expression takes into account the folded noise components inherent of CDS techniques. The noise folding factor $N_f \approx \pi f_b/f_s$, where f_b is the OTA bandwidth, is essentially defined by the requested settling accuracy. Equation (7) also considers the multiplexing range, M, through the sampling frequency f_s which is $M\times$ larger than the sampling rate per channel. Fig. 9 plots $S_{IA}(\omega)$ for IA_1 using both electrical simulations and (7). The discrepancy between the plots is lower than 2% in the range from 1 Hz to $4/T_s$, thus confirming the accuracy of the model. Note that the $4\,\mathrm{sinc}^2(\omega T_s/2)$ factor in (7), which accounts for the hold operation of the amplifier, provides additional anti-aliasing filtering. The side lobes of the noise spectral density are more than 2 orders of magnitude smaller than the spectral density in the passband. The noise equivalent bandwidth f_{NEB} is approximately given by $\pi f_{IA}/2$ (assuming a first-order roll-off model), and, hence, similar to the sampling frequency per channel, f_c. This allows attenuating the out-of-band noise folded components arising from time multiplexing as illustrated in Figs. 4(c-d). Hence, the approach effectively reduces the integrated input-referred noise compared to the case in Fig. 4(b), while power consumption remains at approximately the same level [12]. From (7) and using the noise bandwidth concept, the output-referred noise spectral density due to IA_1 in Mode-1 before the decimation and filtering stage takes the form [42]:

$$S_{o,IA}(\omega) \approx M\, S_{IA}(\omega)\, \frac{2\, f_{NEB}}{f_s} \left(1 + \frac{C_{DAC}}{C_{in}}\right)^2 \tag{8}$$

where factor M accounts for the noise folding due to multiplexing. Equation (8) also considers the noise contribution of feedback DACs. After decimation and filtering to the bandwidth of interest, B_w (approximately 200 Hz in Mode-1), the total input-referred noise power is given by

$$\overline{v_{n,IA}^2} \approx \frac{S_{IA}(0)}{G_{IA}^2}\, f_{NEB} \left(1 + \frac{C_{DAC}}{C_{in}}\right)^2 \frac{1}{OSR} \tag{9}$$

Note that the in-band noise power is actually divided by the oversampling ratio OSR, thus palliating the noise folding due to the CDS operation and the signal multiplexing. Furthermore, assuming the same noise folding factor, the OTA bandwidth increases with the oversampling ratio, thus decreasing the OTA noise floor and, hence, the overall folded noise compared to a non-oversampled system. This is at the cost of additional power and area consumption; however these increments are averaged by the number of channels multiplexed, as will be shown next.

C. Scalability

The scalability of the proposed analog front-end in terms of M (in Mode-1) and f_c (in Mode-2) has been explored with electrical simulations. In both cases, power and area consumption, as well as, in-band IRN have been the estimated performance metrics. Both AFE and electrode noise contributions (this latter assuming the microwire and silicon array *in vivo* models reported in [12]) have been considered in the analysis. Electrode noise source has not been band-limited in any way along the experiments. In all the evaluated configurations, the OTA structure of Fig. 6, the capacitances in Fig. 5, the oversampling ratio OSR, and the supply voltage have been preserved as in the current design; however, OTAs have been resized to guarantee operation in weak inversion and correct settling behavior. This latter demands that $2\pi f_b = g_m/C_{eq,i} > -\ln(\epsilon_{sett})/(T_s/2)$, where g_m is the OTA transconductance, $C_{eq,i}$ is the equivalent load capacitance during the i-th clock phase ($i = 1, 2$) – see Appendix for expressions –, and ϵ_{sett} is the tolerable dynamic settling error (0.1% for 10-bit accuracy). It has also been assumed that the power consumption of the ADC scales linearly with the sampling frequency while preserving its area occupation.

Fig. 10 illustrates the impact of the number of multiplexed channels (from 16 to 128), assuming the same signal bandwidth of interest as in the presented design. Fig. 10(a) shows that the power consumption per channel remains fairly constant with M. This is because the power consumption of the OTAs in IA_1 and IA_2 have to increase with the number of multiplexed channels to meet bandwidth requirements. Fig. 10(b) shows that the electronic and electrode IRNs slightly increase with the number of multiplexed sites. As the transconductance of the OTAs has to increase with M, the intrinsic in-band thermal noise floor of the IAs decreases, thus, partially compensating for the noise folding due to channel multiplexing. Note that the in-band input-referred noise contribution of the electrodes for the presented prototype ($M = 32$) is about 3 $\mu\mathrm{V_{rms}}$ in Mode-1 for both the microwire and the silicon array models. This value considers noise folding issues of out-of-band components as well as the increase of the noise equivalent bandwidth with the number of channels. Finally, Fig. 10(c) shows that, although the dimensions of the OTAs have to scale with their power consumption to keep input transistors in weak inversion, the total area occupation per channel of the analog circuitry (only 10 % of the total active area)

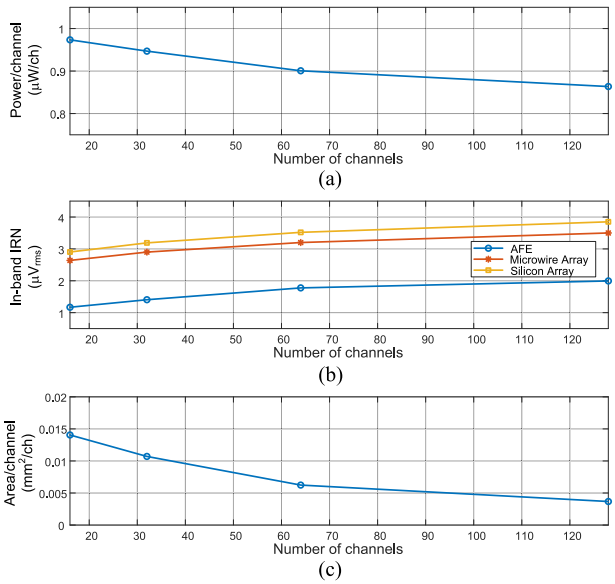

Fig. 10. System scalability in terms of the number of multiplexed channels in Mode-1 (bandwidth of interest of 200 Hz): (a) Power consumption per channel; (b) in-band IRN; and (c) area per channel occupation (only analog circuitry).

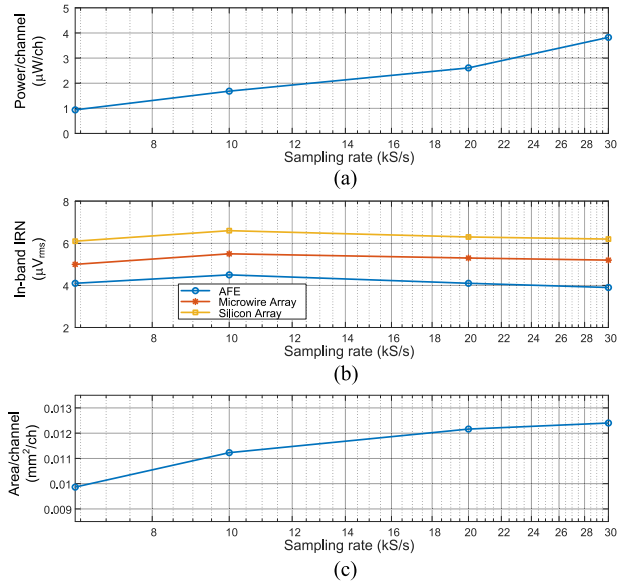

Fig. 11. System scalability in terms of bandwidth in Mode-2 (bandwidth of interest of 0.5–5 kHz), excepting when $f_c = 6$ kS/s for which the upper limit is 3 kHz: (a) AFE power consumption per channel; (b) in-band IRN; and (c) area per channel occupation (only analog circuitry).

actually decreases. All the designs represented in Fig. 10 meet the requested settling accuracy, however, the impact of OTA parasitics becomes more and more noticeable for multiplexing factors larger than $M = 96$. To reduce the system transfer function variability caused by these parasitics, other design aspects than the size of the transconductors should be modified as well, for instance, input and feedback capacitors, gain distribution between IA_1 and IA_2 or even the OTA structure itself, among others. In an electrical simulation of a non-optimized design in which the weak inversion operation constraint has been relaxed to make the system less sensitive to parasitics, it was found that the in-band system IRN only increases by 0.2 $\mu\mathrm{V}_{\mathrm{rms}}$ for M $= 128$ compared to the results in Fig. 10(b). Hence, similar to the windowed integration sampling approach [12], the proposed technique does not result in prohibitively large integrated noise when the multiplexing factor increases.

Fig. 11 illustrates the impact of increasing the sampling rate per channel in Mode-2 from 6 kS/s, the nominal value of the presented design, to 30 kS/s as typically used for the recording of action potentials [43]. The number of multiplexed channels is $M = 32$. In Mode-2, the output signal is not decimated by the oversampling ratio and thus the in-band noise worsens compared to Mode-1 operation. Fig. 11 assumes, as in [13], that the AFE and the electrode noise components are integrated in the 500 Hz–5 kHz band to estimate the noise expected after spike filtering. In the nominal case of $f_c = 6$ kS/s, the band is defined between 500 Hz and 3 kHz. As expected, Fig. 11(a) and (c) show that the power consumption and the area occupation per channel increase with the sampling rate. However, increasing the recording bandwidth involves increasing the OTAs bandwidths which, in turn, decreases the noise thermal floor and, thus the aliased noise due to multiplexing. Accordingly, as shown in Fig. 11(b), the AFE in-band IRN slightly decreases with the sampling rate. A similar decrease with f_c is also observed with the electrode noise, being the IRN of the silicon array about 1 $\mu\mathrm{V}_{\mathrm{rms}}$ larger than with microwires. Both for the AFE and the electrodes, the IRN has been estimated by referring back the digital system output to the input and the band of interest has been implemented via digital post-filtering. The slight decrease of IRN for sampling frequencies per channel above 20kS/s is explained by the smaller f_{IA}/f_c ratio due to the large parasitics after OTAs resizing. Similar as for Fig. 10, the system AFE should be redesigned for large rates to reduce the impact of parasitics. Following the same approach as for Fig. 10, it is shown that the IRN slightly increases although with values similar to those represented in Fig. 11(b).

IV. Digital Processing

The samples converted by the SAR ADC are demultiplexed in digital domain by cyclically filling a 32-location memory block using a 5-b counter for address selection. This effectively decreases the sampling rate per channel to f_c. As shown in Fig. 2, the stored codes, V_{ADC}, are then serially transferred to either the auto-ranging block or the DC servo-loop, this latter via a decimation and filtering circuit which is implemented by a 2^{nd}-order Cascaded Integrator-Comb filter (see Fig. 12).

A. DC Servo Loop

The purpose of the DSL is twofold: (i) to limit the offset at the input of the front-end IA and (ii) to place a high-pass pole in the AFE transfer function. The proposed architecture is shown in Fig. 13 and consists of two main elements; a digital integrator and a binary search algorithm block, both operating serially over the 32 multiplexed channels. The former has been

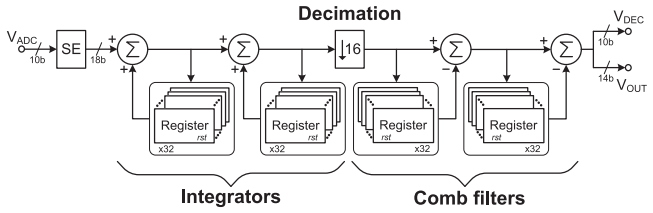

Fig. 12. Block diagram of 2^{nd}-Order CIC filter with decimation.

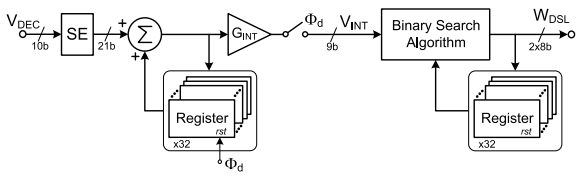

Fig. 13. Block diagram of the Binary Search DC Servo Loop.

preferred for filtering instead of high-order FIR/IIR structures as they require larger area occupation and may even lead to stability problems [44]. Similar to [12], a binary search block has been chosen for driving the DACs instead of $\Sigma\Delta$ modulators [30], [45]. Because of the TDM operation, such modulators would require large oversampling frequencies and/or high-order topologies, which would demand large power consumption and area occupation. In the proposed approach, the DSL output code is only updated when necessary (for instance, if offset drifts are detected), avoiding the onset of potential oscillations at the AFE input.

The gain factor, G_{INT}, of the integrator has been chosen as the largest integer power of 2 satisfying [44]

$$f_{hp} \leq \frac{B_w}{\pi} \ln\left(\frac{1}{1 - R_C \cdot G_{DC} \cdot G_{INT}}\right) \tag{10}$$

where f_{hp} is the intended frequency for the high pass pole of the AFE transfer function (in the proposed design $f_{hp} = 0.5$ Hz), G_{DC} is the DC gain of the AFE feedforward path and R_C is the ratio between the total DAC capacitance, i.e., $C_{tot} = C_u(2^8 - 1)$, and the input capacitor, C_{in}. In this design, G_{INT} must be at least 1/6000 so it has been rounded off to $1/2^{13}$ for easy implementation through bit shifting.

The integrator accumulates the V_{DEC} values (extended to 21-b to avoid overflows) provided by the decimation and filtering stage. Every $T_d = 2^9/B_w$ period (aprox. 3 seconds long) at instances of pulses Φ_d, the output of the integrator, V_{INT}, is transferred to the binary search block and then it is initialized to 0 to start a new count.

Either at start up or on-demand through a reset operation, the binary search block solves the binary words of the input DACs, W_{DSL}, sequentially from MSB to LSB, based on the sign of the V_{INT} values provided by the integrator. During the process, the auto-ranging block is disabled so it does not interfere in the binary search. Once the search is completed, the block verifies that the following V_{INT} instances satisfy that $|V_{INT}| < V_{BS}$, where V_{BS} is a threshold value corresponding to the maximum tolerable offset at the AFE input. In this design, $V_{BS} = V_{LUT}(2_{10})$, i.e., the ADC code stored in the LUT after calibration corresponding to 2 DAC LSBs. If the condition is met, W_{DSL} preserves its previous values, otherwise, it is incremented or decremented by 1 DAC LSB to compensate for potential DC drifts as large as 0.4 mV/s (this is 25% larger than the drift rates experimentally measured in [13]). This mechanism provides dc baseline stabilization.

B. Auto-Ranging Loop

The purpose of the ARL is to make the recording system tolerant to undesired high amplitude interferers or artifacts [25]. More specifically, the feedback loop avoids the onset of saturation in the AFE main signal path whenever the input signal exhibit variations below 40 V/s and, in case of faster transitions, it provides mechanisms for quick recovery into non-saturated system operation. This is particularly relevant in monopolar sensing mode where signals are acquired with respect to a common reference and may exhibit larger voltage swings than in bipolar mode.

The ARL operation is triggered when the input neural signal, contaminated by the interferer, exceeds the threshold voltages, $\pm V_{th}$, beyond the useful signal range. In this work, V_{th} amounts 2.5 mV_p and, hence, much larger than the peak amplitude of LFP/ECoG signals which is typically below 1 mV_p [30]. If the input signal surpasses these limits, the ARL block generates voltage increments which are added or subtracted at the AFE input to take the signal back to the $\pm V_{th}$ range. Similar auto-ranging procedures were proposed in [46], [47]. Along this operation, no attempt is made to distinguish between neural signals and interferers, as the ARL block does not rely on the use of complex filtering stages or template-based mechanisms for artifact detection and suppression [15].

The block diagram of the ARL circuit is shown in Fig. 15. First, a dead zone operator with bounds at $\pm V_{th}$ is applied in the incoming V_{ADC} signal to obtain

$$V_Z(l) = \begin{cases} V_{ADC}(l) - V_{th} & , V_{ADC}(l) > V_{th} \\ 0 & , |V_{ADC}(l)| \leq V_{th} \\ V_{ADC}(l) + V_{th} & , V_{ADC}(l) < -V_{th} \end{cases} \tag{11}$$

where l is a time index at a clock rate f_c. Any $V_Z(l)$ outside the dead zone is deemed to be affected by a high amplitude interferer. Then, the auto-ranging block generates the correction code

$$W_A(l) = \begin{cases} W_A(l-1) - \alpha \cdot V_Z(l) & , V_Z(l) \neq 0 \\ W_C(l-1) & , V_Z(l) = 0 \end{cases} \tag{12}$$

which is fed back to the AFE input (see Fig. 2).

If $|V_{ADC}(l)| > V_{th}$, the correction code $W_A(l)$ aims to take the next V_{DAC} instance back, or at least closer, to the dead zone. No overflow is permitted, i.e., the magnitude of $W_A(l)$ is limited by an all-ones word. The scaling factor α is nominally given by the voltage gain from the DAC input to the ADC output as,

$$\alpha = \frac{V_{BG}}{V_{DD}} \frac{2}{R_C \cdot G_{DC}} \tag{13}$$

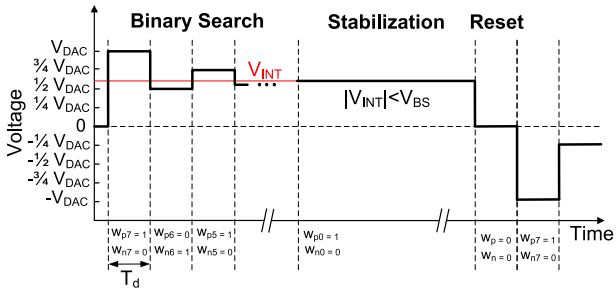

Fig. 14. Illustration of the different operation modes of the binary Search block.

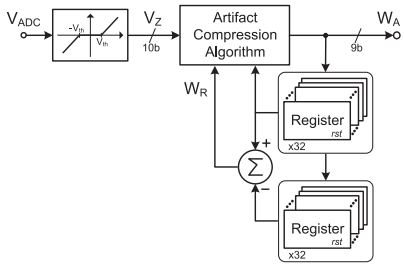

Fig. 15. Block diagram of the auto-ranging circuit.

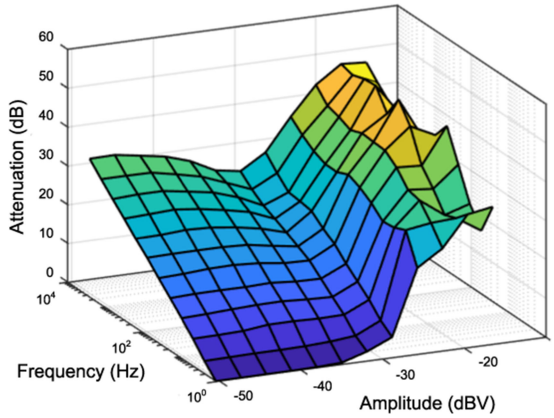

Fig. 16. Attenuation of sinusoidal artifact versus tone frequency.

where the factor 2 accounts for the 1-b difference between the DAC and ADC resolutions. In practice, α has been rounded to the nearest power of 2 so scaling can be simply implemented through bit shifting.

If $|V_{ADC}(l)| \leq V_{th}$, two cases can be distinguished; either there is no artifact or an artifact is ongoing but V_{ADC} is comprised within the dead zone. Accordingly, variable W_C in (12) is ddfined as,

$$W_C(l) = \begin{cases} 0 & ,|W_R(l)| \leq W_{BS} \\ W_A(l) & ,|W_R(l)| > W_{BS} \end{cases} \tag{14}$$

where W_{BS} amounts 2 DAC LSBs and the control variable $W_R(l)$ to decide between both states is simply given by the W_A increment, $W_R(l) = W_A(l) - W_A(l-1)$. From (14), if the accumulated value of $W_R(l)$ remains below a given tolerable offset deviation W_{BS}, it means that the artifact has concluded and $W_C(l) = 0$. Otherwise, $W_C(l)$ takes on the current correction code $W_A(l)$. This is done to avoid that a potentially large residual offset is held at the AFE input. In Fig. 15, the control variable W_R is serially calculated per channel by taking the difference between corresponding positions of two daisy-chain memories, one for $W_A(l)$ and the other for $W_A(l-1)$.

The correction codes W_A are transferred to the AFE DACs at a rate f_s to voltage shift input samples and compress, within the dead zone limits, the high-amplitude input signal formed by the superposition of the neural record and the interferer (no matter its morphology or origin). These auto-ranged input samples pass through the AFE direct signal path to obtain the system outputs. In Mode-1 operation, the neural information in the band of interest can be recovered after decimation and filtering, although contaminated by the filtered residues of the interference and the ARL voltage compensation. These residues are due to the limited quantization of the DAC and, in sum, account for the finite attenuation of the artifact. Such attenuation depends on the amplitude and frequency content of the interference. In both cases, the larger the values, the higher the attenuation because the larger are the differences between the neural signal of interest and the artifact. This is illustrated in the 3D plot of Fig. 16 which shows the achievable attenuation versus the frequency and amplitude of the interference when the system is configured in monopolar sensing mode with no delta encoding. In this plot, input signals are formed by the superposition of two tones: a 2 $\mathrm{mV_{pp}}$ tone at 30 Hz emulating useful neural signal and a variable tone, representing the artifact, with amplitude larger than 3 $\mathrm{mV_{pp}}$ (for triggering the auto-ranging mechanism) and frequency lower than half the sampling rate per channel, f_c. Note that the attenuation is smaller in the baseband and grows significantly for larger frequencies, particularly for high amplitude interferers. Larger attenuations could be accomplished by narrowing the dead zone, however, this is at the expense of increasing the activity of the auto-ranging loop and, therefore, its power consumption. Similarly, the attenuation could be improved for low frequency interferers by increasing the scaling factor α; however, this increases the chance for saturation at higher frequencies. For all the artifact configurations in Fig. 16, the tone at 30 Hz is recovered with eventual artifact-induced perturbations which, in any case, do not take the output signal out of the threshold limits. This will be illustrated in Section V.

In Mode-2, input signals are fully reconstructed, including artifacts, by reverting in digital domain the correction codes W_A previously injected at the AFE input. To this end, the V_{ADC} values corresponding to each possible W_A code have to be determined, taking into account not only the DAC nonidealities (mainly due to capacitor mismtach) but also any deviation in the AFE signal path. This vector mapping is obtained through an off-line calibration process in which the DAC is externally driven by a ramp sequence sweeping all W_A values. The process does not modify any circuit in the AFE nor use any extra technique; it just stores in a 9×10 Look-Up Table (LUT) the ADC-converted versions of the referred deviations. Based on these values, the losslessly restoration of the input voltage at instant l, $V_R(l)$,

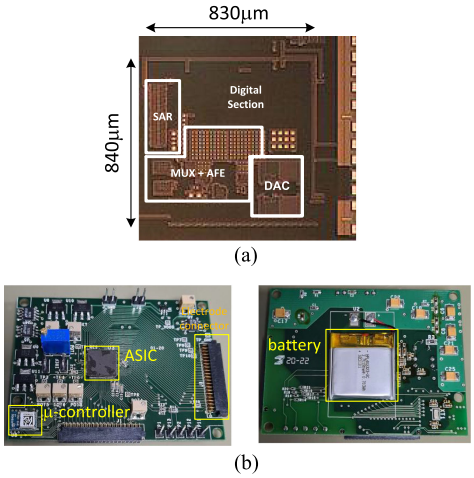

Fig. 17. (a) Die photograph of the ASIC prototype. (b) PCB for the testbench.

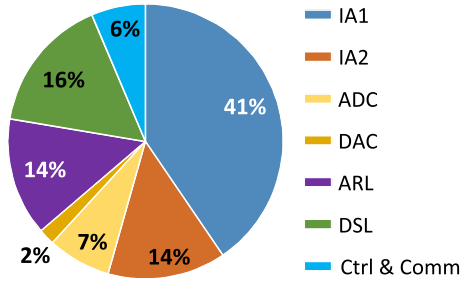

Fig. 18. System's power budget.

including uncompressed artifacts, can straightforwardly be obtained as,

$$V_R(l) = V_{ADC}(l) + V_{LUT}[W_A(l-1)] \qquad (15)$$

where the last term represents the voltage stored in the LUT for the correction code W_A.

V. Experimental Results

Fig. 17(a) shows a die photograph of the ASIC, fabricated in a standard 180 nm CMOS process. Its total active area is 0.70 mm^2. Fig. 17(b) shows both sides of the test PCB. The ASIC, together with the μ-C and the electrode connector, is placed at the top (picture on the left), while a battery is located at the bottom (picture on the right). The power supply of the ASIC, provided by a voltage regulator connected to the battery, is 1.2 V. In Mode-1, the ASIC consumes 48 μ W so the power consumption per channel is 1.5 μW/ch. The power budget, dominated by the first IA, is illustrated in the pie chart of Fig. 18. In Mode-2 for artifact restoration, the power consumption raises to 82 μW due to the increased data transfer rate to the μ-C.

Figs. 19 –21 show measurements for single input channel characterization. Unless otherwise stated, the ASIC was configured in Mode-1, using monopolar sensing mode without delta encoding and the output was taken directly from the decimation stage with no extra processing. Channel #1 was indistinctly

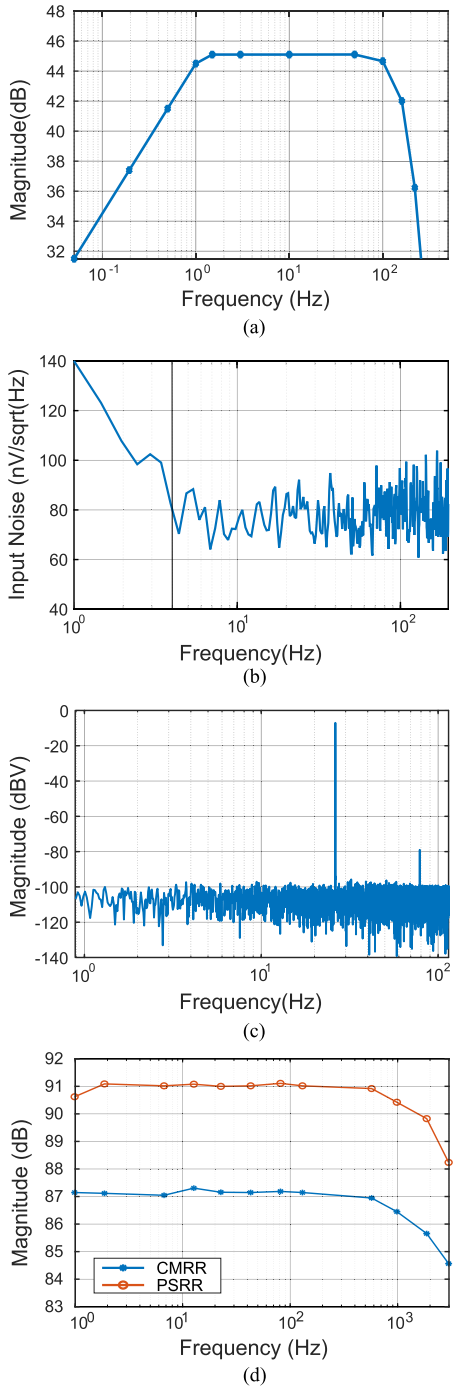

Fig. 19. (a) Measured AFE transfer function. (b) Input referred noise of the AFE. (c) Output spectrum of the AFE with input tone of 5 mV$_{\rm pp}$ at 27 Hz. (d) CMRR and PSRR.

taken for analysis – no meaningful differences were observed for the other channels. In all cases, the reference was connected to ground.

Fig. 19(a) shows the transfer function of the AFE, obtained by applying input tones of 1 mV$_{\rm pp}$ amplitude at different frequencies (solid dots in the figure). The bandpass characteristic is bounded by the 0.5 Hz one-pole roll-off due to the DSL integrator and the 200 Hz cut-off frequency of the CIC filter

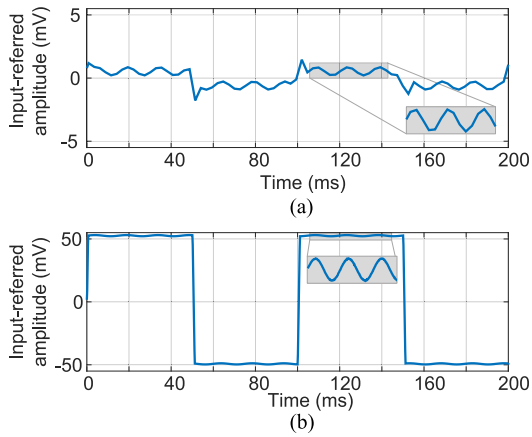

Fig. 20. Measured transient response to large input signal (a) after filtering and decimation (Mode-1), (b) after signal reconstruction (Mode-2).

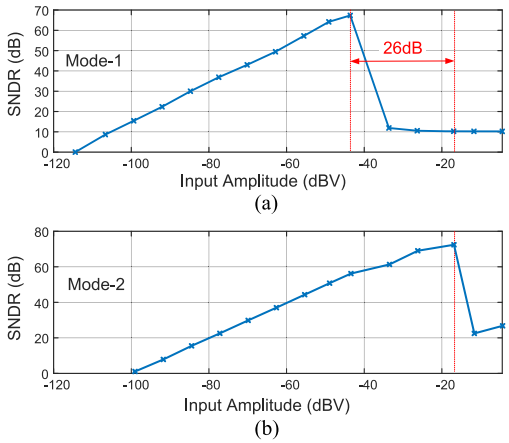

Fig. 21. SNDR versus input amplitude for (a) Mode-1 and (b) Mode-2.

at the decimation stage. The gain in the passband is 45 dB. The input referred noise of the front-end is illustrated in Fig. 19(b). It was measured by shorting channel #1 and the reference and referring the decimated codes back to the AFE input. The noise floor in the passband is 85 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ average for a total in-band rms input-referred noise of 1.4 $\mu\mathrm{V_{rms}}$. This includes the kT/C noise from the input switches which contribute less than 0.2 $\mu\mathrm{V_{rms}}$ to the total IRN, regardless of the DAC settings. The noise generated by the DAC voltage reference is negligible compared to the DAC switching noise. Taking into account the $1/f^2$ spectral content of LFP and ECoG signals [48] and the fact that power peaks are typically observed in the alpha and beta frequency bands [49], [50], the linearity of the AFE was evaluated in these bands. Fig. 19(c) shows the measured output referred spectrum for a 5 $\mathrm{mV_{pp}}$, 27 Hz tone in beta band. It shows a Total Harmonic Distortion (THD) of 75 dB. Fig. 19(d) shows the experimental measurements of the Common-Mode Rejection Ratio (CMRR) and the Power Supply Rejection Ratio (PSRR). In this case, measurements were taken from the output of the ADC (Mode-2), without decimation and filtering. In the CMRR case, a set of 5 $\mathrm{mV_{pp}}$ tones with a common mode of 200 mV was applied to the input and reference electrodes at the same time. As shown, the CMRR amounts 87 dB in the passband. Measurements also demonstrate a common-mode input range as large as 600 $\mathrm{mV_{pp}}$. For PSRR measurement, the regulated power suply was replaced by a 20 $\mathrm{mV_{pp}}$ tone superposed to V_{DD}. Approximately a PSRR of 91 dB is obtained.

The equivalent input impedance, Z_{in}, of channel #1 was measured w/ and w/out multiplexing using an input signal of 1 mV_{pp} at 100 Hz. Before multiplexing, Z_{in} was obtained for all the possible settings of the capacitive bank, C_{ib}, in the Impedance Boosting Loop (IBL) around amplifier IA_1 (see Fig. 5). The measured values were: 41-, 71-, 104- and 64- MΩ. The system was then operated in TDM with the highest Z_{in} configuration to evaluate the input impedance of channel #1 again. It was observed that Z_{in} slightly decreased to 100 MΩ. This decrease is attributed to the leakage currents of the switches in OFF state. According to simulations, the input impedance without IBL is only 800 kΩ, so there is about 100 × improvement in Z_{in} when IBL is used.

To illustrate the auto-ranging block operation a 67 Hz, 1 $\mathrm{mV_{pp}}$ input tone was superposed to a large 100 $\mathrm{mV_{pp}}$ pulse train [46]. The output signals obtained by the recording system in both operation modes (in two independent tests) are shown in Fig. 20. In Mode-1, Fig. 20(a) shows that, after a short transient, the filtered and decimated output wave tracks the full-swing signal excursions without saturation. In Mode-2, Fig. 20(b) shows the reconstructed output signal after the deterministic decoding of the ARL word. In this case, no transient is observed and the time resolution is larger; however, this is at the expense of a higher noise level because the ARL output is not decimated.

Fig. 21 shows the AFE Signal-to-Noise and Distortion Ratio (SNDR) as a function of the in-band input signal amplitude for both Mode-1 and Mode-2. In Mode-1, the dynamic range amounts 71 dB. In this design, the quantization noise of the ADC after decimation falls well below the noise floor of the AFE and, accordingly, the lower bound in Fig. 21(a) is essentially due to the input-referred noise. The upper bound is at approximately −43 dBV, however, interferences as large as -17 dBV can be tolerated without saturation thanks to the auto-ranging block. In that sense, the input dynamic range extends in practice to 71 dB + 26 dB (with ARL). In Mode-2, the dynamic range amounts 83 dB based on the lossless reconstruction of input signals. However, in this case, the input referred noise raises to 4.8 $\mu\mathrm{V_{rms}}$.

The experimental measurements in Figs. 22–23 were carried out by reproducing with 2 function generators (Tek AFG3102) 4 pre-recorded 100 s long *in-vivo* LFP segments repeated 8 times in the same order along the 32 input channels. To this end, a small auxiliary board for connections was implemented. These signals were previously recorded from a Long-Evans rat model using 4 adjacent channels of a Utah array (Blackrock Microsystems, LLC) [43]. From top to bottom, Fig. 22 shows (a) the input signals applied to channels #1 to #4, (b) the input-referred output signals obtained in Mode-1 using bipolar sensing, (c) the decoded signals calculated with (5) using the ASIC outputs, (d) the decoded signals when the residual offsets are filtered out by the high-pass filter in the micro-controller and (e) the differences between the signals shown in (a) and

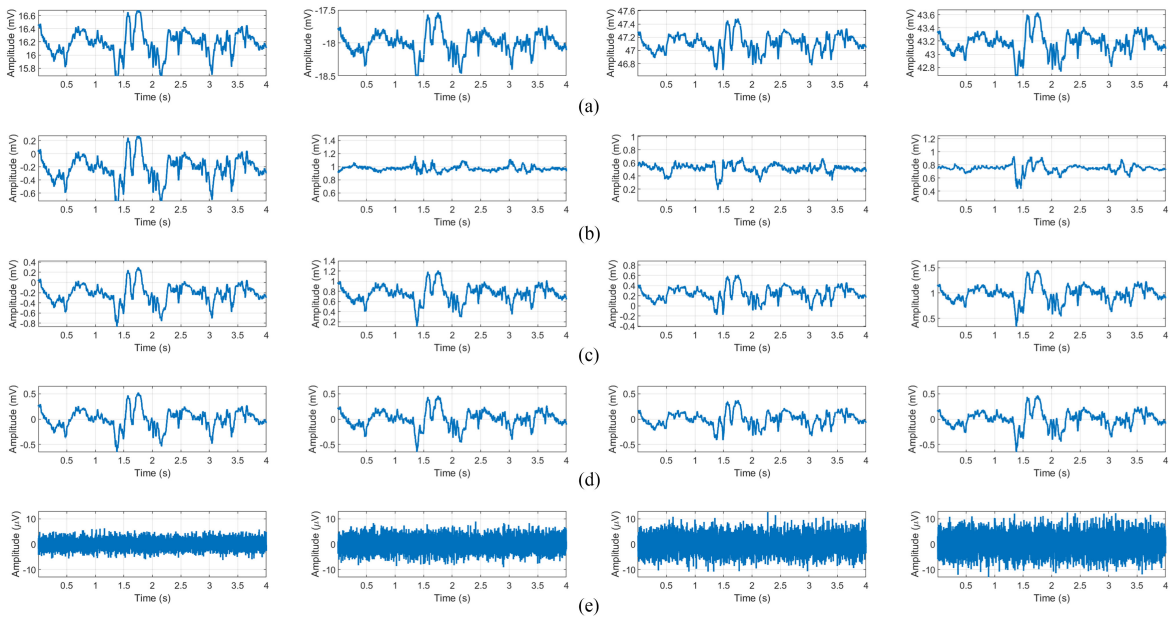

Fig. 22. Signal set from channels #1-#4 to illustrate the spatial delta encoding techniques implemented in the ASIC: (a) Input signals, (b) input-referred signals using bipolar sensing mode, (c) input-referred signals after decoding, (d) same with residual offsets removed with the HPF in the micro-controller and (e) Input-referred decoding error.

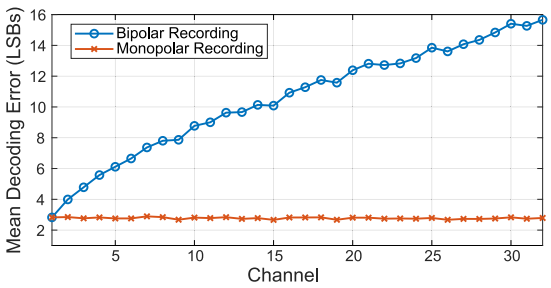

Fig. 23. Average decoding output error obtained by the monopolar and bipolar spatial delta-encoding in terms of the channel index i.

(d), after removing the intentional offsets superposed in (a). Note that the input signals exhibit quite different DC offsets to illustrate the correct settling behavior of the AFE and the effectiveness of the DC servo loop. Comparing Fig. 22(a) and (b), it can be also observed that the amplitude range of spatial delta encoded signals, inherently available in bipolar sensing mode, is smaller than the input channel voltages, excepting for channel #1 which is measured against the reference electrode according to (4). Indeed, it has been measured that the effective output code range is compressed by about 60% average with spatial delta encoding. Similar results were also obtained with delta-encoded monopolar signals.

It is worth observing from Fig. 22(e) that decoding errors in bipolar sensing mode increase with the channel order. This is due to the cumulative nature of (5). In fact, it can be shown that the output-referred noise power, $\overline{v_{no,k}^2}$, of the k-th reconstructed signal can be approximated as,

$$\overline{v_{no,k}^2} \approx \frac{i}{OSR}\left[\frac{h^2}{12} + G_{AFE}^2 \cdot \overline{v_{n,\Delta}^2}\right] \tag{16}$$

where i is given by (2), h represents the ADC resolution after decimation and filtering and $\overline{v_{n,\Delta}^2}$ is the in-band input-referred noise variance of the Δ_k increments in (4) before conversion. Hence, the output rms noise increases with the square-root of index i. This problem observed with bipolar sensing is not present in delta-encoded monopolar signals because both coding and decoding are implemented in digital domain [see (3) and (5)] and errors cancel out along signal decoding. This is illustrated in Fig. 23 which compares the experimental output signals generated by the encoded monopolar and bipolar techniques after decoding. In both cases, the reconstructed signals are compared to the input signals and the mean absolute value deviations are quantified in effective LSBs. Measurements have been taken over the 32 available channels. Clearly, with monopolar signals, coding errors remain independent of the channel order. This suggests that bipolar recordings can relax specifications on AFE dynamic range, DC offset rejection or CMRR but they should be periodically refreshed to avoid that decoding errors increase indefinitely.

The following experiments were made with recording electrodes immersed in a phosphate buffered saline (PBS) solution. Electrical signals, either in current or voltage form, were applied to the solution through a platinum electrode and recordings were captured in monopolar, non-coded configuration. Fig. 24 shows the experimental setup.

The crosstalk between channels was evaluated in saline by applying a set of 5 $\mathrm{mV_{pp}}$ tones to channel #1 (aggresor) and measuring the impact on the other channel (victims) which were referenced to ground. These measurements showed that interferences remain below -62 dB for all channels across the signal band. However, this result cannot be attributed to the ASIC because same results were measured from the unmounted PCB alone. The capacitive couplings between the long

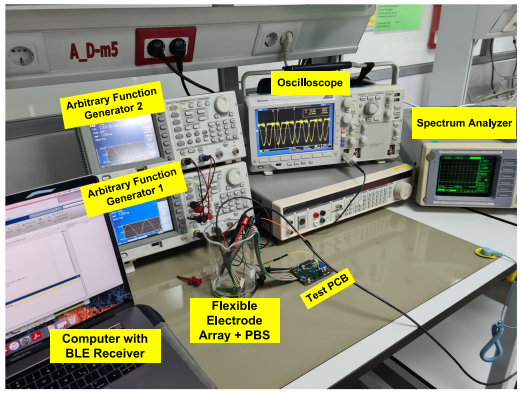

Fig. 24. Experimental setup.

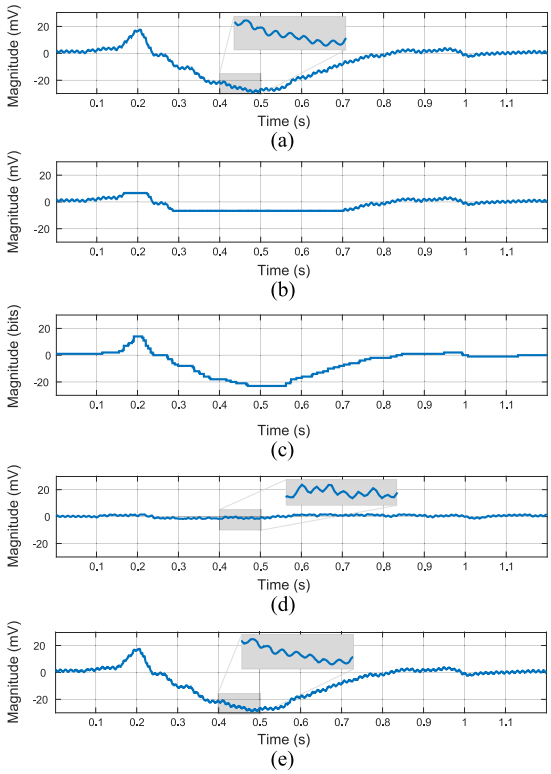

Fig. 25. (a) Pre-recorded motion artifact plus in-band 1.5 mV_{pp} tone applied to the saline solution, (b) output with ARL disabled, (c) artifact compression code, (d) Mode-1 output signal and (e) reconstructed signal in Mode-2.

interconnection lines running in parallel on the PCB are likely the cause of the observed crosstalk. Hence, it can be estimated that the crosstalk induced by the ASIC is lower than the referred value (-85 dB according to simulations). This is similar to the -92 dB crosstalk measured in [15].

Fig. 25 shows the results obtained when the solution was voltage driven by a long pre-recorded motion artifact superposed on a 1.5 mV_{pp}, 78 Hz tone as signal of interest. A custom-made polymide-based sub-dural microelectrode array with 32 nanoporous gold electrodes separated by 300 μ m (diameter 60 μm) was used for signal recording. The input waveform is shown in Fig. 25(a), while Figs. 25(b–e) show the outputs obtained from channel #1. Fig. 25(b) shows the output in Mode-1

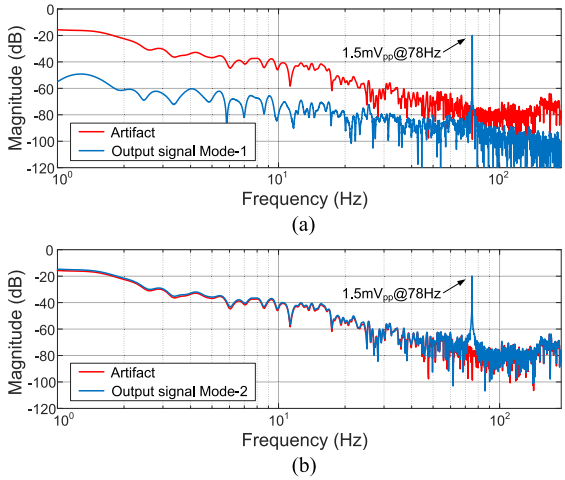

Fig. 26. Spectrum of pre-recorded motion artifact plus in-band 1.5 mV_{pp} tone applied to the saline of (a) Mode-1 output signal, (b) reconstructed signal in Mode-2. The artifact spectrum with no tone superposed is represented in red in both plots.

when the ARL is disabled, resulting in the saturation of the AFE main signal path and, therefore, the lost of information. Figs. 25(c–e) show, respectively, the compression code, and the system outputs in Mode-1 and Mode-2, when the ARL is enabled. Note from Fig. 25(d) that the signal of interest can be recovered in Mode-1 although perturbed by the imperfect cancellation of the artifact, which is attenuated by 25 dB in average (in agreement with Fig. 16). In any case, the output safely remains within the linear range of the AFE. The reconstructed signal in Mode-2 shows 99% correlation accuracy with respect to the original signal. The output signal spectra for Mode-1 and Mode-2 are shown in Figs. 26(a–b), respectively, together with the spectrum of the artifact alone. Although the motion artifact contaminates the low-frequency components of the recorded signal, the applied tone at 78 Hz can still be clearly distinguished in Mode-1 operation (see Fig. 26(a)). The attenuation of the artifact can be also appreciated by comparing the low frequency spectral content of Figs. 26(a-b).

Using the same setup as in Fig. 25, a symmetric biphasic stimulation current pulse was applied to the PBS solution through a voltage-controlled Howland current pump circuit. The duration of the cathodic/anodic phases is 14 ms, with an interphase delay of 2 ms, and a peak current amplitude of 750 μA. Fig. 27(a) shows the voltage recorded at the electrode interface with a commercial acquisition system (USB-ME32-FAI, Multi Channel Systems MCS, GmbH, Reutlingen Germany). The amplitude of the signal is about 300 mV_{pp}. Fig. 27(b) shows the output in Mode-1 with no auto-ranging resulting in saturation. Fig. 27(c–e) show, respectively, the correction code, the system output in Mode-1 and the reconstructed output in Mode-2, when ARL is enabled. Note that in Fig. 27(d) the output signal samples eventually saturate. This is due to the fact that the slope of the input signal is larger than the maximum tolerable by the ARL. In any case, the reconstructed signal, including the artifact, shows 96.7% correlation with the voltage in saline of Fig. 27(a) and the average attenuation of the artifact in Mode-1 amounts 38 dB.

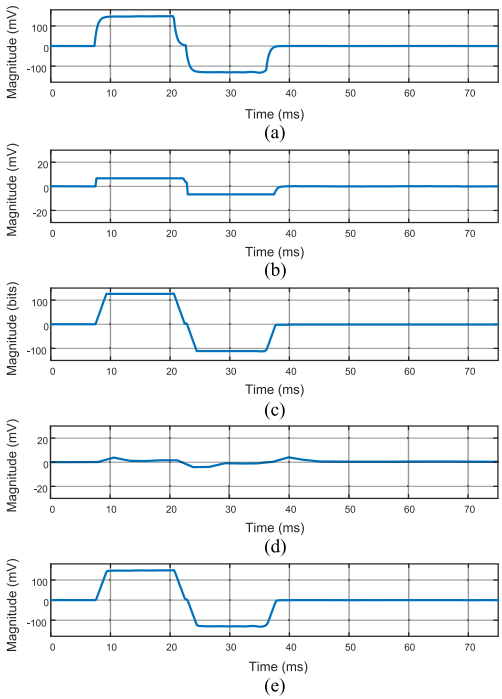

Fig. 27. (a) Voltage in the saline solution after applying a biphasic stimulation current pulse, (b) output with ARL disabled, (c) artifact compression code, (d) Mode-1 output signal and (e) reconstructed signal in Mode-2.

A. *In Vitro Measurements*

In vitro measurements were carried out by immersing a flexible microelectrode array with TiN electrodes (30 μm electrode diameter, 300 μm inter-electrode distance; FlexMEA36, Multi Channel Systems, MCS GmbH, Reutlingen Germany) in a cellular culture. The culture was grown as follows: Primary cortical neurons from mouse E18 embryos were obtained following standard protocol as described in [51]. Briefly, cells were dissociated with papain solution and cultured on Poly-D-lysine and Laminin covered plates with Neurobasal medium supplemented with B27, N2 and 0.1 % of Fetal Bovine Serum. One third of the medium was replenished every two days. After 4 days *in vitro*, BDNF (10nl/ml) was added to the medium to promote dendrite sprouting.

Fig. 28 shows a 60 s recording session in Mode-1 using monopolar sensing without delta encoding. For enhanced clarity, only 16 out of 32 signals are shown in Fig. 28. The power spectra of the recorded signals, plotted in Fig. 29, follow a $1/f^2$ characteristic in agreement with the typical power law with frequency of LFP activity [48]. Similar measurements were also carried out with bipolar encoding. They confirmed our findings derived from Fig. 22, namely: (i) bipolar encoding allows to reducing voltage swings due to the high spatial correlation of LFPs (up to 90% in some cases), and (ii) noise levels increase with the channel index due to the reconstruction errors in (16).

Fig. 30 shows the reconstructed neural response acquired in one channel after applying a symmetric biphasic stimulation current pulse. As in Fig. 26, an arbitrary function generator and a current pump circuit were used for the stimulation pulse (about 2 ms long and 30 mV_{pp} amplitude). In this measurement, the circuit was configured in Mode-2 with bipolar coding and the

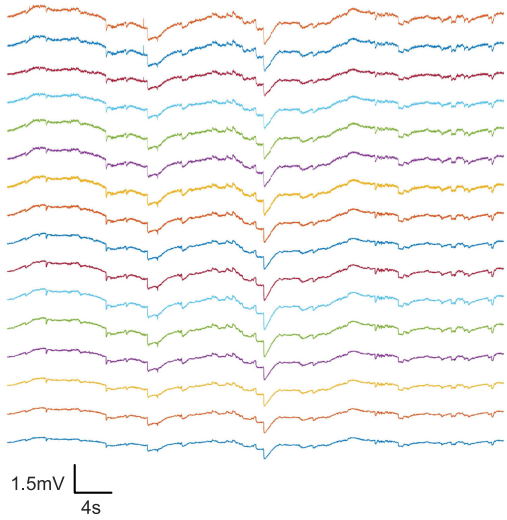

Fig. 28. Simultaneous *in vitro* measurements in Mode 1 operation with monopolar coding.

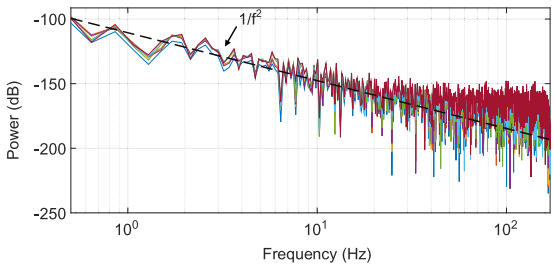

Fig. 29. PSDs for simultaneous 16-channel *in vitro* measurements.

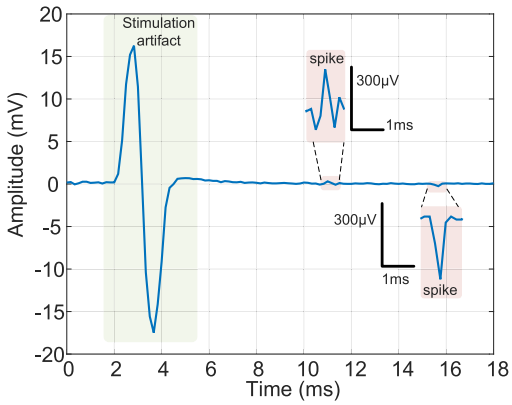

Fig. 30. Reconstructed signal after applying a symmetric biphasic stimulation current pulse in Mode 2 operation.

output was high-pass filtered off-chip at 100 Hz. As shown in the insets, high amplitude spikes were detected after stimulation. In this mode, isolated and burst of spikes were also observed without any current injection, as shown in Fig. 31.

B. *Comparison to State-of-the-Art*

Table III compares the presented prototype to other state-of-the-art high dynamic range neural recording systems, including the TDM-based proposals in [12], [16] and the artifact-aware works in [22], [46], [47], [52]. Although operation in Mode-2

TABLE III
COMPARISON WITH STATE OF THE ART

	[47]	[52]	[12]	[46]	[22]	[15]	[53]	This work Mode-1	This work Mode-2
Year	2014	2017	2018	2018	2019	2020	2020	**2020**	
Technology (nm)	180	180 HV	180	65	130	65	65	**180**	
Supply voltage (V)	1	1	1	0.8	1.2	2.5	1.2	**1.2**	
Power per channel (μW)	4.53	8	7	0.8	0.99	2.98	0.82	**1.5**	**2.5**
Area per channel (mm^2)	0.129	-	0.0039	0.024	0.011	0.0023 ‡	0.0039	**0.022**	
Artifact suppression method	folding	PCA denoising ‡	-	auto-ranging	track&zoom	template-matching ‡	clamping	**auto-ranging**	
# multiplexed channels	1	1	20	1	1	64	1024	**32**	
Input differential range (V_{pp})	8	100	17 †	260	10	110	-	**300**	
IRN per channel (μV_{rms})	3.83	1,6	5.6	1	2.6	1.66 ⋆	5.96	**1.4**	**4.8**
Signal bandwidth	5.7 kHz	-	15 kHz	500 Hz	1-500 Hz	1-1000 Hz ⋆	0.05-12.5kHz	**0.5-200 Hz**	**0.5-3000 Hz**
NEF/PEF per channel	3.09/9.72	7.8/60.8	4.7/22.4	1.8/2.6	3.5/15.2	2.21/12.2 ⋆	2.88/9.95	**4.5/24**	**5/20**
CMRR (dB)	-	-	50	81@28mV$_{pp}$	78	76@1.25V$_{pp}$	-	**87@600mV$_{pp}$**	
THD	<1%@3mV$_{pp}$	0.7%@100mV$_{pp}$	2%@17mV$_{pp}$ †	71 (SFDR)	70.1 (SFDR)	<1%@5mV$_{pp}$	-	**0.1%@5mV$_{pp}$**	**<1%@80mV$_{pp}$**
Dynamic Range (dB)	66	90	66-68 †	92	60 †	91	69.1	**71+26 (w/ARL)**	**83**
Channel FoM (pJ/c-step) [a]	0.139	0.309	0.401	0.025	0.052	0.013 ⋆	0.014	**0.065**	**0.036**

† Estimated value not explicitly mentioned in the reference.
⋆ For nominal recording operation, w/out CM artifact suppression.
‡ Off-chip DM artifact suppression.
△ ADC not included.
a. Channel-FoM$(DR) = P_{ch}/(2\,BW \cdot 2^{ENOB(DR)})$, where $ENOB(DR) = (DR(\text{dB})\text{- }1.76)/6.02$.

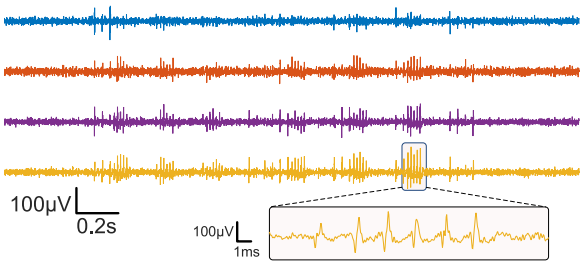

Fig. 31. Spikes detection for 4 adjacent channels.

is conceived in this work as an auxiliary testing facility, it has also been included in the table for completeness. The power and area consumption per channel have been calculated taking into account the power and area of the whole integrated system, although, in some cases, part of the functionality is implemented off-chip. As can be seen, this work performs comparably to other proposals along all metrics with noticeable improvements on input range, CMRR, linearity and dynamic range. Furthermore, all the functionalities discussed in this work have been implemented on-chip with the exception of the reconstruction operation in Mode-2, done in the μ-C.

VI. DISCUSSION

Charge-sampling (CS) [6], [14] and open-loop windowed integration sampling (WIS) [12] have been proposed to reduce the noise folding effect in TDM recorders. The basic structure in both techniques consists in a G_m cell driving a sample-and-hold capacitor. The hold operation attenuates high frequency noise components and effectively reduces the noise equivalent bandwidth to $f_{NEB} = f_s/2$. Whilst simple, thus, leading to efficient implementations in terms of area and power consumption, this circuit is not without drawbacks: the DC-gain and time constant of the AFE suffers from deviations due to process variations which may demand for some tuning mechanism; flicker noise, falling in the LFP/ECoG frequency band, and dc offsets are not reduced; large common-mode signals can drastically change the operation point of the transconductor, giving rise to distortion or even saturation; and the common-mode rejection ratio (CMRR) can be significantly lower than in closed-loop architectures. The two latter points can be solved by means of active or passive SC circuits before the charge-sampling stage [14], [16], but this is at the expense of increasing the noise floor of the AFE. Additional considerations on noise performance, clock jitter tolerance and other implementation nonidealities can be found in [54], [55].

In this work, a different approach based on oversampled narrow-band Correlated Double Sampling (CDS) instrumentation amplifiers [33] is proposed. Similar to the CS and WIS methods, signal integration is used to reduce high frequency noise effectively; however, while those techniques integrate in analog domain, our proposal carries out integration in digital domain. In the proposed architecture, DC gain is well-defined by ratioed capacitances and the circuit inherently exhibits low-pass filtering characteristics which effectively reduces the noise bandwidth of the AFE. In fact, the cut-off frequency of the amplifier, f_{IA}, can be made much lower than the sampling frequency f_s so that folded noise components falling in the bandwidth of interest are attenuated [34], [35]. Additionally, the technique offers high linearity, large common-mode range and is tolerant against process variations. It also attenuates DC offsets and flicker noise [34] with no need for an additional dummy channel [16]. As a shortcoming, the CDS operation subsamples and folds back thermal noise into the baseband. In this work, this effect has been compensated via signal oversampling at the expense of larger power consumption. Nevertheless, this increase is not prohibitive as shown in Table III. Other techniques, a priori more suitable for reducing noise folding, such as chopping modulation [9], [11], [56], are difficult to implement in rapid time-multiplexing systems due to the need to remove up-modulated noise and offset components per channel with large time-constant low-pass filters [6], [12].

VII. CONCLUSION

In this paper, a 32-channel time-division multiplexed neural front-end for LFPs/ECoG recordings has been presented. The system features two recording modes, monopolar and bipolar. This latter is based on spatial delta encoding techniques and is aimed to take advantage of the large correlations between nearby channels. A combination of narrow-band Correlated

TABLE IV
INSTRUMENTATION AMPLIFIER PARAMETERS

Parameter	Definition
$C_{az,m}$	$C_{az} + C_m$
$C_{fb,m}$	$C_{fb} + C_m$
β_1	$C_{az,m}/(C_{in} + C_{fb} + C_{az,m} + C_p)$
β_2	$C_{fb,m}/(C_{in} + C_{fb,m} + C_p)$
$C_{eq,1}$	$(C_{az,m} \cdot (1-\beta_1) + C_L)/\beta_1$
$C_{eq,2}$	$(C_{fb,m} \cdot (1-\beta_2) + C_L + C_{az})/\beta_2$
ϵ_1	$1/(\beta_1 A_0)$
ϵ_2	$1/(\beta_2 A_0)$

Double-Sampling (CDS) amplification and signal oversampling is used at the front-end to reduce flicker noise and counteract the thermal noise excess due to aliasing. Two digital-feedback loops provide robustness against large interferences with little impact on power consumption, area occupation or noise behavior. One loop implements a voltage-triggered auto-ranging algorithm which allows to attenuate large interferers in digital domain while preserving neural information, thus effectively increasing the dynamic range of the system to 71 dB + 26 dB. The other is a DC servo loop for electrode offset cancelling which extends the front-end input range to $300\,\mathrm{mV_{pp}}$. The front-end provides state-of-the-art specifications, particularly in terms of dynamic range, noise and power consumption. Measurements in saline and *in vitro* confirm the suitability of the approach.

APPENDIX
NOISE ANALYSIS OF THE CDS AMPLIFIER

The method explained in [41] has been used for the noise analysis of the instrumentation amplifier in Fig. 5(a). The analysis has covered all major noise sources in the circuit, including the thermal noise from the switch-on resistances as well as the white and flicker noise contributions of the OTA. However, only the white noise component of the OTA is herein presented as it has the largest impact on the noise spectral density of the circuit. The method is based on the calculations of (i) the continuous-time transfer functions $F_{x,p}(s)$ between the noise source and the circuit capacitor C_x during the clock phase Φ_p, $(p = 1, 2)$ and (ii) the transfer functions $H_{x,p}(z)$ between the noise voltage across capacitor C_x and the circuit output on phase Φ_p. Taking into account the parameter definitions in Table IV, where A_0 is the OTA dc gain, C_p is the parasitic capacitance at the input of the OTA and C_L is the load capacitance – the other capacitances are identified in Figs. 5–6, functions $F_{x,p}(s)$ from the input node of the OTA to the input (C_{in}), feedback (C_{fb}), and hold (C_{az}) capacitances are given by:

$$\mathbf{F}(s) = \begin{bmatrix} F_{in,1}(s) = \frac{1}{1+\epsilon_1+s/p^{(1)}} \\ F_{fb,1}(s) = \frac{1}{1+\epsilon_1+s/p^{(1)}} \\ F_{az,1}(s) = \frac{-1+\beta_1}{\beta_1 \cdot (1+\epsilon_1+s/p^{(1)})} \\ F_{in,2}(s) = \frac{1}{1+\epsilon_2+s/p^{(2)}} \\ F_{fb,2}(s) = \frac{-1+\beta_2}{\beta_2 \cdot (1+\epsilon_2+s/p^{(2)})} \\ F_{az,2}(s) = \frac{-1}{\beta_2 \cdot (1+\epsilon_2+s/p^{(2)})} \end{bmatrix} \tag{17}$$

where it is assumed that the frequency response of the closed-loop circuit can be modelled on each clock phase by a single pole at $p^{(q)} = g_m/C_{eq,p}$.

Similarly, the discrete-time transfer functions on phases 1 and 2 between said capacitors and the output node are given by:

$$\mathbf{H}(z) = \begin{bmatrix} H_{in,1}(z) = \frac{C_{in} \cdot (C_3 - C_1 \cdot z)}{C_3 C_4 - C_1 C_2 \cdot z} \\ H_{fb,1}(z) = \frac{C_{fb} \cdot (C_3 - C_1 \cdot z)}{C_3 C_4 - C_1 C_2 \cdot z} \\ H_{az,1}(z) = \frac{-1}{(1+\beta_1 \cdot \epsilon_1)} \\ H_{in,2}(z) = \frac{C_{in} \cdot (C_4 - C_2 \cdot z)}{C_3 C_4 - C_1 C_2 \cdot z} \\ H_{fb,2}(z) = \frac{-1}{(1+\beta_2 \cdot \epsilon_2)} \\ H_{az,2}(z) = -1 \end{bmatrix} \tag{18}$$

where

$$\begin{aligned} C_1 &= C_{fb,m} \cdot (1+\epsilon_2) \; C_3 = C_1 + C_{az} \\ C_2 &= C_{az,m} \cdot (1+\epsilon_1) \; C_4 = C_1 - C_{fb} \end{aligned} \tag{19}$$

Let us build the square matrices $|\mathbf{F}(s)|^2 = \mathbf{F}(s)\mathbf{F}^{\mathrm{t}}(-s)$ and $|\mathbf{H}(z)|^2 = \mathbf{H}(z)\mathbf{H}^{\mathrm{t}}(z^{-1})$, as well as the cross-spectral density matrix $\mathbf{S}(j\omega) = S_a(\omega) \cdot |\mathbf{F}(j\omega)|^2$ where $S_a(\omega)$ is the input-referred thermal noise spectral density of the OTA in Fig. 6, approximately given by:

$$S_a(\omega) \approx \frac{16\,\eta\,V_t\,k_B\,T}{3\,I_b} \tag{20}$$

where I_b is the biasing current of the OTA, V_t is the thermal voltage, η is the sub-threshold slope factor, k_B is the Boltzmann constant and T is the temperature.

According to [41], the k-th replica due to sampling of the output noise power spectral density of the circuit due to the input white noise component of the OTA is given in compact form as,

$$S_k(\omega) = \frac{1}{T_s^2} \sum_{p,q=1}^{2} \mathbf{u}_p \left(|\mathbf{H}(z)|^2 \circ \mathbf{S}(j\Omega_k) \right) \mathbf{u}_q^{\mathrm{t}} \cdot e^{-j\Omega_k \frac{T_s(p-q)}{2}} \tag{21}$$

where T_s is the sampling period, $z = e^{j\omega T_s}$, $\Omega_k = \omega - 2\pi k/T_s$ and '$\circ$' denotes the element-wise Hadamard product. Vectors $\mathbf{u}_1$ and $\mathbf{u}_2$ are respectively given by $\mathbf{u}_1 = [111000]$ and $\mathbf{u}_2 = [000111]$. Summing over all the replicas, the output noise spectrum of the CDS amplifier in Fig. 5(a) is given by

$$S_{CDS}(\omega) = \sum_{k=-\infty}^{\infty} S_k(\omega) \tag{22}$$

Although too complex to gain direct insight, this expression provides an accurate mechanism, as demonstrated in Fig. 9, for exploring and optimising the design space of circuit components.

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