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Grid-Following Voltage Source Converters: Basic Schemes and Current Control Techniques to Operate With Unbalanced Voltage Conditions

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ABSTRACT The growing relevance of voltage source converters (VSCs), and the deep impact they have on the development and maintenance of the electrical grid, increase the necessity of further research on how to deal with nonideal grid conditions from the VSCs control. This paper is aimed to summarize the basic techniques and schemes that might be required for a grid-connected VSC to work under these conditions: grid synchronization schemes, sequence decomposition, current reference generation, and current controllers. At the same time, some alternative schemes that improves the basic ones are cited. Modelling and the two typical current controllers design and tuning under stationary and synchronous reference frames are also exhibited. Given the importance of the current control stage in the VSC behaviour, five control schemes, designed to track negative sequence currents, are shown and tested in simulation and experiments. According to the experiments, it is shown that the standard proportional-resonant controller achieves the best performance in negative sequence tracking due to the robustness of its non-ideal version, the improved implementation thanks to the delta operator, and the non-dependence on grid-synchronization schemes. Alternatively, one approach based on dual synchronous reference frame is also highlighted for easiness of implementation and good performance.

INDEX TERMS Current controller, current reference generation, negative sequence, unbalanced grid, voltage source converter (VSC).

I. INTRODUCTION

The development of power semiconductors and the flexibility required for power converters are the main reasons for the popularity of voltage source converters (VSCs) [1]. By modulating different voltage levels, they can control the power flow demanded by the design application [2], [3]. Either if VSCs are grid-connected or working in islanded operation mode [4], [5], the flow of energy is controlled by means of the phase currents. Thus, determination of the desired phase currents (current reference generation) and the design of the stage that regulates them (current controller) are crucial [6]. In the following, some fundamental concepts and the state-of-art of unbalanced grids are exhibited.

A. UNBALANCED GRIDS

1) UNBALANCED GRID FORMULATION

The constant enlargement of the electrical grid makes it more vulnerable to short-circuits [7], [8], voltage dips [9], imbalances [10] or any kind of faults. Therefore, VSCs are demanded to handle such situations whether by assisting on the grid restoration [11], [12], or by not worsening it [13],

[14]. Such events can be regarded as distortion of the desired sinusoidal grid voltages, which can be mathematically derived as the addition of a negative and zero sequence to the balanced one, usually referred as positive one [15]. This transformation facilitates the modelling and control design under such conditions [16], and it is referred as sequence decomposition. Thus, sequence decomposition is vital to know the grid state and to develop proper control strategies [17], [18]. Similarly, the phase currents can be decomposed into positive and negative sequences, whereas zero sequence current component is not present in three-wire systems. Thanks to this transformation, their interaction with the phase voltages can be further analyzed [6], [8]. Harmonics and interharmonics are also a source for unbalanced voltage conditions that generate voltage drop along the line [19], which may require the use of additional VSCs as active power filters to compensate for such a condition [20]. Plenty of mitigation techniques have been developed to compensate the presence of harmonics that renewable energy sources may introduce into the grid [21]. Nevertheless, this paper focuses on the negative sequence presence as source of unbalance.

2) EFFECTS ON THE SYSTEM PERFORMANCE

The effect the negative sequence voltage and current have on the system performance has been deeply explored [5]–[8], [22]–[24]. It generates oscillations of twice the fundamental frequency in the active power [6], which can have consequences on the dc bus, generating additional harmonics (namely 3 rd one) in the phase currents [7]. Unfortunately, it has been shown that achieving no power ripple and injecting positive balanced phase currents are opposite targets [25]. Several proposals have been presented to diminish the power ripple

- Modifying the current reference generation stage [23]–[29].
- By means of averaged modelling techniques to design a control strategy [6], [30].
- Modifying the voltage commands [8].

Some strategies based on modifying the current reference generation stage are exposed later.

3) SEQUENCE DECOMPOSITION TECHNIQUES

The knowledge of the positive, negative and zero sequence components of the grid voltage facilitates the designing of control strategies that considers the voltage unbalance condition. However, such an obtention is not instantaneous and some voltage imbalances in a grid may appear due to sudden faults or unbalanced load connections [31]. Therefore, the voltage and current sequence decomposition computation should be fast enough to detect a grid fault on time [32]. On this matter, several solutions have been presented in the literature

- The use of delayed signal cancellation (DSC) tools [9], [18].
- Second order generalized integrators with quadrature signal generation (SOGI-QSG) [33], [34].
- Derivation of a model from generic equations of the three sequences [17].
- The use of filters or moving average windows [10], [35].

Nonetheless, filter-based approaches have been reported as the slowest and least reliable approach due to its dependence with the filter dynamic [10].

B. PHASE CURRENTS UNDER UNBALANCED VOLTAGE CONDITION

1) CURRENT REFERENCE GENERATION

As it was stated, one strategy to deal with the power ripple generated under unbalanced voltage condition is by means of the current reference generation. These references can be defined for each sequence component allowing the control to achieve specific objectives, such as only positive sequence current [26], no active power ripple [27], a trade-off in active and reactive power ripple attenuation [25], or grid voltage support [24], among others.

An issue that should not be underestimated is that the positive and negative reference value of the current may increase the rms value of any of the three-phase currents without increasing the effective energy flow. However, some of the previous control objectives require the injection of negative sequence current. Consequently, some constraints in the current reference generation might be necessary if the hardware limits require it. This can be done either dynamically, such as [22], which restricts each sequence component of the current reference proportionally to the nominal values; or, by using fixed limits, such as [7], which clamps the susceptance and conductance values used for current reference generation. It is worth noting that, due to these current limits, the active or reactive power capabilities might be compromised if the negative sequence current references are not zero [7].

2) CURRENT CONTROLLERS

Once the references are computed, the current controller (CC) should provide tracking capabilities of the positive and negative sequence components. Since the phase-amplitude control (PAC) [36] appeared as one of the first CC, plenty of CCs have been developed in the literature [5]–[10], [22]–[30], [37]–[43] targeting different objectives, although, it is always desired to achieve zero steady-state error and have the fastest and most damped transient as possible [10], [44]. Some CCs depend on the current sequence decomposition of the measured current and voltage as they track each sequence individually [24], [27]. In contrast, those approaches that do not depend on it [23], [28], [29] avoid the additional delay this process may introduce in the current closed-loop control [10]. In this paper, five CCs with negative sequence tracking capabilities are exposed and tested in simulation and experiments.

3) COMMON CURRENT CONTROLLERS

Regarding the most common linear controllers, two approaches are the most used ones due to its robustness and easiness of implementation

- A proportional integral (PI) controller [1], [42] in synchronous reference frame (SyRF) [45].
- A proportional resonant (PR) controller [41], [46] in stationary reference frame (StRF) [15].

The former takes advantage of the fundamental component being a dc value in SyRF, whereas the later implements a resonant term that acts as an integrator for the resonant frequency. Thanks to this, the controller bandwidth covers the fundamental component in both cases.

However, the PI controller bandwidth does not cover the negative sequence component, that appears as a component at twice the frequency in SyRF. To solve this, some modifications have been considered

- Adding negative sequence feedforward terms in the closed loop [10].
- Using full feed-forward schemes of the grid voltage for *LCL*-type grid-connected converters [47].
- Using parallel PI schemes for each sequence [27], [43], referred as dual SyRF (DSRF).
- Using a PI+PR scheme in SyRF to track the component at twice the fundamental [48].

In contrast, when operating on the StRF using the PR scheme, the knowledge of the grid frequency can be used to properly track the positive and negative sequences at the same time [34]. However, the ideal behaviour of the resonant part narrows the controller bandwidth [49], and thus it is common to use a nonideal PR instead [50], where the bandwidth is widened at the cost of a more limited magnitude response.

4) ALTERNATIVE CURRENT CONTROLLERS

Some additional linear current controllers for VSCs can be found in the literature as follows

- The plug-in repetitive controller, which tracks the fundamental component and its multiples [51], and can be used to cancel out the harmonic appearance [52].
- Those controllers based on state-feedback [53].
- Controllers that are based on passivity with disturbance observer [6].

C. REFERENCE FRAME: STRF AND SYRF

1) PLL AND FLL

In order to simplify the current control design, it is common to refer the ac variables in StRF (known as $\alpha\beta\gamma$) using the Clarke transformation, where the zero sequence component can be isolated [15]. Alternatively, the SyRF (known as $dq0$) rotates the StRF using the Park transformation in such a way that the fundamental positive-sequence ac component appears as a dc magnitude, which further simplifies the modelling and control. However, the Park transformation requires the knowledge of the grid angle θ_g, which implies the use of a synchronization scheme. In this regard, a general classification can be derived whether they are open-loop, such as the transformation angle detector [45]; or closed-loop, such as the phase-locked loop (PLL) [54]. The closed-loops are the most common ones, however, in order to increase its robustness against harmonic presence, phase-shift or faults, some more complex schemes may be required [53], [55], [56]. Some PLL schemes are summarized as follows

- Based on sequence decomposition [17], [57], [58].
- Based on delayed signal cancellation (DSC) [59], [60].
- Based on filters of moving average windows (MAF) [61].
- Based on second-order generalized integrator (SOGI) [62].

In contrast, the resonant term in the CC in StRF requires the knowledge of the fundamental frequency ω_g. For this, a frequency-locked loop (FLL) is usually implemented [63]. Some FLL approaches are

- Based on SOGIs [64].
- Based on dual SOGI with quadrature-signal generation (SOGI-QSG).
- Based on adaptive vectorial filters [65].

In general terms, the difference between FLL and PLL lies in the feedback loop: FLL tries to lock the frequency such that the output frequency equals the input one, while the PLL aims the same but for the input phase. Consequently, the FLL's effect on the closed-loop system control is usually less noticeable than the PLL's one, considering that the grid frequency does not have abrupt changes like the ones the grid phase may have under grid voltage sags. Besides, PLLs are more accurate than FLLs—a phase-locked variable implies to be frequency-locked, but not necessarily the opposite as it may exist some phase-shift [66].

2) PI IN SYRF AND PR IN STRF

Focusing on the two most typical CC schemes, PI in SyRF and PR in StRF [42], several comparisons have already been reported [38], [44], [57]. From this comparison, PR in StRF are highlighted for their simplicity in VSC applications, as they do not require the grid phase information [41]; but PI in SyRF are not undermined due to its easy tuning process and the well-established stability criteria of PI controllers [67]. It is also analytically shown that an ideal well-tuned PR in StRF has the same frequency response that the DSRF scheme [68]. Nevertheless, some applications may use both CCs and reference frames

- Scheme in [69] uses SyRF and StRF to control unbalanced and nonlinear loads in four-wire voltage source inverters.
- Works [48], [70] present a CC in SyRF that uses both PI and PR controllers and improves the transient behaviour under unbalanced grid voltages.
- Work [71] proposes a modified SyRF such that the developed PLL transient performance is improved, specially against distortion, noise and grid disturbances.

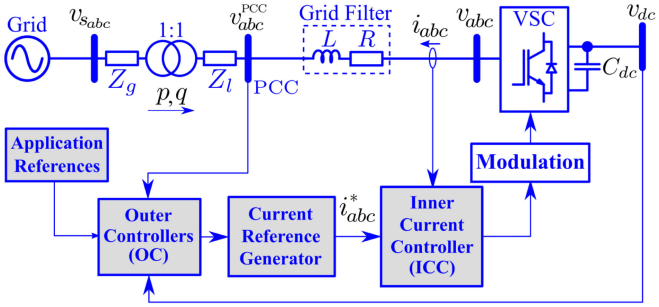

FIGURE 1. Control diagram of a grid-connected VSC.

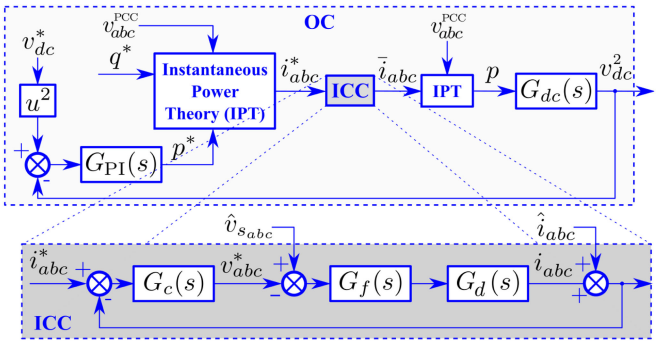

FIGURE 2. Generic diagram of the cascaded configuration with two linear feedback controllers.

D. CONTRIBUTIONS AND STRUCTURE

This paper exhibits some of the basics techniques and fundamentals of VSCs to deal with unbalanced grid voltage conditions. For this, VSC modelling, control, and the two most typical CCs: PI and PR in SyRF and StRF, respectively, are initially exhibited. Some issues and solutions found in the literature related to unbalanced grid voltage conditions are exhibited and discussed: sequence decomposition, grid synchronization and current reference generation. Additionally, several current control schemes to operate under unbalanced voltage conditions are also presented and tested both in simulation and experiment.

The rest of the paper is organized as follows. The basics of grid-connected VSCs, that are modelling, control schemes and tuning in SyRF and StRF are presented in Section II. Section III presents the unbalanced grid voltage conditions. For this, common strategies and approaches to deal with it are exhibited: sequence decomposition, and current reference generation with different objectives. Section IV shows five existing current controllers devoted to work under grid voltage unbalanced conditions, i.e. they are able to track negative sequence of the phase currents. Section V shows the results of testing these controllers in simulation with changes in the current references. Similarly, section VI shows the results of testing these controllers in experiments considering the same changes in the negative sequence current reference.

II. VSC PRINCIPLES UNDER BALANCED CONDITIONS

A. MODEL AND BASIC CONTROL SCHEME

Fig. 1 depicts a generic grid-connected VSC scheme. The grid-side line impedance is denoted by Z_g, while the VSC-side one is referred as Z_l. The depicted variables are described as follows: Grid voltages $v_{s_{abc}}$; phase currents i_{abc}; phase voltages at the point of common coupling (PCC) v_{abc}^{PCC}; dc-link voltage v_{dc}; instantaneous active p and reactive q power; plug-in filter inductance L and parasitic resistance R; current references i_{abc}^*; and converter output voltage v_{abc}.

Fig. 1 also depicts a generic control scheme based on a cascaded configuration with an outer controller (OC) and an inner current controller (ICC). The cascaded configuration is one of the most standard approach for the control of grid-connected VSC using linear controllers [72]. It is composed by the OC forwarded by the ICC, but it can be further expanded by including parallel or serial controllers/stages without losing generality.

The OC along with the current reference generator determines the references for the ICC in such a way that the specific objectives of the VSC are fulfilled, such as grid voltage support or grid restoration [73], regulation of the dc-link voltage v_{dc} [74], among others. The references that the OC generates may require to be transformed to current references, usually achieved by means of the instantanous power theory (IPT) [75], or the considered current reference generation strategy.

The ICC takes the current references from the previous stages, and implements a control law to define the control action, which is a voltage vector that has to be modulated in the VSC output. In this way, ICC regulates i_{abc} towards i_{abc}^*. Thanks to this, the OC loop, whose bandwidth is much smaller than the ICC one, can fulfill its control objectives. The modulation stage (usually PWM at a fixed switching frequency f_s), that is placed before the ICC, is in charge of commanding the switching devices of the VSC in such a way that it reassembles such desired voltage vector. This is the common scheme of an inner current controller with modulator. However, there exist techniques that do not use a modulator [76] or explicitly model the modulator inside their formulation as an attempt to combine both strategies [77].

In case of a passive dc side, the task of regulating v_{dc} towards v_{dc}^* is carried out by the OC which will define the active power reference p^*. Other objectives can be considered depending on the dc-link nature, such as charging/discharging an energy storage system, or supplying the grid in case of a blackout, among others [74]. The reactive power reference q^* can be computed independently to v_{dc}^* to pursue different objectives, such as unity power factor ($q^* = 0$), reactive power compensation, or grid voltage regulation [78].

A generic diagram of the cascaded configuration with the two controller loops is shown in Fig. 2. The transfer functions that appears in it are explained in the next section. Using this diagram, the noise induced by measurements or the implementation are modelled using variables $\hat{v}_{s_{abc}}$ and $\hat{i}_{abc}$, respectively.

B. PI FOR DC-LINK VOLTAGE REGULATION

Consider the active power balance of the system (Fig. 1), neglecting the losses and assuming that a resistor is attached to the dc-link R_{dc}, the following expression is obtained

$$p = v_{dc}\left(\frac{v_{dc}}{R_{dc}} + C_{dc}\frac{dv_{dc}}{dt}\right), \tag{1}$$

where p is the active power, and C_{dc} is the capacitance of the dc-link capacitor. From (1), the transfer function $G_{dc}(s)$ can be obtained

$$G_{dc}(s) = \frac{v_{dc}^2(s)}{p(s)} = \frac{1}{C_{dc}\left(\frac{1}{R_{dc}C_{dc}} + s\right)}. \tag{2}$$

A PI controller acting on p could regulate v_{dc} towards a reference v_{dc}^*. Moreover, the neglected losses could be included in (2) as a proportional term to p, changing the model gain, but keeping the feasibility of using a PI controller. Work presented in [72] gives some guidance on how to tune the PI controller, resulting in

$$k_p = \frac{C_{dc}}{\sqrt{3T_sT_i}},\ k_i = \frac{C_{dc}}{\sqrt{3T_sT_i^3}},\ T_i = \alpha^2 3T_s \tag{3}$$

where k_p and k_i are, respectively, the proportional and integral terms of the PI controller, T_s is the sampling time of the system ($T_s = 1/f_s$), and T_i is the integral time constant whose value should be tuned to limit the controller bandwidth to 1/50 and 1/10 of the ICC's, i.e. $\alpha \in [10, 50]$ [72]. For simplicity's sake in the OC design, the closed-loop ICC transfer function was simplified to be a first-order system

$$G_{\text{ICC}}(s) \approx \frac{1}{1 + 3T_s s} \tag{4}$$

with a bandwidth of $1/(2\pi(3T_s))$ rad/s.

C. TUNING AND DESIGN OF COMMON CC

The current dynamic model of a grid-connected VSCs can be obtained from the Kirchhoff's laws (KL) in Fig. 1 as follows

$$v_{s_i} = R_t i_i + L_t\frac{di_i}{dt} + v_i\ , \quad i = a, b, c \tag{5}$$

where R_t represents the line and filter resistance, and L_t the line and filter inductance. Defining v_i^* as the control output and $T_f = L_t/R_t$ as the time constant of the system, the transfer function $G_f(s)$ is extracted from (5) and commonly used to design and tune the ICC

$$v_i^* := v_{s_i} - v_i$$
$$G_f(s) = \frac{i_i(s)}{v_i^*(s)} = \frac{1}{R_t + L_t s} = \frac{T_f}{L_t(1 + T_f s)}. \tag{6}$$

Besides, a transfer function $G_d(s)$ that represents the delay of digital systems and PWM implementation is usually forwarded with $G_f(s)$ in the model [79] as follows

$$G_d(s) = \frac{1}{(1 + 1.5T_s s)}. \tag{7}$$

In the following sections, the common current controllers used either in StRF or SyRF are shown.

1) PR IN STRF

The common controller used in StRF is a proportional-resonant (PR) controller with control parameters k_p and k_r. It corresponds to a proportional term and a resonant term tuned at the target frequency. Ideally, it has infinite gain at this frequency, but the limited accuracy of digital systems and noise measurements requires a wider bandwidth to obtain a more robust controller [41]. Therefore, the resonant scheme is modified in such a way that its bandwidth is widened by $\pm\omega_f$, resulting in the nonideal PR controller, whose transfer function is

$$G_c^{\text{St}}(s) = k_p + \frac{k_r\omega_f s}{s^2 + 2\omega_f s + \omega_r^2}, \tag{8}$$

where the resonant frequency ω_r is selected to be equal to the grid one ω_g. With this, the robustness against grid frequency variations is increased [50], [79]. The tuning of such controller can be made by designing the phase margin (PM) of the open-loop system composed by (5), (7) and (8). Summarizing the procedure proposed in [79], the following equations can be used to tune the control parameters. As a result, a PM with the desired value PM_{bw}^* at the resulting bandwidth frequency f_{bw}, and a minimum PM with value PM_{res}^* around the resonant frequency are achieved simultaneously

$$f_{\text{bw}} = \frac{2}{3}\left(\frac{1}{4} - \frac{\text{PM}_{\text{bw}}^*}{360^\circ}\right) f_s \tag{9}$$

$$k_p = 2\pi f_{\text{bw}} L_t\sqrt{(3T_s\pi f_{\text{bw}})^2 + 1} \tag{10}$$

$$\angle G_c^{\text{st}}(s)G_d(s)G_f(s)|_{s=j(\omega_g+\omega_f)} = 180^\circ - \text{PM}_{\text{res}}^* \tag{11}$$

Note that eqs. (9), (10) and (11) fix f_{bw}, k_p and k_r respectively.

For the tuning process, $\omega_r = \omega_g$ can be selected as the nominal of the grid, but a robust implementation of the PR controller [23] requires a more accurate value of ω_g, which can be obtained by means of a FLL [33], [63], [65]. In terms of robustness against unbalanced and distorted grids, the SOGI-QSG scheme is gaining popularity [64]. The generic diagram of a FLL based on SOGI-QSG is depicted in Fig. 3(a). Basically, the SOGI-QSG performs as a filter tuned at a given frequency—selected as ω_g for the FLL application. The quadrature output (qv_s') outputs such magnitude, but with a phase-delay of 90°, as shown in the Bode plot of Fig. 3(b). Similarly, the same magnitude with no phase-shift can be obtained from this scheme, as shown in the Bode plot of Fig. 3(c). From this, a FLL scheme can be implemented as shown in Fig. 3(a) where an auto-tune block (gain γ) is used.

In summary, the ICC diagram for StRF using the PR controller (8) and SOGI-based FLL is depicted in Fig. 4.

2) PI IN SYRF

During normal operation, a vector represented in the $\alpha\beta\gamma$ frame is rotating with the grid angle θ_g at the fundamental

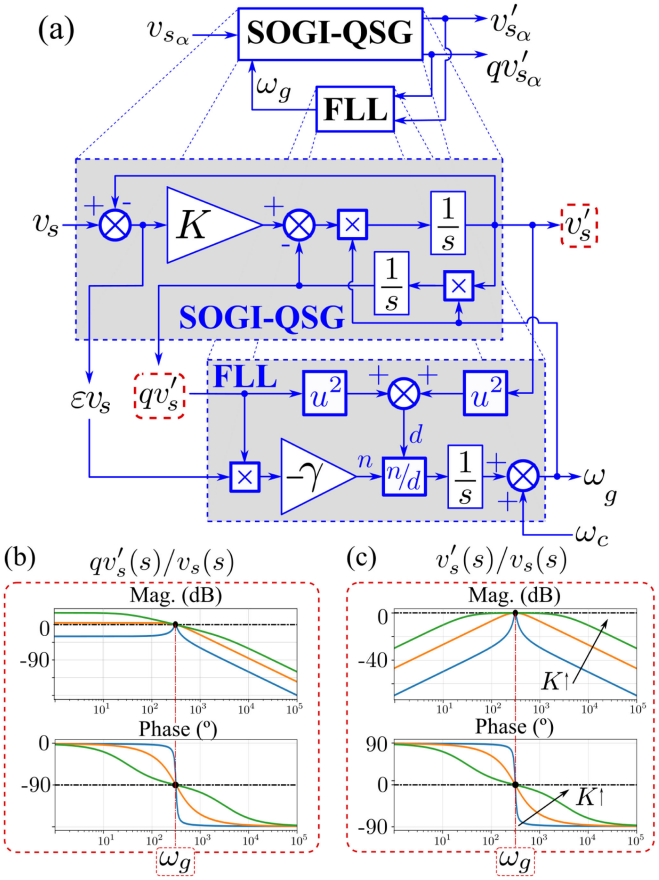

FIGURE 3. FLL based on SOGI-QSG with v_{s_α} as input: (a) General diagram, (b) Bode plot of SOGI quadrature qv'_s/v_s, and (c) Bode plot of SOGI v'_s/v_s.

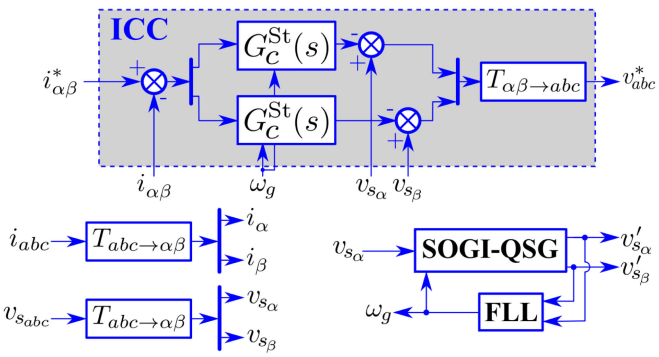

FIGURE 4. ICC diagram for StRF using the PR Controller with grid voltage feedforward term and SOGI-based FLL.

frequency. By rotating the reference frame using the Park transformation, the vector will stay static in the SyRF, also known as direct-quadrature-zero ($dq0$) axes. Thus, the ac components at the fundamental frequency are transformed to dc ones. In this reference frame, the component of the γ axis is kept equal and referred as zero component. In contrast to StRF, this transformation modifies the VSC model (5) to

$$v_{s_d} = R_t i_d + L_t \frac{di_d}{dt} - \omega_g L_t i_q + v_d \tag{12}$$

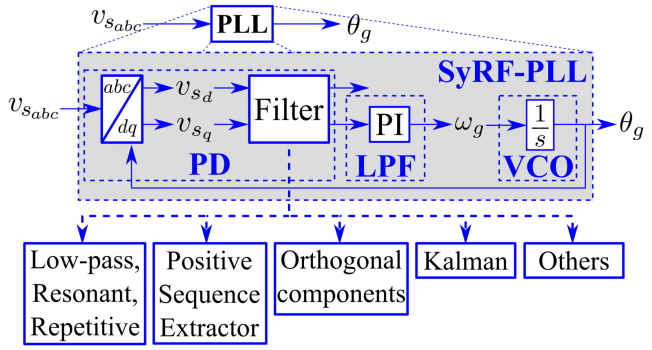

FIGURE 5. Diagram of a basic three-phase SRF-PLL with filter stage. Several types of filter stage are mentioned in [54].

$$v_{s_q} = R_t i_q + L_t \frac{di_q}{dt} + \omega_g L_t i_d + v_q \tag{13}$$

where the cross-coupling terms ($\mp\omega_g L_t i_{qd}$) appear due to the derivative applied to the Park transformation matrix. For this, the control outputs are redefined as

$$v_d^* := v_{s_d} - v_d + \omega_g L_t i_q\,, \quad v_q^* := v_{s_q} - v_q - \omega_g L_t i_d,$$

in such a way that the same model (6) can be used for SyRF. As a result, each sequence d or q can be controlled separately. Paper [80] makes a comparative of some cross-coupling decoupling techniques for SyRF that take parameter uncertainty into account.

Given that the inputs have a dc nature, PI controllers can be used

$$G_c^{\mathrm{Sy}}(s) = \mathrm{PI}(s) = k_p + \frac{k_i}{s}. \tag{14}$$

There exist several techniques for the tuning process of the PI control parameters. Following the procedure exhibited in [72], where the closed-loop ICC is formulated as a second-order system with a damping ratio of $1/\sqrt{2}$ and the integrator time constant $T_i = k_p/k_i$ is selected to match T_f, the control parameters for the PI controller can be obtained as

$$k_p = \frac{L_t}{3T_s} \tag{15}$$

$$k_i = \frac{L_t}{3T_s T_f}. \tag{16}$$

The SyRF scheme requires the knowledge of the grid angle θ_g to perform the Park transformation, which can be obtained by means of a PLL [40], [54], [55], [59]. The basic scheme usually comprises a phase detector (PD), a low-pass filter (LPF) and a voltage controlled oscillator (VCO) [45]. Accordingly, the most basic configuration of synchronous reference frame PLL (SRF-PLL) uses the abc to dq transformation as PD, a PI as LPF, and an integrator as VCO. This diagram of SRF-PLL with a filter stage for unbalanced and distorted grid rejection is shown in Fig. 5 [54]. Alternatively, more complex schemes can be used, such as the Dual SOGI-PLL (DSOGI-PLL) [81], which combines the SOGI scheme to filter the grid voltage measurements and the conventional SRF-PLL,

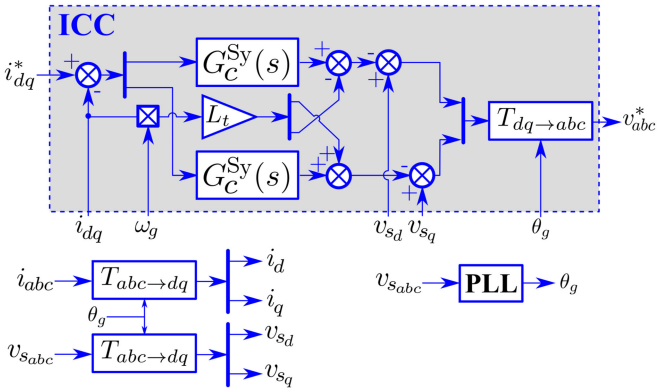

FIGURE 6. ICC diagram for SyRF using the PI Controller with a SRF-PLL.

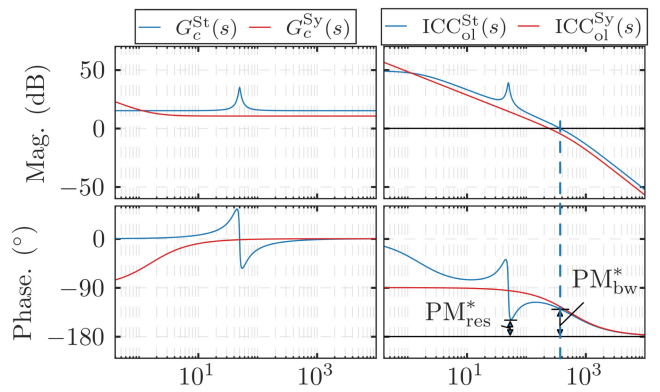

FIGURE 7. (Left) Bode plot of PI and a nonideal PR controller tuned according to (10)–(11) and (15)–(16), respectively. (Right) Bode plot of the open-loop ICC. $PM^*_{bw} = 50$, $PM^*_{res} = 30$, $L_t = 2$ mH, $R_t = 0.02\,\Omega$, $w_f = 10$ rad/s and $T_s = 1/5000$ s.

the Dual SRF-PLL (DSRF-PLL) [57] that decouples each sequence and implements the SRF-PLL in the positive one, or the complex-vector-filter that implements a prefilter in one single complex function to achieve sequence decomposition prior to the PLL [58].

In summary, the ICC diagram for SyRF using a PI controller and a SRF-PLL is shown in Fig. 6.

Fig. 7 shows the Bode plot of both the non-ideal PR and the PI controller. Besides, the open-loop transfer function of the ICC considering (6) and (7) as $ICC_{ol}^{St}(s) = G_c^{St}(s)G_d(s)G_f(s)$ is also depicted. As it can be seen, the PR controller can be tuned by selecting the corresponding values of the desired phase margin, while the PI controller can be tuned by knowing the system parameters.

III. WORKING UNDER UNBALANCED VOLTAGE CONDITIONS

This section will present some existing approaches of sequence decomposition, and current reference generation, which are used to operate under unbalanced grid voltage conditions.

A. SEQUENCE DECOMPOSITION

Sequence decomposition is the cornerstone to diagnose the grid voltage unbalanced state. Besides, some CCs rely on the voltage and current sequence decomposition affecting its performance. The sequence decomposition involves the use of a technique that separates one sequence from another, either by means of filtering or another analytical tool. Some of these techniques are

- Delayed signal cancellation (DSC).
- Filter-based techniques, usually low-pass (LPF) or Notch filters.
- Gradient descent method (GDM)
- Schemes with SOGI-QSG.

Considering the previous techniques, sequence decomposition schemes can be implemented using them.

In the case of DSC, it is based on operating with the voltage vector ($v_{s_{\alpha\beta}}$) and the delayed version—one fourth of the fundamental frequency period ($T_g = 2\pi/\omega_g$)—in such a way that only the positively/negatively rotating vector remains [10]. However, any sudden change would take this delay time to be noticed, limiting its speed response. The technique based on DSC can also be used to filter out the harmonic content [60].

If the grid voltage vector is transformed to the SyRF, the positive/negative sequence component appear in the negative/positive SyRF as a ripple at twice the fundamental frequency. Therefore, a filter can be placed to suppress it, achieving sequence decomposition. Large variety of filters can be used for this purpose: band-stop, notch and low-pass, among others. However, the authors of [10] conclude that the transient of filter-based approaches are much slower and less accurate than those based on DSC.

Alternatively, [17] uses the GDM, although its settling time of 50 ms is much larger than the one obtained with DSC, which makes it less appealing for sequence decomposition exclusively.

SOGI-QSG schemes, which can be considered a particular type of filtering technique, are also a feasible option [33]. They are based on a similar principle to DSC-based techniques, where an operation with the filtered and quadrature outputs results in the positive or negative sequence. More complex schemes, such as the Dual SOGI-QSG (DSOGI-QSG), stands out for its robustness and fast transient compared with other filter-based approaches.

To depict the different properties, Fig. 8 shows a comparative between the techniques DSC, GDM, LPF, SOGI-based, and Notch filter for negative sequence extraction. The parameters for GDM are selected according to the guidelines provided in [17], the first-order LPF is tuned at 10 Hz and the notch filter is tuned with $r = 0.5$ as shown in [10]. The Notch filter gives the fastest response at the cost of a considerable overshoot, followed by DSC with a transient time of its delay time $T_g/4$, and SOGI-QSG that takes a similar amount of time. The remaining solutions—LPF and GDM—are much slower or inaccurate at steady state, thus they are not recommended for sequence decomposition. Note that the GDM presented

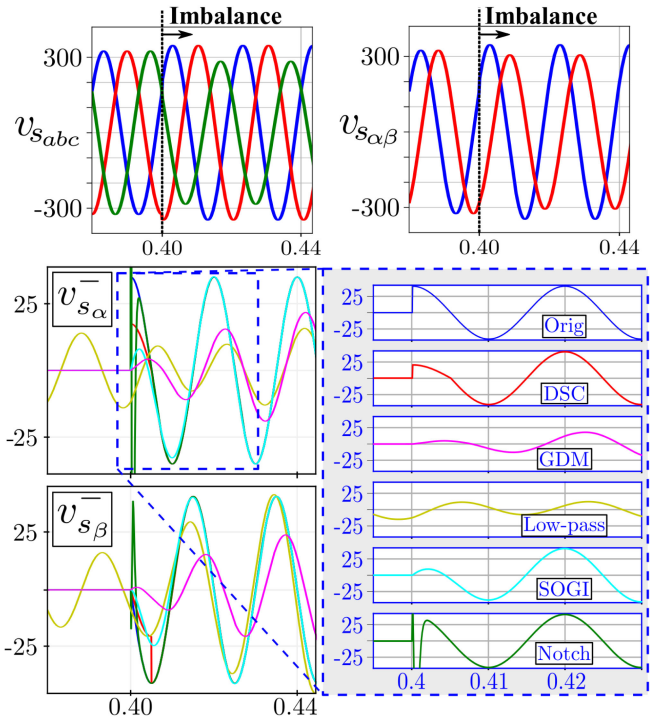

FIGURE 8. Sequence decomposition techniques. Negative sequence detection response to sudden grid voltage imbalance at $t = 0.4\,s$.

in [17] was intended to be used as a FLL, and thus it is not optimized for this purpose.

B. CURRENT REFERENCE GENERATION

The current reference generation stage determines which general objectives are aimed, however some of them may not be accomplished simultaneously. The common objectives seen in the literature are:

- Voltage support: The interaction of the current with the line and filter impedance contributes to compensate deviations from the nominal voltage conditions at the PCC.
- Balanced current injection: The references are computed in such a way that they transfer the desired power but using only the positive sequence.
- Power ripple attenuation: The current references achieve active power ripple attenuation, reactive power ripple attenuation, or both at the cost of injecting unbalanced currents.

Note that a SyRF can be defined for each sequence, and thus, the current references can be computed in its corresponding SyRF as dc signals: i_d^{+*}, i_q^{+*}, i_d^{-*} and i_q^{-*}. The transformation to StRF can be performed as follows

$$i^*_{\alpha\beta} = \underbrace{R(\theta_g) i^{+*}_{dq}}_{i^{+*}_{\alpha\beta}} + \underbrace{R(-\theta_g) i^{-*}_{dq}}_{i^{-*}_{\alpha\beta}}, \tag{17}$$

$$R(\theta_g) = \begin{bmatrix} \cos(\theta_g) & -\sin(\theta_g) \\ \sin(\theta_g) & \cos(\theta_g) \end{bmatrix} \tag{18}$$

where $R(\theta)$ is the rotation matrix. In the following, some approaches found in the literature to achieve the stated objectives are exhibited.

1) VOLTAGE SUPPORT

With this objective, it is expected that the currents cause a voltage drop by the interaction with the line impedance achieving a compensation of the unbalanced grid voltages at the PCC. One technique, presented in [26], uses the knowledge of the line and filter impedance to achieve such compensation. Given a reference for the active (p^*) and reactive power (q^*), and the value of the sequences component of the grid voltage in StRF ($v^+_{s_\alpha}$, $v^+_{s_\beta}$, $v^-_{s_\alpha}$, $v^-_{s_\beta}$), the references can be computed in StRF as follows

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix}_P = \frac{1}{V_k^+ + r_R V_k^-} \begin{bmatrix} k^+ v^+_{s_\alpha} + r_R k^- v^-_{s_\alpha} \\ k^+ v^+_{s_\beta} + r_R k^- v^-_{s_\beta} \end{bmatrix} p^* \tag{19}$$

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix}_Q = \frac{1}{V_k^+ + r_X V_k^-} \begin{bmatrix} -k^+ v^+_{s_\beta} - r_X k^- v^-_{s_\beta} \\ k^+ v^+_{s_\alpha} + r_X k^- v^-_{s_\alpha} \end{bmatrix} q^* \tag{20}$$

$$V_k^+ = k^+ (v^{+\,2}_{s_\alpha} + v^{+\,2}_{s_\beta});\; V_k^- = k^- (v^{-\,2}_{s_\alpha} + v^{-\,2}_{s_\beta})$$

$$r_R = \frac{\mathrm{Re}(Z_t) + R}{||Z_t + R + L||};\; r_X = \frac{\mathrm{Im}(Z_t) + L}{||Z_t + R + L||}$$

$$\begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix} = \begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix}_P + \begin{bmatrix} i^*_\alpha \\ i^*_\beta \end{bmatrix}_Q;\quad k^+ + k^- = 1, \tag{21}$$

where r_R and r_X are respectively the normalized line and filter impedance between the VSC and the considered PCC; operator $||x|| = \sqrt{\mathrm{Re}(x)^2 + \mathrm{Im}(x)^2}$ provides the module of x; parameters k^+ and k^- are tuning parameters; and variables V_k^+ and V_k^- are the quadratic amplitudes of the positive and negative sequence of the grid voltage scaled by parameters k^+, k^-, respectively. By means of k^+, a trade-off between voltage support (values of k^+ close to zero) and balanced current injection (values of k^+ close to one) is given. In other words, parameters k^+ and k^- balance which sequence of the grid voltage to use to transport the active and reactive power. Consequently, voltage support comes at the expenses of unbalanced phase currents and larger active and reactive power ripple.

Another technique, given in [22], is based on the dynamics of an LC filter, which implements a control loop to regulate the positive voltage at the PCC towards its nominal value. However, it requires grid voltage sequence decomposition and notch filters to eliminate coupling terms, increasing its complexity and slowing its transient response.

2) POWER RIPPLE ATTENUATION

These schemes aim to reduce the power ripple caused by the presence of negative sequence in the voltage grid. [23] proposes to compute the references in such a way that active and reactive power ripple are rejected simultaneously. However, the obtained references include negative sequence, and some

low-order harmonics which, apart from requiring the CC to be able to track such frequencies, might be unfeasible for the current harmonic injection limits established by the grid codes.

Alternatively, active or reactive power ripple suppression may be aimed individually. In this line, [24], [28], [30] use a current reference generation approach in SyRF with a tuning parameter K that considers this trade-off as follows

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}_P = \frac{1}{V_{dq}^+ - KV_{dq}^-} \left(\begin{bmatrix} v_{s_d}^+ \\ v_{s_q}^+ \end{bmatrix} - KR(-2\theta_g) \begin{bmatrix} v_{s_d}^- \\ v_{s_q}^- \end{bmatrix} \right) p^* \quad (22)$$

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}_Q = \frac{1}{V_{dq}^+ + KV_{dq}^-} \left(\begin{bmatrix} -v_{s_q}^+ \\ v_{s_d}^+ \end{bmatrix} + KR(-2\theta_g) \begin{bmatrix} -v_{s_q}^- \\ v_{s_d}^- \end{bmatrix} \right) q^* \quad (23)$$

$$V_{dq}^+ = v_{s_d}^{+2} + v_{s_q}^{+2}; \; V_{dq}^- = v_{s_d}^{-2} + v_{s_q}^{-2}$$

$$\begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix} = \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}_P + \begin{bmatrix} i_d^* \\ i_q^* \end{bmatrix}_Q, \quad (24)$$

where $v_{s_d}^+$, $v_{s_q}^+$, $v_{s_d}^-$, $v_{s_q}^-$ are the positive and negative sequence components of the grid voltage in SyRF; V_{dq}^+ and V_{dq}^- are their quadratic amplitudes, respectively; and $R(-2\theta_g)$ is the rotation matrix that translates the components from the negative SyRF to the positive SyRF. Depending on the tuning parameter K, different objectives may be aimed

- $K = 0$ yields only positive balanced current references and no power ripple attenuation.
- $K = -1$ results in no reactive power ripple.
- $K = 1$ results in no active power ripple.

Notice that hybrid solutions can be adopted by selecting $K \in [-1, 1]$. In this regard, [25] proposes a particle swarm optimization to obtain the value of K aiming to reduce the reactive ripple as much as possible, while fulfilling a predefined maximum active power ripple.

Work [7] presents a similar approach by means of the susceptance ($b^{\pm}$) and conductance ($g^{\pm}$) for each sequence

$$i_{dq_P}^{+*} = g^+ v_{s_{dq}}^+ \quad (25)$$

$$i_{dq_P}^{-*} = g^- v_{s_{dq}}^- \quad (26)$$

$$i_{dq_Q}^{+*} = -Jb^+ v_{s_{dq}}^+ \quad (27)$$

$$i_{dq_Q}^{-*} = -Jb^- v_{s_{dq}}^-, \quad (28)$$

where J is the 90° rotation matrix. Parameters g^+, g^-, b^+, b^- are computed and related between them in [7] resulting in a similar trade-off than the previous technique.

3) BALANCED CURRENT INJECTION

This objective is considered in the previous approaches for a particular value of the corresponding tuning parameter. Accordingly, either $k^+ = 1$ in (19)–(21) or $K = 0$ in (22)–(24) would aim for balanced currents. Similarly, making the negative susceptance and conductance equal to zero in (26)–(28) would have the same result. In other words, the references have only positive sequence and only the positive sequence of the grid voltage is considered to achieve the desired active and reactive power. In this line, a droop controller would keep the currents balanced while aiming for grid voltage and frequency support by modifying the references of active and reactive power [38].

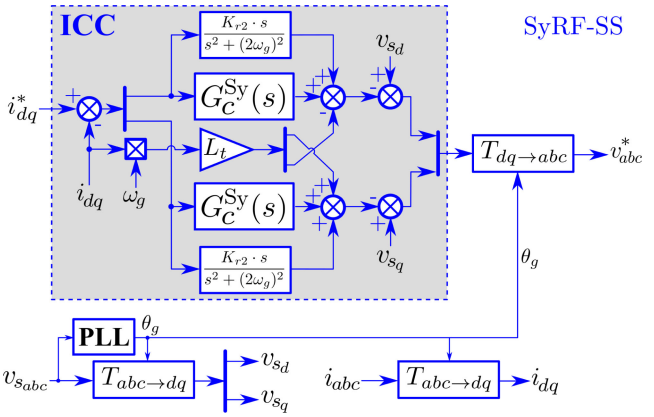

FIGURE 9. SyRF-SS scheme extracted from [48] where a resonant term is used for the negative sequence tracking.

IV. CCS UNDER UNBALANCED GRID VOLTAGE CONDITIONS

In this section different CCs that have negative sequence tracking capabilities are exposed. The two most common approaches for balanced grid operation were presented previously, however, when the current references have positive and negative sequence components, both sequences have to be tracked, which may require some modifications. The following CCs are classified according to the controller that provides this capability: resonant or integral.

A. PR-BASED ICC

The transfer function of the nonideal PR controller was shown in (8), whose digital implementation based on the delta operator can be extracted from [23]. Some papers exhibit that the resonant term is equivalent to an integrator for the components at frequencies ω_g and $-\omega_g$ [46]. Thus, it is expected to achieve tracking capabilities at $\pm\omega_g$ with the only requirement of proper ω_g obtention. The nonideal PR widens the bandwidth around $\pm\omega_g$ and makes the gain noninfinite, which increases the robustness of the closed-loop scheme. This paper considers two control schemes that uses resonant terms for ICC under unbalanced grid voltage conditions.

1) The non-ideal PR in StRF (PR) [46] depicted in Fig. 4.
2) A resonant term added to the standard PI in SyRF, whose resonant frequency is twice the fundamental one. Given that only one SyRF is used, this scheme is referred as SyRF single stage (SyRF-SS) [48], and it is depicted in Fig. 9.

The first approach achieves negative sequence tracking thanks to the resonant term in StRF. The second one achieves

the same by tracking the component at twice the fundamental in the positive SyRF by means of a resonant term. In both schemes, no decoupling network between sequences or sequence decomposition are employed.

B. PI-BASED ICC

As exhibited in previous sections, once the currents are expressed in SyRF, a PI controller can achieve proper tracking of the references that appear as DC variables. However, the negative sequence appears in the positive SyRF as a component at $2\omega_g$, as it can be noted in (22)–(23). Consequently, this scheme alone does not guarantee zero steady-state error for the negative sequence.

One solution is the use of the dual SyRF (DSRF), where one positive ($+\omega_g$) and negative ($-\omega_g$) SyRF are used simultaneously. Therefore, a PI controller for each sequence (dq^+ and dq^- for the positive and negative sequence, respectively) in its corresponding SyRF can be used [43]. However, when the currents are transformed to the SyRF of one sequence, the components of the opposite one appear as AC variables, degrading the PI performance. As a workaround, several proposals look for a scheme that neglects the presence of the opposite sequence in the corresponding SyRF. Some that are present in the literature are

1) Use of a decoupling network (DN) between the two SyRF to eliminate the other sequence presence whether in the forward path of the ICC (DSRF-DNF) [27] or in the references (DSRF-DNR) [28]. In the case of DSRF-DNF, the formulation of the current that inputs the CC is as follows

$$i_{dq}^{+\prime} = i_{dq}^{+} - R(-2\theta_g)\mathrm{LPF}(i_{dq}^{-\prime}) \tag{29}$$

$$i_{dq}^{-\prime} = i_{dq}^{-} - R(2\theta_g)\mathrm{LPF}(i_{dq}^{+\prime}), \tag{30}$$

where a low-pass filter have been used to obtain the uncoupled currents $i_{dq}^{\pm\prime}$. Alternatively, In the case of DSRF-DNR, the formulation of the current references that inputs the CC is as follows

$$i_{dq}^{+*\prime} = i_{dq}^{+*} + R(-2\theta_g)i_{dq}^{-*} \tag{31}$$

$$i_{dq}^{-*\prime} = i_{dq}^{-*} + R(2\theta_g)i_{dq}^{+*}, \tag{32}$$

where $i_{dq}^{\pm*\prime}$ is the used current references.

2) Use a current sequence decomposition stage prior to the ICC (DSRF-SD). For this, the DSC technique can be used in the negative SyRF to isolate the negative sequence components [82]. With this, the negative sequence can be properly tracked with a PI controller, whereas the PI controller in the positive SyRF is tuned to track the positive sequence.

The schemes of the considered DSRF-DNF, DSRF-DNR and DSRF-SD are depicted in Fig. 10, Fig. 11 and Fig. 12, respectively.

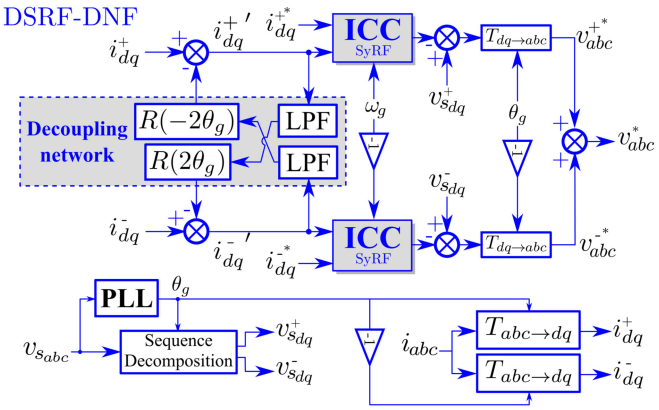

FIGURE 10. DSRF-DNF scheme extracted from [27] where a decoupling network is used in the forward path of the ICC.

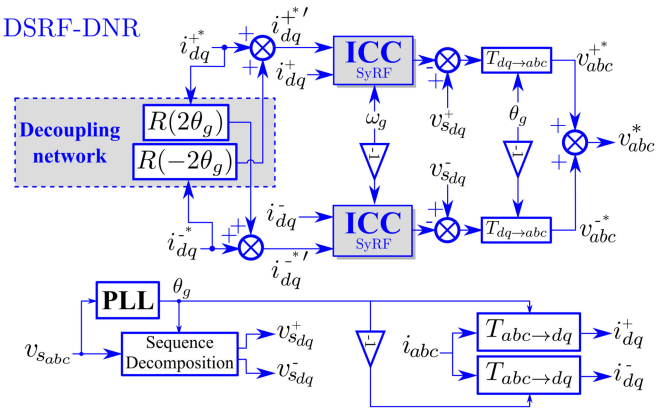

FIGURE 11. DSRF-DNR scheme extracted from [28] where a decoupling network is used in the reference computation.

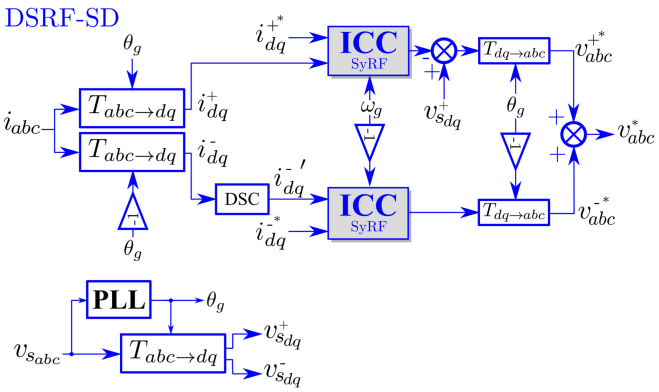

FIGURE 12. DSRF-SD scheme extracted from [82] where the DSC technique is used as sequence decomposition in the negative SyRF.

Alternatively, other current control approaches can be applied, such as the one presented in [83], complex-coefficient-based controller [84] in the *abc* reference frame, PI plus resonant in a direct power control scheme [85], etc. There

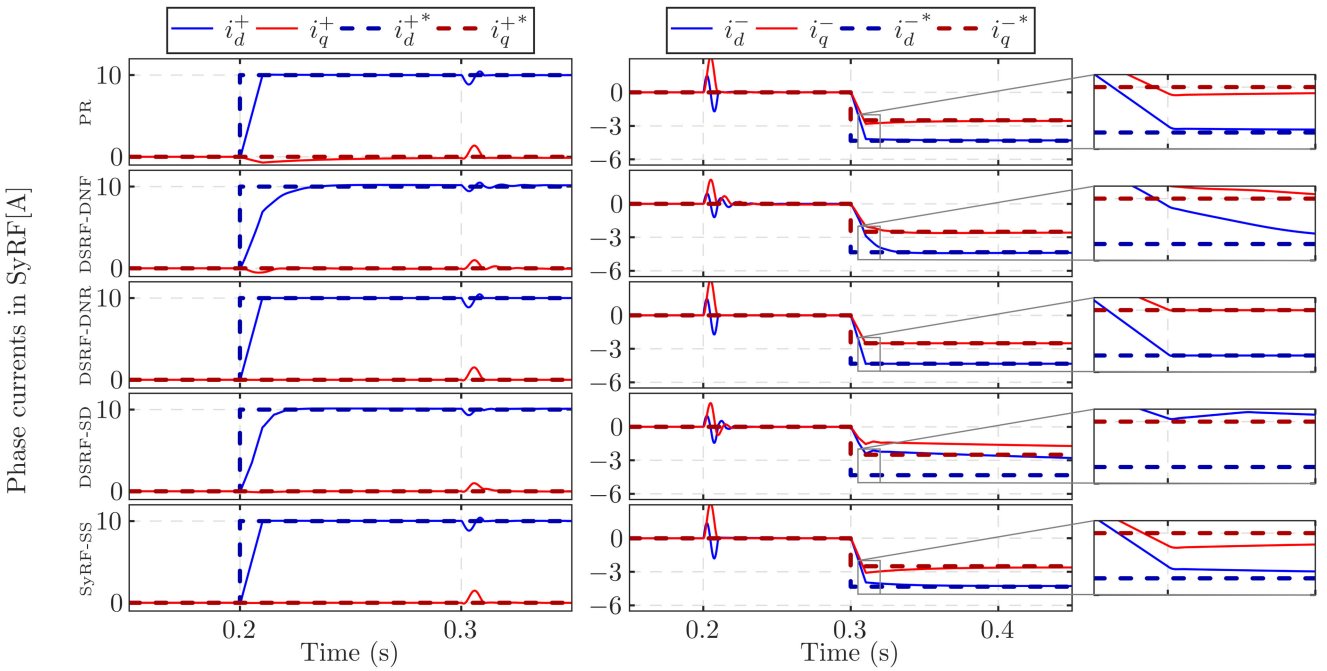

FIGURE 13. **Simulation: Phase current evolution for each considered approach in the positive and negative SyRF under steps in the references. The depicted currents have gone through a MAF of 100 Hz to achieve current sequence decomposition.**

TABLE I **Control Parameters and Test Values**

Parameter	Value	Parameter	Value
Switching freq., f_{sw}	10 kHz	Inductance, L_t	2 mH
Line Resistance, R_t	0.01 Ω	Grid freq., ω_g	$2\pi 50$ rad/s
Prop. term, k_p	7.88	Integ. term, k_i	39.4
Ph. marg. res., PM^*_{res}	40°	Res. term, k_r	90
Ph. marg. f_{bw}, PM^*_{bw}	60°	cut-off PR, ω_f	5 rad/s
DSRF-DNF LPF freq.,	$\frac{\omega_g}{\sqrt{2}}$ rad/s		

exist other controllers based on finite control sets, optimizations, hybrid formulation, etc. that do not require a modulation stage. However, this paper focuses on linear current controllers with modulation stages, and thus they are not exhibited here.

V. SIMULATION RESULTS

In this section, the five CCs exposed in the previous section are compared in terms of tracking during transient. Note that the main issue for CC regarding unbalanced conditions is the tracking of the negative sequence current references. The considered CC schemes are the following ones

1) PR: Proportional-resonant in StRF.
2) SyRF-SS: PI and resonant term in SyRF.
3) DSRF-DNF: Dual PI in SyRF with decoupling network in the measured currents.
4) DSRF-DNR: Dual PI in SyRF with decoupling network in the references.
5) DSRF-SD: Dual PI in SyRF with DSC as sequence decomposition in the negative SyRF.

In this simulations, the model of the system (6)–(7), also shown in Fig. 2, is considered, whose parameters are shown in Table 1. The tuning of the proportional control parameter (k_p) have been performed in such a way that $\text{PM}^*_{\text{bw}} = 60°$ with a bandwidth frequency of 555.5 Hz. Variable ω_f of the non-ideal resonant controllers (ω_f) is 5 rd/s and the resonant control parameter (k_r) fulfills $\text{PM}^*_{\text{res}} = 40°$.

The simulation consists in an step from 0 to 10 A at $t = 0.2$ s in i_d^{+*} followed by two simultaneous steps in the negative sequence components at $t = 0.3$ s of -2.9 A and -4.3 A in i_d^{-*} and i_q^{-*}, respectively. For the sake of clarity, the phase currents in dq^+ and dq^- during this jump are exhibited in Fig. 13 where each current are filtered with a moving average filter (MAF) of 100 Hz. As it can be seen, both sequences are tracked with every approach, but some differences can be noticed. Defining the rise time t_r as the time that the slowest current component (d or q) takes to reach the 67% of its reference, and the settling time $t_{s_{95}}$ as the same indicator but with the 95% of its reference, some comparisons can be made. Regarding the positive sequence tracking

- PR, DSRF-DNR and SyRF-SS have similar response in terms of rise and settling time.
- DSRF-DNF and DSRF-SD have a slower response than the previous ones, being DSRF-DNF the slowest one. This is due to the slow dynamic the decoupling technique of these approaches has, as it does not contribute as fast as the previous ones to restore the perturbance seen in the negative sequence frame.

Nevertheless, the differences in the positive sequence tracking are small due to the fact that they were tuned to have similar control bandwidths, and hence similar response to changes. One could boost the response of one particular control scheme by increasing its bandwidth, but this would come at the cost

TABLE II Comparative Simulation Results

Approach	t_r (ms)	$t_{s_{95}}$ (ms)	$\text{SSE}^{\max}$ (%)
PR	7.2	49.0	2.07
DSRF-DNF	10.5	24.9	1.98
DSRF-DNR	6.8	9.6	0.07
DSRF-SD	179.9	944.6	0.60
SyRF-SS	7.6	106.3	4.00

of decreasing phase margin, and thus increasing possible overshoots and getting the system closer to unstability. In terms of the negative sequence tracking

- DSRF-SD is the one that takes more time to reach the steady-state conditions. This is due to the DSC being in the forward path of the currents whose dynamic slows down the one of the closed loop. Faster sequence decomposition schemes may be used, but their bandwidth should be kept away from the ICC one, otherwise the closed-loop behaviour may be unstable (see Notch filter overshoot in Fig. 8). In summary, some works [28] do not recommended to use sequence decomposition stages in the forward path of the IC.
- SyRF-SS follows the previous one in terms of largest settling time. However, it is among the three with the fastest rising time, which may make it feasible for applications that requires fast grid-fault overrides. Besides, the settling time can be reduced by means of readjusting the integral term k_i.
- DSRF-DNF has larger rising time, but it reaches the steady-state faster. This is due to the dynamics of the low-pass filter used as decoupling network, that determine when the currents are uncoupled. For this, there is a trade-off between transient time and uncoupling effect, as faster filters have poorer ripple rejection. Higher-order or other type of filters may be considered, but resonant frequencies have to be taken into account, as they may introduce harmonics in the uncoupling terms, and thus in the ICC.
- PR has a faster transient than the previous ones, but larger settling time than DSRF-DNF. Larger values of k_r would reduce this time at the cost of reducing the phase margin PM_{res}, which might affect the overshoot during transients.
- DSRF-DNR have the fastest transient, reaching steady-state conditions in less than half a period. However, the robustness of such approach has still to be tested in a real application.

Given that the MAF is employed to filter each sequence, the changes that happens faster than 0.01 s can not be properly seen. For this, the phase current responses are also depicted without MAF in Fig. 14 where similar conclusions can be derived in terms of positive and negative tracking.

The results from simulation of the negative sequence tracking are summarized in Table 2, where the following parameters have been measured: the rise time t_r, the settling time, and the maximum steady-state error $\text{SSE}^{\max}$ in % of steady-state

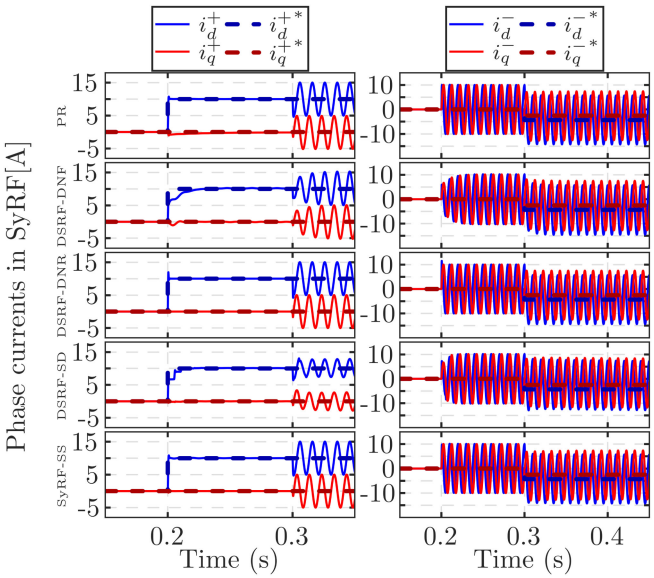

FIGURE 14. Simulation: Phase current evolution without using MAF.

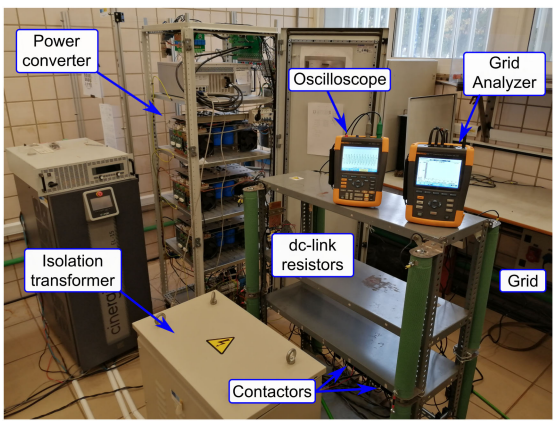

FIGURE 15. Experimental setup.

value as follows

$$\text{SSE}^{\max} = \max\left(\frac{i_{dq}^{-*} - i_{dq}^{-}}{i_{dq}^{-*}}\right) \cdot 100 \tag{33}$$

VI. EXPERIMENTAL COMPARISON

Following the same idea of the previous section, some experimental tests have been carried out to compare the considered current controllers. The same techniques of the previous section are considered, with the same control parameters and same nomenclature. The experimental setup used to carry out the experiments is shown in Fig. 15.

The system is working as a rectifier with the power flowing from the grid to a resistor connected to the dc-link. The dc-link voltage reference v_{dc}^{*} is set to 750 V and the resistor has a value of 60 Ω. The references for the positive sequence are obtained from the outer control loop, that fixes unity power

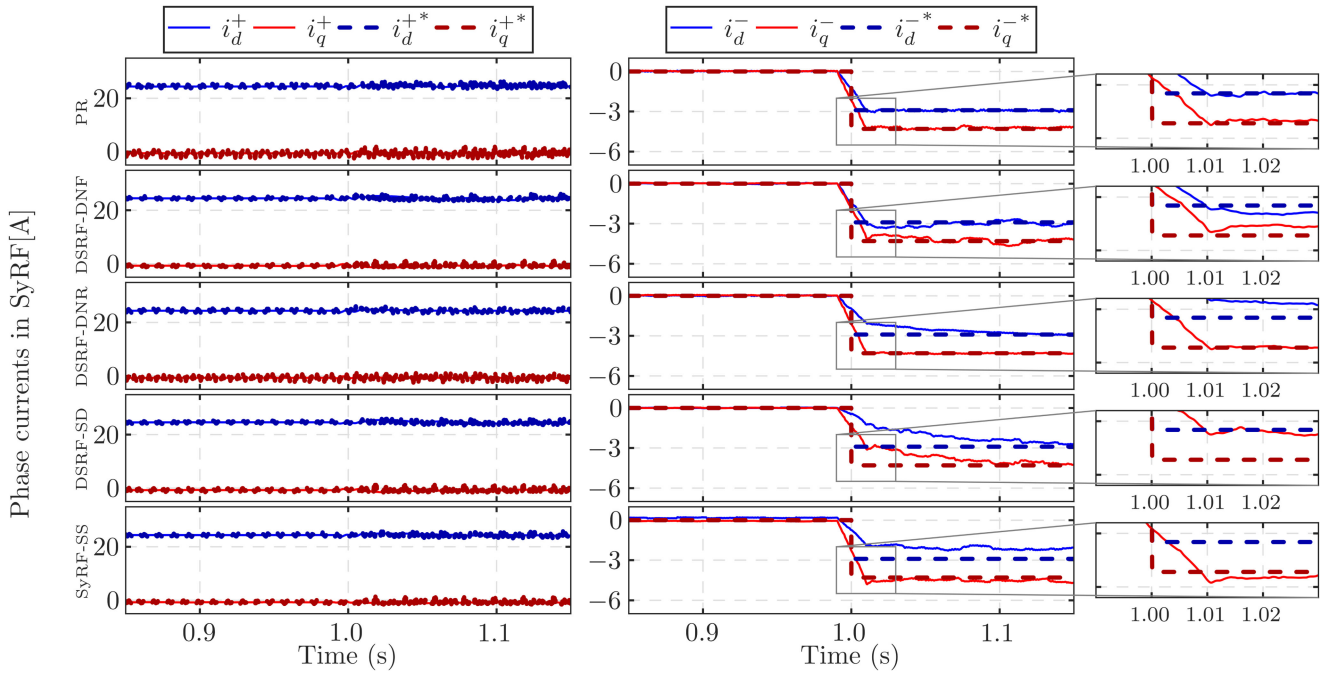

FIGURE 16. Experiment: Phase current evolution for each considered approach in the positive and negative SyRF during the carried-out experiment. The depicted currents have gone through a MAF of 100 Hz to achieve current sequence decomposition.

TABLE III Current References in *dq* for the Experimental Test

Reference	Value	Reference	Value
i_d^{+*}	24.7 A	i_q^{+*}	-0.6 A
i_d^{-*}	$0 \rightarrow$ -2.9 A	i_q^{-*}	$0 \rightarrow$ -4.3 A

factor and compute p^* in such a way that v_{dc} tracks its reference. The references for the negative sequence follows a change at $t = 1$ s equal to that carried out in simulations. These references are summarized in Table 3. From this, the behaviour of the current controllers in terms of negative sequence tracking can be evaluated and compared among them.

All controllers have been implemented using the Tustin's method for discretization, while the resonant term has been implemented using the delta operator [23]. The used PLL scheme for the experiments is based on the DSRF-PLL one [57], where the grid voltage measurements follow some transformations based on DSC to eliminate low-order harmonics [18] prior to input the PLL.

Fig. 16 shows the responses of the phase currents of both sequences in their corresponding synchronous reference frame, using a MAF at 100 Hz to eliminate the opposite sequence presence. The same phase currents without the MAF are shown in Fig. 17. Lastly, the phase currents in *abc* are shown in Fig. 18 where the introduction of the negative sequence at $t = 1$ s can be noticed.

As it was expected, and similarly to the simulation results, every approach has negative sequence tracking capabilities but with some differences. For this, the same performance indicators that were used in the simulation section are computed here and shown in Table 4: rise time (t_r), settling time ($t_{s_{95}}$),

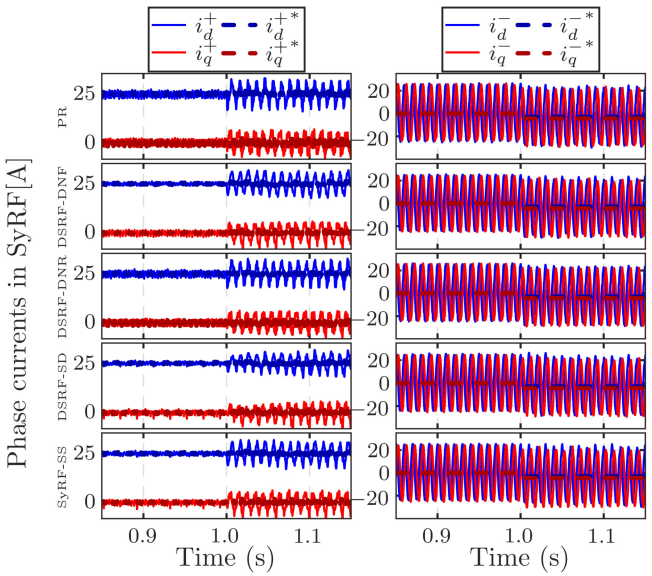

FIGURE 17. Experiment: Phase current evolution without using MAF.

and maximum steady-state error ($\text{SSE}^{\max}$). Focusing on the negative sequence tracking

- DSRF-SD offers the slowest transient, but it reaches practical zero steady-state error—see value of $t_{s_{95}}$ and $\text{SSE}^{\max}$ in Table 4. Similarly to simulations, the former is caused by the bandwidth of MAF that limits the speed of the controller response.
- SyRF-SS improves considerably in terms of rising time, but it has a large steady-state error in the negative

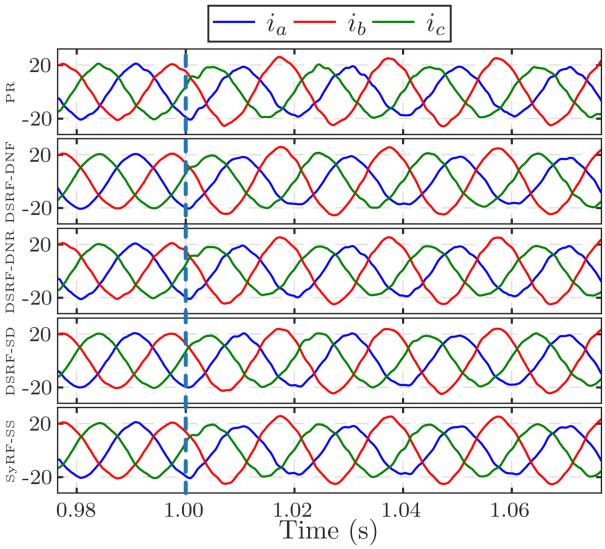

FIGURE 18. Experiment: Phase current evolution in *abc* without using MAF.

TABLE IV Comparative Experimental Results

Approach	t_r (ms)	$t_{s_{95}}$ (ms)	$\text{SSE}^{\max}$ (%)
PR	4.6	9.2	0.91
DSRF-DNF	5.7	55.5	0.78
DSRF-DNR	9.4	95.2	1.92
DSRF-SD	53.5	175.6	0.93
SyRF-SS	13.7	∞	37.65

sequence tracking. This error may be caused by a deviation between the tuned resonant frequency and the frequency of the ripple caused by the negative sequence in the positive SyRF—ideally, both should be 100 Hz. As a result, the controller gain at the resonant frequency is not high enough, which requires to reconsider the controller parameters or a more accurate tuning of the resonant frequency.

- DSRF-DNR follows in terms of rising and settling time, achieving zero steady-state error from a practical perspective. As it can be seen, the main difference with the simulations is in the settling time, which is considerably larger for the experiments. However, the behaviour is still satisfactory.
- DSRF-DNF has the second best results with similar values than those obtained from simulation.
- PR, in these experiments, offers the best results, with a more robust integration thanks to the delta operator and the non-ideal resonant controller scheme.

Note that carrying out experiments involve implementing other schemes that are not considered in the simulation section, such as outer control loop, dead-times, system parameter uncertainties, etc. The main difference exhibited in these results, when compared to the simulation ones, is that the outstanding approach is the PR one. This fact could be derived from using the delta operator for the discretization stage that achieves better results when compared with the standard shift operator—used for the integral terms in the PI controllers—, as it is stated in [86]. Additionally, the PR approach is implemented in StRF, which avoids relying on the PLL performance and achieves a more robust implementation.

VII. CONCLUSION

This paper covers some basics and foundations of grid-connected VSC when operating under unbalanced grid conditions. The basic formulation of unbalanced grid conditions, the effects on the system performance, and some techniques to diagnose it are exposed. Later on, some phase current-related aspects are mentioned, such as current reference generation techniques that fulfill different objectives, the two typical reference frames, and the scheme and tuning of some current controllers used under these conditions. Additionally, some PLL and FLL schemes that takes this unbalance state into account are cited. Lastly, five published current controllers are exhibited, and simulation and experimental results are carried out with each of them for comparison purposes. Simulations are based on continuous transfer functions, exhibiting the ideal response of the CC. On the contrary, experiments suffers from additional aspects, such as discretization, dead-time implementation, parameter uncertainties, etc. offering a more complete view of the CC responses. We expect this paper to provide an insight on how to deal with unbalanced grids, specially from the current control perspective.

According to the experimental results, the proportional-resonant controller is still highlighted as the most outstanding approach due to its robust and easy implementation thanks to its nonideal version and the delta operator. Besides, it is an approach that does not depend on a grid-synchronization scheme, which makes it more robust and less dependant on the tuning of other schemes.

Taking the simulations into account, among the four approaches that are established in SyRF, the DSRF-DNR is remarked for its easiness of implementation and satisfactory response. It is worth mentioning that this approach requires neither a sequence separation stage nor any LPF. The decoupling is properly achieved at the current reference generation stage, so the PI controllers can be tuned to maximize the speed of their response. The different results given for this approach in simulation and experiments (especially for the settling time) suggest the impact the grid synchronization scheme may have in a real system, as the simulation does not consider this effect in the closed loop.

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