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Super-Gain-Boosted AB-AB Fully Differential Miller Op-Amp With 156dB Open-Loop Gain and 174MV/V MHZ pF/μW Figure of Merit in 130nm CMOS Technology

ANINDITA PAUL[1], (Member, IEEE), JAIME RAMÍREZ-ANGULO[2,3], (Life Fellow, IEEE), ALEJANDRO DÍAZ SÁNCHEZ[3], (Member, IEEE), ANTONIO J. LÓPEZ-MARTÍN[4], (Senior Member, IEEE), RAMON GONZALEZ CARVAJAL[5], (Fellow, IEEE), AND FRANK X. LI[1], (Member, IEEE)

[1]Rayen School of Engineering, Youngstown State University, Youngstown, OH 44555, USA
[2]Klipsch School of Electrical and Computer Engineering, New Mexico State University, Las Cruces, NM 18003, USA
[3]Department of Electronics, National Institute of Astrophysics, Optics and Electronics, Puebla 72000, Mexico
[4]Institute of Smart Cities, Public University of Navarra, 31006 Pamplona, Spain
[5]Department of Electronic Engineering, University of Seville, 41092 Sevilla, Spain

Corresponding author: Anindita Paul (apaul@ysu.edu)

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ABSTRACT A fully differential Miller op-amp with a composite input stage using resistive local common-mode feedback and regulated cascode transistors is presented here. High gain pseudo-differential auxiliary amplifiers are used to implement the regulated cascode transistors in order to boost the output impedance of the composite input stage and the open-loop gain of the op-amp. Both input and output stages operate in class AB mode. The proposed op-amp has been simulated in a 130nm commercial CMOS process technology. It operates from a 1.2V supply and has a close to rail-to-rail differential output swing. It has 156dB DC open-loop gain and 63MHz gain-bandwidth product with a 30pF capacitive load. The op-amp has a DC open-loop gain figure of merit FOM_{AOLDC} of 174 (MV/V) MHz pF/μW and large-signal figure of merit FOM_{LS} of 3(V/μs) pF/μW.

INDEX TERMS Class-AB op-amp, fully differential amplifier, Miller-compensation, regulated cascode, resistive local common-mode feedback, voltage follower.

I. INTRODUCTION

Increasing demands for battery-operated portable electronics equipment like smartphones, wearable medical gadgets, and internet of things (IoT) devices drive the demand of IC's operating at low voltages and low power and in some applications with high speed. It is necessary to scale down device sizes and supply voltages to introduce more functionalities and reduce power dissipation. However, scaling down of device-size and supply voltage generate negative impacts on device performances. Due to the scaling down of CMOS technology, the intrinsic gain A_i of MOS transistors has decreased continuously [1]. For example, it is typically in the order of $A_i = g_m r_o$ ~20-30 V/V in 130nm CMOS technology. Here g_m is the transconductance gain and r_o is the output impedance of the MOS transistor. It can be shown that, as a first-order approximation, if transistors operate in strong inversion the intrinsic gain can be expressed by $A_i = 2/(\lambda V_{DSsat})$, where $V_{DSsat} = V_{GS}$-V_T is the drain-source saturation voltage and λ is the channel length modulation parameter (typically $\lambda \sim$ 0.3-0.5 V^{-1} in 130nm CMOS technology). In practice, the intrinsic gain is also strongly dependent on V_{DS}. Transistors with low V_{DS} have lower intrinsic gains. CMOS op-amps are indispensable for analog integrated circuits [2]–[4], such as, in switched-capacitor filters, delta-sigma modulators, A/D and D/A converters, etc. The op-amps should have a very high DC open-loop gain [5], high unity-gain frequency, high phase-margin, high slew-rate with low power dissipation to obtain high accuracy, speed, and fast settling time in a power-efficient manner.

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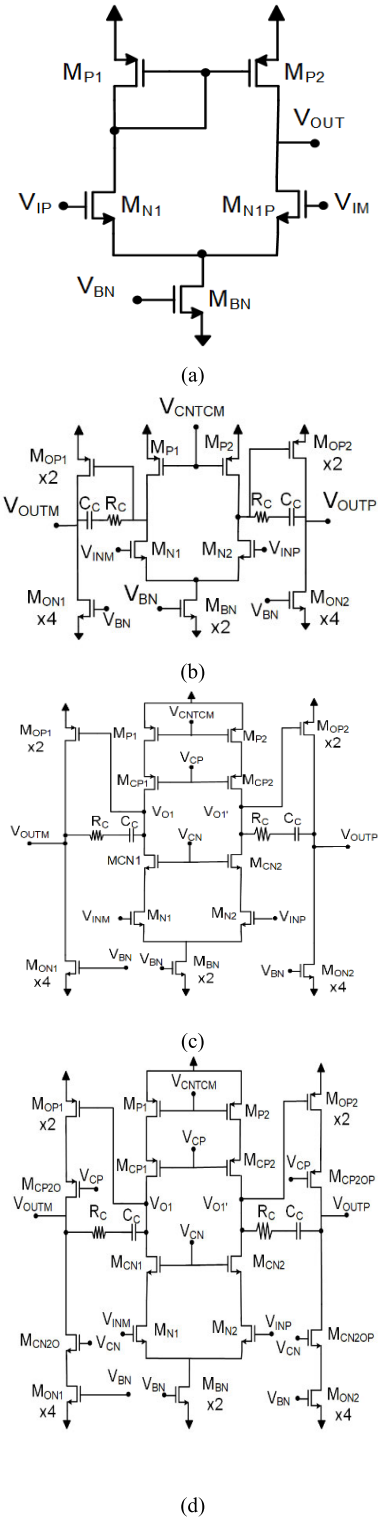

FIGURE 1. (a) Basic one-stage op-amp b) Conventional two-stage Miller op-amp c) Telescopic input two-stage Miller op-amp (d) Two-stage Miller op-amp with cascoded input/ output stages.

One-stage and two-stage (Miller) op-amps (Figures 1(a) and (b)) have been widely used for many years in various applications. They have a DC open-loop gain A_{OLDC} in the range of $(A_i/2) < A_{OLDC} < (A_i/2)^2$,

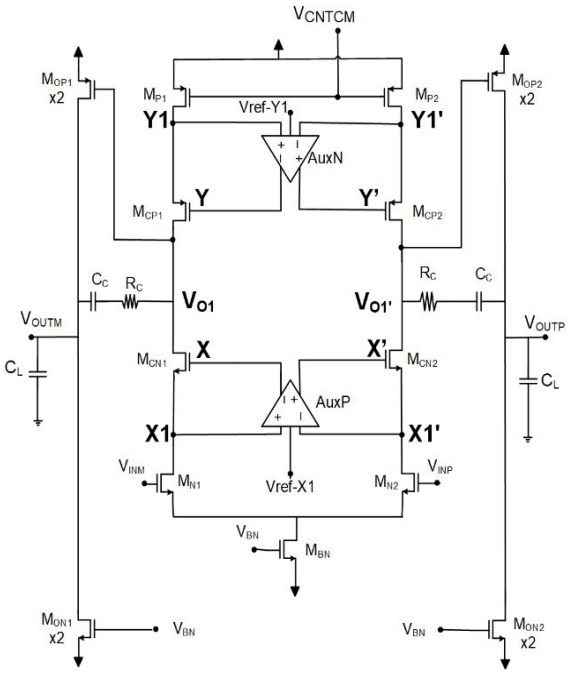

FIGURE 2. Gain boosted Miller op-amp using regulated cascode technique.

respectively. This gain is currently insufficient for most modern technology applications, especially for applications that require high accuracy and low distortion. It is possible to increase the Miller op-amp gain by a factor A_i using a telescopic input stage with cascode transistors in the input stage, as shown in Figure 1(c). These cascode transistors provide higher impedance at the internal nodes V_{o1}, V_{o1}', which increases the first stage's gain. They do not degrade output swing since internal nodes V_{o1} and V_{o1}' require only a small maximum swing $V_{ppo1,o1'} = V_{OUTM,P}/A_{II}$ of approximately $40mV_{pp}$, which corresponds to the rail-to-rail output swing divided by the gain A_{II} ~30 of the output stage.

The open-loop gain can be boosted by another factor A_i by using cascode transistors in the output stage, as shown in Figure 1(d). However, due to the scaling down of technology, reduced supply voltages prevent the usage of cascoding devices in the output stage since they severely limit the output swing and do not allow resistive output loading which is required in many applications. The only choice to achieve higher open-loop gain and high output swing with low supply voltages is the utilization of two-stage or multi-stage cascaded amplifiers. The latter require complex nested Miller compensation schemes [6]–[8] and are in practice limited (for stability reasons) to a maximum of three cascaded stages, which allows to achieve only a moderate high op-amp gain $A_{OLDC} \sim (A_i/2)^3$.

The telescopic input stage of an op-amp has a gain on the order of $(A_i)^2/2$. It is possible to further enhance the gain of the telescopic stage using regulated-cascode technique [9]. This technique enhances the effective gain of cascode transistors by the gain AuxP, AuxN of auxiliary amplifiers used

in a local negative feedback loop connected between the gate and source of the cascode transistors. Figure 2 shows an example of a fully differential Miller op-amp with a telescopic input stage that uses regulated-cascode transistors with auxiliary amplifiers AuxP, AuxN (assumed to have similar gains $A_{AuxP} = A_{AuxN} = A_{Aux}$). This increases the open-loop gain of the op-amp by the factor A_{Aux} to a value $A_{OLDC} \approx ((A_i)^3/4)A_{Aux}$. Other high gain approaches based on regulated cascode transistors have been reported in [10]–[12].

Given that [10], [11] are cascoded one stage op-amps, these have very limited output swing in modern technology (50% or less of V_{supply}). They cannot be loaded resistively since, in this case, their open-loop gains are severely degraded. As they are class A architectures, their slew rate is limited by the bias current. Therefore, they have very modest large-signal figures of merit like the current efficiency $CE = I_{outMax}/I_{totalQ}$ where I_{outMax} is the maximum output current, and I_{totalQ} is the total op-amp quiescent current.

In this paper, a power-efficient super-gain-boosted bandwidth enhanced fully differential class AB-AB Miller op-amp based on regulated cascode techniques with a DC open-loop gain $A_{OLDC} = (A_i^6/8)$ ($\sim$156dB *in 130nm CMOS technology)* is introduced. Very high gain pseudo-differential auxiliary amplifiers that do not require a common-mode feedback network are implemented using two novel single-ended folded double cascoded amplifiers in combination with a cascoded flipped voltage follower [13], [14] (CASFVF). The CASFVF operates as a DC floating voltage source that accurately sets the internal voltages X1, X1' and Y1, Y1' to convenient reference values V_{ref-X1} and V_{ref-Y1}, respectively. This warrants that all transistors operate in saturation with the constraint of the low supply voltage. The CASFVF also generates a floating very low impedance node, which serves as AC ground for the pseudo-differential auxiliary amplifiers, as explained in Section-II. The utilization of a Miller architecture allows close to rail-to-rail output swing and resistive loading with minimum degradation of the open-loop gain. The input and output stages operate in class AB mode. This increases the op-amp current efficiency and the large-signal figure of merit. The circuits are explained in detail in the following section. The op-amp's performances are measured using a) the conventional large-signal figure of merit $FOM_{LS} = (\mathrm{SR}.C_L)/P^Q$, b) the range figure of merit $FOM_R = V_{outPP}/V_{supply}$. Here P^Q is quiescent power dissipation, SR is the op-amp slew-rate, C_L is the load capacitance, V_{supply} is the supply voltage, and V_{outPP} is the output swing. The proposed op-amp's small-signal figure of merit is measured using a conventional measure defined by $FOM_{ss} = (GBW.C_L)/P^Q$. Two new figures of merit related to the op-amp open-loop gain are also used in this paper. They are a) an open-loop gain figure of merit $FOM_{AOLDC} = (A_{OLDC}.GBW.\ C_L)/P^Q$ and b) an area open-loop gain figure of merit $AFOM_{AOLDC} = (A_{OLDC}.GBW.\ C_L)/(Area.\ P^Q)$. Both take into account the open-loop DC gain A_{OLDC} of the op-amp which is not taken into account by other conventional figures of merit commonly used to measure the op-amp's performance. The second one also takes into account the Silicon area required to implement the op-amp.

The paper is organized as follows: Section-II describes the proposed op-amp designed in 130nm CMOS technology operating with $\pm$600mV dual supplies and with a bias current $I_B = 30\mu$A. Section-III presents the proposed and conventional op-amps' simulation results and comprehensive comparison with recently reported high gain op-amps. Post-layout simulations are shown in Section-IV. Section-V provides the conclusions.

II. AMPLIFIER ARCHITECTURE

A. TOPOLOGY OF PROPOSED OP-AMP

The proposed fully differential (FD) super-gain-boosted op-amp (SGB-OPAMP) has a composite class AB input stage and a class AB differential output stage. The composite input stage is formed by a first stage (M_{INL1}, M_{INL2}, M_{INP}, $M_{INM.}$, M_{TAIL}) that uses resistive local common-mode feedback RLCMFB [15], [16]. The RLCMFB in the first stage boosts the gain-bandwidth product (GBW) and the open-loop gain by approximately a factor 3 and provides class AB operation at the internal nodes V_{o1}, V_{o1}' at the output of the composite input stage. It does so by increasing the effective transconductance g_{meff} (by approximately the same factor 3) with respect to the transconductance g_{mIN} of the differential pair transistors and by generating signal currents in the cascoded branch or in the second stage (M_{N1}, M_{N2}, M_{CN1}, M_{CN2}, M_{P1}, M_{P2}, M_{CP1}, M_{CP2}), which can be higher (by approximately a factor of 6) than the bias current, as explained in Section II.B. This increases the slew rate at the output nodes $V_{o1,}$ V_{o1}' of the composite input stage. The second stage uses regulated cascode techniques to increase the gain of the cascode transistors M_{CN1}, M_{CN2}, $M_{CP1,}$ and M_{CP2} by the gain A_{Aux} of auxiliary amplifiers. The combination of the first and second stages (enclosed in a red box in Figure 3(a)) is denoted here as the ''composite input stage''. The third (output) stage provides moderate gain $\sim A_i/3$ and close to rail-to-rail output swing. It uses a non-cascoded push-pull power-efficient and very simple free class AB [15], [17] technique to provide very large and symmetrical positive and negative output currents without additional quiescent power dissipation. This increases the current efficiency of the op-amp and the bandwidth as well.

Two high gain pseudo-differential auxiliary amplifiers AuxN and AuxP are used to implement regulated cascode transistors M_{CP1}, $M_{CP2,}$ and M_{CN1}, M_{CN2}, in the second stage, respectively. The pseudo-differential auxiliary amplifiers with gains A_{AuxN} and A_{AuxP} consist of two single-ended folded double cascoded amplifiers in combination with a cascoded flipped voltage follower (CASFVF) [14]. This CASFVF acts as a DC ***floating voltage*** source to set the voltages at nodes Y_1, Y_1', X_1, X_1' of the second stage at convenient values V_{ref-Y1} and V_{ref-X1}. For simplicity, it is assumed that A_{AuxN} and A_{AuxP} have similar values, i.e., $A_{AuxN} = A_{AuxP} = A_{Aux}$. The auxiliary amplifiers enhance the output impedance

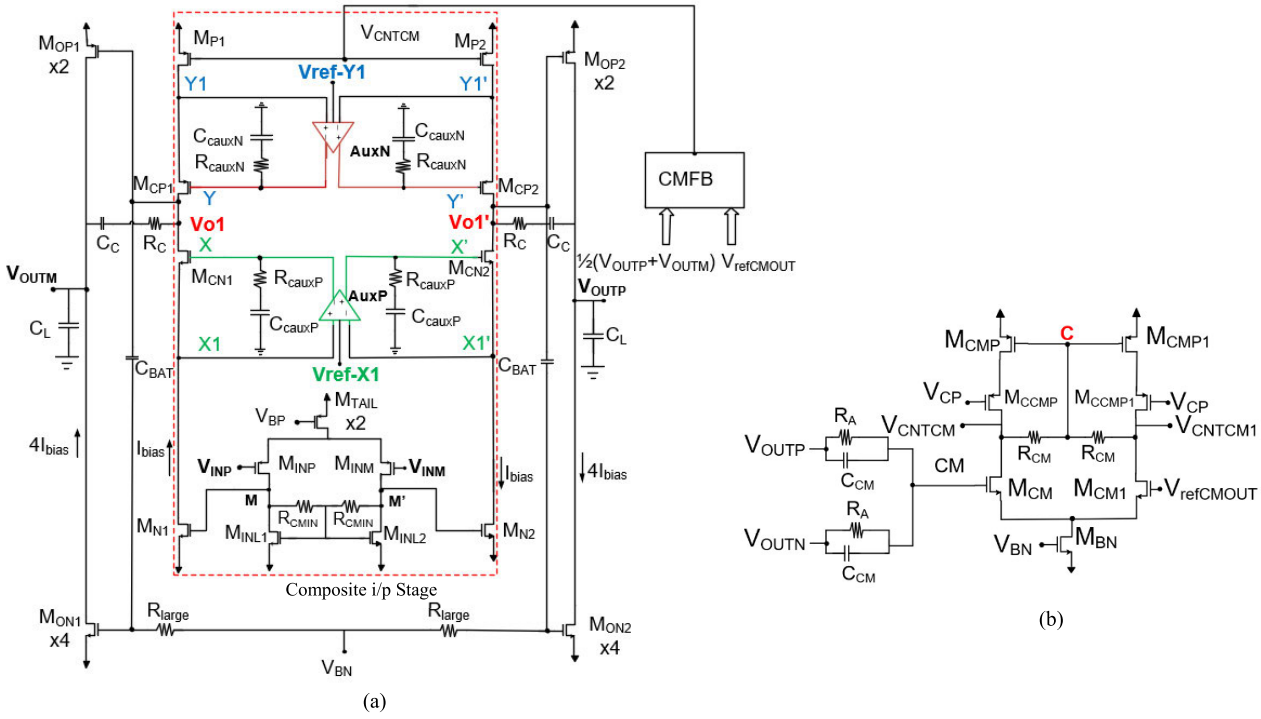

FIGURE 3. (a) Proposed topology of the gain boosted op-amp (b) GBW boosted common-mode feedback network.

(and open-loop DC gain of the op-amp) of the composite input stage at nodes $V_{o1}(V_{o1}')$ by a factor $A_{Aux} \sim A_i^3/4$. The voltages V_{ref-X1} and V_{ref-Y1} applied at the input terminals of the auxiliary amplifiers accurately set the values of the drain voltages of M_{N1}, M_{N2}, and M_{P1}, M_{P2}. This is very important in order to keep all transistors in saturation within the constraint of the low supply voltages used in modern technologies. Since the auxiliary amplifiers are pseudo-differential, they do not require a common-mode feedback network.

As the op-amp is fully differential, the common-mode feedback (CMFB) network is used to set the op-amp output common-mode voltage to a mid-supply value $V_{refCMOUT} = 0$ that allows maximum symmetrical peak-peak output swing. A resistive local common-mode circuit is also used in the CMFB network to achieve a similar unity gain frequency(f_u) as in the differential amplifier. The CMFB loop has similar DC open-loop gain, GBW, and phase margin as the differential loop as it is required in FD op-amps. The CMFB circuit is shown in Figure 3(b).

B. CLASS-AB OPERATION OF COMPOSITE INPUT STAGE

All transistors in the composite input stage (except the tail transistor M_{TAIL} which is scaled by a factor of 2) have the same W/L dimensions and the same bias current I_{bias}. The first stage of the op-amp uses RLCMFB. This increases the effective transconductance of the composite input stage by approximately a factor of 3 and generates signal currents in the cascoded branch which can be much higher than the bias current. This increases the current available to the compensation capacitor C_C and increases the slew rate at the op-amp internal nodes V_{o1}, V_{o1}'. The maximum current in transistors M_{N1}, M_{N2} can be expressed by (1).

$$I_{MN1,2\,\max} = \beta_{MN1,2}(M+1)^2 V_{DS\ satMN1,2}{}^2 = I_{bias\,MN1,2}(M+1)^2 \quad (1)$$

Here $M = I_{bias}.R_{CMIN}/V_{DSsatMN1,2}$ (see Appendix A). Hence depending on the value of R_{CMIN} and I_{bias}, enhanced positive and negative peak currents $I_{peakVo1,o1'}$ can be delivered to the compensation capacitor C_C at nodes $V_{o1,o1'}$. In this design values $R_{CMIN} \approx 8k\Omega$, $|V_{DSsatMN1,2}| = 160mV$, and $I_{bias} = I_{biasMN1Q} = 28\mu A$ were used. These selections result in $M + 1 \approx 2.4$, which leads to peak currents with values $I_{MN1max} \approx 6I_{biasMN1Q} \approx 6I_{bias} \approx 168\ \mu A$ at nodes $V_{o1,o1}$.

C. CLASS-AB OPERATION OF OUTPUT STAGE

In order to obtain a large negative dynamic output current, a free class AB technique [17] is incorporated at the output stage using a capacitor C_{BAT} and a large resistor R_{large} that provides a large time constant $\tau = R_{large}C_{BAT}$. Thus, C_{BAT} cannot discharge rapidly and acts as a floating battery for fast dynamic changes. At the quiescent condition, R_{large} provides a DC bias voltage V_{BN} to $M_{ON1,2}$. The output transistors M_{ON1} and M_{ON2} are scaled up by factor four compared to the unit transistor sizes so that the output branches have quiescent currents with value $I_{QMON1,2} = I_{QMOP1,2} = 4I_{bias}$. When the op-amp is slewing in the negative direction under dynamic conditions, nodes $V_{o1,1}$ have large positive voltage changes. These changes are transferred to the gates of

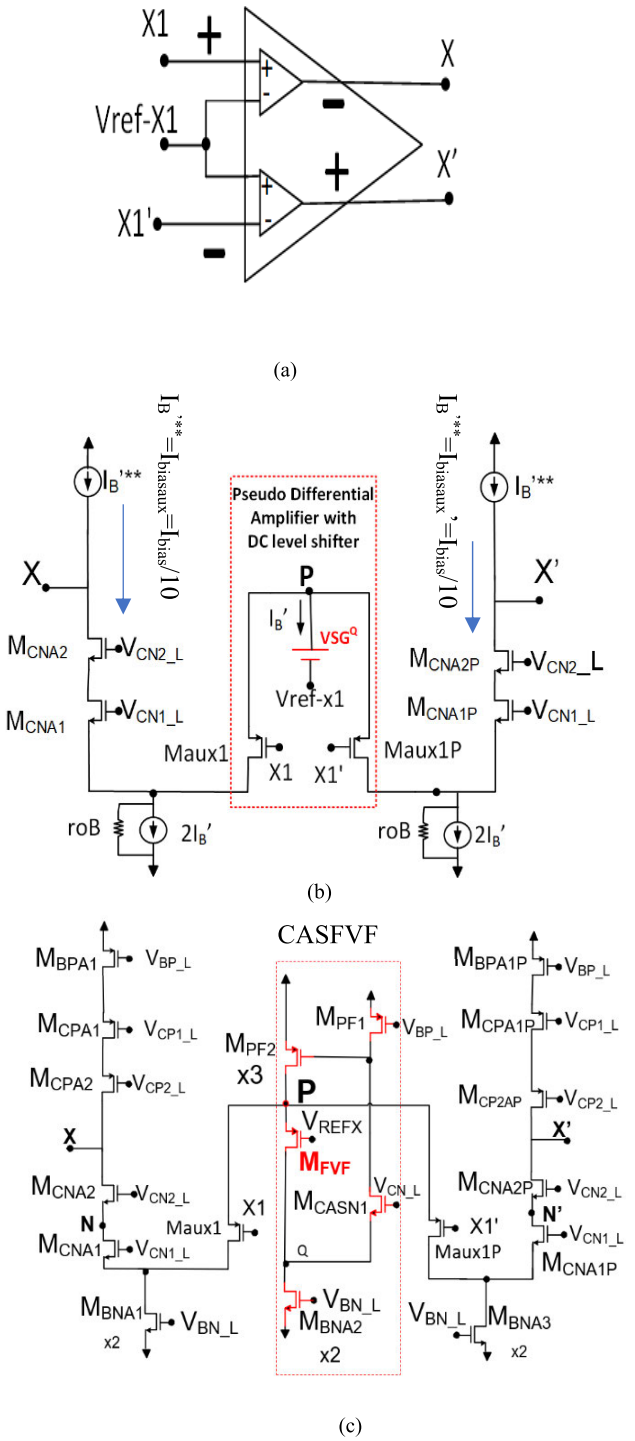

FIGURE 4. **(a), (b) Block and (c) Schematic diagram of the AuxP amplifier.**

$M_{ON1,2}$ through C_{BAT} and provide large negative dynamic output currents that can be much higher than their quiescent current. These larger dynamic currents enhance the op-amp's negative slew rate and the current efficiency CE, which is given by $CE = I_{Outmax}/I_{QTotal}$. Thus, the op-amp can achieve a higher slew rate, which improves its large-signal figure of merit FOM_{LS}.

D. GAIN OF AUXILIARY AMPLIFIERS

Two high gain auxiliary amplifiers AuxN and AuxP are used to boost the gain of the op-amp with regulated cascode transistors [9] present in the second stage of the op-amp. In order to provide enough headroom, an auxiliary amplifier AuxP with PMOS input stage (shown in Figure 4) is used for M_{CN1} and M_{CN2}, whereas an auxiliary amplifier AuxN with NMOS input stage is used for M_{CP1} and M_{CP2}. Auxiliary amplifier AuxN is not shown here, as it is a complimentary version of AuxP. The auxiliary amplifiers are pseudo-differential amplifiers. These consist of two single-ended folded double cascoded amplifiers. They share a cascoded FVF or CASFVF [13], [14] that generates an AC signal ground at node P. The CASFVF also operates as a DC level shifter. It sets accurately the voltages V_{X1}, V'_{X1} and V_{Y1}, V'_{Y1} to the reference values $V_{X1} = V'_{X1} = V_{ref-X1}$ and to $V_{Y1} = V'_{Y1} = V_{ref-Y1}$ in conjunction with the single-ended amplifiers using negative feedback. This is very important in order to ensure that all transistors in the composite input stage operate in saturated mode within the constraint of the 1.2V total supply used. In Figure 4 transistors, M_{aux1} and M_{aux1P} implement single-ended folded double cascoded amplifiers with an AC signal ground at node P that corresponds to their source nodes. The CASFVF causes the impedance at node P to be very low ($R_P \sim 3/g_m(g_m r_0)^2 \sim 20\Omega$), and this node is used as a virtual AC ground with a quiescent voltage $V_P = V_{ref-X1} + V_{SGQMFVF}$. In order to achieve a high gain, the single-ended auxiliary amplifiers use double cascoded transistors and double cascoded (high impedance) biasing current sources I_B'**. The bias current in the auxiliary amplifiers ($I_{biasaux}$) is 10 times lower than the bias current used in the main op-amp, which in turn helps to reduce quiescent power dissipation.

The output impedance at nodes X, X' of the auxiliary amplifiers is given by (2).

$$R_{X,X'} = (r_{oBP}.g_{mCP1}r_{oCP1}.g_{m\ CP2}r_{o\ CP\ 2}) \,||\, \times \left((r_{oaux1}||r_{oB}).g_{mCN1}r_{oCN1}.g_{mCN2}r_{o\,CN2}\right) \quad (2)$$

For simplicity, it is assumed that all transistors' have equal g_m and r_o values. Thus, $R_{X,X'}$ is given by $R_{X,X'} = (A_i)^2\, r_o/4$. Hence, gain A_{Aux} of the auxiliary amplifiers is given by (3).

$$A_{Aux} = g_{maux1,1P}R_{X,X'} \approx A_i^3/4 \quad (3)$$

E. OPEN-LOOP GAIN ANALYSIS OF THE PROPOSED OP-AMP

The proposed op-amp has three gain stages. The gain from the first stage $A_I = (V_{M'}\text{-}V_M)/V_{id}$ is moderate $A_I \sim 3$ and given by(4).

$$A_I = g_{mIN}R_M \quad (4)$$

The impedance at the output nodes V_{o1}, $V_{o1'}$ of the composite input stage ($R_{Vo1,o1'}$) is given in (5).

$$\begin{aligned} R_{Vo1.o1'} &= \left(A_{Aux}g_{mC_{P1}}r_{oCP1}r_{oP1}\right) || \left(A_{Aux}g_{m\ CN1}r_{oCN1}r_{oN1}\right) \\ &\approx A_{Aux}\left(g_m r_o^2\right)/2 \\ &= A_{Aux}\,(A_i r_o/2) \end{aligned} \quad (5)$$

The impedance of the output stage R_{oIII}, which corresponds to the output impedance of the op-amp $R_{out} = R_{oIII}$, is given by (6).

$$R_{oIII} = r_{oON}||r_{oOP} \tag{6}$$

The DC open-loop gain of the op-amp $A_{OLDC.}$ is given by (7).

$$\begin{aligned} A_{OLDC} &= A_I A_{II} A_{III} = g_{mIN} R_M . g_{mN1} R_{Vo1} . g_{mOP} . R_{oIII} \\ &\approx g_{mIN} R_M . A_{Aux} \left(A_i^2/2\right) . A_i/3 \approx g_m R_M . A_{Aux} \left(A_i^3/6\right) \end{aligned} \tag{7}$$

In this design, a value $A_I = g_{mIN} R_M$ ~3V/V was selected. The $A_{OLDC.}$ obtained by combining (3) and (7)has a very high value as given in (8).

$$A_{OLDC} \approx \left(A_i^6/8\right) \tag{8}$$

F. POLE-ZERO ANALYSIS OF THE PROPOSED OP-AMP

Frequency Response of Auxiliary Amplifiers: Auxiliary amplifiers introduce negative local feedback loops that should have a gain-bandwidth $GBW_{auxN,P}$ at least equal or greater than the main op-amp and sufficient phase margin ($PM_{aux} > 60^o$). The main op-amp was designed for a unity gain frequency of 70MHz.

In order to achieve stability of the local feedback loop of the auxiliary amplifiers and a $GBW_{auxP,N}$ comparable to the main op-amp, a small compensation capacitor $C_{cauxP,N}$ in series with a resistor $R_{cauxP,N}$ are used at nodes X, X' and Y,Y'. The Compensation capacitors in conjunction with the parasitic capacitances at nodes X, X' and Y, Y' provide dominant poles that determine the gain-bandwidth product of the auxiliary amplifiers $GBW_{auxP,N}$.

The GBW_{auxP} of auxiliary amplifier AuxP (Figure 4) is given by $GBW_{auxP} = (1/2\ \pi)\ g_{maux1}/C_x$. Here, C_X is the capacitance at node X at the output of the auxiliary amplifier. This feedback loop has a very high-frequency pole at the source terminal of the cascode transistor which is given by $\omega_{pVHFFB} = g_{mCN1}/C_{X1}$, where C_{X1} is the parasitic capacitance at node X_1. This pole does not affect the phase margin since it is essentially higher than GBW_{auxP}. The only pole that affects the auxiliary amplifier's phase margin is the high-frequency pole ω_{pHFN} at the source of M_{CNA2} (node N). The value of resistor R_{cauxP} is selected so that the zero that it generates, given by $\omega_z = 1/(R_{cauxP} C_{cauxP})$, matches approximately the high-frequency pole ω_{pHFN}.

For the proposed design, values C_{cauxN}= *130fF,* R_{cauxN} = 9k Ω, and C_{cauxP} = 60fF, R_{cauxP} = 18k Ω were used in AuxN and AuxP, respectively which led to 93MHz open-loop unity gain frequencies in both amplifiers with a phase margin of approximately 60^o. Figure 5 shows the open-loop gain and phase response of the auxiliary amplifiers AuxN and AuxP. It can be observed that both amplifiers have open- loops gains of 77dB and 70dB, phase margin of 61^0, and unity gain frequencies of 94MHz (AuxN) and 93 MHz (AuxP), respectively.

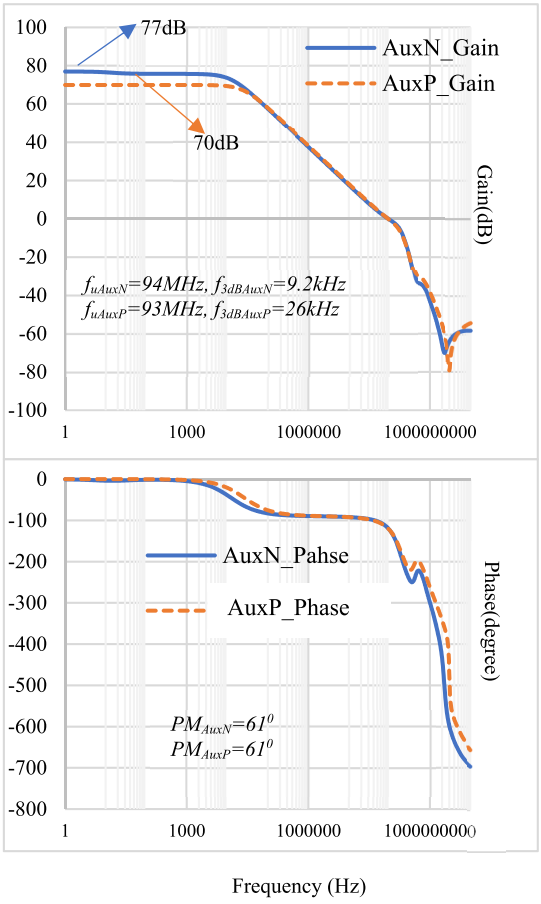

FIGURE 5. Open-loop frequency response of auxiliary amplifiers.

Open-Loop Response of Op-amp: The op-amp is compensated using Miller capacitors C_C in series with a resistor R_C based on the conventional Miller pole splitting principle. The transfer function of the Miller compensated op-amp can be expressed approximately by (9).

$$A_{OL}(s) \approx \frac{A_{OLDC}\ (1 + s/\omega_z)}{\left(1 + s/\omega_{pDOM}\right)\left(1 + s/\omega_{pHFOUT}\right)\left(1 + s/\omega_{pM}\right)} \tag{9}$$

Here A_{OLDC} is the DC open-loop gain given by (8), ω_{pDOM} is the dominant pole at the outputs of the composite input stage $V_{o1,1'}$ caused by Miller effect, ω_{pHFOUT} is the high-frequency pole at the output nodes of the op-amp, ω_z is a zero generated by the compensation resistor R_C in series with C_C, and $\omega_{pM,M'}$ are the high-frequency poles at nodes M, M' of stage 1. The high-frequency pole ω_{pM} is given by (10).

$$\omega_{pM} = 1/(C_M R_M) \tag{10}$$

Here $C_M = C_{gdINP}(1 + 1/A_1) + C_{gdINL} + C_{gsMN1} + C_{dbINL} + C_{dbINP}$ is the small parasitic capacitance at nodes M, M'. R_M is given by (11).

$$R_M = R_{CMIN}||r_{oINP}||r_{oIN\,L1} \tag{11}$$

The value of R_M plays a vital role in determining the gain $A_I = g_{mIN}R_M$ of the first stage and the position of the poles at nodes M, M'. There exists a tradeoff between the maximum gain of the first stage and phase margin of the op-amp. R_{CMIN} should be smaller than $r_{oINP,M}$ and $r_{oINL1,2}$ in that case, $R_M \approx R_{CMIN}$. The maximum value of R_{CMIN} has to be selected in such a way so that the poles ω_{pM} at nodes M, M' satisfy the conditions: a) $\omega_{pM,M'} \gg \omega_{pHFOUT}$ and b) $\omega_{pM,M'} \gg$ GBW. In that case poles $\omega_{pM,M'}$ cause negligible degradation in the phase margin of the op-amp. Thus, the transfer function of the proposed op-amp can be simplified and approximated by (12).

$$A_{OL}(s) \approx \frac{A_I A_{II} A_{III}\,(1 + s/\omega_z)}{(1 + s/\omega_{pDOM})\,(1 + s/\omega_{pHFOUT})} \tag{12}$$

In the proposed design values $R_{CMIN} = 8\text{k}\Omega$ were selected that lead to a moderate low gain $A_I \sim 3$. *As* a result, the poles $\omega_{pM,M'}$ are located at a factor 4 times higher than *GBW*. As indicated in the analysis below, the effective transconductance g_{meff} and *GBW* of the op-amp are also enhanced by the factor $A_I = 3$. These essential enhancements are achieved with a very modest increase in power dissipation and a negligible effect on PM.

Nodes $V_{o1,1'}$ have a very high impedance and large capacitance due to Miller multiplication effect. Thus, the dominant pole ω_{pDOM} at nodes $V_{o1,1'}$ can be expressed approximately by (13).

$$\omega_{pDOM} \approx \frac{1}{R_{Vo1,1'} A_{III} C_C} \tag{13}$$

The Gain-bandwidth product (*GBW*) of the proposed op-amp is given by (14).

$$\begin{aligned} GBW &= A_{OLDC}\omega_{pDOM} \\ &= (A_I A_{II} A_{III})\, 1/(R_{Vo1,1'} A_{III} C_C) \\ &= (A_I A_{II})\, 1/(R_{Vo1,1'} C_C) \\ &= A_I g_{mN1} R_{Vo1,1'} 1/(R_{Vo1,1'} C_C) \\ &= (A_I g_{mN1})/C_C = (g_{meff})/C_C \end{aligned} \tag{14}$$

The high-frequency poles at the output nodes are given by the usual expression (15).

$$\omega_{pHFOUT} = \frac{g_{mOUT}^{eff}}{C_L} \tag{15}$$

Here g_{mOUT}^{eff} is given by $g_{mOUT}^{eff} = g_{mOP1,2} + g_{mON1,2}$. Note that due to class AB operation the effective output transconductance of the op-amp at high frequencies is the sum of the transconductances of $M_{OP1,2}$ and $M_{ON1,2}$ since capacitor C_{BAT} connects the gates of $M_{OP1,2}$ and $M_{ON1,2}$ at high frequencies.

The zero ω_z is given by (16).

$$\omega_z = 1/\left(C_C R_C^{eff}\right) \tag{16}$$

where $R_C^{eff} = R_C - 1/g_{mOUT}^{eff}$

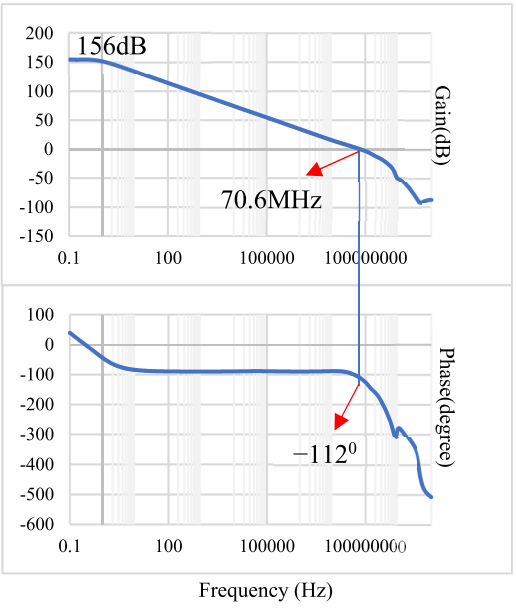

FIGURE 6. Open-loop Frequency response of Common-Mode Feedback network of Figure 3(b).

Now, to achieve high *GBW* and high phase margin with low silicon area, C_C is selected to have a moderately low-value $C_C = C_L/7$ and the output quiescent current is chosen with a value $I_{QMON1,2} = I_{QMOP1,2} = 4I_{bias}$. R_C was selected so that the ω_z approximately matches ω_{pHFOUT}.

Open-Loop Gain of Common-Mode Feedback Network: The common-mode feedback network (CMFBN) of Figure 3(b) should also have a gain-bandwidth product GBW_{CMFBN} equal to or higher than the *GBW* of the open-loop gain of the op-amp of Figure 3(a) and a phase margin of at least 60°. Hence a RLCMFB network using resistors with value R_{CM} is also incorporated in this circuit. This in order to enhance its gain-bandwidth product GBW_{CMFBN}. A moderate valued R_{CM} is selected that provides a gain and GBW enhancement factor of also approximately 3. This results in high-frequency poles at nodes V_{CNTCM} and V_{CNTCM1}, which are also about four times larger than GBW_{CMFBN}. With this, the CMFBN has similar open-loop gain, dominant pole, GBW, high-frequency pole, and zero as the differential loop of the op-amp. Figure 6 shows the open-loop frequency response of the CMFBN. It can be observed that it has a very high DC open-loop gain $A_{OLDCCMFBN} = 156\text{dB}$, 68^0 phase margin, and unity gain frequency $f_u = 70\text{MHz}$, which is comparable to the unity gain frequency of the differential loop of the op-amp.

III. SIMULATION RESULTS

The proposed op-amp was simulated with Cadence Design Framework II using commercial 130nm CMOS technology parameters provided by MOSIS [18]. Equal unit NMOS and PMOS transistor sizes $(W/L)_{N,P} = 10\mu\text{m}/0.27\mu\text{m}$ were used in the input stage (see Table 1 for transistor sizes and other design parameters) of the proposed circuit. NMOS and

TABLE 1. Design parameters values for sections of proposed op-amp: differential op-amp, auxiliary amplifier, and CMFBN.

Differential op-amp	Parameter	AuxiliaryP/ AuxiliaryN	Parameter	CMFBN	Parameter
I_{bias}(µA)	30	$I_{biasaux}$(µA)	3	I_{bias}(µA)	30
R_{large}(kΩ)	500	C_{cauxP},C_{cauxN}(fF)	60,130	R_{CM}(kΩ)	15
R_{CMIN}(kΩ)	8	R_{cauxP},R_{cauxN}(kΩ)	18 , 9	*NMOS, PMOS (unit transistor's W/L)(µm)*	10/0.27
C_C (pF)	4	*NMOS, PMOS (unit transistor's W/L)(µm)*	10/0.27	$g_{mCM,}$ g_{mCMP} (µA/V)	743,441
C_L (pF)	30	g_{mauxP1},g_{mCNA1},g_{mCNA2},g_{mCPA1},g_{mCPA2} (µA/V)	56,102,102,74,75	g_{dsCM},g_{dsCMP}(µA/V)	22, 25
R_C(kΩ)	2.2	g_{dsBPA1},g_{dsCPA1},g_{dsCPA2},gd_{sCNA1},$g_{dsCNA2,}$ $g_{dsauxP1}$(µA/V)	2.1,2.9,1.9,4.8,4.9,6.6,1.52	R_A(kΩ)	100
C_{bat}(pF)	2	g_{mauxN1},g_{mCNA1N},g_{mCNA2N},g_{mCPA1N}, g_{mCPA2N}(µA/V)	80,104,104,76,76	C_{CM}(pF)	2
NMOS, PMOS (unit transistor's W/L)(µm)	10/0.27	$g_{dsBPA1N}$,$g_{dsCPA1N}$,$g_{dsCPA2N}$,$g_{dsCNA1N}$,$g_{dsCNA2N,}$ $g_{dsauxP1}$(µA/V)	3.6, 3, 2.2, 4.3,5.2, 3.8, 3.46		
g_{minp},$g_{mN1,}$ $g_{mP1,}$ g_{mCP1}, g_{mCN1}, $g_{mOP,}$ g_{mON}(µA/V)	399,627,365,374,626,1500 , 3846				
$g_{dsinp,}$ $g_{dsNL1,}$ g_{dsMN1}, $g_{dsCN1,}$ $g_{dsCP1,}$ g_{dsP1} $g_{dsOP,}$ g_{dsON} (µA/V)	9, 21, 22, 20, 11, 17,51,99				

PMOS transistors in the output stage were scaled by factors of 4 and 2, respectively. The op-amp was simulated with a bias current $I_{bias} = 30\mu$A. To reduce quiescent power dissipation (P^Q), the auxiliary amplifier's bias current was scaled down by a factor of 10 i.e. $I_{biasaux} = 3\mu$A. Values $V_{ref-X1} = -380$mV, $V_{ref-Y1} = 400$mV were used as reference voltages for the auxiliary amplifiers in order to keep all transistors in saturation within a safe range in the second stage. Dual ± 0.6V supply voltages and load capacitances $C_L = 30$pF on each output were used.

Figure 7 shows the open-loop frequency responses of the Conventional Miller op-amp of Figure 1(b) (Conv-Miller), of the telescopic input 2-stage Miller op-amp (TEinp-Miller) of Figure 1(c), and of the proposed super-gain-boosted op-amp using the same bias currents. In order to make a fair comparison, the NMOS output transistors $M_{ON1,2}$ of all op-amps are scaled up by the same factor 4 as it was done in the proposed op-amp. It can be seen that the conventional and telescopic input Miller op-amps have DC open-loop gains of 47dB and 71dB and lower unity gain frequencies (f_u) of 23MHz and 26MHz, respectively.

The proposed op-amp has open-loop gain, phase margin, and unity gain frequency of $A_{OLDC} = 156$dB, $PM = 74^o$, and $f_u = 70$MHz, respectively. It can be seen that the proposed op-amp improves significantly (by 85dB to 109 dB) the open-loop DC gain and the unity gain frequency by a factor of approximately three compared to the conventional and telescopic input Miller op-amps. This comes at the expense of relatively moderate (30%) additional power dissipation.

The common-mode rejection ratio (CMRR) of the Proposed, Conv-Miller, and TEinp-Miller are shown in Figure 8. Fully differential (FD) op-amps can ideally reject common-mode disturbances almost completely when no mismatch is taken into account. In this paper, the simulation of CMRR is performed by introducing a typical 1% mismatch in the transistors' W/L dimensions and measured differentially. The CMRRs at DC of the proposed, Conv-Miller, and TEinp-Miller are 224dB, 88dB, and 105dB, respectively, at DC. The high CMRR of the proposed op-amp is achieved due to its very high A_{OLDC}.

The op-amp was simulated using the unity gain closed loop inverting amplifier configuration, shown in Figure 9, to determine transient response and output resistance. Equal R_{in} and R_f values of 100kΩ were used in the simulation The output resistances of the proposed, the TEinp-Miller, and the Conv-Miller op-amps are −74dB Ω (0.2mΩ), 7dB Ω (2.2Ω), and 34dB Ω (50Ω), respectively, at DC. Figure 10 shows the frequency responses of the output resistance of the op-amps.

The proposed opamp has an extremely low output resistance at low frequencies due to its very high open-loop gain. The frequency responses of the op-amps in unity gain inverting amplifier configuration are shown in Figure 11. The amplifier using the proposed op-amp has a bandwidth (BW) of 55MHz whereas the amplifiers using TEinp-Miller and

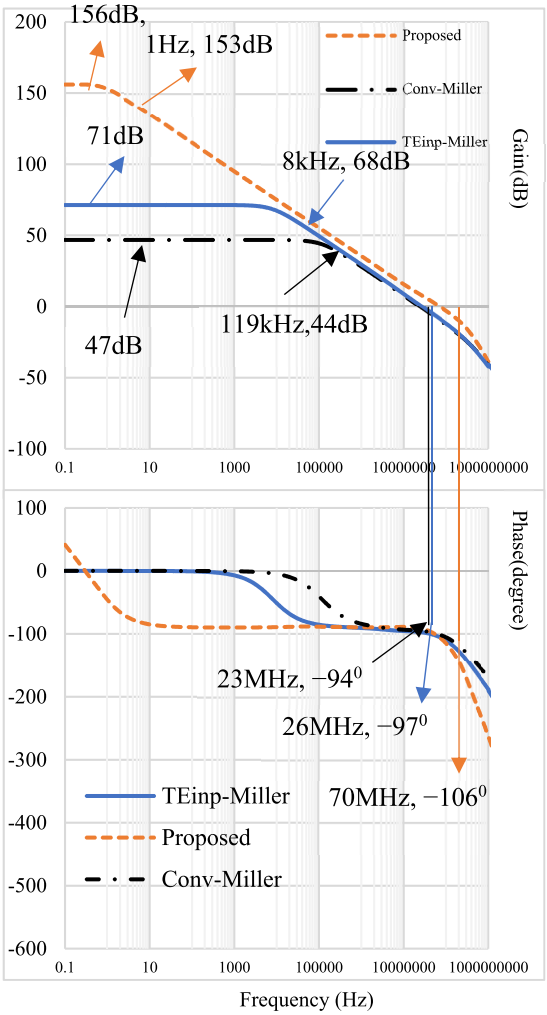

FIGURE 7. Comparison of open-loop frequency responses of conventional, telescopic input and proposed op-amps.

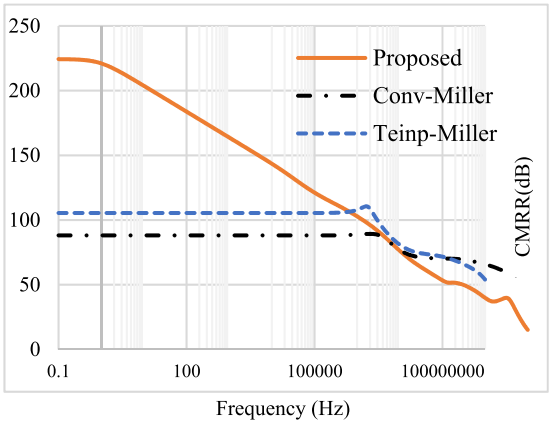

FIGURE 8. CMRR of op-amps.

Conv-Miller have bandwidths of 16MHz and 13MHz, respectively.

The op-amps' transient responses are shown in Figure 12 for a 5MHz input pulse with ± 500mV amplitude. Positive and negative slew rates (SR) obtained from the proposed op-amp's transient response are approximately equal

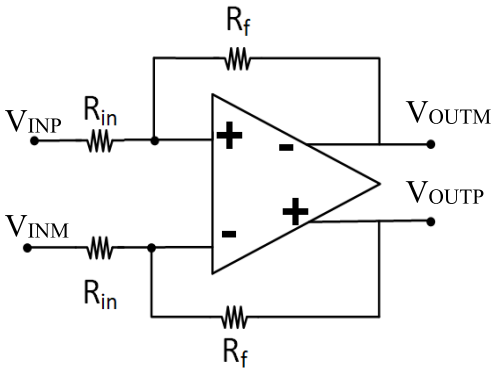

FIGURE 9. Unity gain inverting differential amplifier.

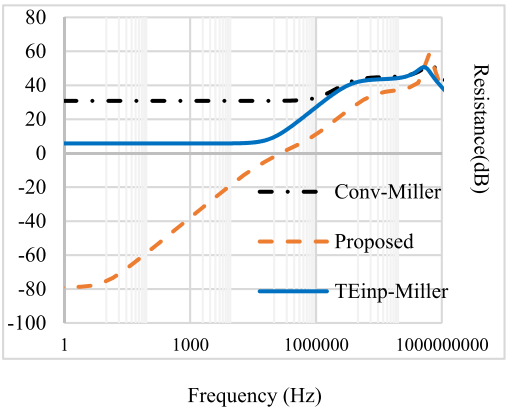

FIGURE 10. Output resistance of op-amps connected as unity gain amplifiers.

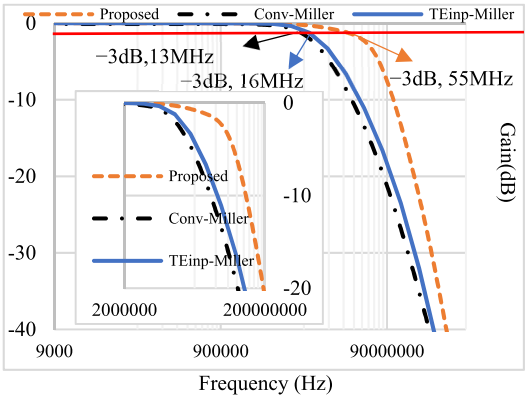

FIGURE 11. Frequency response of op-amps in unity gain inverting amplifier configuration.

with values 70V/μs and 69V/μs, respectively. Whereas the TEinp-Miller has $SR^+ = 9.5$V/μs, $SR^=$ 12 V/μs, and the Conv-Miller has $SR^+ = 8.7$V/μs, $SR^- = 10.2$ V/μs. Neither the Conv-Miller nor the TEinp-Miller can follow the input signal due to their low slew rates and low current efficiency, as both of them are class-A op-amps. The proposed op-amp can provide 2.1mA positive and negative output peak currents at each output at the expense of a total of 572μA quiescent current. As the proposed fully differential opamp is driving two load capacitors of 30pF simultaneously, the current efficiency CE can be expressed as $CE = I^{Tot}_{outMAX}/I_{Qtotal}$.

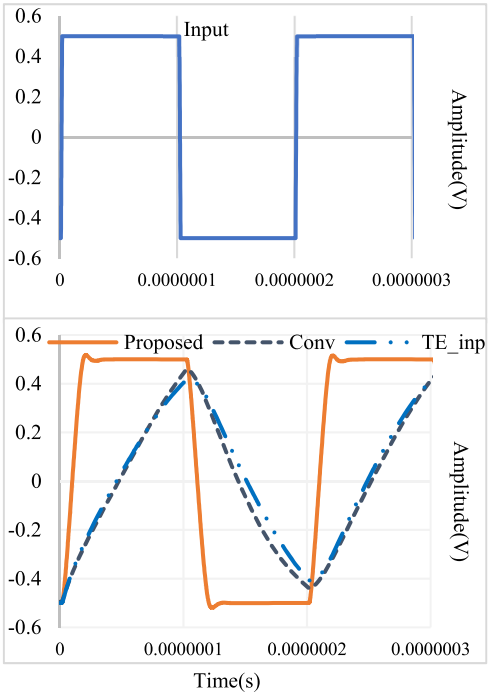

FIGURE 12. Transient response of the op-amps for 5MHz pulse input.

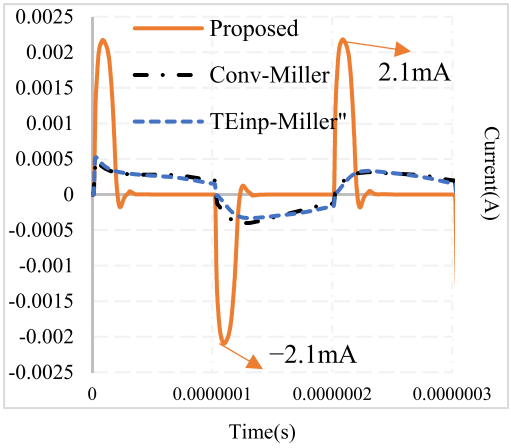

FIGURE 13. Output Load Currents of the op-amps.

Here I_{outMAX}^{Tot} is the summation of the load currents in the two output nodes. The CE of the proposed op-amp is $CE = 7.16$, while the Conv-Miller and TEinp-Miller have current efficiencies of 1.2 and 1.2, respectively, which are both a factor 6 lower than the proposed op-amp. Figure 13 shows the output currents of the op-amps. Figure 14 shows the transient responses of the proposed op-amp for different values of R_C(changing by ±20%). These pulse responses of Figure 14 help to observe the effect of pole-zero doublet mismatches in the settling time (t_{setl}) [19]. The t_{Setl} of the op-amp is measured considering the time required for the response to reach and stay within a range of ±0.1% of the final value. The positive settling time $t_{Setl}+$ varies from 60ns-40ns and the negative settling time t_{Setl}^{-} varies from 60ns to 30ns when R_C varies from 1.8kΩ-2.6kΩ. Figure 15 shows that the proposed op-amp has 0.1% positive settling time

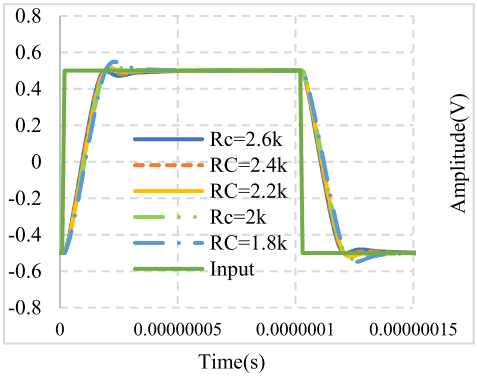

FIGURE 14. Pulse responses of the proposed op-amp for different values of RC.

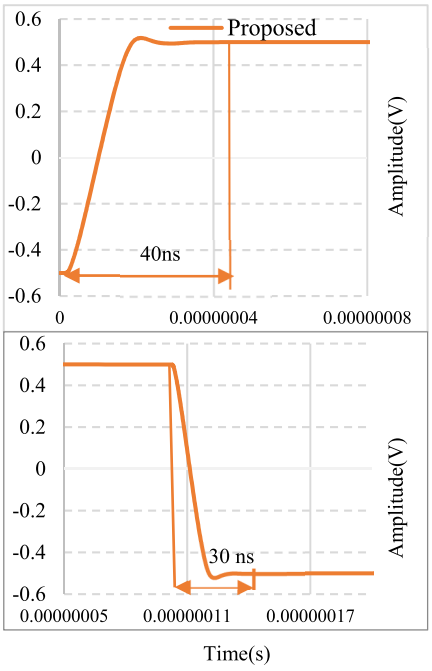

FIGURE 15. ±0.1% settling time of proposed op-amp.

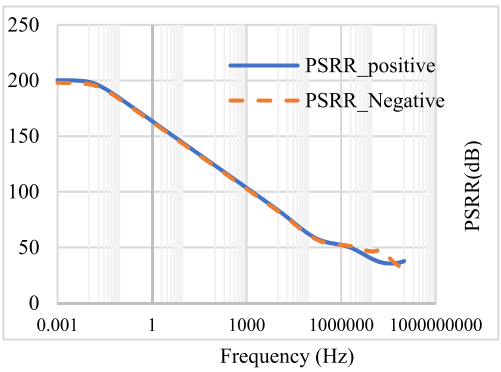

FIGURE 16. Positive and Negative PSRR of proposed op-amp.

$t_{Setl}+ = 40$ns and the negative settling time $t_{Setl}^{-} = 30$ns for $R_C = 2.2$kΩ when a 1MHZ 500mVpp amplitude step input is applied. The simulations of the power supply rejection ratio (PSRR) of Conv-Miller, TEinp-Miller, and Proposed op-amps were performed by introducing a typical 1%

TABLE 2. Corner analysis of Op-Amp Operating at different temperatures.

	At T=27^{0}C						At T=90^{0}C						At T=−20^{0}C					
Corner	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**	tt	ff	fs	sf	ss	**SD**
I_{TotalQ}(μA)	572	562	553	574	598	**15**	539	536	541	540	543	**2.3**	590	580	572	610	600	**14**
THD (dB)	−67	−68	−65	−66	−66	**1**	−66	−69	−65	−67	−60	**3**	−65	−69	−62	−68	−64	**2.5**
f_u(MHz)	70	76	65	75	65	**4**	64	71	75	70	69	**3.5**	85	91	77	92	80	**5.9**
PM (deg)	76	74	76	74	74	**1**	76	77	70	72	74	**2.6**	70	65	64	68	74	**3.6**
Gain(dB)	156	156	153	158	154	**1.7**	147	152	154	152	150	**2.4**	159	155	159	154	159	**2.2**
SR^+(V/μs)	71	77	76	63	60	**6.7**	66	69	62	66	59	**3.5**	73	78	66	72	65	**4.8**
SR^-(V/μs)	69	74	74	62	58	**6.4**	65	68	61	65	56	**4.1**	71	78	67	74	63	**5.2**

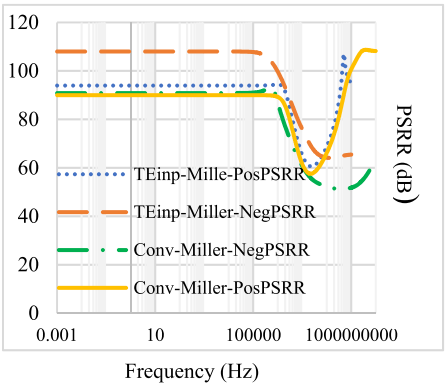

FIGURE 17. Comparison of PSRR of Conventional and Telescopic input Miller op-amp.

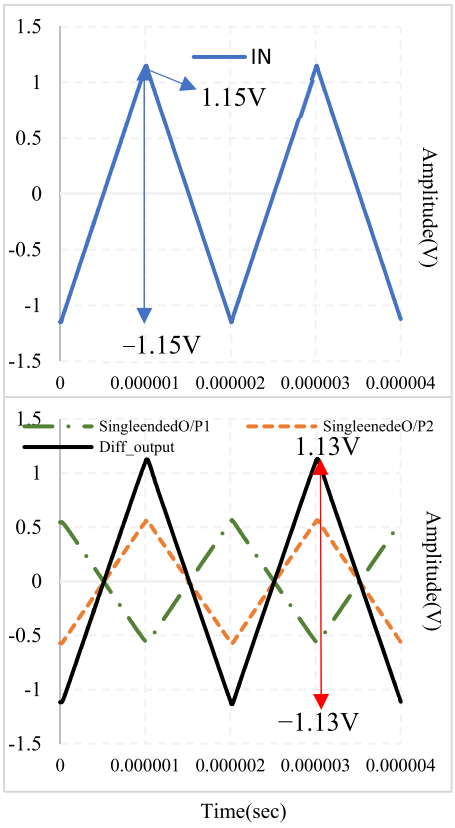

FIGURE 18. Determination of output swings of the proposed op-amp using ±1.15V, 500kHz input triangular signal.

mismatch in the dimensions of the transistors and it is shown in Figures 16 and 17. The positive PSRRs of the proposed, Conv-Miller, and TEinp-Miller are 200dB, 89dB, and 93dB, respectively, at DC. The negative PSRRs are 198dB, 90dB, and 108dB of the proposed, Conv-Miller, and TEinp-Miller, respectively. All the PSRRs are measured here differentially.

The amplifier with the proposed op-amp has close to rail-to-rail output swing from −1.13V to 1.13V for a ±1.15V, 0.5MHz triangular input signal, as shown in Figure 18. As the phase-change occurs between the differential outputs, the dynamic range increases by a factor two over that of a single-ended output with the same peak-peak voltage swing. The range figure of merit $FOM_R = V_{outPP}/V_{supply}$ of the proposed op-amp is $FOM_R = 1.9$ for ±0.6V supply voltage. The total harmonic distortion (THD) of the proposed op-amp for a 1V peak-peak amplitude sinusoidal signal of 100kHz is −60dB.

Corner analysis of the proposed op-amp at different temperatures is given in Table 2. It can be observed that the proposed op-amp is stable against process and temperature variations. The Standard Deviation (SD) of each parameter for variation of the process has been given in Table 2 for the considered temperatures (−20^{0}C, 27^{0}C, 90^{0}C). The layout of the proposed op-amp is given in Figure 19. It occupies 410μm x197μm Si area.

A comprehensive comparison of the proposed op-amp's performance with other state-of-the-art op-amps [20]–[29] is given in Table 3. The proposed op-amp has large-signal, small-signal, and open-loop gain figures of merit with values $FOM_{LS} = 3$(V/μs)(pF/μW), $FOM_{SS} = 2.8$ (pF.MHZ/μW), and $FOM_{AOLDC} = 174$(MV/V.pF.MHZ/μW), respectively. The area figure of merit $AFOM_{AOLDC}$ of the proposed circuit is 2175(MV/V) pF.MHz/((mm^2).μW). From the table, it can be asserted that the proposed op-amp has the highest FOM_{AOLDC} and FOM_{LS}. The small-signal figure of merit FOM_{SS} is comparable with other state-of-the-art amplifiers [21]. From the simulation results, it can also be seen that the proposed op-amp offers very high gain, moderate-high speed, and the highest area figure of merit. It also offers the well-known advantages of Miller op-amps: close to rail-to-rail output swing and ability to drive resistive loads with minor gain degradation so that it can be used in continuous-time circuits as opposed to one stage regulated

TABLE 3. Summary of Simulation results and comparisons.

Parameter	[20]	[21]	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	Conv-Miller (Figure 1 (b))	TEinp-Miller (Figure 1(c))	**This work**
Process (µm)	0.35	0.35	0.18	0.18	0.045	0.35	UMC 0.11	0.18	0.18	0.022	0.13	0.13	**0.13**
Supply (V)	±1.3	2	1.8	1.8	2	3.3	5	1.8	1.8	0.8	1.2	1.2	**1.2**
I_{Qtotal} (µA)	3000	158	477	1000	600	2121	147	310	472	55	434	444	**572**
P^Q (µW)	7800	316	860	1800	1200	7000	735	558	850	44	521	532	**686**
C_L (pF)	16	500	5	1	1	5	4	2.3	5	1	30	30	**30**
Gain (dB)	100	100	82.7	85.6	141	156	164.1	66	105.5	103	47	71	**156**
PM (degree)	57	51	68.7	66.7	60	69	63	58.5	53	74	86	83	**74**
GBW (MHz)	80	1.89	88.7	987	101	1.1	17.09	60	231.7	50	26	29	**63**
SR+ (V/µs)	56	0.7	8.67	-	57.7	-	-	95	13.25	-	8.7	9.5	**70**
SR- (V/µs)	-	-	-	-	-	-	-	-		-	10.2	12	**69**
settling time (ns)	280	-	79.5	-	906	22.3	-	-	99	-	-	-	**40 (0.1%)**
CMRR (dB)@dc/1k/ 100k	-	-	127	-	136	107	288	-	-	67	88	105	**224, 161,119,**
PSRR+/- (dB)	-	-	83.2	-	57/67	>90	186	-	-	120	89/90	93/108	**200/198**
CE ($I_{outMAX}^{Tot}/I_{Qtotal}$)	0.59	2.2	0.18	-	0.1	-	-	0.5	0.14	-	1.2	1.2	**7.2**
Fully Differential/ no of stages	Yes/ 3	No/3	Yes/2	Yes/1	No/2	No/2	Yes/1	No/2	No/3	No/2	Yes/2	Yes/2	**Yes/3**
Exp*/Sim**	Exp	Exp	Sim	Sim	Sim	Sim	Sim	Sim	Exp	Sim	Sim	Sim	**Sim**
Area (mm^2)	0.04	0.02	.003	.001	-	-	-	-	0.45	-	-	-	**.08**
FOM_{SS} (pF.MHz/ µW)	0.16	2.9	0.5	0.5	0.08	.000 7	0.09	0.24	1.3	1.1	1.5	1.6	**2.8**
FOM_{LS} (V/µs)(pF/ µW)	0.11	1.1	.05	-	.05	-	-	0.39	0.08	-	0.5	0.5	**3**
FOM_{AOLDC} MV/V.pF. MHz/µW	0.02	0.3	.007	.01	0.9	0.05	15	0.00 05	0.25	0.2	.0003	.006	**174**
$AFOM_{AOLDC}$ (MV/V.pF. MHz)/(µW. mm^2)	0.5	15	2.3	10	-	-	-	-	0.6	-	-	-	**2175**
Equivalent input noise (nV/√Hz)	-	-	39.8@ 10kHz 4.68@ 1MHz	118000 @ (1Hz-100MHz)	-	-	-	-	194,22 4@(1H z-100MH z)	-	14@10k Hz 3@1MHz	13@10 kHz 3@1M Hz	**30@10kHz 4@1MHz**

***Exp- Experimental Results ** Sim- Simulation Results**

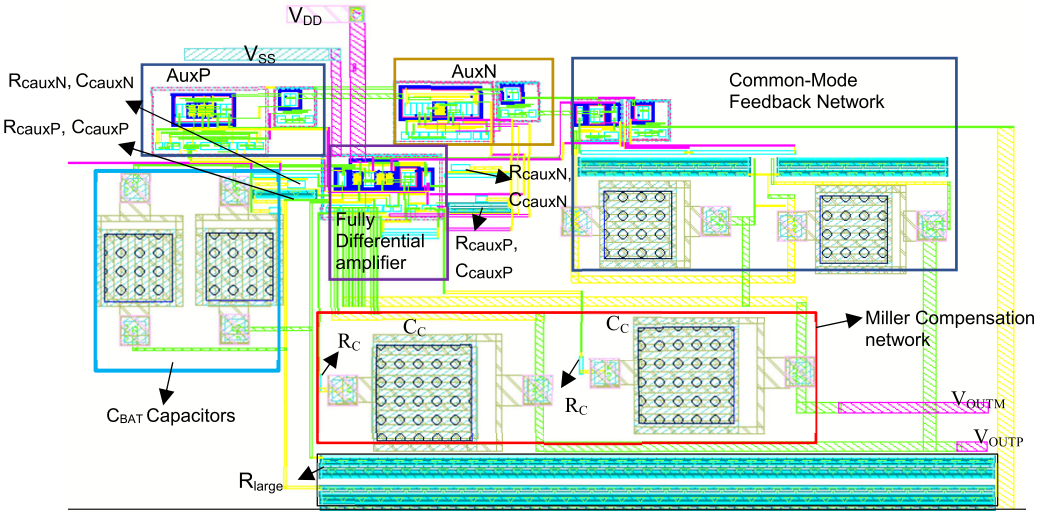

FIGURE 19. Layout of the proposed op-amp.

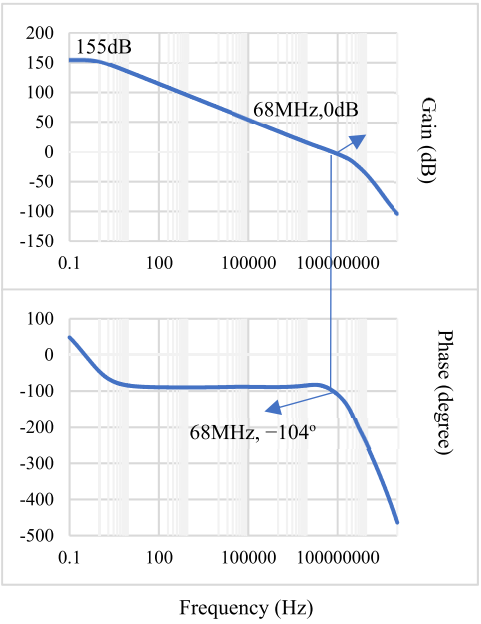

FIGURE 20. Post-layout Open-loop frequency response of proposed op-amps.

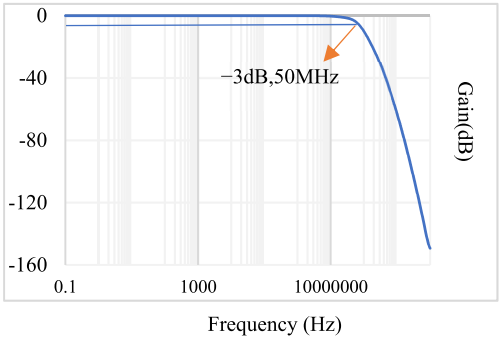

FIGURE 21. Post-layout Frequency response of op-amps in unity gain inverting amplifier configuration.

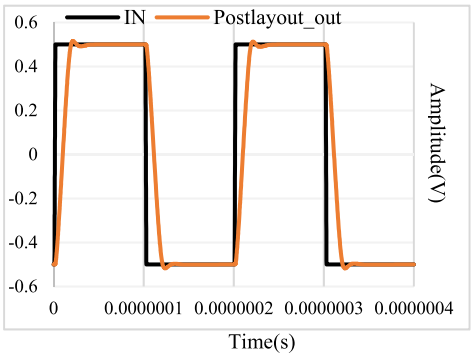

FIGURE 22. Post-layout Transient response of the op-amps for 5MHz pulse input.

cascoded op-amps that have essentially reduced output swing (by at least 50% in modern CMOS technologies) and that cannot drive resistive loads.

IV. POST-LAYOUT SIMULATIONS

The post-layout simulation of the proposed amplifier was completed using the layout of Figure 19. Figure 20 shows the open-loop frequency response of the post-layout simulation of the proposed op-amp. It is found there is only a minor change in the frequency response of the proposed op-amp for the consideration of the parasitic capacitances of the layout. There are only 1dB gain and 2° phase differences in the open-loop frequency response between the ideal and post-layout simulation of the proposed op-amp. The frequency response and the transient response of op-amps in unity gain inverting amplifier configuration of the proposed op-amp from the post-layout simulation are given in Figures 21 and 22. The bandwidth of the unity gain inverting amplifier obtained using the proposed op-amp is 50MHz in post-layout simulation. The positive and negative slew

rates of the proposed op-amp obtained from the post-layout simulations are 66V/μs and 65V/μs.

V. CONCLUSION

A fully differential super-gain-boosted AB-AB Miller op-amp with high swing and extremely high open-loop gain is presented. Additionally, it has a very high common-mode rejection ratio, power supply rejection ratio, and moderately high FOM_{SS} and CE. It can drive both capacitive and resistive loads. It can find applications in high-resolution A/D and D/A converters and in high precision amplifiers with resistive loads. It has the highest FOM_{AOLDC} of any op-amp reported in literature.

APPENDIX

CACULATION OF OUTPUT CURRENT AT NODES V_{o1}, AND V_{o1}' OF COMPOSITE INPUT STAGE

Under quiescent conditions, M_{INL1}-M_{N1} and M_{INL2}-M_{N2} perform as a conventional current mirror. As no current flows through the two matched R_{CMIN} resistors the gate-source voltages of M_{INL1}, M_{INL2}, $M_{N1,}$ and M_{N2} are all equal. In the presence of a differential input signal $V_{id,}$ the signal current $i = g_m V_{id}/2$ flows through the R_{CMIN} resistors. As a result, complementary voltage variations ΔV_M, $\Delta V_M'$ appear at nodes M and M' with a maximum swing of $\Delta V_{Mmax} = I_{bias} R_M$. R_M is given by (A1).

$$R_M = R_{CMIN} || r_{oINP,M} || r_{oINL1,2} \approx R_{CMIN} \tag{A1}$$

In order to achieve a high phase margin, the internal poles at nodes M, M' should be at a sufficiently high frequency ($f_{pM}, f_{pM}' > GBW$), and this requires to select values for R_{CMIN} smaller than $r_{oINP,M}$, and $r_{oINL1,2}$. Thus, R_M is approximately equivalent to $R_M \approx R_{CMIN}$.

The maximum gate-source voltage of M_{N1} and M_{N2} under dynamic conditions is given by $V_{GSMN1,2}^{max} = V_{GSMN1,2}^{Q} + \Delta V_{Mmax} = V_{DSsatMN1,2} + |V_{th}| + I_{bias} R_{CMIN}$. The maximum current at nodes $V_{o1,o1'}$ is then given by (A2).

$$\begin{aligned} I_{MN1,2}{}^{\max} &= \beta_{MN1,2} (V_{GSMN1,2}^{\max} - |V_{th}|)^2 \\ &= \beta_{MN1,2} (V_{DSsat\,MN1,2} + |V_{th}| + I_{bias} R_{CMIN} - |V_{th}|)^2 \end{aligned} \tag{A2}$$

where $\beta_{MN1,2} = \frac{1}{2} \mu_n C_{OX} \left(\frac{W}{L}\right)_{MN1,2}$.

Considering $M = I_{bias} R_{CMIN} / V_{DSsatMN1,2}$, $I_{MN1,2max}$ can be expressed by (A3).

$$\begin{aligned} I_{MN1,2\,\max} &= \beta_{MN1,2} (M+1)^2 V_{DSsatMN1,2}^2 \\ &= I_{biasMN1,2} (M+1)^2 \end{aligned} \tag{A3}$$

As mentioned in Section II.B, in the proposed design, values $R_{CMIN} = 8k\Omega$ were used, which led to $M = 1.4$ and $I_{MN1,2max} \approx 6 I_{biasMN1,2}$.

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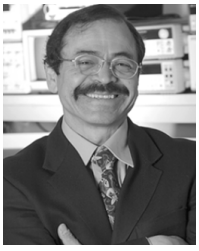
ANINDITA PAUL (Member, IEEE) received the degree in VLSI design from the Institute of Radio Physics and Electronics, University of Calcutta, and the Ph.D. degree in electrical engineering from the Klipsch School of Electrical Engineering, New Mexico State University (NMSU). She worked as a Visiting Assistant Professor with the Department of Electrical and Computer Engineering, Manhattan College, New York, in 2020. She is currently working as an Assistant Professor with the Rayen School of Engineering, Youngstown State University, Youngstown, OH, USA. Her research interests include low-voltage and low-power analog integrated circuit design. She was a recipient of the Graduate Assistant Award for Academic and Research Achievement from the College of Engineering, NMSU, in 2019.



JAIME RAMÍREZ-ANGULO (Life Fellow, IEEE) received the B.Sc. and M.S.E.E. degrees from the National Polytechnic Institute, Mexico City, Mexico, in 1974 and 1976, respectively, and the Ph.D. degree from the University of Stuttgart, Germany, in 1982. He was a Professor with the National Institute for Astrophysics Optics and Electronics, Mexico, and Texas A&M University, College Station, TX, USA. He is currently a Distinguished Award Professor with the National Institute for Astrophysics Optics and Electronics. He has authored 200 papers in international conferences. His current research interests include low-voltage low-power analog circuit design, A/D and D/A conversion, and analog and mixed-signal processing.

ALEJANDRO DÍAZ SÁNCHEZ (Member, IEEE) received the B.E. degree from the Madero Technical Institute, México, the M.Sc. degree from the National Institute for Astrophysics, Optics, and Electronics, México, and the Ph.D. degree in electrical engineering from New Mexico State University at Las Cruces, NM, USA. He is currently working as a Full Professor with the National Institute for Astrophysics, Optics, and Electronics, Tonantzintla, Mexico. His research interests include analog, mixed-signal and digital integrated circuits, high-performance computer architectures, and signal processing.

ANTONIO J. LÓPEZ-MARTÍN (Senior Member, IEEE) received the M.S. and Ph.D. degrees (Hons.) from the Public University of Navarra, Pamplona, Spain, in 1995 and 1999, respectively. He was a Visiting Professor with New Mexico State University, USA. He is currently a Professor with the Public University of Navarra. He has authored or coauthored over 400 technical contributions in books, journals, and conferences. He holds six international patents. His current research interests include wireless transceivers and sensor interfaces with emphasis on low-voltage low-power implementations. He was a recipient of the Talgo Technological Innovation Award, in 2012, the Caja Navarra Research Award, in 2007, the Young Investigator Award from the Completeness University of Madrid, in 2006, the 2005 IEEE Transactions on Education Best Paper Award, and the European Center of Industry and Innovation Award for excellence in the transfer of research results to industry, in 2004. He was an Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, from 2006 to 2007, and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I: REGULAR PAPERS, from 2008 to 2009.

RAMON GONZALEZ CARVAJAL (Fellow, IEEE) received the M.Sc. degree in electrical engineering and the Ph.D. degree (Hons.) from the University of Seville, Seville, in 1995 and 1999, respectively. He joined the Department of Electronic Engineering, School of Engineering, University of Seville, as an Associate Professor, in 1996, where he became a Professor, in 2002. He joined the Klipsch School of Electrical Engineering, USA, in 1999. He has authored or coauthored over 60 articles in international journals. He has authored 200 papers in international conferences. His current research interests include low-voltage low-power analog circuit design, A/D and D/A conversion, and analog and mixed-signal processing.

FRANK X. LI (Member, IEEE) received the B.S. degree in electrical engineering from Ohio State University, in 1996, the master's degree from Youngstown State University, in 1999, and the Ph.D. degree from Case Western Reserve University, in 2005. He joined the Department of Electrical and Computer Engineering, Youngstown State University, as an Assistant Professor, in August 2006, after serving ferrous and non-ferrous metal industry for eleven years. He advanced in academic rank to an Associate Professor and a Professor, in 2011 and 2016, respectively. He is currently working as the Acting Chair of the Rayen School of Engineering, YSU. His current research interests include autonomous power conversion, software engineering, RF engineering, wireless networks, VLSI, and applied magnetic fields.