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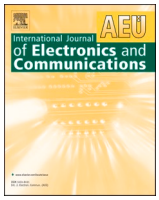

Regular paper

Reducing the nonlinearity and harmonic distortion in FD-SOI CMOS current-starved inverters and VCROs

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ABSTRACT

This paper demonstrates experimentally how to reduce the nonlinearity of some analog and mixed-signal circuits by using the enhanced body effect provided by Fully-Depleted Silicon on Insulator (FD-SOI) CMOS technology. A current-starved CMOS inverter and a Voltage-Controlled Ring Oscillator (VCRO) are considered as case studies. The inverter is configured as a simple amplifier stage in which the harmonic distortion can be reduced and even removed by the combined action of the control voltages applied at the gate and bulk terminals of the current-source transistors. This current-starved inverter is used as the basic building block of a VCRO, where a more linear voltage-to-frequency characteristic can be achieved if the bulk terminal is used as the control voltage of the oscillator. The circuits under study have been designed and fabricated in a 28-nm FD-SOI technology and experimental results are shown to validate the presented approach.

1. Introduction

As CMOS technology is evolving towards the nanoscale, there are a number of design challenges that arise to design Analog and Mixed-Signal (AMS) circuits. One of the most limiting factors is the reduction of supply voltages below 1 V, which makes it difficult to design such circuits while keeping the required Dynamic Range (DR) with low power consumption and high linearity. Among the technology alternatives, those based on Fully Depleted (FD) devices are becoming mainstream processes, namely: Fin-FET and FD Silicon-On-Insulator (FD-SOI). The former is widely used nowadays as mainstream for Digital Signal Processing (DSP) [1,2], while the latter is featuring very promising results to design AMS/RF circuits and systems where ultra-low power consumption is a must [3–7].

The use of the so-called *digital-based analog solutions* and *time-based signal processing* postulate as a good alternative for the implementation of AMS and Radio-Frequency (RF) front-ends and analog/digital interfaces in many diverse applications such as biomedical devices and Internet-of-Things (IoT) end-terminals [8–11]. However, one of the main limitations of time/frequency-based analog techniques is the nonlinear error associated to the voltage-to-frequency (V-to-F) transformation required to move from amplitude-based to time-based signal processing [11].

Prior art on FD-SOI shows that this technology is potentially better than (bulk) CMOS to design high-linearity AMS circuits with reduced supply voltages [12,13]. However, to the best of authors' knowledge, previous works were only based on theoretical analyses and simulation results [14]. This paper goes from theory to practice and shows the first experimental evidences which demonstrate that the use of the bulk terminal, rather than gate terminal – used as either input or control node – can benefit from the enhanced body effect provided by FD-SOI to improve the linearity of AMS circuits. Two circuits – integrated in a 28-nm technology – are considered as case studies: a current-starved CMOS inverter and a VCRO. These circuits are building blocks of a number of AMS circuits and systems, including filters, Analog-to-Digital Converters, Phase-Locked Loops (PLLs), just to cite some examples. Measurement results are shown to validate prior theoretical predictions and open the doors to exploit FD-SOI technology to design analog and mixed-signal circuits and systems with enhanced linearity and DR in those applications requiring low energy consumption with reduced supply voltage.

The paper is organized as follows. After this introduction, Section 2 describes the current-starved inverter circuit used as example, and analyses its performance in terms of linearity and harmonic distortion. The use of such inverter as the basic cell of VCROs is shown in Section 3. Finally, experimental results are shown in Section 4 and conclusions are

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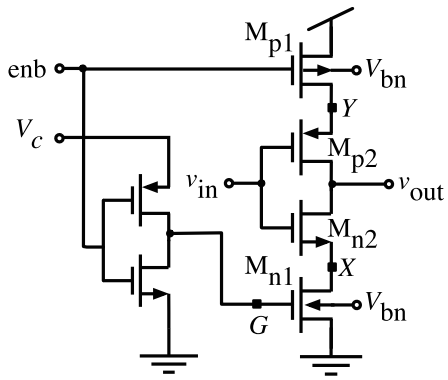

Fig. 1. Schematic of the bulk-controlled current-starved inverter.

drawn in Section 5.

2. Bulk-controlled Current-Starved Inverter

Fig. 1 shows the schematic of the current-starved inverter under study [14]. The bias current which flows through the inverter – made up of transistors M_{p2} and M_{n2} – is provided by transistors M_{p1} and M_{n1}, which are configured as current sources. These current-source transistors are controlled by voltage V_c – connected at the gate of M_{n1} through a source-follower circuit – and by the bulk voltage, V_{bn} – connected at the body terminal of both M_{p1} and M_{n1}. An enable signal, denoted as `enb` in Fig. 1, is used to turn the inverter off or on – a functionality used by some types of VCROs such as Gated switched-Ring Oscillators (GROs) in order to make the oscillator either to oscillate or to stop running [9]. For the analysis that follows, it will be considered that the node `enb` is connected to ground.

2.1. Enhanced Body Effect in FD-SOI Technology

The proposed current-starved inverter has been designed in a FD-SOI process in order to take advantage of its enhanced body effect as compared to a bulk CMOS process [3]. The bulk terminal of MOS transistors in FD-SOI technology can be biased by a wider voltage range, which increases the body effect, and therefore, the tuning range of the threshold voltage, V_{th}, with the voltage applied at the bulk terminal, by a linear relationship given by [3]:

$$V_{thn} = V_{thn0} - r_n \cdot V_{bn}, |V_{thp}| = |V_{thp0}| + r_p \cdot V_{bp} \tag{1}$$

where V_{bn} and V_{bp} are the voltages applied at the bulk terminals of an nMOS and a pMOS transistor; V_{thn0} and V_{thp0} are the zero-bias threshold voltages of nMOS and pMOS, respectively; and r_n and r_p stand for the corresponding body factors. In the technology under study, a 28-nm FD-SOI process, the values of V_{thn0} and V_{thp0}, are respectively $V_{thn0} = 326\text{mV}$ and $V_{thp0} = 335\text{mV}$ for minimum-size transistors, while $r_n \simeq 70\text{mV/V}$ and $r_p \simeq 80\text{mV/V}$ [14].

2.2. Harmonic Distortion in Current-Starved Inverter Amplifiers

For the analysis that follows, let us consider that all transistors are working in strong inversion and in saturation region, so that the drain-source current of an nMOS transistor can be expressed as[2]:

$$I_{DS} = \frac{\beta_n}{2}(V_{GS} - V_{th})^2 \cdot (1 + \lambda \cdot V_{DS}) \tag{2}$$

where V_{GS} and V_{DS} stand for the gate-source and drain-source voltages; $\beta_n = \frac{W}{L}\mu_n C_{ox}$; μ_n is the mobility of electrons; C_{ox} is the gate-oxide capacitance per unit area; λ is the channel-length modulation parameter; and W and L, are respectively the transistor channel width and length of the nMOS transistor. The small-signal transconductance, $g_m \simeq \beta_n(V_{GS} - V_{th})$, and its derived performance metrics, such as intrinsic voltage gain, $A_v \equiv g_m/g_{ds}$, transconductance efficiency, $gm\text{ID} \simeq g_m/I_{DS}$, and transit frequency, $f_T \equiv g_m/C_g$, can also benefit from the body biasing [3].

In the case of a current-starved inverter as that shown in Fig. 1, the current flowing through the main inverter, denoted as I_Q, can be expressed as:

$$I_Q = I_{DS}|_{n1} = I_{DS}|_{n2} = I_{DS}|_{p1} = I_{DS}|_{p2} \tag{3}$$

where $I_{DS}|_{n1,2}$ and $I_{DS}|_{p1,2}$ stand for the drain-source currents of $M_{n1,2}$ and $M_{p1,2}$, respectively given by:

$$I_{DS}|_{n1} = \frac{\beta_n}{2}(V_G - V_{thn})^2 \cdot [1 + \lambda \cdot V_X] \tag{4}$$

$$I_{DS}|_{n2} = \frac{\beta_n}{2}(V_{in} - V_X - V_{thn0})^2 \cdot [1 + \lambda \cdot (V_{out} - V_X)] \tag{5}$$

$$I_{DS}|_{p1} = \frac{\beta_p}{2}(V_{dd} - |V_{thp}|)^2 \cdot [1 + \lambda \cdot (V_{dd} - V_Y)] \tag{6}$$

$$I_{DS}|_{p2} = \frac{\beta_p}{2}(V_Y - V_{in} - |V_{thp0}|)^2 \cdot [1 + \lambda \cdot (V_Y - V_{out})] \tag{7}$$

where V_{dd} is the supply voltage; β_n and β_p stand for the β of $M_{n1,2}$ and $M_{p1,2}$ respectively; $V_{G,X,Y}$ are the voltages at internal nodes G, X, Y (see Fig. 1), and it has been assumed that λ is the same for both nMOS and pMOS transistors.

Let us consider the expressions of $V_{thn,p}$ given in (1). Replacing these expressions in (4) and (6), and solving the set of equations in (4)–(7), the output voltage of the inverter, V_{out}, can be derived as a function of the input, V_{in}, and the control voltages, V_c and V_{bn}, i.e.

$$V_{out} = f[V_{in}, V_c, V_{bn}] \tag{8}$$

Applying a Taylor series expansion of (8), it can be shown that the input–output characteristic of the inverter in its amplification region can be approximated by a polynomial function as:

$$V_{out} \simeq \alpha_{0_{[V_c,V_{bn}]}} + \alpha_{1_{[V_c,V_{bn}]}} \cdot V_{in} + \alpha_{2_{[V_c,V_{bn}]}} \cdot V_{in}^2 + \alpha_{3_{[V_c,V_{bn}]}} \cdot V_{in}^3 + \ldots \tag{9}$$

where α_0 is the DC (operating-point) output voltage; α_1 stands for the linear gain of the inverter; and coefficients α_i (with $i > 1$) are the i-th order nonlinear gain coefficients. Note that all these polynomial coefficients, α_i, depend on the control voltages V_c and V_{bn} – denoted in (9) as $\alpha_{i_{[V_c,V_{bn}]}}$.

For the sake of simplicity, let us assume that $\beta_n = \beta_p$. Considering that a sinewave signal is applied at the input, the second- and third-order Harmonic Distortion (HD) coefficients can be approximated by the following expressions:

$$HD_2 \equiv \frac{\alpha_1}{2\alpha_2} \cdot V_{in} \simeq \left[\frac{1}{4(V_{inDC} - V_{thn0})} - \frac{3\lambda(V_{dd} - V_{thn})^2}{4(V_c - V_{dd})(V_c + V_{dd} - 2V_{thn})}\right] \cdot V_{in} \tag{10}$$

$$HD_3 \equiv \frac{\alpha_1}{4\alpha_3} \cdot V_{in}^2 \simeq \frac{\lambda(V_{dd} - V_{thn})^2}{4(V_{dd} - V_c)(V_{inDC} - V_{thn0})(V_c + V_{dd} - 2V_{thn})} \cdot V_{in}^2 \tag{11}$$

where V_{in} is the amplitude of the input sinewave and V_{inDC} stands for the

[2] A simplified first-order model is used in this work to get some insight about the harmonic distortion in FD-SOI inverters. More accurate models (including second-order effects) can be considered, although they will lead to more complex mathematical expressions, without adding significant information to the purposes of this research work.

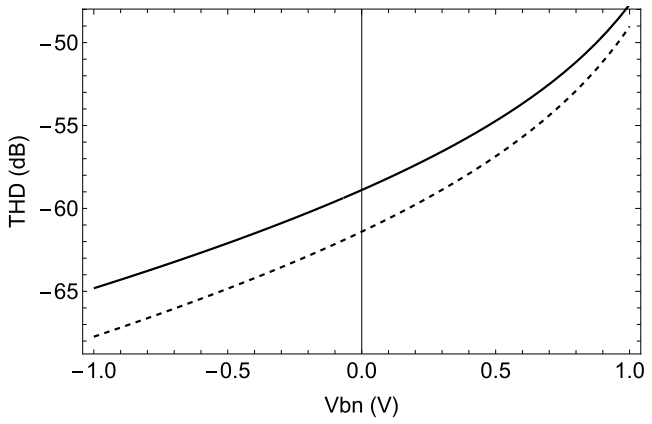

Fig. 2. THD vs. V_{bn} for $V_c = 0.5$V (dashed line) and $V_c = 0.8$V (solid line).

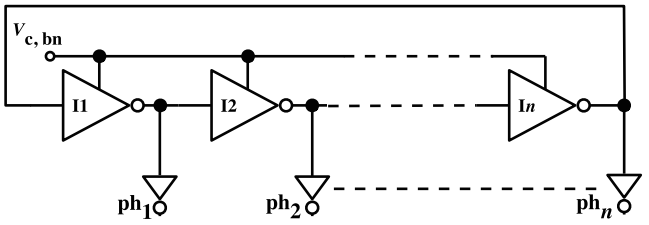

Fig. 3. Conceptual schematic of the bulk-controlled VCRO under study.

DC (operating-point) input voltage. The Total Harmonic Distortion (THD) can be approximated by the sum of the contributions of the first two harmonic coefficients (HD_2 and HD_3) as:

$$\text{THD} \equiv \sqrt{\sum_{n=1}^{\infty} \text{HD}_i^2} \simeq \sqrt{\text{HD}_2^2 + \text{HD}_3^2} \tag{12}$$

Fig. 2 depicts the theoretical estimation of THD vs. V_{bn}, where it can be seen how the harmonic distortion can be modulated by the combined action of V_c and V_{bn} as will be demonstrated by experimental measurements.

3. Bulk-controlled VCRO

Fig. 3 shows the conceptual schematic of the bulk-controlled VCRO used as circuit example in this work. It consists of a ring oscillator made up of current-starved inverters (`I1, 2...n`) as that shown in Fig. 1. The output of each inverter – denoted as ph_i ($i = 1, 2...n$)– can be taken to generate a multi-phase output. Note that the circuit can be configured either as a GRO or as a VCRO, depending on the value of the enable signal –denoted as `enb` in Fig. 1. Thus, if `enb` switches between OFF (logic "0") and ON (logic "1") states, this will cause the VCO to oscillate or get frozen. The operation of the VCRO is governed by voltages V_c and V_{bn}. These voltages control the operation of each VCO (inverter) cell – depicted in Fig. 1.

The oscillation frequency, f_{osc}, can be expressed as:

$$f_{osc} = \frac{1}{2 \cdot m_{ph} \cdot \tau_d(V_c, V_{bn})} \tag{13}$$

where m_{ph} is the number of inverters, i.e. the number of phases of the VCRO (see Fig. 3), and τ_d stands for the propagation delay of each inverter-based VCRO cell. This delay depends on the charging/discharging time of the load capacitance at each inverter output, which is in turn a function of the current flowing through the inverter – controlled by V_c and V_{bn}. Thus, the overall propagation delay can be expressed as:

$$\tau_d = \tau_{LH} + \tau_{HL} \tag{14}$$

where τ_{LH} and τ_{HL} stand respectively for the charging ("Low–High") and discharging ("High-Low") transient times.

Let us consider that the VCRO cell is implemented using FD-SOI, and hence, V_{thn} depends on V_{bn} according to (1). In this case, it can be shown that [14]:

$$f_{osc} \simeq f_q + k_{VCO_2} \cdot V_{bn} + k_{22} \cdot V_{bn}^2 \tag{15}$$

where $f_q = \alpha_{osc} \cdot (V_c - V_{thn0})^2$, $k_{VCO_2} = 2 \cdot \alpha_{osc} \cdot (V_c - V_{thn0})$, $k_{22} = \alpha_{osc} \cdot r_n^2$ and $\alpha_{osc} = \beta_n / (2 \cdot m_{ph} \cdot C_L \cdot V_{dd})$.

Note from (15) that only a second-order nonlinearity is obtained in the case of FD-SOI bulk-input controlled VCRO cells. However, in the case of conventional bulk processes, higher-order nonlinear terms (3rd-order, 4th-order, etc.) are obtained [14]. Let us consider now the most conventional situation in which the control voltage of the VCRO cell is V_c, and there is not any body effect, i.e. $V_{bn} = 0$. In this case, it can be shown that the oscillation frequency is given by:

$$f_{osc} \simeq \alpha_{osc} \cdot V_{thn0}^2 - 2\alpha_{osc} \cdot V_{thn0} \cdot V_c + \alpha_{osc} \cdot V_c^2 \tag{16}$$

Comparing (15) and (16), it is clear that in both cases, quadratic dependencies on the control voltages are obtained. However, the second-order nonlinear term (k_{22}) in FD-SOI case – Eq. (15) is attenuated by the body factor, which in a 28-nm technology process is $r_n \simeq 70$mV/V, i.e. almost two orders of magnitude lower than the nonlinearity obtained in the case of conventional gate-controlled VCROs – Eq. (16).

An estimation of the nonlinear error can be computed as [15]:

$$\epsilon_{osc} = \frac{f_{osc} - f_{osc-ideal}}{f_{osc-ideal}} \tag{17}$$

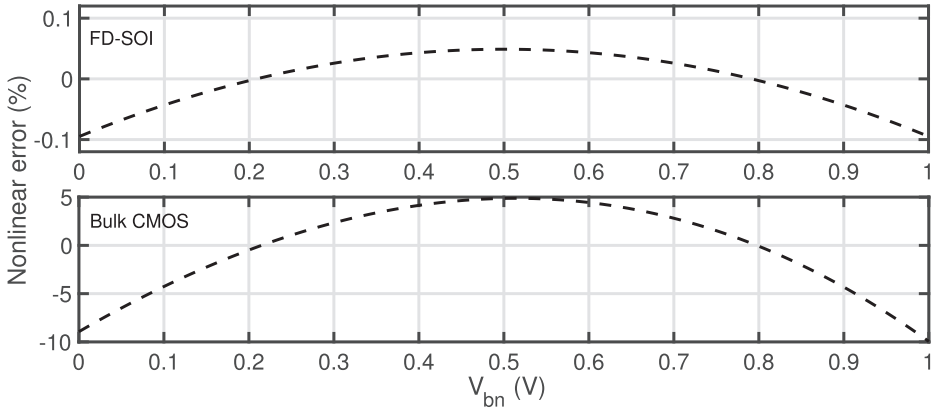

Fig. 4. Nonlinear error of the V-to-F characteristic in VCROs: FD-SOI versus bulk CMOS.

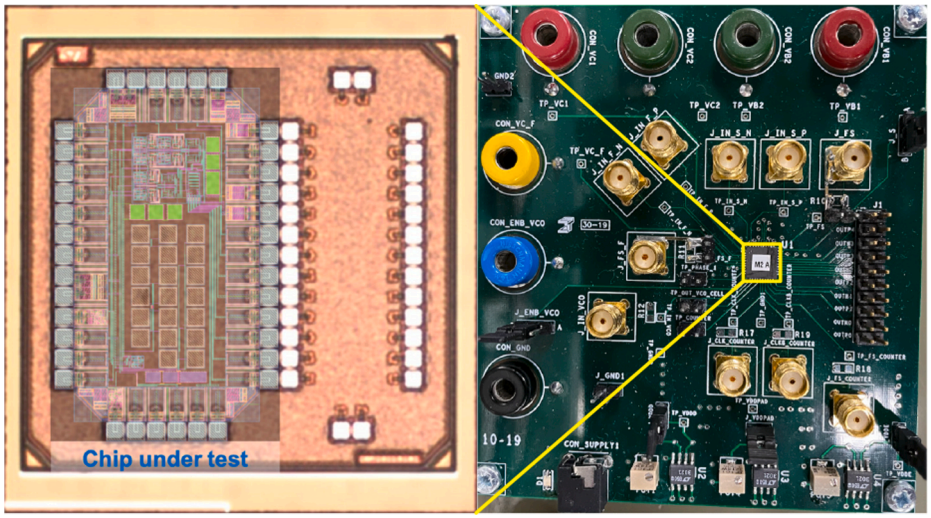

Fig. 5. Chip microphotograph (including the chip layout superimposed inset) and test PCB.

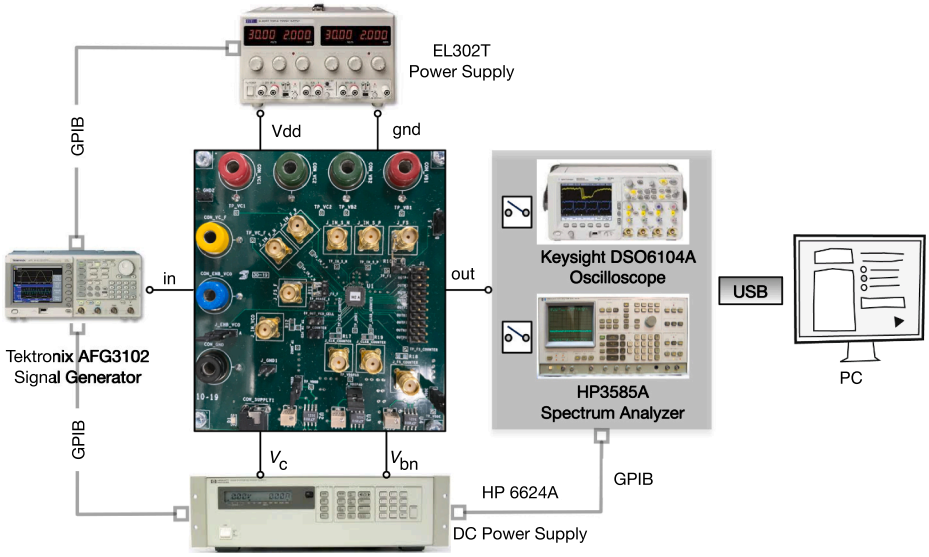

Fig. 6. Conceptual diagram of the test set-up.

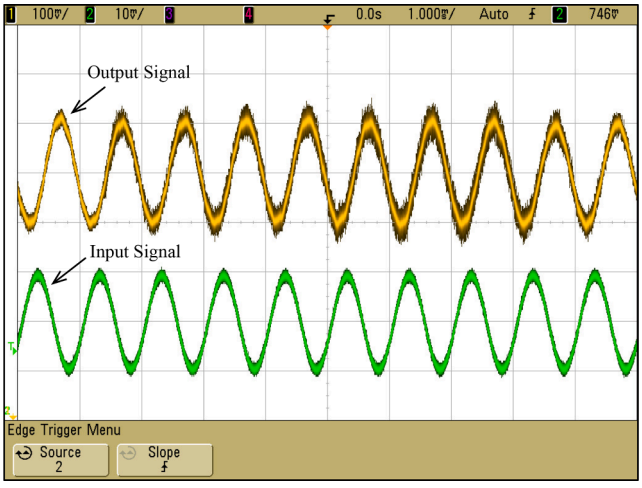

Fig. 7. Input and output waveforms of the current-starved inverter (VCO-cell).

where $f_{\mathrm{osc-ideal}}$ stands for the ideal (perfectly linear) V-to-F characteristic.

As an illustration, Fig. 4 shows the theoretical nonlinear error of a VCRO by considering an FD-SOI technology and a bulk CMOS process. It can be shown how the use of enhanced body effect allows to reduce ϵ_{osc} by more than two orders of magnitude. This theoretical prediction is confirmed by experimental results as shown below.

4. Experimental results

In order to validate the presented approach, the circuits under study have been designed and fabricated in a 28-nm FD-SOI technology from STMicroelectronics. Fig. 5 shows a microphotograph of the chip and a picture of the Printed Circuit Board (PCB) used for testing purposes. The latter includes additional circuitry such as voltage regulators, decoupling capacitors and connectors for the instruments required to measure the chip. Due to the opacity of passivation materials and top metals, the layout of the chip is superimposed on the chip microphotograph in order to distinguish the different subcircuits inside the chip. A 40-pin Quad-Flat No-leads (QFN) package is used for the device under test, which

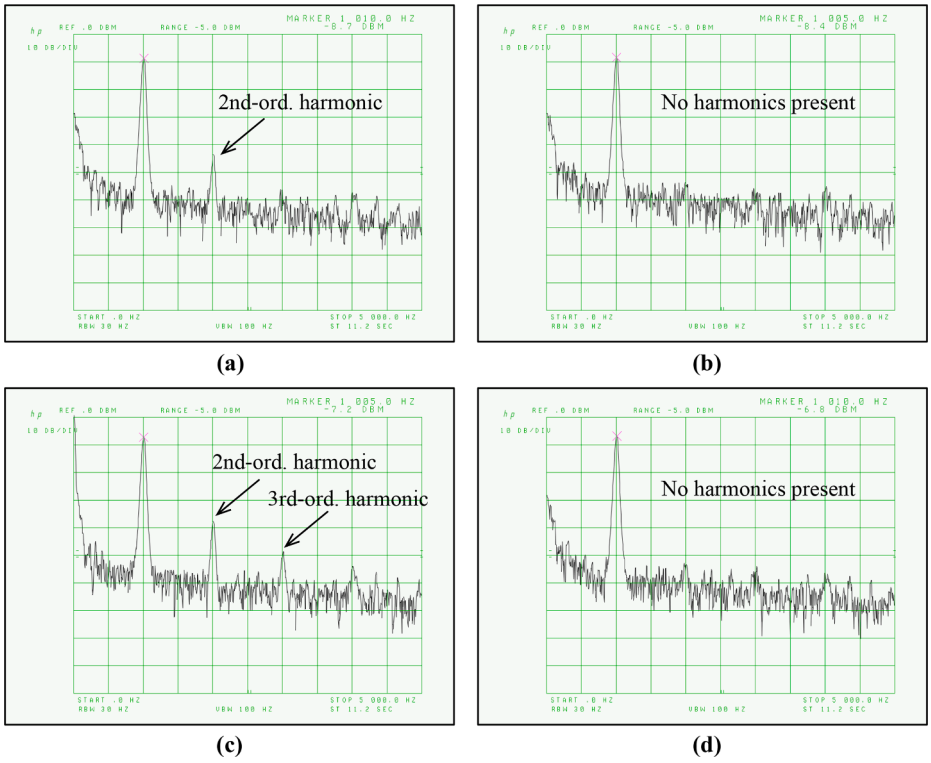

Fig. 8. Effect of varying V_c and V_{bn} on the harmonic distortion of the VCO-cell, considering an input signal amplitude of (a)-(b) V_{in} = 25mVpp and (c)-(d) V_{in} = 30mVpp.

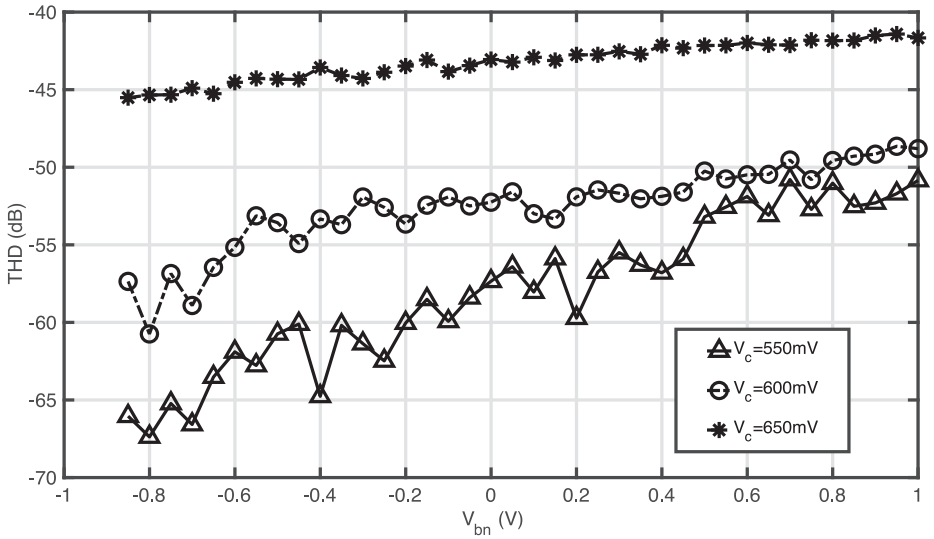

Fig. 9. THD vs. V_{bn} for different values of V_c and V_{in} = 25mVpp.

is integrated in the same die with another chip not related to this work. The silicon area is 590μm x 975μm including bonding pads and a nominal supply voltage of 1 V and regular-V_{th} transistors [3] have been used to design the circuits in this work.

Fig. 6 shows the measurement set-up. A programmable DC signal supply generator (HP 6624A) is used to sweep the values of V_c and V_{bn}, while an EL302T equipment provides the supply voltage of 1 V. In the case of the current-starved inverter (VCO-cell), a sinewave signal is generated using a Tektronix AFG3102 signal generator. The output voltage of both circuits, i.e. the inverter and the VCO, are captured by a (Keysight DSO6104A) oscilloscope to get the waveforms and an (HP3585A) spectrum analyzer to obtain the output spectra. All instruments are controlled through General Purpose Interface Bus (GPIB) and USB by a PC, where the measured data is processed in MATLAB®.

4.1. Harmonic Distortion in Current-Starved Inverters

Let us consider that a sinewave signal with amplitude 25mVpp and 1-kHz frequency is applied at the input node of the current-starved inverter in Fig. 1. The input DC voltage is V_{inDC} = 746mV, such that the inverter is operating in the amplification region, i.e. it behaves as an inverting amplifier. The output voltage amplifies the input signal as illustrated in the measured waveforms shown in Fig. 7, where a voltage

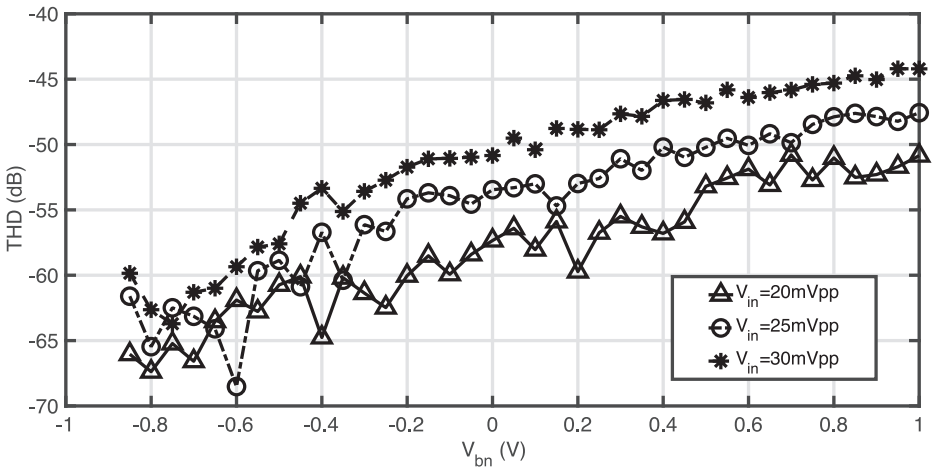

Fig. 10. THD vs. V_{bn} for $V_c = 550$ mV and different values of V_{in}.

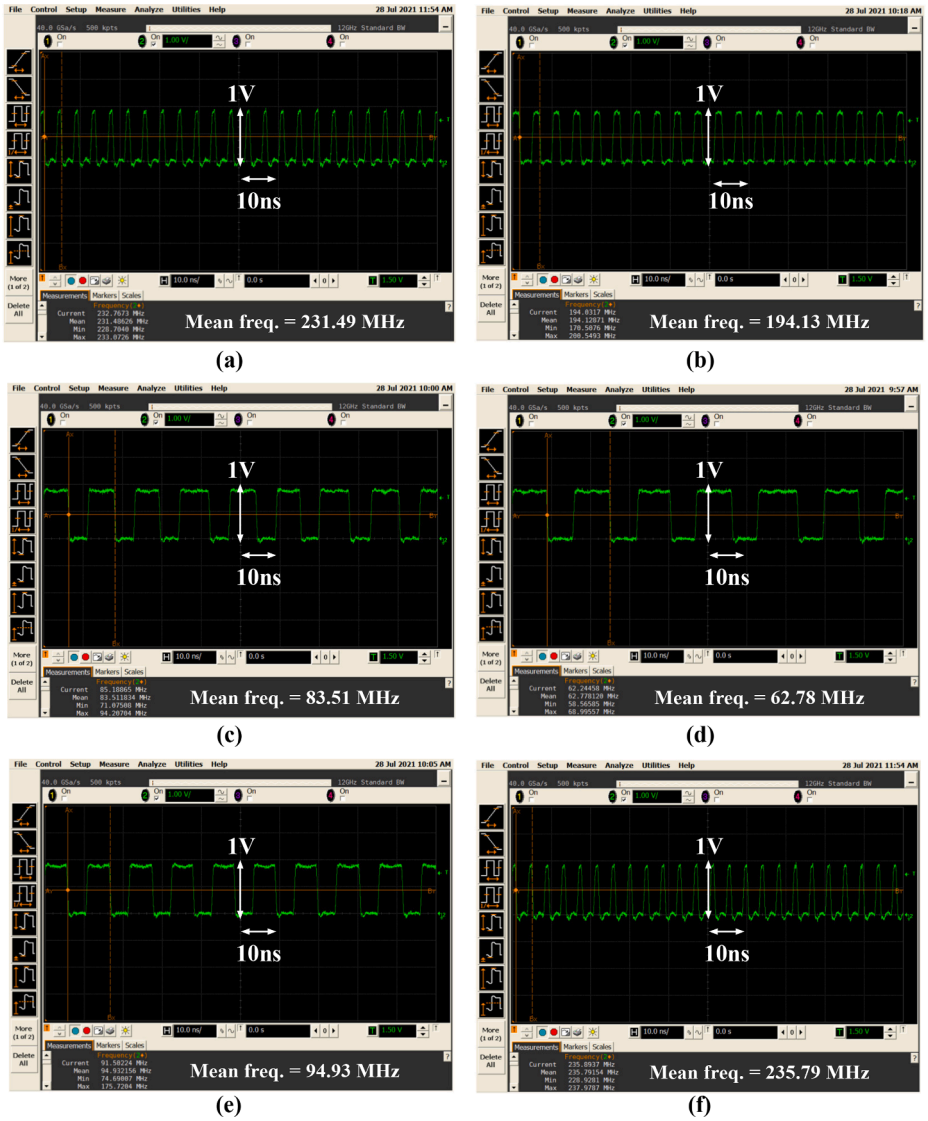

Fig. 11. VCO output waveforms for different cases of V_c and V_{bn}. (a) $V_c = 900$ mV, $V_{bn} = 500$ mV; (b) $V_c = 700$ mV, $V_{bn} = 500$ mV; (c) $V_c = 500$ mV, $V_{bn} = 750$ mV; (d) $V_c = 500$ mV, $V_{bn} = 250$ mV; (e) $V_c = 500$mV, $V_{bn} = 1$V; (f) $V_c = 1$ V, $V_{bn} = 500$ mV.

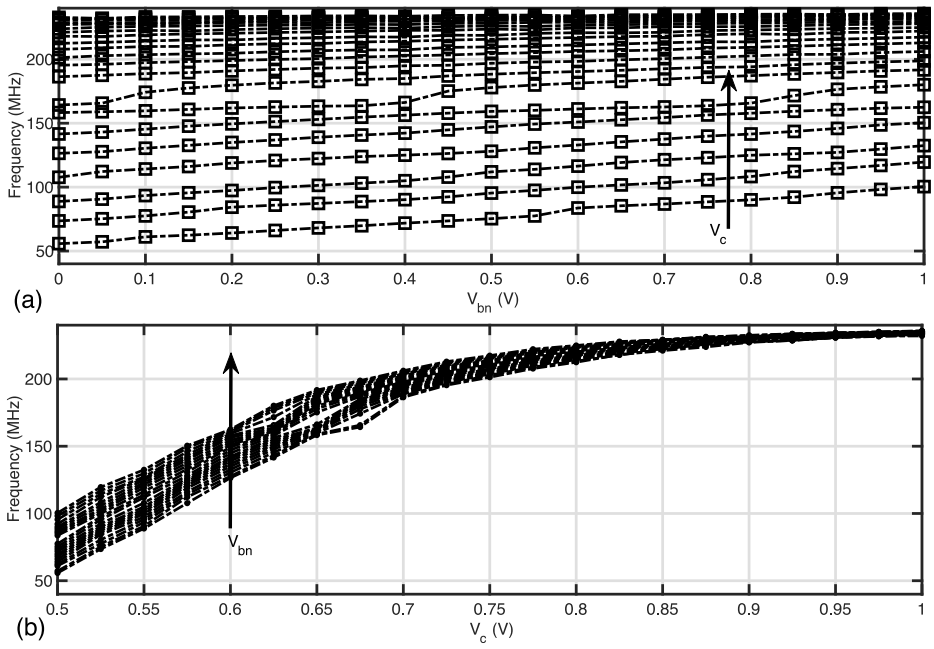

Fig. 12. Measured V-to-F characteristic of the VCRO considering (a) a bulk-input (V_{bn}) and (b) a gate-input (V_c).

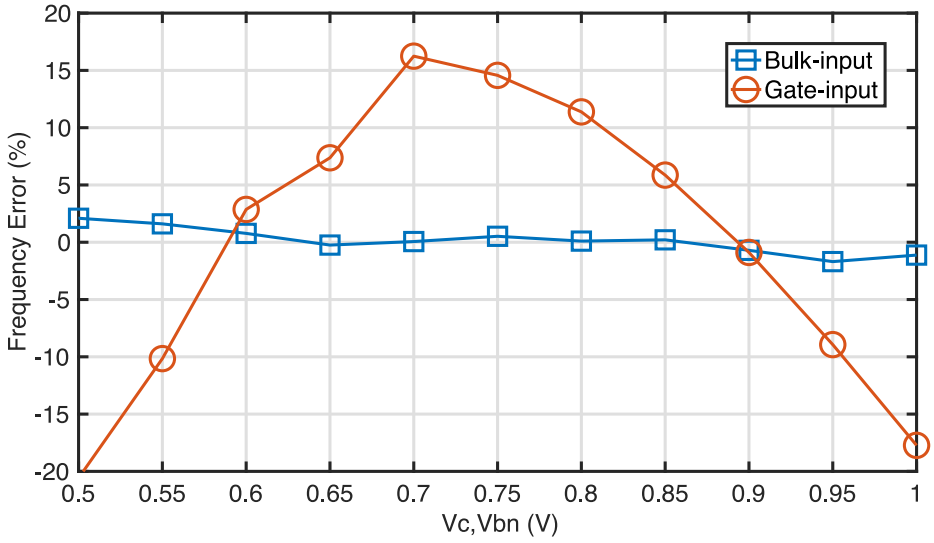

Fig. 13. Measured nonlinear error of the VCRO considering a bulk-input (V_{bn}) and a gate-input (V_c).

gain of about 10 can be observed.

As stated in previous sections, the combined action of V_c and V_{bn} can improve the linearity of the circuit. This is illustrated in Fig. 8, where several output spectra of the circuit in Fig. 1 are shown for different values of the input signal amplitude, V_{in} = 25Vpp (Fig. 8)) and V_{in} = 30Vpp (Fig. 8(c)-(d))). Note that in both cases, the harmonic distortion can be reduced, and even removed, by properly choosing the values of V_c and V_{bn}.

Fig. 9 represents the measured THD versus V_{bn} for V_{in} = 25mVpp and different values of V_c. It can be shown how the enhanced body effect inherent to FD-SOI MOS transistors allows to improve the linearity of the circuit, thanks to the wider tuning range of V_{bn} and the enhanced body effect, as stated in Section 2. The influence of this enhanced body effect on the linearity is modulated by the value of V_c as predicted by theory, since the operating point of the current-starved inverter is more sensitive to the variation of V_c as compared to the changes in V_{bn}. Obviously, as the input signal amplitude increases, the THD will increase as well, as depicted in Fig. 10, where THD is shown as a function of V_{bn} for V_c = 550mV and different values of V_{in}. Overall, an improvement of 25–30 dB in the THD can be achieved by properly choosing the values of control voltages V_c and V_{bn}.

4.2. Nonlinear Error in VCROs

Compared with bulk CMOS technologies, the enhanced body effect allows to further reduce the harmonic distortion and improve the linearity of some circuits based on inverters. This is the case of the VCRO shown in Fig. 3. The oscillation frequency of this circuit can be varied by two different control signals, either the gate voltage, V_c, or the bulk voltage, V_{bn}. This is illustrated in the waveforms shown in Fig. 11, where the measured output signal waveform is shown for different cases of V_c and V_{bn}.

Fig. 12 shows the measured Voltage-to-Frequency (V-to-F) characteristic of the circuit, considering two control voltages, either gate-

controlled, i.e. V_c as control voltage, or bulk-controlled, i.e. V_{bn}. As expected, the bulk-controlled case features a more linear V-to-F characteristic than the gate-controlled case. This is better illustrated in Fig. 13, where it is shown how the use of bulk-input voltage drastically reduces the nonlinear error, at the price of reducing the frequency tuning range with respect to the gate-input control case. However, both control voltages, i.e. V_c and V_{bn} can be combined to increase the programmability of the VCRO in terms of frequency range – by using V_c – and nonlinear frequency error – by using V_{bn}, thanks to the combined action of both voltages. This feature – predicted by theory in [14] – is confirmed by the experimental results shown in this paper.

5. Conclusions

The enhanced body effect provided by FD-SOI CMOS technology can be used to improve the performance of analog and mixed-signal circuits as compared to the use of bulk-based CMOS. This has been demonstrated in this paper by several experimental results taken from a current-starved inverter and a bulk-controlled VCRO. It has been shown how measurements of the THD of an inverter amplifier and the nonlinearity of the V-to-F characteristic of a VCRO can be notably reduced or even removed by the combined action of gate- and bulk-based control voltages. These experiments validate prior theoretical predictions and provide an alternative approach to design high-performance analog circuits in deep nanomenter processes with reduced supply voltages.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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