Efficient Realization of RTD-CMOS Logic Gates

Juan Núñez, María J. Avedillo and José M. Quintana
IMSE-CNM-CSIC and Universidad de Sevilla
Av. Américo Vespucio s/n
41092, Seville (SPAIN)
+34954466666
{jnunez, avedillo, josem}@imse-cnm.csic.es

ABSTRACT
The incorporation of Resonant Tunnel Diodes (RTDs) into III/V transistor technologies has shown an improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption. Currently, the incorporation of these devices into CMOS technologies (RTD-CMOS) is an area of active research. Although some works have focused the evaluation of the advantages of this incorporation, additional work in this direction is required. This paper compares RTD-CMOS and pure CMOS realizations of a set of logic gates which can be operated in a gate-level nanopipelined. Lower average power and energy per cycle are obtained for RTD/CMOS implementations.

Categories and Subject Descriptors
B.7.1 [**Integrated circuits**]: Types and Design Styles - *advanced technologies*.

General Terms
Design

Keywords
Resonant Tunneling Diode, Emerging Technologies, Logic Gates, CMOS.

1. INTRODUCTION
Resonant tunneling devices (RTDs) are nowadays considered the most mature type of quantum-effect devices. They are already operating at room temperature and they exhibit very attractive characteristics as high-speed operation and low power consumption. RTDs are very fast non linear circuit elements which have been integrated with transistors to create novel quantum devices and circuits. This incorporation of tunnel diodes into III/V transistor technologies has shown an improved circuit performance: higher circuit speed, reduced component count, and/or lowered power consumption [1], [2], [3].

The degree of development of resonant tunneling devices is very different. RTDs fabricated in III-V are, undoubtedly, the most mature and most reported circuits based on resonant tunneling use them combined with different types of transistors. Since the currently dominant technologies use silicon, plenty of efforts are being devoted to develop devices with negative resistance in this material. The resulting diodes have provided worse performance than those achieved in III-V technologies. Currently, the realization of tunnel diodes in silicon is a very active research area where progresses are expected. In fact, it has been suggested that the addition of RTDs to CMOS technology could extend its life and even make investments rentable. It has been shown the integration of Resonant Interband Tunneling Diodes (RITDs) with standard CMOS [4] and SiGe HBT [5]. It has been also reported a RITD with a cutoff frequency of 20GHz, allowing for the first time, applications of mixed signal, RF and high speed logic circuits [6]. Simpler and compatible with CMOS process to fabricate Tunneling Diodes have been recently reported: structures that do not need Ge are described in [7], and in [8] a fabrication process based on CVD (Chemical Vapor Deposition) instead of MBE (Molecular Beam Epitaxy) is presented.

Another explored option is the development of procedures for III-V RTDs compatible with silicon substrates. Recently importance advances have been achieved in this area, such us the Tunneling Diodes in III-V materials and Ge using ART (Aspect Ratio Trapping) [9], [10].

Some works have focused the evaluation of the advantages of incorporating RTDs to CMOS technologies. In [11], the keeper transistor of the domino logic gates is replaced by an RTD, which significantly increases the noise immunity without affecting the area, delay and power consumption. A static memory cell is described in [12], consisting of the incorporation of a well-known DRAM cell topology with a pair of RTDs. This structure improves the performance of a typical 6-transistors SRAM cell in terms of the static power consumption in three orders of magnitude.

However, in our opinion, additional work in this direction is required. In particular, in the field of logic circuits, estimations of performance/count devices improvements obtained through the addition of RTDs have been evaluated for a set of logic functionalities (combinational gates and flip-flops) [13], [14], [15], but without taking into account their usage in gate networks. This is a key point, because as it will be explained in next section, RTD logic gates allow the implementation of a pipeline at the gate level. That is, each gate is a pipeline stage and thus it should be compare to CMOS logic styles operating in a similar way. Moreover, up to our knowledge there is a lack of recent studies in this area and as a consequence no data involving current technologies are available. This paper addresses these

issues and contributes to provide results on how RTD-CMOS realizations compare to pure CMOS gate-level pipelined ones when implemented in a commercial 130nm technology.

The paper is organised as follows: in Section II, RTD based logic gates working on the basis of the MOnostable to BIstable operating principle are described. In Section III, we present the set of logic gates that has been designed and evaluated. A comparison in terms of the average power consumption with the CMOS TSPC realizations of these structures is described in Section IV. Finally, some conclusions are given in Section V.

2. RTD-BASED MOBILE LOGIC GATES

Logic circuit applications of RTDs are mainly based on the MOnostable-BIstable Logic Element (MOBILE) which exploits the negative differential resistance of their *I-V* characteristic (Figure 1*a*). The MOBILE (Figure 1*b*) is a rising edge triggered current controlled gate which consists of two RTDs connected in series and driven by a switching bias voltage, V_{CK}. When V_{CK} is low, both RTDs are in the on-state (or low resistance state) and the circuit is monostable. Increasing to an appropriate maximum value ensures that only the device with the lowest peak current switches (*quenches*) from the on-state to the off-state (the high resistance state). Output is high if the driver RTD is the one which switches and it is low if the load does. Logic functionality can be achieved if the peak current of one of the RTDs is controlled by an input. In the configuration for an inverter MOBILE shown in Figure 1*c*, the peak current of the driver RTD can be modulated using the external input signal. RTD peak currents are selected such that the value of the output depends on whether the external input signal is "1" or "0". Assuming the same peak current density, j_p, for all the RTDs, the peak current is proportional to their area. For V_{CK} high, the output node maintains its value even if the input changes. That is, this circuit structure is self-latching allowing to implement pipeline at the gate level.

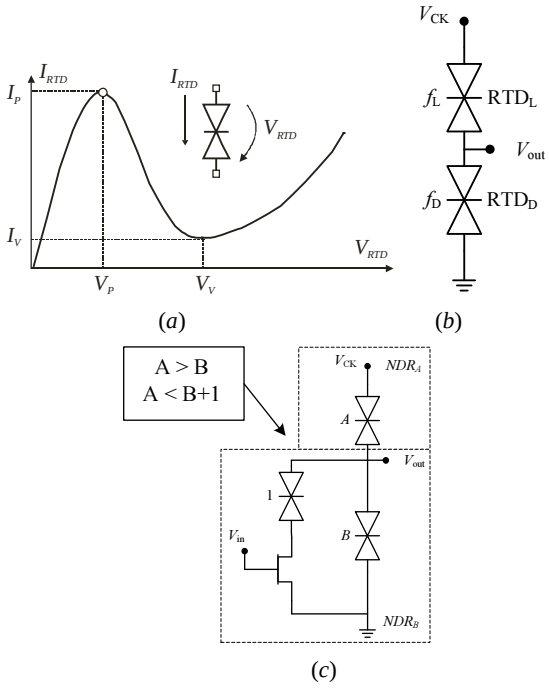


Figure 1. RTD MOBILE circuits. (*a*) RTD *I-V* characteristic and symbol. (*b*) Basic MOBILE. (*c*) MOBILE inverter.

Cascaded MOBILE gates can be operated in a pipelined fashion using a four phase overlapping clocking scheme. Second stage evaluates ($V_{CK,2}$ rising) while the first stage ($V_{CK,1}$) is in the hold phase ($V_{CK,1}$ high). Because of self-latching behavior, second stage is not affected by the reset of the first one. For a number of logic levels greater than three, four bias signals are required. It has been demonstrated that a network of MOBILE-based gates can be operated with a single clocked bias signal [17]. To achieve this operation, positive edge triggered (PET) gates and negative edge triggered (NET) gates are alternated and latches are added. In summary, each gate in a network constitutes a pipeline stage. A gate-level pipeline is implemented. In other words, network operation speed is independent of logic depth but is determined by the clock frequency at which single gates can be operated.

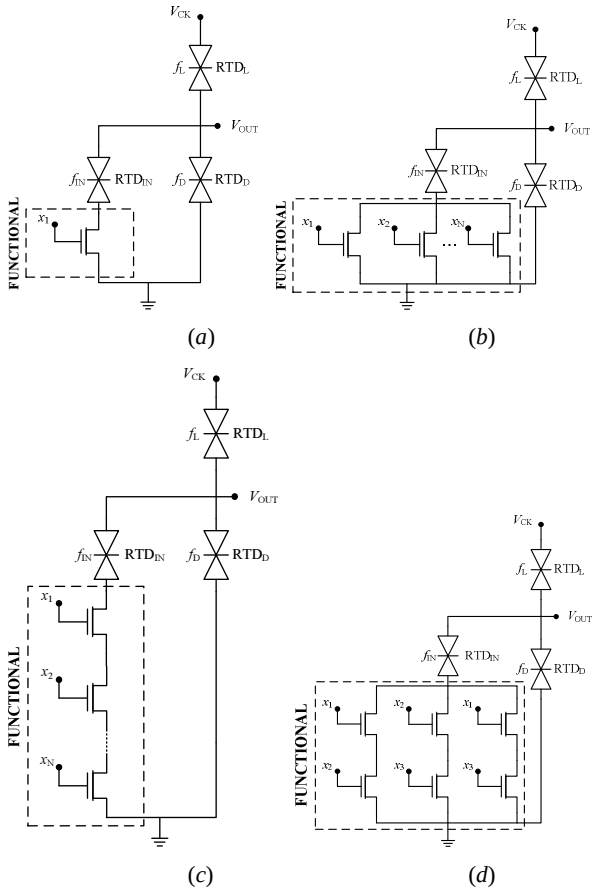


Figure 2. RTD MOBILE circuit implementations. (*a*) Inverter (*b*) NOR (*c*) NAND (*d*) NMAJ.

3. STUDY DESCRIPTION

The performance of several logic gates implemented with RTDs and commercial CMOS transistors has been evaluated. The selected basic logic gates are: inverter, NAND, NOR and inverted majority (NMAJ), which are depicted in Figure 2.

We have compared them with True Single Phase Clock (TSPC) CMOS realizations, since they also implement gate-level pipeline (nanopipeline). TSPC network structures are based on the connection of N-type and P-type dynamic logic gates, placing latches between them. Figure 3*a* depicts the schematic diagram of a N-type realization of a binary inverter. The N-type structures preload the output voltage, V_{OUT}, to V_{DC} when the clock voltage, V_{CK}, is low and evaluates when V_{CK}, is high. For detailed functional description of TSPC refer to [18]. TSPC counterparts for the RTD-based circuits are shown in Figure 3.

The study uses transistors from a standard 130nm CMOS process. For the RTDs, we have started the experiments using a model from LOCOM [19]. This model corresponds to a III-V RTD and has been experimentally validated. Experiments varying RTD characteristics with impact on circuit performance have been also carried out as well as using data from a reported silicon RITD.

Power supply has been independently scaled for the RTD-based circuits and the TSPC structures. For the RTD-based structures, a supply voltage (V_{DD}) of 0.8V has been used, which better suits the available RTD *I-V* characteristics as it will be shown in next Section. To make comparison as fair as possible, we have considered the same supply voltage used in RTD-based circuits. We have also repeated the experiment with V_{DD}=1.2V, the standard voltage value of the technology.

In order to explore the performance of the different gates, HSPICE© parametric simulations of both the RTD-based and the TSPC gates have been carried. For both structures, we have varied a set of some key parameters, taking a discrete number of samples of each one in a given range. We have simulated the structures obtained after combining all the feasible values of the parameters. An automatic verification tool based on Matlab© has been developed to process the results provided by HSPICE© and determine which sets of parameters give structures that operate correctly. Parameters included in the design space exploration are described below.

3.1 RTD-based circuits

For these structures, we have varied the RTD areas (f_x) and the operation frequency. This RTD has j_P equal to 21KA/cm^2 and an intrinsic capacitance, C_{RTD}, of 4fF/um^2 (speed index = j_P / C_{RTD} = 53mV/ps). Transistor length and transistor widths have been set to the minimum

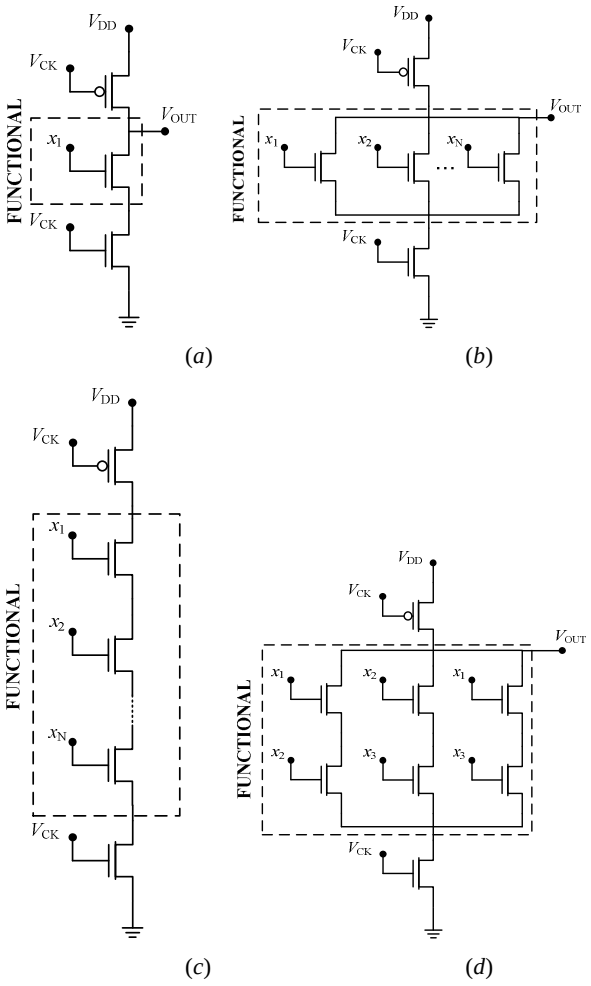


Figure 3. TSPC circuit implementations. (*a*) Inverter (*b*) NOR (*c*) NAND (*d*) NMAJ.

values associated to the technology (0.12 µm and 0.16µm, respectively). Range of RTD areas to be explored have been selected such that the peak current values suitably fit transistor current levels for proper operation of the MOBILE structures. The upper limit is determined by the requirement of the transistor to behave as a switch. The minimum area of the RTD has been selected to be comparable to the minimum area of the CMOS transistors (W=0.16µm and L=0.12µm). The values of f_x have been varied from 0.04µm^2 to 0.4µm^2. The operation frequency range (4GHz to 6GHz) has been selected according to pipelined designs which have been implemented in similar CMOS technologies [20], [21].

3.2 TSPC circuits

We have varied the widths of the MOS transistors, W, and the operation frequency. Minimum gate-length transistors are also used. These structures have been sized considering that the PMOS transistor width is $K \cdot W$ (K=3.5 for this technology), and when m NMOS transistors are connected in series their widths are set to $m \cdot W$. W has been varied from 0.16µm to 1.6µm. The operation frequency has been also explored in the range from 4GHz to 6GHz.

4. SIMULATION SETUP

We have considered ideal clock waveforms for both structures. For the RTD-based circuits, we have considered a clock in which the rising (T_R), falling, hold and reset times are the same, and, thus, the operation frequency is equal to $0.25/T_R$. In TSPC structures a pulse train clock with a duty cycle of 50% has been used. Both clocks vary between 0V and the corresponding value of V_{DD}.

The input signals, which are pulse trains between 0V and V_{DD}, have been chosen in order to cover all the feasible combinations.

We have performed the experiments considering that the gates have been loaded with 1, 2 and 3 minimum-size TSPC latches.

Since MOBILE RTD-based circuits can be affected by mismatching, we have carried out Monte Carlo simulations modeling both transistor and RTD intrachip variations. Standard mismatch models from the technology have been used with the MOS transistors. Since there are no

mismatch models available for the LOCOM technology and no information about variability, Gaussian distributions have been associated to the peak voltage and the j_P of each device. The absolute error of the current density of the RTDs is given by $aej=E \cdot A$, where A is the area of the RTD and E the relative error. On the other side, the absolute error of the peak voltages is given by $aev=E \cdot V_P$.

5. RESULTS

The performance of the circuits has been measured in terms of the average power consumption at the maximum operation frequency, P_{AV}, and the minimum average energy per clock cycle, E_{AV}, which is defined as the ratio between the average power consumption, P_{AV}, and the operation frequency in which it has been measured.

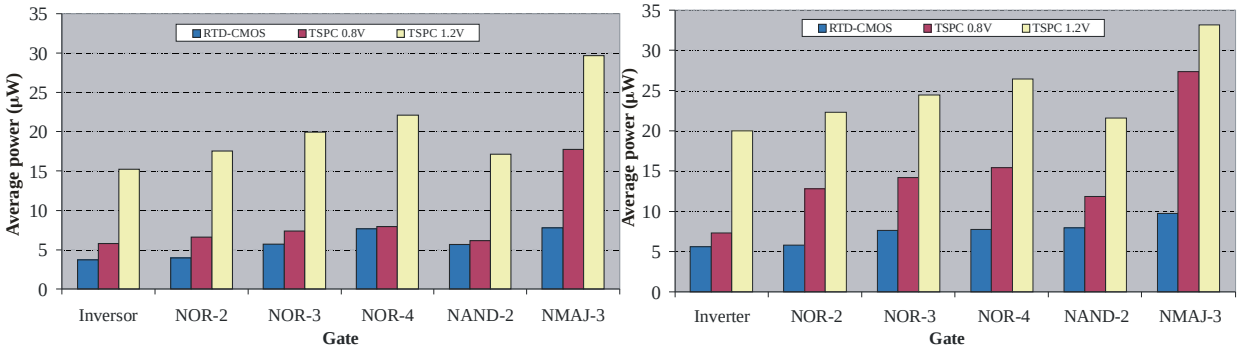
RTD-CMOS simulation results are given in Table 1 in which we have summarized the obtained values of f_x that minimize E_{AV} and P_{AV} at the maximum frequency of operation. The experiment has been performed for different load conditions. Table 2 shows the results corresponding to the TSPC experiments.

Table 1. RTD-CMOS gates. Simulation results.

RTD-CMOS		Inverter	NOR-2	NOR-3	NOR-4	NAND-2	NMAJ-3
Maximum Freq. Load 1	f_X **(µm²)**	0.08	0.08	0.12	0.16	0.12	0.16
	f_{max} **(GHz)**	6	6	6	6	6	6
	P_{AV} **(µW)**	3.705	3.919	5.749	7.653	5.632	7.886
Minimum Energy Load 1	f_X **(µm²)**	0.04	0.08	0.08	0.12	0.08	0.12
	f_{min} **(GHz)**	0.456	0.653	0.814	0.993	0.762	1.283
	E_{AV} **(fJ)**	4.2	6	4.7	5.8	4.2	4.7
Maximum Freq. Load 2	f_X **(µm²)**	0.12	0.12	0.16	0.16	0.16	0.20
	f_{max} **(GHz)**	6	6	6	6	6	6
	P_{AV} **(µW)**	5.635	5.828	7.657	7.758	7.972	9.779
Minimum Energy Load 2	f_X **(µm²)**	0.08	0.08	0.12	0.16	0.12	0.16
	f_{min} **(GHz)**	0.687	0.952	1.127	1.287	1.061	1.557
	E_{AV} **(fJ)**	5.6	4	5.1	6	4.9	5.3
Maximum Freq. Load 3	f_X **(µm²)**	0.16	0.16	0.20	0.20	0.20	0.24
	f_{max} **(GHz)**	6	6	6	6	6	6
	P_{AV} **(µW)**	7.577	7.749	9.577	9.563	9.431	11.705
Minimum Energy Load 3	f_X **(µm²)**	0.12	0.12	0.12	0.20	0.16	0.20
	f_{min} **(GHz)**	1.081	1.231	1.401	1.593	1.357	1.887
	E_{AV} **(fJ)**	5.6	4.7	4	6	5.3	5.3

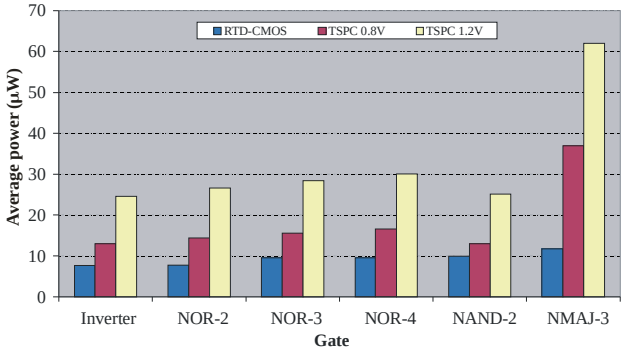
Table 2. TSPC gates. Simulation results.

TSPC		Inverter		NOR-2		NOR-3		NOR-4		NAND-2		NMAJ-3	
		0.8V	1.2V	0.8V	1.2V	0.8V	1.2V	0.8V	1.2V	0.8V	1.2V	0.8V	1.2V
Maximum Freq. Load 1	W (µm)	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.32	0.16
	f_{max}(GHz)	6	6	6	6	6	6	6	6	6	6	6	6
	P_{AV} (µW)	5.77	15.18	6.63	17.58	7.34	19.94	7.94	22.08	6.12	17.14	17.75	29.67
Minimum Energy Load 1	W (µm)	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16
	f_{min} (GHz)	0.96	2.53	1.15	2.92	1.22	3.32	1.32	3.68	1.02	2.85	2.10	4.94
	E_{AV} (fJ)	6	6	6	6	6	6	6	6	6	6	4.9	6
Maximum Freq. Load 2	W (µm)	0.16	0.16	0.32	0.16	0.32	0.16	0.32	0.16	0.32	0.16	0.48	0.16
	f_{max}(GHz)	6	6	6	6	6	6	6	6	6	6	6	6
	P_{AV} (µW)	7.33	20.01	12.82	22.30	14.21	24.47	15.39	26.41	11.82	21.57	27.72	33.12
Minimum Energy Load 2	W (µm)	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.16	0.32	0.16
	f_{min} (GHz)	1.22	3.33	1.18	3.71	1.59	4.07	1.81	4.40	1.37	3.59	3.58	5.52
	E_{AV} (fJ)	6	6	6	6	5.3	6	5.1	6	5.3	6	5.3	6
Maximum Freq. Load 3	W (µm)	0.32	0.16	0.32	0.16	0.32	0.16	0.32	0.16	0.32	0.16	0.64	0.32
	f_{max}(GHz)	6	6	6	6	6	6	6	6	6	6	6	6
	P_{AV} (µW)	12.98	24.55	14.35	26.63	15.52	28.43	16.53	30.04	13.01	25.13	36.94	61.94
Minimum Energy Load 3	W (µm)	0.16	0.16	0.16	0.16	0.16	0.16	0.32	0.16	0.32	0.16	0.32	0.16
	f_{min} (GHz)	1.90	4.09	2.21	4.43	2.48	4.73	2.75	5.00	2.17	4.18	4.25	6.84
	E_{AV} (fJ)	6	6	6	6	4.2	6	6	6	6	6	4.9	5.3



(*a*)

(*b*)



(*c*)

Figure 4. Comparison between average power consumptions for (*a*) Load 1 (*b*) Load 2 (*c*) Load 3.

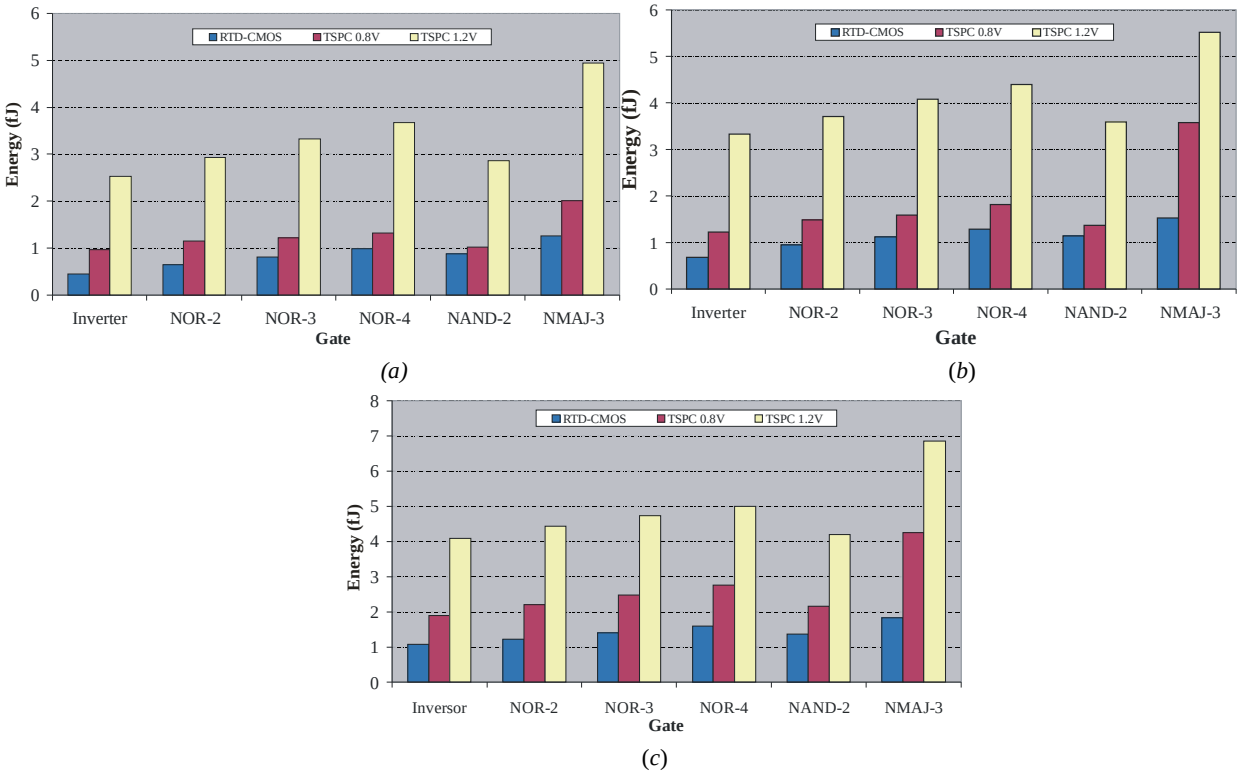


Figure 5. Comparison between average energy per cycle for (*a*) Load 1 (*b*) Load 2 (*c*) Load 3.

Figures 4 and 5 depict the performance of the structures exhibiting the smallest P_{AV} and E_{AV} among those that have been simulated. Results with different load conditions are shown.

Even with V_{DD}=0.8V, RTD-CMOS gates improve the performance regarding TSPC structures. Particularly, these differences are especially significant when the logic functionality is increased. When the circuits are loaded by a single inverter, the average power consumption of the RTD-CMOS NMAJ-3 is reduced in 9.87μW (69%) for V_{DD} =0.8V and 21.78μW (79%) for V_{DD} =1.2V. Figures 4*a* and 4*b* show that absolute differences between average power consumptions are even greater when the load increases. The same trend is observed in the behavior of the average energy, as shown in Figure 5: for the NMAJ-3 gate with V_{DD}=0.8V (1.2V), energy savings of 39% (71%), 56% (72%) and 57% (72%) have been measured for load 1, 2 and 3, respectively. In TSPC circuits, most of the power consumption is dynamic and thus, the dependence with the frequency is more significant than in RTD-CMOS gates, in which the static power prevails due to the second positive differential resistance region of the RTD.

The performances of the series connection of four inverters have been analyzed. Energy per cycle for the RTD-CMOS network varies from 20% to 80% of the energy required by the TSPC solution. Savings significantly increase with operating frequency. Moreover, RTD-CMOS network works in all cases with 0.8V supply voltage. Supply voltages requires by TSPC ranges from 1V to 1.2V.

6. CONCLUSIONS

Realizations of RTD-CMOS logic gates working on the basis of the MOBILE operating principle have been introduced. A comparison to only transistor implementations using TSPC logic style, well suitable for gate level pipelined, like the proposed RTD structures, has been carried out. An experiment of design space exploration has been described which shows the efficiency of the RTD-CMOS design over the CMOS TSPC structures in terms of the average power at the maximum operation frequency and the minimum energy per clock cycle.

7. ACKNOWLEDGMENTS

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