Phase Transition FETs for Improved Dynamic Logic Gates

María J. Avedillo, Manuel Jiménez and Juan Núñez

***Abstract*— Transistors incorporating phase change materials (Phase Change FETs) are being investigated to obtain steep switching and a boost in the I_{ON}/I_{OFF} ratio and, thus, to solve power and energy limitations of CMOS technologies. In addition to the replacement of the transistors in conventional static CMOS logic circuits, the distinguishing features of Phase Change FETs can be exploited in other application domains or can be useful for solving specific design challenges. In this paper, we take advantage of them to implement a smart dynamic gate in which undesirable contention currents are reduced, leading to speed advantage without power penalties.**

***Keywords*—Steep subthreshold slope, Phase transition materials, Low voltage, Dynamic logic, Keeper transistor.**

I. Introduction

Scaling limitations of CMOS have motivated active research in very different beyond-CMOS devices. Steep subthreshold slope (*SS*) transistors are receiving much attention since they facilitate low voltage operation reducing power and improving energy efficiency with respect to CMOS circuits. Several *SS* devices have been reported as promising candidates. Among them, recently, Phase-Change transistors (PCFETs) have been proposed by connecting a phase transition material (PTM) to the source terminal of a FET. The abrupt insulator-metal transitions of the PTM are used as a mechanism to obtain steep switching and a boost in the I_{ON}/I_{OFF} [1]. Several PCFETs exhibiting *SS* under 60mV/dec have been experimentally obtained [2], [4]. Values as low as 5mV/dec have been reported [3]. Moreover, a combination of phase-transition material with Tunnel FETs is being explored to enhance their I_{ON}. A device with *SS*=30mV/dec has been recently proposed [5].

In addition to reducing power consumption in conventional logic computation, associated with *SS* reduction, PCFETs are considered as potential candidates to enable new computational paradigms such as neuromorphic architectures or coupled-oscillator based processing [6]. Recently, their distinguishing features are starting to be exploited to enhance specific circuit topologies. An implementation of a PCFET-assisted sense amplifier has been proposed showing higher performance, lower area, and lower power than the standard CMOS topology [7]. A true random number generator composed of just a phase-change device, a transistor, and two flip-flops has also been experimentally shown [8]. In this paper, we describe how the dynamic logic style can take advantage of phase change transistors to alleviate the keeper contention current, which degrades the speed of such gates.

This paper is organized as follows: Section II is devoted to the background on both the phase change transistor and the dynamic logic style, as well as their operating principles. Section III proposes a novel dynamic logic gates and results of simulations carried out to evaluate our proposal are described and analyzed. Finally, key conclusions are provided in Section IV.

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II. Background

A. Phase Change FET

A PCFET (schematic depicted in the insight of Fig 1) integrates a phase-transition material (PTM) into the source terminal of a conventional transistor [1], [9]. PTMs undergo insulator-metal transitions under given electrical (among other) stimuli. That is, they experience abrupt switching from/to a high resistivity state (insulating phase) to/from a low resistivity state (metallic phase). PCFETs use current-driven PTMs to achieve steep switching.

PTMs tend to stabilize in the insulating phase under no electrical stimuli. When a high enough current density ($J_{C\text{-}IMT}$) flows through it, Insulator to Metal Transition (IMT) occurs. Once in the metallic state, when the current density reduces below $J_{C\text{-}MIT}$, the Metal to Insulator Transition (MIT) takes place.

The PCFET transistor takes advantage of the orders of magnitude difference between R_{INS} and R_{MET} to boost the ratio of its *ON* current (I_{ON}) and its *OFF* current (I_{OFF}) achieving steep subthreshold slope. When the transistor is in the OFF state, the small current flowing through the PCFET forces the PTM into the insulating state. Thus, the effective gate-to-source and drain-to-source voltages seen by the intrinsic transistor are reduced and I_{OFF} is also decreased. When the gate to drain voltage is increased, the current through the PCFET is also increased and the switch to the metallic state is triggered. Because of the small metallic resistance, the I_{ON} current of the PCFET is almost not reduced with respect to the intrinsic transistors. Thus, I_{ON}/I_{OFF} is increased. Fig 1 compares the I-V characteristics of a FinFET transistor and of the Phase-Change FET built from it adding the PTM.

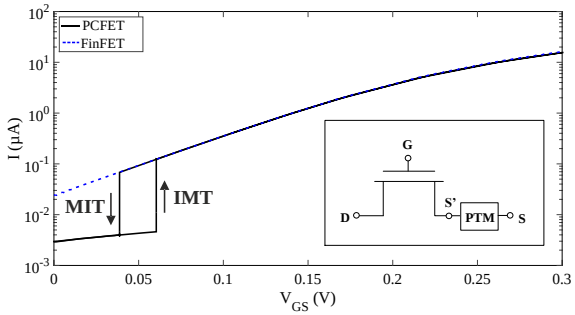

Fig 1. Comparison between the I-V characteristics of the FinFET and the PCFET (its schematic has been included in the insight).

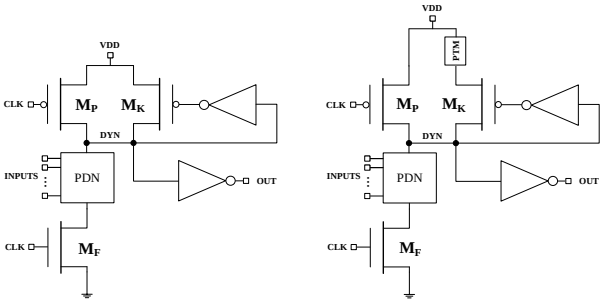

Fig 2. (a) Conventional dynamic gate topology. (b) Proposed dynamic gate topology with PCFET-based variable keeper.

B. Dynamic Logic

Fig 2a shows a generic conventional dynamic gate or domino gate. It operates in two phases called precharge (CLK = "0") and evaluation (CLK = "1"). It is composed of a dynamic stage and a static output stage. Keeper transistor (M_K) is added to protect dynamic node against leakage/noise. The conventional feedback keeper transistor can no longer achieve a reasonable trade-off between performance and robustness in deep submicron technologies. These factors especially limit the implementation of high fan-in dynamic NOR gates, on which basis, read and write ports of register files, as well as other important modules in the critical part of modern microprocessors, are built [10],[11].

Many different gate architectures have been proposed to overcome these limitations. In [12] these contributions are classified into two groups. One comprises those designs reengineering the pull-down network (PDN) to reduce leakage, while the other focuses on the design of innovative keeper circuits. The second approach usually has less overhead than the first. Many of them [13]-[17] work on the basis of the variable keeper concept, in which the strength of the keeper is variable. It is weak (or even OFF) while the gate is at the beginning of evaluation and strong during the rest of the evaluation phase if the dynamic node should remain high. The weak keeper results in reduced contention currents and faster output transitions. Different mechanisms to control activation of the strong keeper are used in those works. Their implementations have penalties in terms of area and power.

III. PROPOSED DYNAMIC GATE

Fig 2b depicts the proposed solution to implement the variable keeper concept on the basis of the Phase-Change FET. The keeper transistor in Fig 2a is replaced by a Phase-Change transistor. The PCFET acts itself like a variable keeper. With itsd PTM in the insulating state, it behaves as a very weak keeper. With its PTM in the metallic state, it behaves as a normal keeper.

Fig 3 shows simulation waveforms illustrating the behavior of a PCFET dynamic inverter. They have been obtained using the model for a PTM-Sim described in [9],[18] and a predictive model for 14nm FinFET transistors obtained from [19],[20], following [9],[18],[21]. The supply voltage is 0.3V as in these references. The input (*IN*), the clock (*CLK*), the dynamic node (*DYN*), the gate output (*OUT*) and a signal that monitors the state of the PTM (*PTM_state*) are shown. If the *PTM_state* signal is high (low), the PTM is in insulating (metallic) state. For comparison purpose, also the waveform at the output of the conventional dynamic gate is depicted (*OUT_FinFET*).

At the beginning of the evaluation phase, *DYN* is charged to V_{DD} and very small current flows through the keeper and the PTM is in the insulating state. If the dynamic node starts to discharge because of the input combination ("A" in the figure), it takes some time before enough density current passes through the PTM devices and it can switch to the low metallic state. In fact, when the dynamic node voltage reduces, the current through the pull-down is also reduced. If this discharge is fast enough, before the PTM switches, the gate output rises and cuts the keeper. This reduces the current circulating through the PTM and it does not switch, as shown in the figure. The gate evaluates correctly the "1" but the contention current in the proposed gate is very low, much smaller than in the conventional gate. This translates into faster discharges of the dynamic node.

When a zero is applied ("B" in the figure), the voltage at the dynamic node begins to fall as a consequence of the leakage currents that circulate and that cause a voltage drop in the PTM, and finally this switches to the metallic state and the PCFET recharges the dynamic node. The gate behaves now like the conventional one with a keeper transistor in series with a very small resistance.

The behavior when there is noise at the input is also shown ("C" in the figure). The PTM switches to the metallic state, protecting the dynamic node from undesired discharges. That is, it would be operating with the keeper activated.

When evaluating a logic one, it may happen that it does not

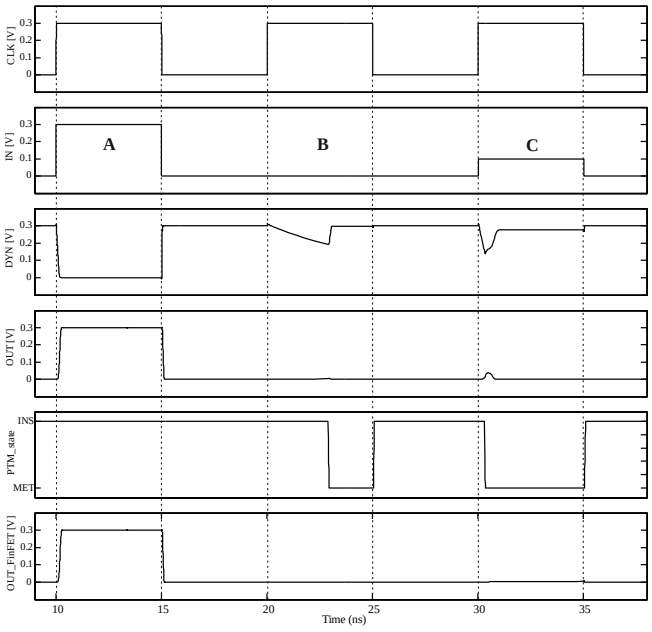

Fig 3. Illustrative waveforms of the operation of a PCFET dynamic inverter.

discharge sufficiently fast and the PTM switches to the metallic state for a time before the output cuts the keeper. Even in this case, there are reductions in the contention current at the beginning of the evaluation phase.

In order to evaluate the proposed topology, a set of NOR gates with a different number of inputs has been designed, both with the conventional topology and with the new one, proposed in this work. Both gates have been sized identically except for the keeper transistor. This has been chosen so that each gate can tolerate a noise pulse of 100mV applied to all its inputs and correctly evaluated a single "1" (only at one of its inputs) with both, nominal and degraded, voltages. Gates have been characterized in terms of delay and power consumption. Table I shows worst case delays (input combination with a single logic one, high voltage level degraded by 10%) of the conventional dynamic gate normalized with respect to the proposed implementation. Delays are measured from 50% of the clock rising to 50% of the dynamic node falling. It is observed that the delays exhibited by the conventional topology are larger than those of the proposed topology in spite of the fact that it has been necessary to size the keeper transistor in the proposed topology slightly stronger than that of the conventional one, compensating in this way that it is disabled for a fraction of time. The observed advantages increase with the complexity of the design. Delay of the 16-input conventional gate is almost 20% larger than the proposed one.

Evaluation of power is also interesting since, on one hand, we expect advantages for the proposed gates associated to the reduction of the contention currents ("A" in Fig 4 depicts currents through the keeper of both topologies during evaluation of a logic 1) and leakage when the PTM is in the insulating state ("B" in Fig 4). But on the other, it was also illustrated that the dynamic node is recharged during the evaluation phase in the proposed gate when a zero is applied to the input, which increases power consumption. "C" in Fig 4 shows the current associated to this recharge. Table I also depicts average power at 500MHz of the conventional dynamic gate normalized with respect to the proposed one. It is observed that the power consumption of both gate topologies is very similar.

Because of the variability exhibited by the PTMs, the analysis of the impact of PTM parameters on the operation of the proposed gate is relevant. The variations of two critical ones, PTM transition time (*TT*) and insulating to metallic transition voltage (V_{IM}) have been explored.

Increasing *TT* has no effect on the speed of the gate. This is because the delay depends on how fast the dynamic node discharges, but when the dynamic node discharges, the PTM does not switch ("A" in Fig 3). However, it affects the noise tolerance. In order to protect against undesired discharges of the dynamic node, the PTM switches to metallic ("C" in Fig 3). If this transition is slower, protection is reduced. For example, for the more complex gate (16 inputs), *TT* = 80ps is the limit to tolerate the noise pulses used in the study. The nominal value is 50ps. On the contrary, decreasing *TT* from its nominal value has a positive effect on noise tolerance. It also modifies the behavior in scenery "A". The PTM momentarily switches to metallic although with insignificant impact on delay.

Similarly to increasing *TT*, increasing V_{IM} does not alter the speed of the gate but reduce noise tolerance. This is because by reducing V_{IM} the change to metallic occurs earlier. The limit is V_{IM} =114mV. The nominal value is 104mV. Also, decreasing V_{IM} is positive for noise and has no impact on delay over 80mV and it is minimal under this value.

Note that the limited tolerance to V_{IM} increment (around 10%, much smaller than the tolerated *TT* variation or V_{IM} reduction) can be enhanced with a stronger keeper. Contention current increment during the evaluation is negligible because PTM is in the insulating state and, so, the effect on delay is just a variation of the dynamic node capacitance.

TABLE I
DELAY AND POWER COMPARISON (NORMALIZED)

#INPUTS	DELAY	POWER
4	1.04	1.00
8	1.07	1.01
12	1.14	1.02
16	1.18	1.03

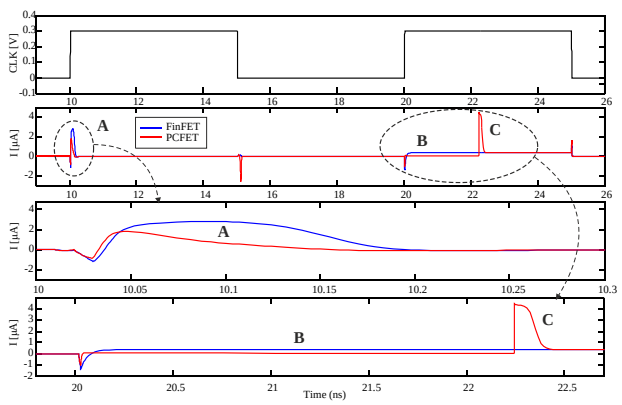

Fig 4. Currents through the keeper transistors for the FinFET (blue) and PCFET topologies.

IV. CONCLUSIONS

A dynamic gate in which the keeper transistor is implemented with a Phase Change FET has been proposed and its operation illustrated. It has been shown how the PCFET alone implements the variable keeper concept without requiring any additional circuitry. The PTM device within the PCFET is in the insulating state when the dynamic node must be discharged due to the applied input combination, while it is in the metallic state when it should not, protecting the dynamic node against noise. Unlike previous implementations of the variable keeper concept, the proposed smart keeper reduces contention currents without area and power penalties.

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