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Energy-Efficient Amplifiers Based on Quasi-Floating Gate Techniques

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Abstract: Energy efficiency is a key requirement in the design of amplifiers for modern wireless applications. The use of quasi-floating gate (QFG) transistors is a very convenient approach to achieve such energy efficiency. We illustrate different QFG circuit design techniques aimed to implement low-voltage, energy-efficient class AB amplifiers. A new super class AB QFG amplifier is presented as a design example, including some of the techniques described. The amplifier has been fabricated in a 130 nm CMOS test chip prototype. Measurement results confirm that low-voltage, ultra-low-power amplifiers can be designed, preserving, at the same time, excellent small-signal and large-signal performance.

Keywords: amplifiers; analog integrated circuits; CMOS integrated circuits; energy-efficient amplifiers; class AB circuits

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1. Introduction

Today, we are facing significant challenges in the design of electronic circuits. Many emerging wireless connectivity and Internet of Things edge computing applications require ultra-low-power wireless devices providing high performance in both indoor and outdoor environments. Energy efficiency is mandatory in such applications in order to increase battery lifetime. In fact, due to maintenance costs, battery replacement or manual recharge becomes impractical or even unfeasible in several scenarios with hard-to-reach wireless nodes (e.g., large civil infrastructures, vast natural ecosystems or implantable medical devices), requiring energy-autonomous wireless devices with batteries lasting several years. In some cases, the limited and often intermittent residual energy harvested from the environment (light, thermal gradients, vibrations, etc.) must be enough to operate the wireless device [1].

Aside from this, modern nanometer integrated circuit (IC) processes pose further challenges since device scaling directly impacts electronic design. Intrinsic gain reduction degrades DC gain. Supply voltage lower than 1 V becomes commonplace to reduce power consumption and to avoid gate oxide breakdown of nanometer devices. To complicate things, transistor threshold voltage cannot scale at the same rate as the supply voltage to keep subthreshold leakage currents low, so the available voltage swing reduces [2].

Preserving circuit performance in these demanding scenarios of energy scarcity and very low-voltage operation is a real challenge, and conventional circuit design techniques are often no longer valid in this framework. Innovative design techniques are required to meet these new demands. A critical block in modern mixed-signal ICs is the amplifier,

which typically accounts for a significant percentage of the IC power budget [3]. Hence, designing high-gain wideband amplifiers operating with low supply voltage and low power requirements has become a major research topic. Conventional class A amplifiers are usually impractical under these constraints, since their maximum load current is limited by their bias current, so dynamic performance can only be improved at the expense of increased static power. These days, class AB amplifiers are preferred for low-voltage, low-power applications, since they allow maximum dynamic currents not bound by the quiescent currents [4]. However, providing class AB operation to the amplifier may degrade other characteristics, such as minimum supply voltage requirements, tolerance to process, supply voltage or temperature (PVT) variations, stability or noise performance. Likewise, to achieve energy efficiency, it is important that the large dynamic currents provided by the class AB circuits are generated in the output branch, without requiring internal copies of these large currents. Therefore, careful design of class AB amplifiers is mandatory.

This paper deals with the design of low-voltage class AB CMOS amplifiers able to maximize performance, preserving, at the same time, energy efficiency. It will be shown that quasi-floating gate (QFG) transistors [5] represent an excellent choice to achieve these goals. The QFG technique allows independent control of static and dynamic operation of the transistor by using separate input terminals for DC bias and AC signals. This allows overcoming the tradeoff between dynamic performance and quiescent power consumption of class A topologies. Very low and accurately controlled quiescent currents can be achieved by properly setting the DC input level. At the same time, large dynamic currents can be provided, since signals are capacitively coupled to the high impedance gate node. Due to these advantages, QFG transistors have found widespread use in the design of amplifiers [5–30] but also in high-performance current mirrors [31–35], mixers [36,37], linearization of active resistors [38,39], DC offset cancellation servo loop circuits [40], bootstrapped switches [5], current conveyors [30,41–43], Voltage Feedback Operational Amplifiers (VFOAs) [44], Current Feedback Operational Amplifiers (CFOAs) [45], buffers [46–51], rectifiers [35,52], capacitance multipliers [35], transconductors [30,53–55], digital-based analog circuits [56], DC–DC converters [57], continuous-time filters [58–61], track and hold circuits [5], data converters [5,62], capacitive sensing interfaces [63], particle detectors [23] and retinal prosthesis [64], to name some representative applications.

The paper is organized as follows: Section 2 provides an overview of QFG transistors and their application to the design of amplifiers. Section 3 reviews various reported amplifier topologies based on QFG techniques. A new energy-efficient class AB amplifier designed and fabricated in a 130 nm CMOS process is described in Section 4. A discussion on the results is provided in Section 5, and some conclusions are drawn in Section 6.

2. Quasi-Floating Gate Transistors

In this section, the fundamentals of QFG transistors are briefly presented, and their application to the design of low-voltage class AB amplifiers is discussed.

2.1. Wideband Capacitive Coupling Using Quasi-Floating Gate Transistors

Capacitive (or AC) coupling is widely used to isolate the DC bias setting circuit of active devices from the driving signal source. A typical example is shown in Figure 1a, where a resistive divider sets the quiescent gate voltage of the transistor. Coupling capacitor C blocks the input DC voltage and allows the input signal to pass through to the gate. A more general biasing scheme is shown in Figure 1b, where DC bias voltage V_B is set using resistor R_B. Note that the circuit of Figure 1a can be regarded as a particular case of Figure 1b, using the Thévenin's theorem, where $V_B = (V_{DD} - V_{SS}) \cdot R_2/(R_1 + R_2)$ and $R_B = R_1 \,||\, R_2$.

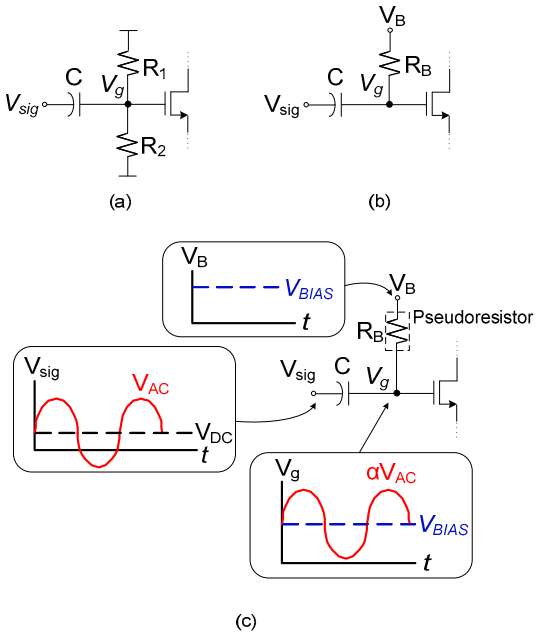

Figure 1. (**a**) Conventional capacitive coupling. (**b**) General scheme. (**c**) Quasi-floating gate transistor.

The circuit of Figure 1b provides a first-order, low-pass filtering from input V_B to the gate and a first-order, high-pass filtering from input V_{sig} to the gate, both with time constant $R_B \cdot C$. Due to the limited practical values of on-chip passive resistors and capacitors, this time constant cannot be too large. Hence, despite the name "AC coupling," this technique is rather employed in ICs for RF narrowband signals with frequencies above the relatively large cutoff frequency of the high-pass input filter.

However, several relevant applications require processing of very low frequency signals (such as biomedical systems, structural health monitoring, geoenvironmental monitoring, etc.) or wideband signals with significant content at low frequencies (for instance, baseband processing circuits in a direct conversion receiver). In these cases, DC-blocking circuits able to allow near-DC frequency components pass through are required. An efficient approach to achieve the large time constant required is replacing resistor R_B in Figure 1b by a pseudo-resistor (also known as quasi-infinite resistor, QIR) [6,7]. The resulting circuit is shown in Figure 1c, which is known as a QFG transistor [5]. Pseudo-resistors are small-area integrated devices that can provide extremely large incremental resistances (in the order of GΩ–TΩ) when they are properly biased. Therefore, very large RC time constants can be obtained using small capacitors that can be implemented on-chip.

From Figure 1c, the transfer functions from inputs V_B and V_{sig} to V_g are:

$$\frac{V_g(s)}{V_B(s)} = \frac{1}{1+s\tau} \tag{1}$$

$$\frac{V_g(s)}{V_{sig}(s)} = \alpha \frac{s\tau}{1+s\tau} \tag{2}$$

with $\tau = R_B \cdot (C + C_g)$ as the time constant, C_g the parasitic capacitance at the gate terminal and $\alpha = C/(C + C_g)$. Note that input V_B is low pass filtered with an extremely large time constant τ, so that the DC bias voltage V_{BIAS} is set to the gate, and any AC noise or interference coming from this input is rejected. The signal at input V_{sig} is high pass filtered with the same time constant, so, in practice, only the DC level at this input is blocked. This input signal is also attenuated by a factor α, due to the nonzero parasitic gate capacitance C_g. The value of C_g sets the minimum required value for C to avoid excessive attenuation. Multiple-input QFG transistors can also be used [5], allowing weighted averaging of signals in a simple and compact way.

Note the different behavior of the circuit of Figure 1c for DC and AC small-signal and large-signal dynamic (or transient) operation. Capacitor C is an open circuit in DC, so the quiescent gate voltage is $V_g{}^Q = V_{BIAS}$, since there is not current flowing through the pseudo-resistor. Hence, the bias point can be accurately set. For AC small-signal operation, the capacitor acts as a short circuit (more precisely, as an attenuator, due to the input capacitive divider), so that the AC gate voltage is $v_g = \alpha v_{ac}$, with v_{ac} the AC voltage at input V_{sig}. For transient operation with input frequencies larger than $1/\tau$ (in practice from near DC), C acts as a floating battery with voltage V_{BIAS}-V_{DC}, with V_{DC} the DC voltage at input V_{sig}. This is because C cannot be discharged rapidly through the pseudo-resistor. The signal is thus level-shifted by V_{BIAS}-V_{DC} and attenuated by factor α when it reaches the gate. In practice, nonlinearity of the pseudo-resistor may lead to nonlinear distortion and offset in the gate voltage. These issues are more relevant for large voltage swings at the pseudo-resistor terminals and depend on the implementation of the pseudo-resistors. Some of the most common fixed and tunable pseudo-resistors are shown in Figures 2 and 3, respectively.

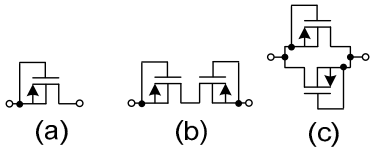

Figure 2. Nontunable pseudo-resistors. (**a**) Single PMOS device. (**b**) Series topology. (**c**) Parallel topology.

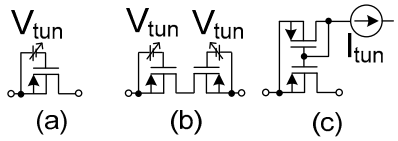

Figure 3. Tunable pseudo-resistors. (**a**) Single voltage-tuned PMOS device. (**b**) Series voltage-tuned topology. (**c**) Current-tuned topology.

The simplest pseudo-resistor is a diode-connected PMOS transistor operating in deep subthreshold, as shown in Figure 2a [5,35,36]. It is very compact, but the resistance obtained cannot be modified once fabricated, and it is very sensitive to PVT variations. Moreover, the I–V characteristics are asymmetric, so it becomes nonlinear for large voltage swings. These drawbacks are usually of minor concern when the pseudo-resistor is used in high-gain amplifiers operating in negative feedback, as long as the resistance remains high enough for the QFG transistor to process the lowest frequency of the input signal V_{sig} in Figure 1c. When symmetric I–V characteristics are required, elementary devices can be mirrored either in series or in parallel, as shown in Figure 2b,c, respectively, for the case of two elements [8]. The series connection is useful when large resistance values for wide voltage ranges are needed.

Some applications require tunable pseudo-resistors, where tuning can be achieved using a DC voltage [8,12] or a DC current [13], as shown in Figure 3. Further details and examples of pseudo-resistors can be found in [8].

2.2. Application of QFG Transistors to Energy-Efficient Amplifier Design

Figure 4 illustrates various techniques based on QFG transistors that can be exploited to achieve low-voltage, energy-efficient amplifiers. They are described below.

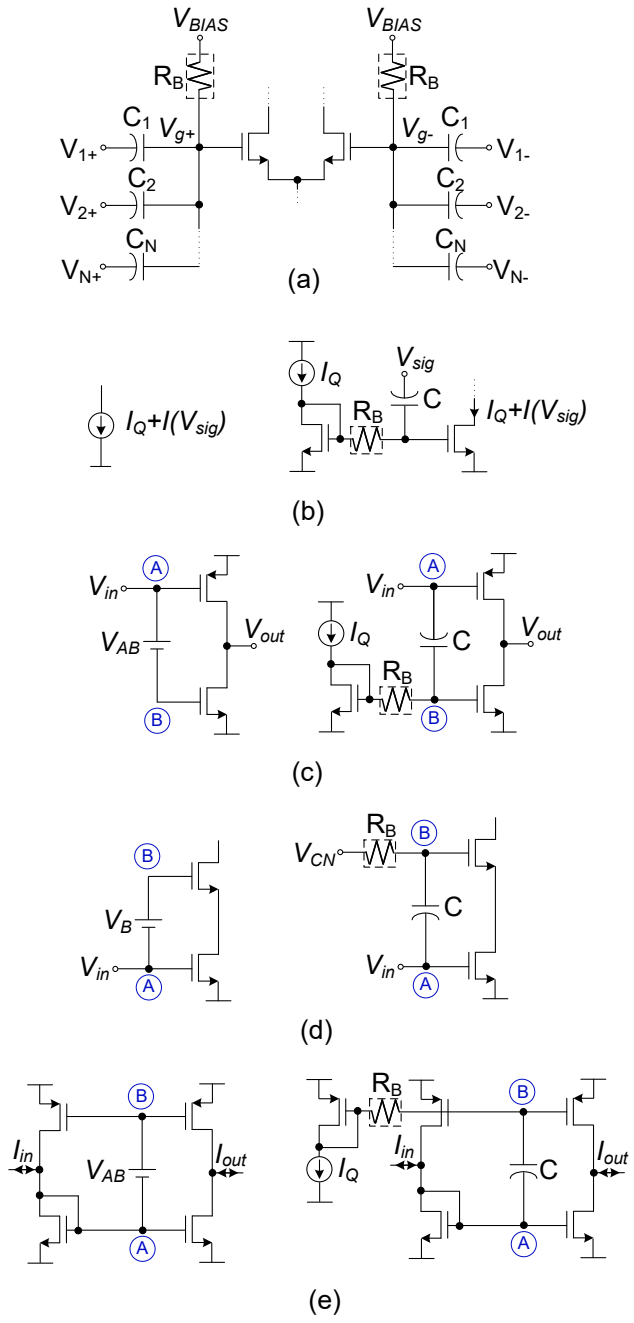

Figure 4. Quasi-floating gate (QFG) techniques for amplifier design. (**a**) QFG input pair. (**b**) Adaptive bias current source. (**c**) QFG class AB stage. (**d**) Dynamic cascode biasing. (**e**) Class AB current mirror.

2.2.1. QFG Input Differential Pair

A QFG differential pair can be used at the input of the amplifier to get AC coupling, as shown in Figure 4a, where the general case of N inputs is depicted [5]. Assuming matched input capacitors C_k, the differential AC voltage at the gates v_{Gd} is a weighted averaging of the AC differential inputs $v_{kd} = v_{k+} - v_{k-}$ set by C_k/C_T capacitor ratios:

$$v_{Gd} = \sum_{k=1}^{N} \frac{C_k}{C_T} v_{kd} \tag{3}$$

with C_k as the coupling capacitance of the k-th input and C_T as the total capacitance at each gate node, which is approximately

$$C_T \approx \sum_{k=1}^{N} C_k + C_{GS} + C_{GD} + C_{GB} + C_{PR} \quad (4)$$

with C_{PR} as the parasitic capacitance of the pseudo-resistor at the gate node. Usually, the first term in Equation (4) is dominant, so all the parasitic terms are negligible. Frequently, two-input QFG transistors are used to provide not only capacitive input coupling but also capacitive feedback. Various implementation examples are presented in Section 3.

2.2.2. Adaptive Bias Current Source

Figure 4b shows how a QFG transistor can be used to implement an adaptive bias current source. In quiescent operation (V_{sig} = 0), the circuit works as a current mirror and the quiescent output current is accurately set to I_Q despite PVT variations. This current may be very low to save quiescent power. However, in dynamic operation ($V_{sig} \neq 0$), large output currents not limited by I_Q can be generated, due to the AC coupling of V_{sig}.

2.2.3. Class AB Output Stage

A basic scheme of a class AB output stage is shown at the left side of Figure 4c. A floating battery V_{AB} allows biasing the NMOS transistor and transfers input signal variations from node A to node B, providing output currents larger than the quiescent current. A QFG implementation is shown at the right side of Figure 4c, where the circuit of Figure 4b is used as active load of the input transistor, with $V_{sig} = V_{in}$. Note that the QFG technique allows an optimal implementation of the floating battery, since it does not influence the biasing of the NMOS transistor, which is set by a matched diode-connected transistor, as in a class A topology. The value of V_{AB} can be either positive or negative; it is adapted to the supply voltage employed, preserving the quiescent gate voltages. This is not the case in conventional implementations of V_{AB} using, e.g., diode-connected transistors or resistors biased by DC current sources [65]. Moreover, the QFG implementation of V_{AB} does not require additional supply voltage or quiescent power and does not add extra nodes.

2.2.4. Dynamic Cascode Biasing

In class AB amplifiers, cascode transistors may restrict the V_{DS} voltage of the transistors that generate the large dynamic currents, making these transistors enter ohmic region and limiting slew rate. To avoid this effect, dynamic biasing of the cascode transistors is required. It is typically done as shown on the left side of Figure 4d. A floating battery V_B transfers a level-shifted version of the input signal in A to node B, so that the cascode gate voltage increases for large signals, increasing the V_{DS} of the input transistor. Again, an efficient implementation of the floating battery can be made by using a QFG cascode transistor, as shown on the right side of Figure 4d. As before, the implemented value of V_B is not fixed; it is the difference between the quiescent cascode bias voltage V_{CN} and the quiescent input voltage, so it is insensitive to PVT variations. As before, no extra quiescent power or supply voltage requirements are needed.

2.2.5. Class AB Current Mirrors

Current mirrors are widely used in amplifier design as current followers, i.e., to convey currents from a low-impedance input node to a high-impedance output node. For instance, they are used in current mirror (symmetric) amplifiers to convey (and optionally scale) the differential pair current to the output node. When these current mirrors must process bidirectional signal currents, class AB operation is required to achieve a class AB amplifier [22]. A schematic diagram of a class AB current mirror is shown on the left side of Figure 4e. Again, a floating battery V_{AB} translates signal variations from node A to B,

allowing dynamic currents larger than the quiescent currents. A QFG implementation is shown in Figure 4e [31], which consists, basically, on the replacement of the PMOS current sources on the left side by a two-output adaptive current source, like in Figure 4b. As before, this implementation features accurate quiescent currents not dependent on PVT variations. V_{AB} is set by the difference between quiescent voltages at nodes A and B and can be either positive or negative. No extra supply voltage or quiescent power is required.

3. Energy-Efficient Amplifiers Based on QFG Techniques

In this section, the application of the QFG techniques and circuits to low-voltage power-efficient amplifiers is illustrated.

3.1. AC-Coupled Amplifiers

AC-coupled amplifiers allow accurate amplification (set by capacitance ratios), providing, at the same time, blocking of near-DC inputs. They are widely used to remove electrode offsets in physiological signals and also in interface circuits for monitoring of seismic activity or mechanical vibrations. For instance, electrode–skin interfaces may lead to offsets larger than 1 V [6], which can limit dynamic range and even saturate the amplifier if they are not removed.

Efficient AC-coupled amplifier implementations can be made using QFG input transistors, as shown in Figure 5 [5,6]. The circuit of Figure 5a can be used for singled-ended input and output, while Figure 5b provides single-ended output for differential inputs. The circuits of Figure 5c,d are fully differential topologies. Note that one (Figure 5a) or two (the other topologies) two-input QFG transistors are employed at the amplifier input. The QFG input capacitor C_1 goes to the input terminal, and the other QFG input capacitor C_2 is connected to the output. The midband gain is, in all cases, C_2/C_1. Note that the QFG pseudo-resistor is connected to the output in Figure 5a–c to provide DC-negative feedback. This is not the case in Figure 5d, where the amplifier is in open loop in DC. Hence, adequate design is required, in this case, to avoid saturation of the output [5]. An advantage of Figure 5d is that the amplifier DC input V_{BIAS} can be set to a supply rail, so the circuit can work with ultra-low-supply voltages. Another advantage is that the pseudo-resistor experiences little voltage swings, so a simple pseudo-resistor implementation can be used [5].

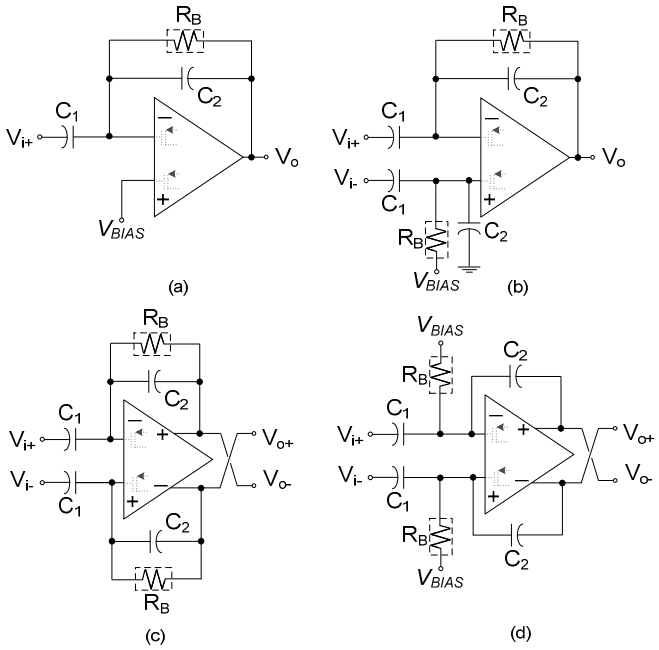

Figure 5. AC-coupled amplifiers. (**a**) Single-ended input and output. (**b**) Differential input and single-ended output. (**c**) Fully differential. (**d**) Alternative fully differential.

3.2. Single-Stage Class AB Amplifiers

In terms of energy efficiency and silicon area, single-stage amplifiers are the best option, since they are load-compensated [65] and can feature near-optimal current efficiency if properly designed [5]. The single-stage differential pair amplifier provides simplicity and high current efficiency. A class AB QFG fully differential implementation can be achieved, as shown in Figure 6a [17], where the common-mode feedback (CMFB) circuit is not shown. Transistors M_{1A}–M_{2A} are adaptively biased using two cross-coupled DC level shifters implemented by flipped voltage followers (FVF) [66] M_{1B}–M_{1C} and M_{2B}–M_{2C}. This adaptive biasing doubles the gain-bandwidth product (GBW) and allows dynamic currents in M_{1A} and M_{2A} larger than I_B. The active load is implemented by adaptive QFG current sources M_{3B} and M_{3C}, like in Figure 4b.

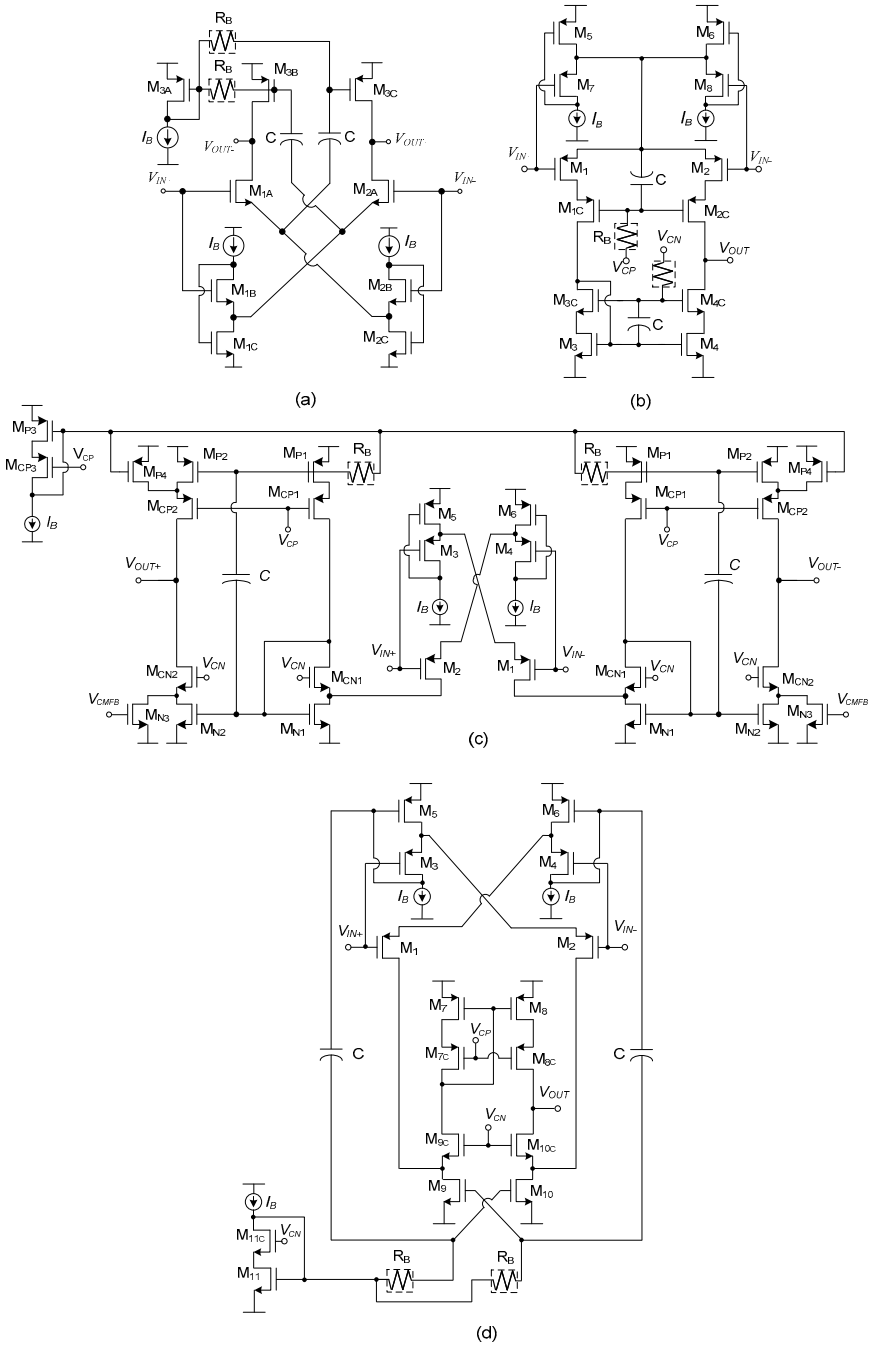

Figure 6. Single-stage class AB amplifiers. (**a**) Differential pair amplifier. (**b**) Telescopic cascode amplifier. (**c**) Current mirror amplifier. (**d**) Folded cascode amplifier.

To provide more DC gain, preserving current efficiency, a class AB telescopic cascode implementation can be used, as shown in Figure 6b [20]. In this case, adaptive biasing of the differential pair is also implemented by two FVFs, but in this case, the FVF outputs are connected. Hence, both FVFs act as a winner-take-all (WTA) circuit [67], setting the maximum of the input voltages level shifted by a DC voltage $V_B = V_{SG7,8}{}^Q$ to the common source of M_1–M_2. This, again, allows differential pair currents much larger than the quiescent current I_B. Dynamic QFG cascode biasing, as in Figure 4d, is used to avoid that transistors M_1–M_2 and M_3–M_4 enter triode region when such large dynamic currents are generated.

Despite the high power efficiency of the amplifiers of Figure 6a,b, output swing is limited, since the input transistors are at the output branch. Alternative single-stage configurations with increased output swing can be obtained by including a current follower or a current amplifier to convey (and eventually scale) the differential pair current to the output terminal. This current follower/amplifier can be implemented by either a current mirror or a common-gate configuration, leading to the current-mirror (symmetric) and folded cascode amplifiers, respectively [22]. An example of class AB current mirror amplifier is presented in [23]. If high gain is required, a cascode current mirror implementation can be used, as shown in Figure 6c, in fully differential version (CMFB circuit not shown) [22]. The same adaptive biasing of Figure 6a is used, and two class AB cascode current mirrors, following the idea of Figure 4e, convey the current of the input transistors to the output terminals. A class AB folded cascode topology is shown in Figure 6d [19]. The same adaptive bias circuit is used for the input pair, and the NMOS current sources at the folding nodes are replaced by adaptively bias current sources following the scheme in Figure 4b. Dynamic biasing of cascode transistors can be used in Figure 6c,d to prevent slew rate (SR) degradation, as done in Figure 6b.

3.3. Multistage Class A/AB Amplifiers

When both high gain and high output swing are required, usually multistage amplifier topologies are employed. For instance, the conventional Miller amplifier can provide class AB output by employing the circuit of Figure 4c at the output stage [25]. The resulting circuit is shown in Figure 7a, yielding output currents much larger than the bias current I_B and increasing GBW, due to the extra transconductance provided by M_8. It is denoted as a class A/AB amplifier, since the input stage operates in class A and the output stage in class AB. Other examples of class A/AB amplifiers can be found in [26,27].

3.4. Multistage Class AB/AB Amplifiers

A drawback of class A/AB amplifiers is that the input stage can limit slew rate if it is not able to drive the compensation capacitor fast enough. To solve this drawback, class AB operation can also be included at the input stage, leading to class AB/AB topologies. Any of the class AB circuits of Figure 6 can be used at the first stage to this aim. A slightly different approach is shown in Figure 7b [28], where a scaled replica of the current in the output transistor M_5 is fed back to the differential pair. Another example of class AB/AB QFG implementation can be found in [29].

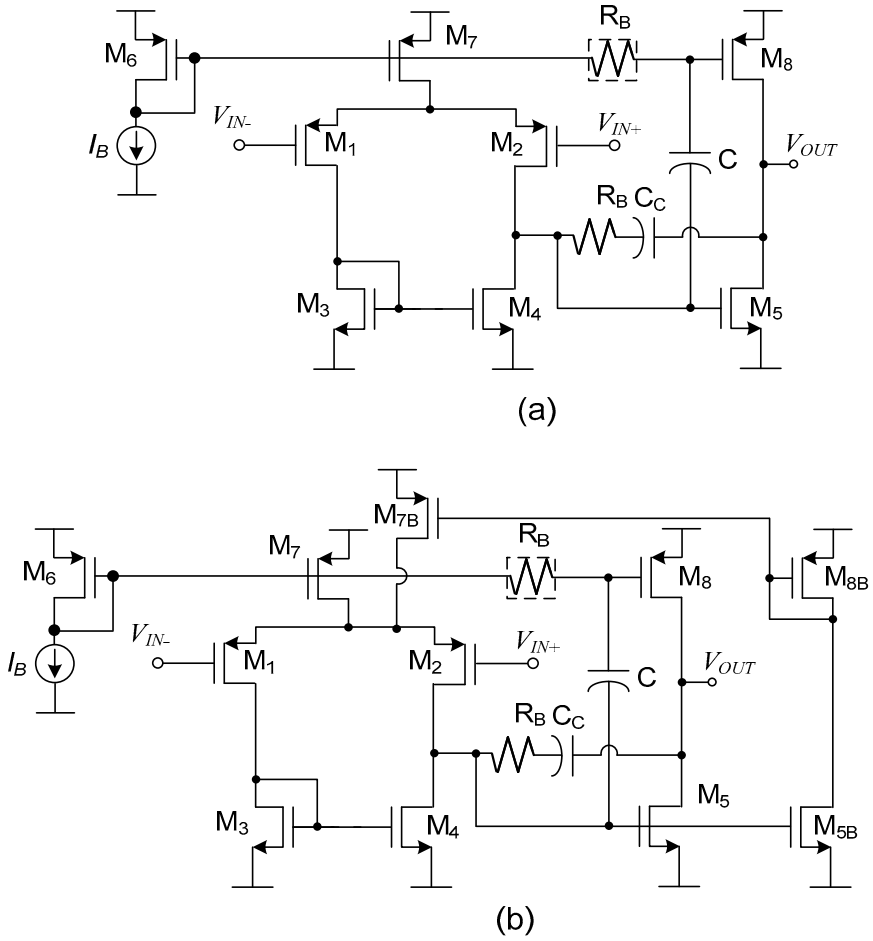

Figure 7. Two-stage Miller amplifiers. (**a**) Class A/AB. (**b**) Class AB/AB.

4. Design Example: Super Class AB QFG Amplifier in a 130 nm CMOS Process

To illustrate the different approaches that can be employed to design energy-efficient amplifiers, a novel topology is presented in this section. It combines various techniques to achieve high performance and very low power consumption. Some of these techniques have been described above and some others are introduced here.

4.1. Requirements and Figures of Merit for Energy Efficiency

An ideal amplifier, in terms of energy efficiency, should achieve the highest small-signal and large-signal performance for a given (and small) quiescent current. A usual way to quantify these requirements is using two conventional figures of merit [68]. The first one is $\text{FoM}_\text{L} = \text{SR}\cdot C_L/I_{supply} = I_{maxL}/I_{supply}$, with SR as the Slew Rate, C_L the load capacitance, $I_{maxL} = \text{SR}\cdot C_L$ as the maximum load current and I_{supply} as the total quiescent current consumption. FoM_L quantifies the large-signal performance for a given I_{supply}. The second one is $\text{FoM}_\text{S} = \text{GBW}\cdot C_L/I_{supply}$, which quantifies the small-signal performance for a given I_{supply}. A power-efficient amplifier should also maximize current utilization [69], defined as the portion of supply current delivered to the load, which is optimal when the large dynamic currents are generated directly at the output branch without internal replication of them.

An optimal choice in terms of energy efficiency is the so-named super class AB amplifiers [69]. They are single-stage topologies combining adaptive biasing at the input differential pair and nonlinear current amplifiers to convey and additionally boost the differential pair current to the output. Super class AB amplifiers can potentially achieve very large FoM_L, due to this double current boosting process, and can also achieve very large FoM_S if the adaptive biasing and nonlinear current amplifiers employed provide enhanced

transconductance. Moreover, current utilization is very high, as the large dynamic currents achieved are generated directly at the output transistors of the nonlinear current amplifier, right at the output branch.

4.2. Proposed Super Class AB Amplifier

Figure 8a shows the proposed circuit, which is based on a recycling folded cascode topology [70]. The same adaptive bias circuit used in Figure 6b, formed by the FVFs M_{1C}–M_{1D} and M_{2C}–M_{2D}, is employed. In quiescent conditions, M_{1C}–M_{2C} have the same $V_{GS}{}^{Q}$ as M_{1A}, M_{1B}, M_{2A} and M_{2B}, and, since they have also the same size, neglecting mismatch and channel length modulation, they set a quiescent current I_B in M_{1A}, M_{1B}, M_{2A}, and M_{2B}. When a differential signal is applied, the largest (winning) input voltage level shifted by the $V_{SG}{}^{Q}$ of M_{1C}–M_{2C} appears at the common source of M_{1A}, M_{1B}, M_{2A} and M_{2B}. Hence, currents in these transistors are not limited by I_B, due to the large currents that can be provided by the FVFs.

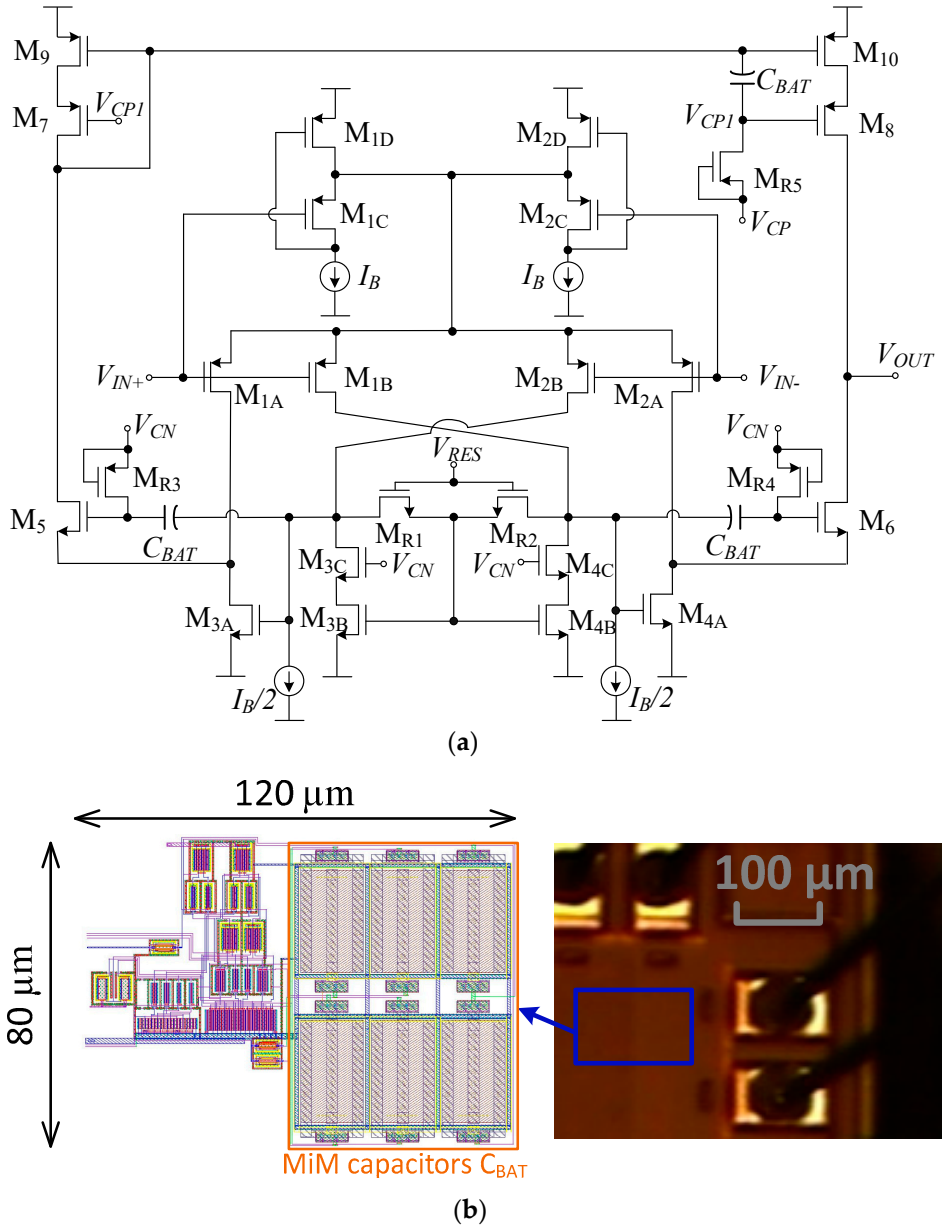

Figure 8. Proposed super class AB QFG amplifier. (**a**) Circuit diagram. (**b**) Microphotograph (layout image also included, due to the opaque die passivation layer).

The differential current amplifier employed to transfer and scale the currents in M_{1B} and M_{2B} to the output is a nonlinear cascode current mirror formed by M_{3A}, M_{3B}, M_{4A}, M_{4B}, M_{3C}, M_{4C}, M_5 and M_6. It employs local common-mode feedback [69] by transistors M_{R1}–M_{R2} acting as tunable active resistors. When a large differential current appears in M_{1B}–M_{2B}, a large voltage drop appears in M_{R1}–M_{R2}, which creates a large current in either M_{3A} or M_{4A}, which reaches the output. Hence, this nonlinear current mirror provides an additional dynamic current boosting.

Current starving is implemented in Figure 8a by two DC current sources that subtract part of the DC input current to the NMOS current mirrors. For a fixed current mirror gain K, current starving allows for decreasing the quiescent current of the current mirror output, thus increasing the amplifier output resistance and DC gain [71]. However, here, current starving is used to increase K without increasing static power. The starving factor used is 0.5, so half of the bias current ($I_B/2$) is subtracted. As a result, K can be doubled in Figure 8a for the same quiescent current consumption.

Adaptive biasing of cascode transistors M_5, M_6, M_7 and M_8 is provided using the QFG technique of Figure 4d to avoid M_{3A}, M_{4A}, M_9 and M_{10} entering triode region for large dynamic currents (which would strongly degrade SR). The simple pseudo-resistor of Figure 2a is enough, in this case.

4.3. Circuit Analysis

Routine small-signal analysis of the circuit of Figure 8a leads to a transconductance

$$G_m \approx g_{m1A}[1 + g_{m3A}(R_{DS}||r_{o2B})] \tag{5}$$

with g_{mi} and r_{oi} as the small-signal transconductance and output resistance of transistor M_i, respectively, and R_{DS} as the resistance of triode transistors M_{R1} and M_{R2}, which is

$$R_{DS} \approx \frac{1}{\beta_{R1,2}\left(V_{RES} - \sqrt{\frac{I_B}{\beta_{3B}}} - V_{SS} - 2V_{TH}\right)} \tag{6}$$

where $\beta_i = \mu C_{ox}(W/L)_i$ is the transconductance factor of transistor M_i. The GBW is GBW = $G_m/(2\pi C_L)$, with G_m defined in Equation (5) and C_L as the load capacitor. The small-signal gain is $G_m \cdot R_{out}$, with $R_{out} = g_{m8}r_{o8}r_{o10}||[g_{m6}r_{o6}(r_{o4A}||r_{o2A})]$ as the output resistance of the amplifier. Using the simple MOS square law, an approximate expression can be found for the SR:

$$SR \approx \frac{\beta_{3A,4A}}{2C_L}\left(\sqrt{\frac{\beta_{1B,2B}}{2\beta_{3B,4B}}}A + \frac{R_{DS}\beta_{1B,2B}}{4}A^2\right)^2 \tag{7}$$

with A as the differential input signal amplitude. Note that SR is not limited by the bias current, as expected from a class AB amplifier. Practical values of SR are, however, lower, due to nonideal effects not considered in Equation (7).

Regarding thermal noise and noting that $g_{m1A} = g_{m1B} = g_{m1C} = g_{m2A} = g_{m2B} = g_{m2C}$, $g_{m3A} = g_{m4A}$, $g_{m3B} = g_{m4B}$ and $g_{m9} = g_{m10}$, the input-referred noise density is

$$V_{n,in}^2 = \frac{2\delta k_B T}{g_{m1A}}\left(2 + \frac{g_{m3B}}{g_{m1A}} + \frac{g_{mI}}{g_{m1A}} + \frac{1}{\delta g_{m1A}R_{DS}} + \frac{1}{g_{m1A}g_{m3A}R_{DS}^2} + \frac{g_{m9}}{g_{m1A}g_{m3A}^2R_{DS}^2} + \frac{1}{g_{m3A}^2R_{DS}^2}\right) \tag{8}$$

with k_B as the Boltzmann's constant, T as the absolute temperature, g_{mI} as the transconductance of the transistors implementing the $I_B/2$ current sources and δ as a parameter that varies from 1/2 to 2/3 from weak inversion to strong inversion. Note that transistors in the output branch have little influence on the input-referred noise, due to the large gain, according to theoretical expectations.

Note, also, that decreasing bias voltage V_{RES} increases R_{DS} and, hence, increases gain, GBW and SR and reduces input-referred noise. Unfortunately, it also reduces phase margin, which can be approximated by

$$PM \approx 90^\circ - \tan^{-1}\left(\frac{GBW}{f_{pND}}\right) \approx 90^\circ - \tan^{-1}\left[g_{m1A}g_{m3A}(R_{DS}||r_{o2B})^2\frac{C_X}{C_L}\right] \quad (9)$$

where $f_{pND} \approx -1/[2\pi(R_{DS}||r_{o2B})C_X]$ is the frequency of the lowest nondominant pole, and C_X is the parasitic capacitance at the nodes where the gates of M_{3A} and M_{4A} are connected. Hence, a tradeoff between gain, GBW, SR, input-referred noise and stability exists for a given C_L. Tuning V_{RES} allows for optimally balancing these parameters and compensating for PVT variations.

4.4. Measurement Results

A 130 nm CMOS technology was employed to fabricate a unity-gain, closed-loop version of the proposed super class AB amplifier of Figure 8a. Transistor aspect ratios W/L (in μm/μm) were 72/0.24 (M_{3A}, M_{4A}), 24/0.24 (M_5, M_6), 12/0.12 (M_7, M_8), 6/2 (M_{R1}, M_{R2}), 0.5/5 (M_{R3}, M_{R4}, M_{R5}) and 12/0.24 for the rest. Three metal–insulator–metal (MiM) capacitors C_{BAT} of 1 pF were employed. A microphotograph of the circuit is shown in Figure 8b, where the layout plot is also shown, since the surface of the die is opaque.

Supply voltages were ±0.5 V and I_B = 3 μA. Cascode bias voltages V_{CP} and V_{CN} were −0.34 V and 0.3 V, respectively, and V_{RES} was set to 480 mV. The measurement setup used is shown in Figure 9.

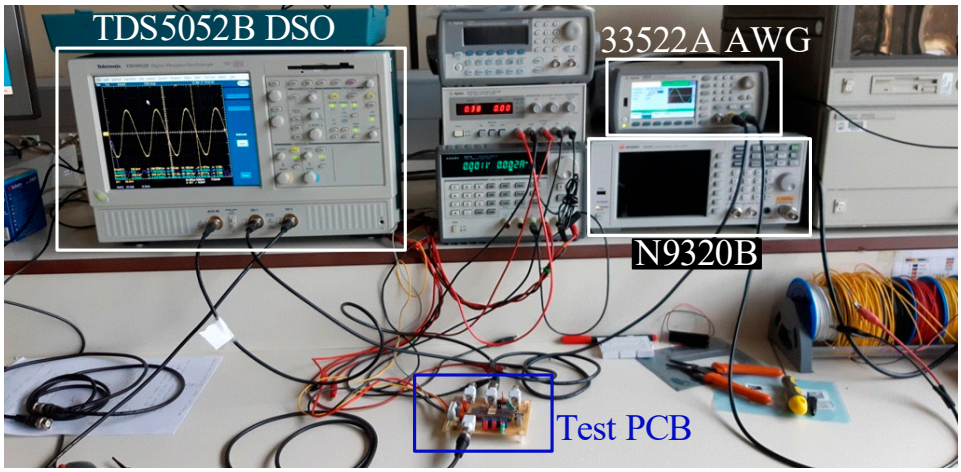

Figure 9. Measurement setup.

For transient response, the input signal was a 1 MHz 0.4 Vpp square wave, with a −0.2 V DC level generated by an Agilent 33522A arbitrary waveform generator, and the output was displayed in a Tektronix TDS5052B oscilloscope. Total load capacitance was 140 pF. Both the input and transient response are plotted in Figure 10. The measured SR values for the rising and falling edge were 5.7 V/μs and −7.1 V/μs, respectively. Figure 11 shows the measured total harmonic distortion (THD) using a 30 kHz input tone, whose amplitude varies from 100 mVpp to 350 mVpp. Note that THD is below 1% in all this range.

The frequency response was also measured (Figure 12) using a Keysight N9320B spectrum analyzer. Since an off-chip buffer was employed to avoid loading the analyzer, total load capacitance was C_L = 120 pF. The cutoff frequency of the proposed OTA was 4.48 MHz, which corresponds approximately to the GBW, because of the dominant pole design.

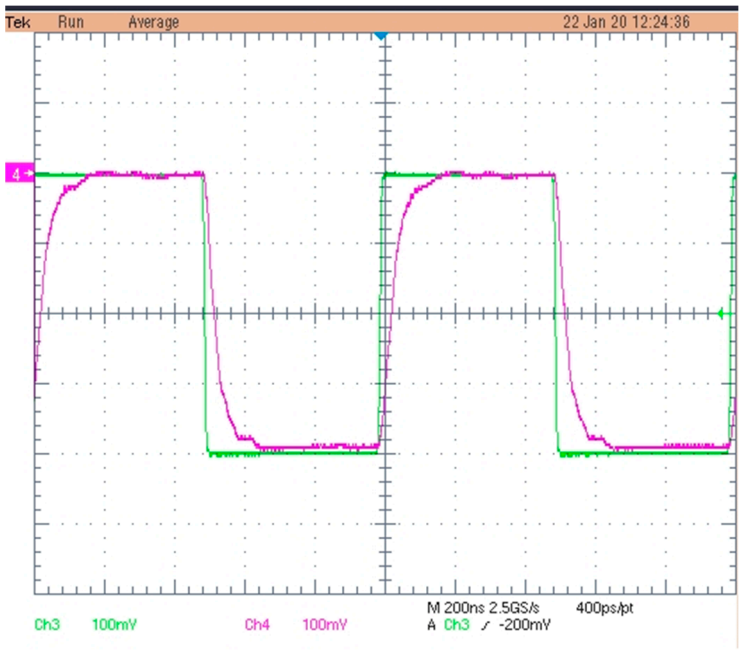

Figure 10. Measured transient response to a square input signal.

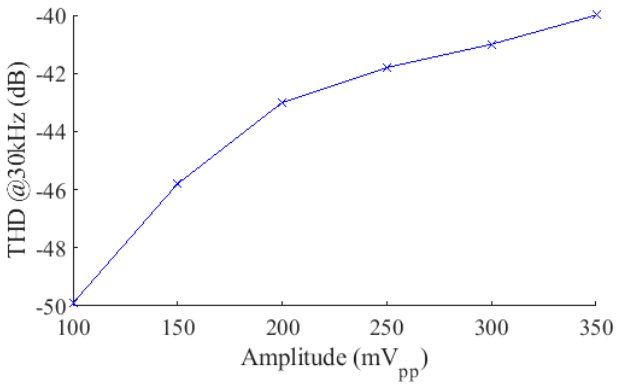

Figure 11. Measured total harmonic distortion (THD) versus input amplitude.

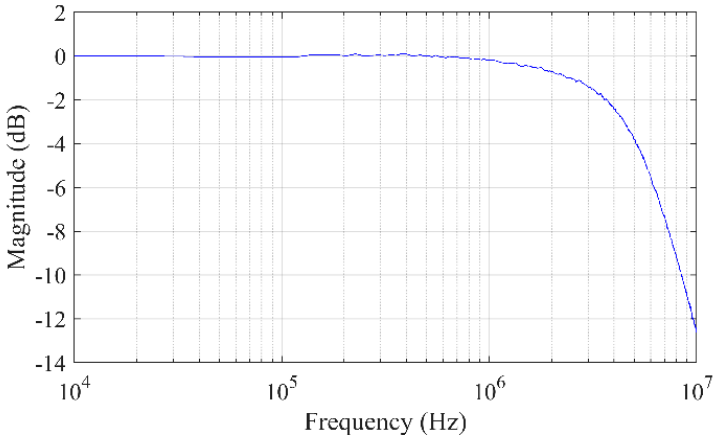

Figure 12. Measured frequency response of the proposed amplifier connected as voltage follower.

5. Discussion

A summary of the main performance parameters of the amplifier is shown in Table 1, including parameters from other reported amplifiers for comparison. Since the fabricated

amplifier is in unity-gain closed loop, open-loop performance parameters (DC gain, Phase Margin PM, Common-Mode Rejection Ratio CMRR and Power Supply Rejection Ratio PSRR) were obtained from post-layout simulations using BSIM4 MOSFET models and the Spectre simulator available in Cadence IC6.1.

Table 1. Summary of measurement results and performance comparison.

Parameter (units)	Figure 8	[18]	[19]	[69]	[70]	[72]	[73]	[74]	[75]	[76]
CMOS process (nm)	130	180	500	500	500	40	180	180	180	130
Supply voltage (V)	±0.5	±0.9	±1	±1	±1	1.1	0.8	0.7	1.8	1.2
Capacitive load (pF)	140/120	23	70	80	70	0.5	8	20	200	5.2
SR+ (V/µs)	5.7	24.11	9.8	100	13.2	1250	0.14	1.8	74.1	98.7
SR- (V/µs)	−7.1	−23.33	−7.6	−78	−25.3	–	–	−3.8	–	–
DC gain (dB)	63.88 [a]	67	81.7	43	76.8	49	51	57.5	72	75.4
PM (°)	61 [a]	84	60	89.5	75.1	65	60	60	50	82.5
GBW (MHz)	4.48	0.57	4.75	0.725	3.4	3600	57	3	86.5	166.1
CMRR @DC (dB)	56.7 [a]	73.2	78	68	112	–	–	19	–	–
PSRR+ @DC (dB)	61.5 [a]	44.1	72	55	92	–	–	52.1	–	–
PSRR- @DC (dB)	71.9 [a]	41.8	74	58	113	–	–	66.4	–	–
Eq. input noise @1MHz (nV/$\sqrt{\text{Hz}}$)	27.5	–	35	230	23	–	–	100	–	–
Power (µW)	30	14.5	120	120	100	3300	1.2	25.4	11900	236.4
Area (mm^2)	0.009	0.030	0.024	0.024	0.030	0.050	0.057	0.020	0.070	–
FoM$_L$ (µA/µA)	29.90	67.72	10.15	118.67	26.95	0.21	0.75	1.54	2.24	2.61
FoM$_S$ (MHz·pF/mA)	17920	1627.4	5541.7	966.7	4760	600	304	1653.5	2616.8	4384.4
$FOM_{AVG} = \sqrt{FOM_S FOM_L}$	732	332	237.1	338.7	358.1	11.18	15.1	50.5	76.6	106.9

[a] Simulation results.

Note that the proposed amplifier showed improved small-signal and large-signal performance just drawing 30 µA from the ±0.5 V power supply. A graphical comparison of FoM$_L$ and FoM$_S$ with different reported amplifiers is shown in Figure 13, where the advantages of the proposed approach are evidenced. Note the good balance between both figures of merit, as deduced from their average value (FoM$_{AVG}$) in Table 1. The main drawback of the proposed amplifier is the extra silicon area required for the capacitors C$_{BAT}$, employed for dynamic cascode biasing, as can be seen in Figure 8b.

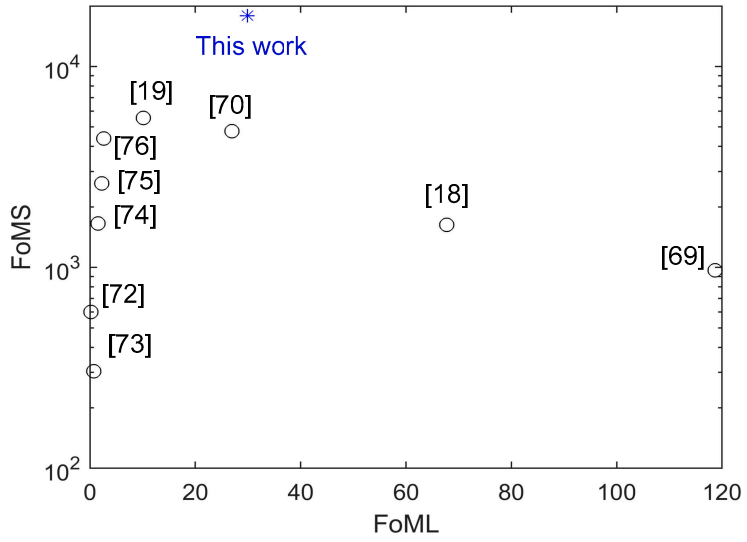

Figure 13. Performance comparison.

6. Conclusions

A comprehensive description of different circuit techniques based on QFG transistors and their application to energy-efficient amplifiers has been presented. Moreover, a new, low-power CMOS amplifier, using adaptive local common-mode feedback with current starving, WTA tail current biasing and QFG transistors for adaptive cascode biasing, has been proposed. Measurement results of the amplifier fabricated in a 130 nm process show very large SR and GBW, maintaining very low static power consumption. The amplifier can be applied in ultra-low-power switched capacitor systems and in general, when both large capacitive loads and low quiescent power are required.

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