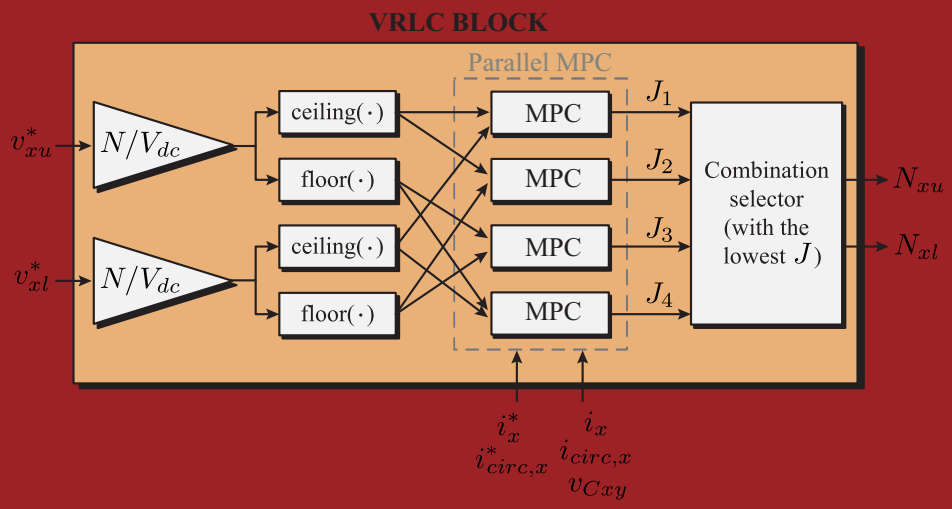
Tesis Doctoral
Ingeniería Electrónica

Cost-Effective Model Predictive Control Techniques for Modular Multilevel Converters



Autor: Jiapeng Yin
Director: José Ignacio León Galván

Departamento de Ingeniería Electrónica
Escuela Técnica Superior de Ingeniería
Universidad de Sevilla

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Profesor Titular

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El tribunal nombrado para juzgar la Tesis arriba indicada, compuesto por los siguientes doctores:

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El Secretario del Tribunal

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A mi madre

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Así termina mi estudio de doctorado de cuatro años. Ha llegado el momento de dar las gracias.

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Jiapeng Yin
Sevilla, 2020

Abstract

In this thesis, model predictive control (MPC) techniques are investigated with their applications to modular multilevel converters (MMCs). Since normally a large number of submodule (SM) capacitor voltages and gate signals need to be handled in an MMC, the MPC schemes studied in this thesis are employed for determining only the voltage levels of converter arms, while gate signals are subsequently generated by the conventional sorting method. Emphasis is given to inner-loop current control in terms of phase current and circulating current, aiming at performance enhancement and computation reduction.

A variable rounding level control (VRLC) approach is developed in this thesis, which is based on a modification of the conventional nearest level control (NLC) scheme: instead of the conventional nearest integer function, a proper rounding function is selected for each arm of the MMC employing the MPC method. As a result, the simplicity of the NLC is maintained while the current regulating ability is improved.

The VRLC technique can also be generalized from an MPC perspective. Different current controllers can be considered to generate the arm voltage references as input of the VRLC block, thus refining the control sets of the MPC. Based on the decoupled current models, the accumulated effect of SM capacitor voltage ripples is investigated, revealing that the VRLC strategy may not achieve a proper performance if the accumulated ripple is nontrivial compared to the voltage per level. Two indexes are also proposed for quantifying the current controllability of the VRLC.

Benefiting from this analysis, A SM-grouping solution is put forward to apply such MPC techniques to an MMC with a large number of SMs, leading to an equivalent operation of an MMC with much reduced number of SMs, which significantly increases the current regulating capability with reduced complexity. As an example, the SM-grouping VRLC proposal is analyzed and its system design principles are described.

This thesis also develops another MPC technique which directly optimizes the cost function using quadratic programming technique. Both a rigorous and a simplified procedure are provided to solve the optimization problem. Compared with the conventional finite control set (FCS)-MPC method which evaluates all voltage level combinations, the proposed scheme presents apparent advantage in terms of calculation cost while achieving similar performance.

Contents

Notation

N	Number of SMs per arm of the MMC
x	$\in \{a,b,c\}$. Phase identifier
y	$\in \{u,l\}$ (upper, lower). Arm identifier
z	$\in \{1,...,N\}$. SM identifier
L_{arm}	Inductance of arm inductor
R_{arm}	Parasitic resistance of arm
C	Capacitance of SM floating capacitor
V_{dc}	DC-link voltage
i_{dc}	DC-link current
v_{Sx}	Grid voltage of phase-x
L	Grid-side inductance (or load inductance in case of load connection)
R	Grid-side resistance (or load resistance in case of load connection)
v_{Cxyz}	Capacitor voltage of SM-xyz
v_{Cxy}	Average SM capacitor voltage of arm-xy
v_{xy}	Arm voltage of arm-xy
i_{xy}	Arm current of arm-xy
i_x	Phase current of phase-x
$i_{circ,x}$	Circulating current of phase-x
W_{xy}	Arm energy of all SMs of arm-xy
$W_{x\Delta}$	Difference of both arm energies of phase-x
$W_{x\Sigma}$	Sum of both arm energies of phase-x
N_{xy}	Number of switched-on SMs (insertion index) of arm-xy
S_{xyz}	Switching state of SM-xyz
f	AC side frequency
ω	Angular frequency of the AC side
f_{sw}	Average switching frequency
T_s	Sampling/control period

f_s	Sampling/control frequency
k	Integer representing a certain time step in the discrete time domain
J_i	Cost function considering current tracking
J_w	Cost function considering arm energy regulating
J_{iw}	Cost function considering both current tracking and arm energy regulating
$p_{1,2,3,4}$	Weighting factors of the original cost functions
u_x	AC output voltage of phase-x considering the decoupled phase-current model
$u_{circ,x}$	Voltage drop across the arm inductor of phase-x considering the decoupled circulating current model
V_C	Reference of SM capacitor voltage
U	Amplitude of ideal expression of u_x
I	Amplitude of ideal expression of i_x
ϕ_x	Initial phase angle of ideal expression of u_x
γ	Phase angle difference between ideal expressions of u_x and i_x
t	Time value in continuous domain
i_{xy}^{SM}	Equivalent SM charging/discharging current of arm-xy
S_{xy}	Average switching function of SMs of arm-xy
v_{Cxy}^{0}	DC component of v_{Cxy}
Δv_{Cx}^{com}	Common-mode ripple component of v_{Cxu} and v_{Cxl}
Δv_{Cx}^{dif}	Differential-mode ripple component of v_{Cxu} and v_{Cxl}
m	Modulation index considering the decoupled phase current model
γ_1	Initial phase angle of Δv_{Ca}^{dif}
N_x^{Σ}	Sum of N_{xu} and N_{xl}
N_X^{Δ}	Difference between N_{xu} and N_{xl}
$\widetilde{N}_x^{\Sigma}$	Error imposed on N_x^{Σ} caused by $\widetilde{u}_{circ,x}$
$\widetilde{N}_x^{\Delta}$	Error imposed on N_x^{Δ} caused by $\widetilde{u}_x$
$\overline{u}_x$	Ideal component of u_x neglecting capacitor voltage ripples
$\widetilde{u}_x$	Synthesized ripple component of u_x
$\overline{u}_{circ,x}$	Ideal component of $u_{circ,x}$ neglecting capacitor voltage ripples
$\widetilde{u}_{circ,x}$	Synthesized ripple component of $u_{circ,x}$
u_{1x}, u_{3x}	Fundamental- and triple-frequency component (respectively) of $\widetilde{u}_x$ normalized by $\frac{NI}{\omega C}$
u_{0x}, u_{2x}	DC and double-frequency component (respectively) of $\widetilde{u}_{circ,x}$ normalized by $\frac{NI}{\omega C}$
γ_2	Initial phase angle of u_{1x}
γ_3	Initial phase angle of u_{2x}
τ	A positive real parameter introduced for current controllability study
τ_{phs}	An index quantifying the phase current controllability
τ_{circ}	An index quantifying the circulating current controllability

Δu_2^{com}	Δv_{Cx}^{com} normalized by $\frac{I}{\omega C}$
δ_{phs}	Variation of predicted phase current value per unit variation of N_x^{Δ}
δ_{circ}	Variation of predicted circulating current value per unit variation of N_x^{Σ}
G_*	Reference point for candidate determination in the two-dimensional $N_{xu} - N_{xl}$ coordinate
$G_{1,2,3,4}$	Candidate points in $N_{xu} - N_{xl}$ coordinate resulted from the VRLC proposal
M	Number of SMs per group in the SM-grouping scheme
B	Number of groups per arm in the SM-grouping scheme
$\lambda_{1,2,3,4}$	Weighting factors of the reformed cost functions
$f_{1,2,3,4}, g_{1,2}$	Intermediate variables for cost-function reformulation
$\boldsymbol{v}_{xy}$	Arm-voltage vector of phase-x
$\boldsymbol{v}_{xy\_0}$	Arm-voltage vector of phase-x corresponding to the minimum value of the unconstrained cost function
v_{xy_0}	Element of $\boldsymbol{v}_{xy\_0}$
v_{dcxy}	Sum of SM capacitor voltages of arm-xy
$\boldsymbol{Q_i}, \boldsymbol{c_i}$	Real-valued coefficient matrices of quadratic function derived from J_i
$\boldsymbol{Q_w}, \boldsymbol{c_w}$	Real-valued coefficient matrices of quadratic function derived from J_w
$\boldsymbol{Q}_{iw}, \boldsymbol{c}_{iw}$	Real-valued coefficient matrices of quadratic function derived from J_{iw}
$q_{i1,2,3}, c_{i1,2}$	Elements of $\boldsymbol{Q_i}$ and $\boldsymbol{c_i}$, respectively
$\boldsymbol{A}, \boldsymbol{b}$	Real-valued coefficient matrices of constraint of optimizing problems
$\mathrm{E}_{1,2}$	Important tangent points in orthogonal coordinate (v_{xu}, v_{xl}) for solving the optimization problems
$v_{xy\_E1,2}$	Coordinate of $\mathrm{E}_{1,2}$

1 Introduction

The age of multilevel converters arrives.

Leopoldo García Franquelo et al., 2008 [1]

1.1 Background

To cater for the ever-increasing global energy demand and reduce the carbon dioxide emission, renewable energy sources (RES) are playing an increasingly important role in the strategy making of many countries aiming at a sustainable development [2]. However, the transition from traditional fossil fuels to the RES is a complicated task which calls for effective coordination of resource management, technological innovation and policy making [3]. Public opinions also need to be well considered by researchers and policymakers to facilitate large-scale integration of the RES [4].

So far, the RES supply only a small portion of the global total amount. According to the statistics from International Energy Agency [5] as shown in Fig. 1.1, the RES comprise a total of 13.8% (not including nuclear power whose renewable nature is still in debate), while the fossil fuels 81.3%, of the global energy power supply in 2018. In particular, solar photovoltaic (PV) and wind power, as RES candidates with the most rapid growth in recent years [6, 7], account for less than 2% in Fig. 1.1 as "other" energy supply sources (together with geothermal, tide/wave/ocean, heat, etc.). Considering the large abundance and accessibility, great potential can be observed in such RES alternatives for resolving global energy crisis and environmental problems. To achieve this goal, technical achievements in power systems are highly involved.

Power electronic converters normally refer to the electrical devices for electrical energy conversions, including DC-to-AC, AC-to-DC, DC-to-DC and AC-to-AC conversions. As core elements of a power system, power converters are employed as fundamental building blocks for both interfaces for integrating the RES into distribution grid [8] and the flexible alternating current transmission system (FACTS) for guaranteeing power quality [9]. In

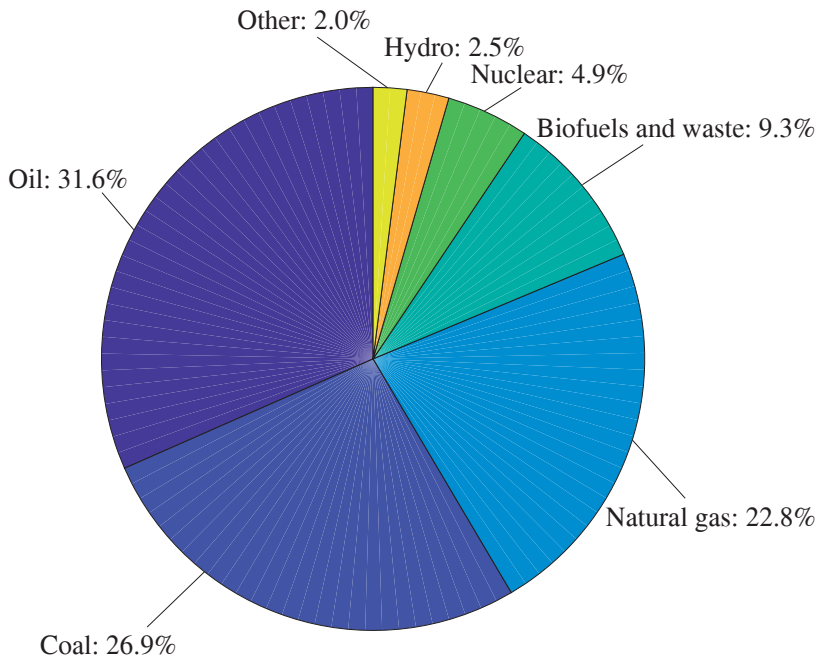


Figure 1.1 Global share of total energy supply by source, 2018 [5].

addition, to power the motor drives for processes in various industrial sectors (such as mining, metal, marine, petrochemical, paper/pulp, cement, etc. [10]) which account for around 40% of the global energy consumption, power converters also play an essential role for their proper functioning. For the most common DC-AC interfacing, conventional power converters are of two levels. With the gate signals determined using pulse-width modulation (PWM) techniques with high carrier frequency, an almost-sinusoidal waveform with low harmonic distortion can be generated at the AC side. However, as world energy demand increases, power converters are required to handle higher power and/or voltage ratings, which demands advancement in either semiconductor technology or new converter topologies.

To meet this increasing requirement of power conversion tasks, the multilevel converters have been considered as a very attractive solution compared with the conventional two-level converters, taking advantage of their ability to achieve medium and high voltage range with mature low-rating power device technology and high-quality output waveforms [1]. Most commonly-used multilevel converter topologies include neutral-point-clamped (NPC) converter [11], cascaded H-bridge (CHB) converter [12], and flying-capacitor (FC) converter [13], while some recently-developed topologies include T-type converter [14],

hybrid multilevel active-NPC [15], etc. All these topologies have been commercialized in industrial applications, each of them possessing unique features and is thus suitable for different application scenarios [16].

In addition to the requirement of increasing power/voltage ratings, the integration and utilization of the RES also lead to more and more distributed energy network of the current and future electrical grid involving multiple energy sources, energy storage and loads. To face this challenge, the high-voltage direct current (HVDC) power transmission systems have emerged [17] owing to their capability of transmitting bulk power, interconnecting asynchronous AC systems, and lower transmission losses compared with the conventional AC transmission systems, leading to better management of power flow within the power systems and enhanced overall stability. The modular multilevel converter (MMC), another important multilevel converter topology proposed in 2003 [18], has been considered as a perfect choice for the HVDC applications [17, 19] and has attracted great interest from power electronics academia and industry. Being comprised of a cascaded connection of independent power cells or the so-called submodules (SMs), the number of which can reach up to several hundreds, the highly modular structure confers the following features on the MMC topology:

- Voltage/power scalability with reduced dv/dt stress, making very high voltage/power achievable by simply adding lower-rating SMs connected in series.
- Possibility of direct connection to medium/high-voltage grid without requiring a step-up transformer, reducing the system complexity.
- Excellent (near sinusoidal) waveform quality of terminal voltage and current when the number of SMs is high enough, eliminating the need of bulky input/output filters for low-order harmonics, leading to a compact size and reduced footprint.
- Low switching frequency (achievable if relaxing the requirements of capacitor voltage balance between SMs without significant negative influences on the converter operation), and thus low switching losses, of individual power devices, resulting in reduced overall loss and very high efficiency.
- Robustness against faulty conditions and easy fault-tolerant operation resulted from modularity, increasing the reliability.
- Easy fabrications and system maintenance enabled by modularized and standardized system layout and buildings.

Owing to the above-summarized advantages, the MMC has been extensively investigated in the previous literatures in a variety of applications apart from the HVDC transmissions, including but not limited to medium-voltage motor drive [20], FACTS [9], active front-end (AFE) [21, 22], DC-DC converter [23, 24], battery energy storage system (BESS) [25, 26], solid state transformer (SST) [27, 28], among others.

In terms of real industrial applications, since its first successful trial, the Trans Bay Cable project in 2010 with a power-transfer capacity of 400 MW and a cable length of 88 km between San Francisco and Pittsburg [29], the MMC has found expanding use in HVDC applications for back-to-back interconnection, multi-terminal transmissions and offshore wind farm integration [30]. In medium-voltage range, commercial applications of the

MMC can be found in motor drives [31] and static synchronous compensator (STATCOM) systems [32]. Commercialized product can be found in many manufacturers including the SVC Light Medium Power from ABB, the HVDC PLUS from Siemens, the MaxSine from Alstom, just to name a few. A more detailed summary of commercial MMC products can be found in [30].

However, the unique structure of the MMC also presents several challenges. To begin with, the circulating currents existing among phases, the SM capacitor voltage ripples, and their coupling effect with each other as well as with the converter input/output voltages/currents, need to be well considered in design and operation. If left uncontrolled, these detrimental effects will lower the efficiency and power quality of the MMC system, even posing threat to the stability of the system. Therefore, effective modulation and control techniques are essential for an MMC in order to achieve a smooth operation with high-quality output currents, and therefore satisfying active/reactive power and/or other desired performance. However, it is not a trivial task considering the multiple involved control objectives. In addition, in an MMC with high number of SMs, a large number of measurements (SM capacitor voltages, arm currents, etc.) and SM gate signals need to be handled, raising higher hardware requirements in order to efficiently carry out the data acquisition and exchange with high-bandwidth communication protocols. Thus, implementation complexity and computational cost of the control and modulation scheme also need to be minimized as much as possible.

Conventional control and modulation schemes for multilevel converters can also be applied to the MMC, among which the PWM (for an MMC with low number of SMs) and the nearest level control (NLC for short, for an MMC with high number of SMs) are the most frequently-used methods. Additionally, a suitable candidate to operate an MMC is the model predictive control (MPC) technique, the effectiveness of which has been reported in a multitude of literatures [33]. The high capability of the MPC in handling multiple control objectives fits perfectly with the nature of the MMC. In addition, fast dynamic, simple design and easy delay compensation are among the advantages of this stream of techniques. However, in an MMC system with multiple number of SMs, a large number of gate signals need to be manipulated, making the MPC implementation relatively complicated in design and costly in calculation, thus calling for more research effort or advancement in high-performance processors. This thesis aims at providing an MPC-based solution for the MMC with enhanced performance and reduced implementation cost, removing the above-mentioned technical barrier.

1.2 Thesis Outline

This thesis can be outlined as follows:

- Chapter 2 provides the literature review and basic background knowledge of the MMC topology and the MPC method.
- Chapter 3 proposes a new VRLC technique as an improved version of the conventional NLC scheme, with the effectiveness validated by several experimental results.

- Chapter 4 generalizes the VRLC as a new stream of MPC strategies with different possible implementations in terms of current controllers, and analyzes the current controllability issues with simulation validation.
- Chapter 5 proposes a SM-grouping operation in order to apply the VRLC method to an MMC with a large number of SMs, with design principles provided, analyzed and verified by several simulation results.
- Chapter 6 develops a new MPC technique with the arm voltage references determined employing the quadratic programming method, the validity of which is supported by both experimental and simulation test results.
- Chapter 7 provides several concluding remarks of the thesis and summarizes possible directions of future research work.

1.3 Main Contributions

The main contributions of this thesis can be summarized as follows:

- Chapter 3
  - The concept of "variable rounding" is proposed for the well-known NLC method for the first time, improving the NLC scheme by selecting proper rounding method from ceiling and floor for different converter arms, overcoming the drawback of the NLC of high arm-voltage-approximation error and thus high current-tracking ripples in medium-voltage applications where the number of SMs per MMC arm (N) is not high, while maintaining the simplicity in controller design and implementation.
  - The merits of both the NLC and MPC schemes are combined in an unified strategy, leading to a simple but effective solution for medium-voltage MMC-based applications with enhanced performance.
- Chapter 4
  - The VRLC technique is generalized as a stream of MPC method, based on the evaluations of only 4 arm-voltage-level combinations per phase per control period, regardless of N, with the arm voltage references derived from either PI/PR, deadbeat or open-loop current controllers.
  - The current regulating capability in terms of phase current and circulating current of the VRLC-MPC scheme is analytically investigated considering the accumulated effect of SM capacitor voltage ripples, and quantified by two newly-proposed indexes.
  - The proposed analysis can be extended to any arm-voltage-level-based control methods for the MMC, providing insight into the functionality and design principles of such methods.
- Chapter 5

  - The applications of the VRLC method and other similar MPC schemes which evaluate very few candidates of arm voltage levels are extended to the MMCs with a large number of SMs, with the help of the current controllability analysis of chapter 4.
  - A SM-grouping technique is presented with which an MMC with a large number of SMs can be analyzed and controlled as an equivalent MMC with much lower number of SMs, simplifying the controller design and alleviating the computational burden.

- Chapter 6
  - The arm voltage references corresponding to the minimum cost function value under the specified feasible set are directly obtained employing quadratic programming technique, instead of evaluating many combinations of arm-voltage levels as required by conventional FCS-MPC schemes, leading to optimal performance defined by the cost function in terms of phase current tracking, circulating current tracking and arm energy regulation.
  - Desired arm voltage levels can be obtained by the VRLC technique with much reduced computational burden since only 4 cost-function evaluations per phase per control period are required, leading to similar (almost identical) performance with the conventional FCS-MPC method [34] that evaluates all the $(N+1)^2$ arm-voltage-level combinations.

- Overall
  - Inner control loops of the MMC are well carried out by the MPC strategy with high current-tracking ability and low implementation complexity, and can be integrated into different MMC-based applications in various operating conditions by simply introducing the conventional outer control loop for the determination of phase/circulating current references.
  - Further removing the barriers for the prospective industrial applications of the MPC techniques to the MMCs, especially those with large number of SMs in high-voltage applications, allowing for an implementation based on micro-processors with reduced processing capability, leading to potential economic gains.

1.4 Publications

During doctoral studies, main publications achieved by the author include

- Yin, Jiapeng, Jose I. Leon, Marcelo A. Perez, Leopoldo G. Franquelo, Abraham Marquez, and Sergio Vazquez. "Model Predictive Control of Modular Multilevel Converters using Quadratic Programming." IEEE Transactions on Power Electronics (2020), doi: 10.1109/TPEL.2020.3034294.

- Yin, Jiapeng, Jose I. Leon, Marcelo A. Perez, Leopoldo G. Franquelo, Abraham Marquez, Binbin Li, and Sergio Vazquez. "Variable Rounding Level Control Method for Modular Multilevel Converters." IEEE Transactions on Power Electronics (2020), doi: 10.1109/TPEL.2020.3020941.
- Yin, Jiapeng, Jose I. Leon, Marcelo A. Perez, Abraham Marquez, Leopoldo G. Franquelo, and Sergio Vazquez. "FS-MPC Method for MMCs with Large Number of Submodules with Reduced Computational Cost." In 2020 IEEE International Conference on Industrial Technology (ICIT), pp. 1083-1088. IEEE, 2020.
- Yin, Jiapeng, Jose I. Leon, Leopoldo G. Franquelo, Sergio Vazquez, and Abraham Marquez. "Cost-effective Design of Modular Multilevel Converter Employing Full-bridge Submodules." In 2019 IEEE 13th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG), pp. 1-6. IEEE, 2019.
- Yin, Jiapeng, Jose I. Leon, Leopoldo G. Franquelo, Sergio Vazquez, and Abraham Marquez. "Generating the Arm Voltage References of Modular Multilevel Converters Employing Predictive Technique." In IECON 2018-44th Annual Conference of the IEEE Industrial Electronics Society, pp. 3949-3954. IEEE, 2018.
- Yin, Jiapeng, Abraham Marquez, Jose I. Leon, Leopoldo G. Franquelo, and Sergio Vazquez. "Improving the operation of the modular multilevel converters with model predictive control." In 2018 IEEE 12th International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG 2018), pp. 1-6. IEEE, 2018.
- Yin, Jiapeng, Jose I. Leon, Leopoldo G. Franquelo, and Sergio Vazquez. "A simple model predictive control strategy aiming at enhancing the performance of modular multilevel converters." In IECON 2017-43rd Annual Conference of the IEEE Industrial Electronics Society, pp. 4247-4252. IEEE, 2017.

Other publications include

- Alcaide, Abraham Marquez, Jose I. Leon, Ramon Portillo, Jiapeng Yin, Wensheng Luo, Sergio Vazquez, Samir Kouro, and Leopoldo G. Franquelo. "Variable-Angle PS-PWM Technique for Multilevel Cascaded H-Bridge Converters with Large Number of Power Cells." IEEE Transactions on Industrial Electronics (2020), doi: 10.1109/TIE.2020.3000121.
- González, Francisco J., Abraham Marquez, Jose I. Leon, Sergio Vazquez, Leopoldo G. Franquelo, and Jiapeng Yin. "Flexible harmonic control for three-level selective harmonic modulation using the exchange market algorithm." In IECON 2018-44th Annual Conference of the IEEE Industrial Electronics Society, pp. 5297-5302. IEEE, 2018.

2 Basics of MMC Operation

This chapter provides the important basic descriptions and literature reviews of the studied topic, which are provided in section 2.1 and 2.2, corresponding to the MMC and the MPC, respectively.

2.1 Modular Multilevel Converters

2.1.1 Structure and topology

The MMC has gained increasing popularity in both academia and industry. Fundamentally, its success can be attributed to its modularity and scalability [18, 35], which can be clearly observed from its unique structure shown in Fig. 2.1. The three-phase configuration is investigated here since it is adopted by most DC-AC applications, while two-phase configuration is adopted more in AC-AC conversion for AC-fed traction vehicles [36, 37], and more-than-three-phase configuration has also been reported [38].

For each one of the three phases ($x = a, b, c$), both the upper and lower ($y = u, l$) arms are equally comprised of a series connection of N SMs, as well as a buffer inductor with inductance value of L_{arm} (R_{arm} represents the parasitic arm resistance accounting for the converter arm losses).

In terms of the SM topology, apart from the half-bridge SM, the full-bridge (or H-bridge) SM has also been extensively adopted for their capability to generate an output voltage with both positive and negative polarity, permitting a reduced DC-link voltage of the MMC but at the cost of increased number of Insulated Gate Bipolar Transistors (IGBTs) [39]. A hybrid MMC configuration with both above-mentioned SM topologies has also been investigated [40]. Other SM topologies are possible through modifications of existing half/full bridges or utilizing conventional multilevel converter topologies, such as the NPC and the FC converters, as building blocks, resulting in new features. Related details can be found in [19].

In this thesis, each SM adopts the most commonly-used half-bridge converter, which outputs zero voltage or the SM floating capacitor voltage v_{Cxyz} (SM number $z = 1, \ldots, N$) by commanding its complementary gate signals. In this way, the MMC is able to achieve

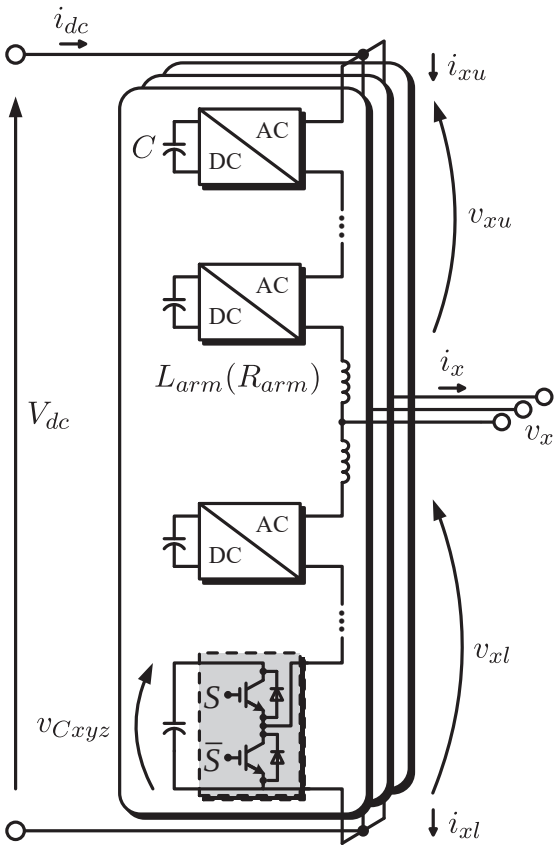


Figure 2.1 Circuit configuration of an MMC.

high-quality voltage waveforms with $N+1$-level arm voltage, $N+1$-level or $2N+1$-level phase voltage depending on specific operating principles (the total number of switched-on SMs per phase is limited as N or not).

When it comes to the circuit configuration, many advanced and hybrid structures have been developed in recent literatures [41], such as the alternate arm MMC [42], modular multilevel matrix converters [43], hexagonal MMC [44], quasi Z-Source MMC [45], etc. In some recent works [46, 47], the CHB converters (in either star or delta configuration) are also called MMC for their "modular" and "multilevel" characteristic. To avoid this confusion, some authors also adopted the terminology of modular multilevel cascade converter (MMCC) proposed in [48] for all such converters, including different possible circuit configurations as the single-star bridge cells (SSBC), the single-delta bridge cells (SDBC), the double-star bridge cells (DSBC), and the double-star chopper cells (DSCC). However, "MMC" is adopted throughout this thesis which refers only to the configuration shown in Fig. 2.1.

2.1.2 Control and modulation

The main control objectives of an MMC generally include the regulation of phase currents, circulating currents and SM capacitor voltages. Typical control structure of an MMC is illustrated in Fig. 2.2.

1) As a primary control objective, the phase current control can be carried out in *abc*, $\alpha\beta$ or *dq* frame, aiming at a well tracking of the corresponding references given according to the requirements of specific applications [30]. Existing control schemes for either two-level converters [49] or conventional multilevel converters [16] can be adopted by the MMC as well. Proportional-integral (PI) or proportional-resonant (PR) controllers are normally chosen [47, 50].

2) The circulating current refers to the common-mode component of both arm currents of the same phase, which is generated by the unavoidable difference between the sum of inserted SM capacitor voltages of the corresponding phase and the DC-link voltage being imposed on the arm impedance (arm inductance and parasitic resistance). It contains a necessary DC component for power exchange between the DC and AC sides of the MMC and harmonic components as a result of the circular interactions between the electrical quantities [51] which add to the converter losses.

The circulating current controllers are normally designed to eliminate the AC components (mainly of second order and negative sequence) for loss reduction, or in some cases to track DC-plus-AC references for SM capacitor voltage regulation (such as ripple reduction) [35]. Resonant controllers tuned at certain harmonic frequencies are commonly used for this control purpose [52]. $abc-dq$ transformation can also be applied to the three-phase circulating currents such that the PI controllers can be employed to regulate the resulted DC signals [53].

3) Since each SM is equipped with a floating capacitor, the capacitor voltages present unavoidable fluctuations through charging/discharging, which will have negative effects on the operation of the MMC. Thus, corresponding regulations are required to maintain the balance between different SMs with the amplitude of ripples as low as possible.

The SM capacitor voltages are normally controlled in two stages, namely the arm-total-capacitor-voltage control (or arm energy control) which regulates the DC component of SM capacitor voltages to the nominal value, and the capacitor voltage balancing among the SMs within the same arm.

The first control stage can be achieved by dedicated controllers which give the circulating current references, the basic principle of which is to adjust the DC and fundamental-frequency components of circulating current references for the regulation of total SM energy and SM energy balance between both arms, respectively, of each phase [54].

The second-step control of within-arm balancing is achieved depending on which modulation scheme is applied once the arm voltage references are determined by the above-mentioned controllers of phase current, circulating current and arm energy. An extra individual capacitor-voltage-balancing controller is required for each SM if the gate signals are determined directly by the conventional PWM strategy [55, 56]. Phase-shifted PWM or level-shifted PWM can be adopted [57]. However, in high-power applications, the MMC usually contains several dozens or even hundreds of SMs per arm, thus making it complex to equip every SM with a carrier and an individual capacitor voltage controller. In addition,

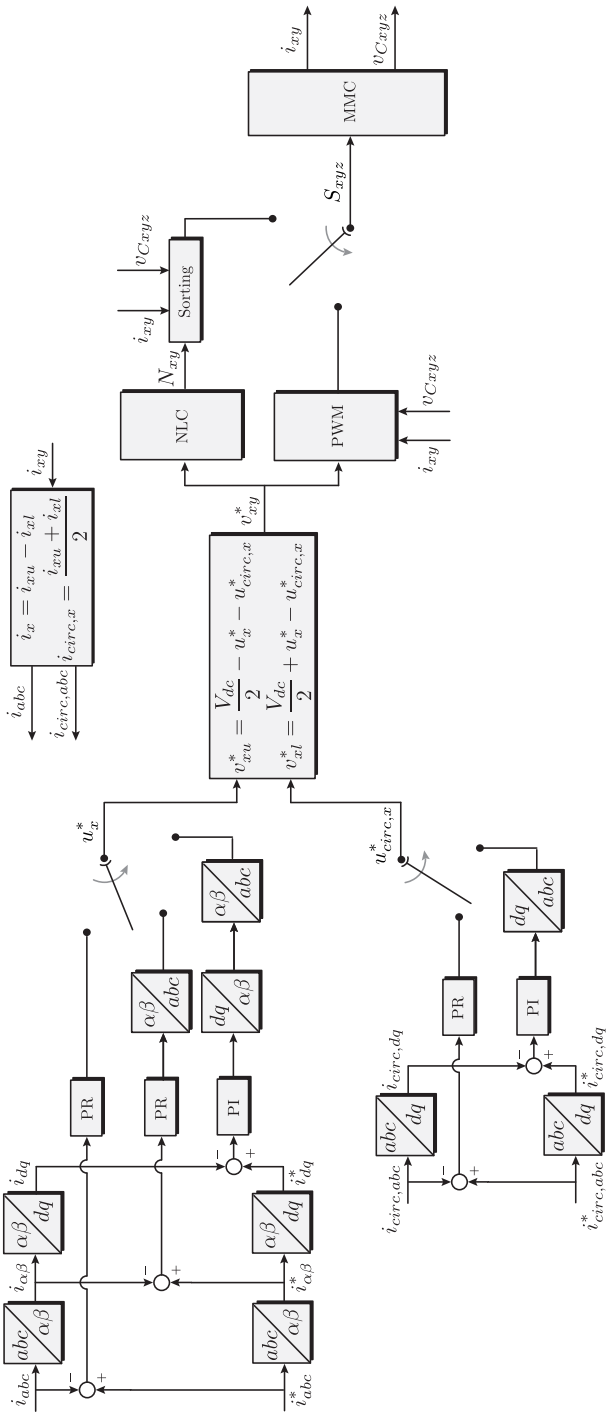


Figure 2.2 Commonly-adopted control structure of an MMC.

carrier-based PWM schemes normally present high switching frequency, and thus high switching losses. For these reasons, it is preferable to determine the gate signals indirectly employing pseudomodulation techniques if the number of SMs of the MMC is not low [58]: the number of SMs to be switched on (also called insertion index) of each arm is obtained first, followed by the sorting-based SM selection technique seeking for the balance of SM capacitor voltages. Among this stream of methods [34, 54, 59–65], the nearest level control (NLC) [60, 61] has been extensively adopted for its simple implementation, which is especially advantageous for an MMC with high number of SMs per arm, such as in the HVDC transmission [16]. The main drawback of the NLC technique is higher phase current distortion in medium and low voltage range, due to its approximative nature derived from rounding function.

SM capacitor voltage balancing is an important control issue that has been extensively investigated. In additional to the above-mentioned individual PI controller and sorting scheme, many advanced balancing algorithms have been developed for reducing switching frequency and/or simplifying hardware implementation [60,66–68]. It is worth mentioning that, as an interesting alternative, this SM capacitor voltage balancing effect can also be achieved by modifying the circuit topology of the MMC [69, 70]. Such methods allow a high-performance sensor-less balancing, but at the cost of higher hardware complexity than standard MMCs.

Other existing modulation techniques for the conventional multilevel converters can be extended to the MMC as well. As examples, the space vector modulation (SVM) has been reported in [71, 72], and the selective harmonic elimination has been reported in [73, 74], etc. However, these methods present increasing complexity as the number of voltage levels of the MMC grows.

Other important issues to be taken into account for the operation of the MMC include: converter loss evaluation [75], thermal balancing [76], unbalanced grid conditions [77], fault-tolerant operation [72], start-up procedures [78], and mission profile evaluation [79], just to name a few.

2.2 Model Predictive Control

The MPC refers to a stream of methods with explicit use of the mathematical models of the system to be controlled. The MPC techniques generally include two categories: the finite control set-MPC (FCS-MPC) and continuous control set-MPC (CCS-MPC) [80].

Coinciding with the discrete nature of power converters, the FCS-MPC methods have been extensively adopted by power electronic applications [81]. The FCS-MPC works with the following fundamental principle: utilizing the discrete mathematical model of the system, objective variables are predicted with different possible control actions and then evaluated by a cost function, in a periodical manner, with the optimal control action (corresponding to the lowest cost function value) being applied at the next instant of control updating. To facilitate understanding, the control diagram of the FCS-MPC technique is illustrated in Fig. 2.3 taking the phase current and circulating current control of the MMC as an example, where those variables with hat operator denote the corresponding predicted currents.

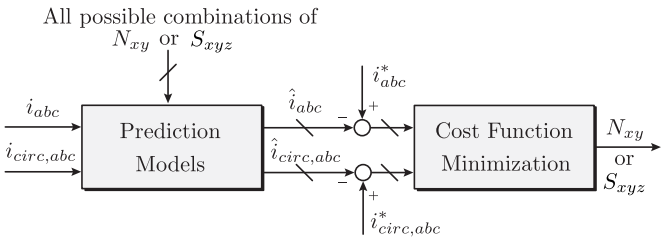


Figure 2.3 Basic concept of the FCS-MPC for controlling an MMC.

Another alternative, the CCS-MPC, operates in a different way: the desired output voltage of the power converters are derived directly using the information of the system model, followed by a posterior modulator (which can be selected freely) to generate the output voltage reference. Two common CCS-MPC techniques are the generalized predictive control (GPC) [82] and explicit MPC (EMPC) [83]. Compared with the FCS-MPC alternative, the CCS-MPC can achieve potential calculation reduction and easier regulation of switching frequency, though it normally presents more complex formulation (of optimization problem solving) as well [80].

Traditionally, the MPC (either FCS-MPC or CCS-MPC) applied to complex power converters (such as multilevel converters) is facing issues about high computational burden that step by step are being overcome. Thanks to the advancement of microprocessors, the MPC schemes have been gaining increasing research attention and expanding applications in recent years [80].

The FCS-MPC is mainly investigated in this thesis, while the CCS-MPC is also employed in chapter 6.

2.2.1 System model

The modelling of the system plays a fundamental role in the functioning of an MPC method. These models are employed for predicting the behaviors of the system, either explicitly in the FCS-MPC schemes or implicitly in the CCS-MPC schemes.

Continuous model

To explain the working principles of the MPC to an MMC, the mathematical models of the MMC-based system need to be introduced first. From the MMC topology shown in Fig. 2.1, considering DC-AC power conversion where the AC side of the MMC is connected through an $R-L$ filter to a grid with phase voltage of v_{Sx}, and treating each phase independently, the per-phase circuit of the investigated MMC-based system is provided in Fig. 2.4a. The common-mode voltage of the AC-side neutral point relative to that of the DC side can be neglected since it is normally trivial in a balanced operation. The model is flexible because in case of off-grid connection, v_{Sx} is equal to zero and R, L denote the corresponding load parameters.

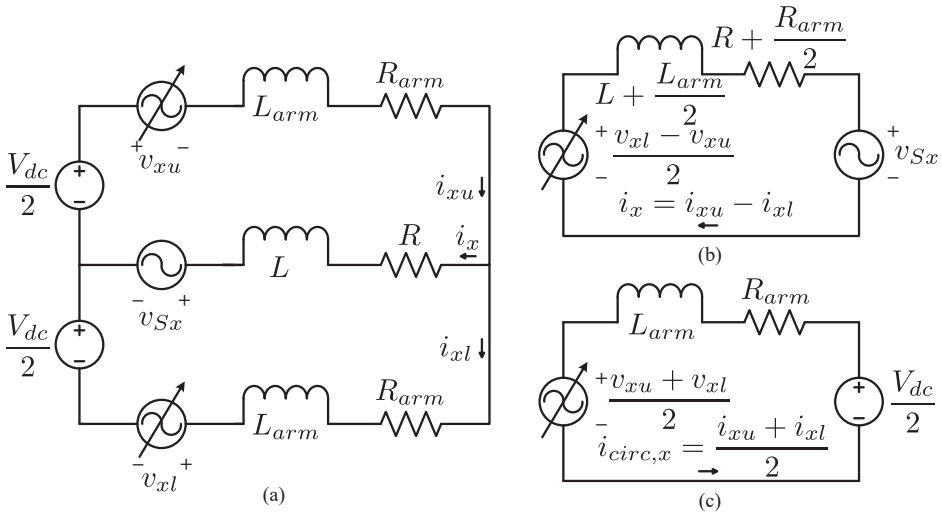


Figure 2.4 Per-phase models of a grid-connected MMC system: (a) circuit of phase-x. (b) equivalent phase-current model. (c) equivalent circulating-current model.

Applying the Kirchhoff's voltage Law (KVL) to an arbitrary phase-x, the following equations can be respectively obtained for the voltage paths of upper arm and lower arm as

$$\frac{V_{dc}}{2} - v_{xu} - L_{arm}\frac{di_{xu}}{dt} - R_{arm}i_{xu} = v_{Sx} + L\frac{di_x}{dt} + Ri_x \tag{2.1}$$

$$-\frac{V_{dc}}{2} + v_{xl} + L_{arm}\frac{di_{xl}}{dt} + R_{arm}i_{xl} = v_{Sx} + L\frac{di_x}{dt} + Ri_x. \tag{2.2}$$

Applying the Kirchhoff's current Law (KCL), the phase current and circulating current can be respectively expressed from arm currents as

$$i_x = i_{xu} - i_{xl} \tag{2.3}$$

$$i_{circ,x} = \frac{i_{xu} + i_{xl}}{2}. \tag{2.4}$$

Imposing sum and difference operations on (2.1) and (2.2) while considering (2.3) and (2.4), the mathematical models of the output current and circulating current can be respectively derived as

$$(L_{arm} + 2L)\frac{di_x}{dt} = (-R_{arm} - 2R)i_x - 2v_{Sx} - v_{xu} + v_{xl} \tag{2.5}$$

$$2L_{arm}\frac{di_{circ,x}}{dt} = -2R_{arm}i_{circ,x} + V_{dc} - v_{xu} - v_{xl}. \tag{2.6}$$

To aid comprehension, the corresponding decoupled phase-current and circulating-current circuits are provided in Fig. 2.4b and 2.4c, respectively.

Each arm voltage v_{xy} is equivalent to a controllable voltage source, the value of which is given by the sum of all SM output voltages of that arm as

$$v_{xy} = \sum_{z=1}^{N} S_{xyz} v_{Cxyz} \tag{2.7}$$

where the switching state $S_{xyz} = 0$ or 1 if the corresponding SM capacitor is bypassed or inserted into the arm voltage. Neglecting the difference between different SM capacitor voltages of the same arm (provided that an effective balancing method is used, this difference is relatively trivial compared to the reference of capacitor voltage, and thus this assumption can be made safely), (2.7) can be reformed to

$$v_{xy} \approx N_{xy} v_{Cxy} \tag{2.8}$$

where N_{xy} denotes the number of switched-on SMs, or the so-called insertion index, of the corresponding arm as

$$N_{xy} = \sum_{z=1}^{N} S_{xyz} \tag{2.9}$$

and v_{Cxy} is defined as the average SM capacitor voltage of the corresponding arm as

$$v_{Cxy} = \frac{\sum_{z=1}^{N} v_{Cxyz}}{N}. \tag{2.10}$$

The total energy of all SMs of a certain arm is denoted by W_{xy} as

$$W_{xy} = \frac{C}{2} \sum_{z=1}^{N} v_{Cxyz}^2 \approx \frac{CNv_{Cxy}^2}{2}. \tag{2.11}$$

In the same phase-x, the difference and sum of the total energy of both arms are defined as

$$W_{x\Delta} = W_{xu} - W_{xl} \tag{2.12}$$

$$W_{x\Sigma} = W_{xu} + W_{xl} \tag{2.13}$$

respectively. Their dynamics satisfy

$$\frac{dW_{x\Delta}}{dt} = i_{xu} v_{xu} - i_{xl} v_{xl} \tag{2.14}$$

$$\frac{dW_{x\Sigma}}{dt} = i_{xu} v_{xu} + i_{xl} v_{xl}. \tag{2.15}$$

Discrete model

As a crucial part of the MPC technique, the above mathematical models need to be discretized for prediction purposes. Applying the commonly-used forward Euler approximation to (2.5), (2.6), (2.14) and (2.15) during time step k to $k+1$ (with sampling time of

T_s), the corresponding discrete models can be derived as

$$\hat{i}_x(k+1) = i_x(k) + \frac{T_s}{L_{arm}+2L}[(-R_{arm}-2R)i_x(k) - 2v_{Sx}(k) - v_{xu}(k) + v_{xl}(k)] \quad (2.16)$$

$$\hat{i}_{circ,x}(k+1) = i_{circ,x}(k) + \frac{T_s}{2L_{arm}}[-2R_{arm}i_{circ,x}(k) + V_{dc} - v_{xu}(k) - v_{xl}(k)] \quad (2.17)$$

$$\hat{W}_{x\Delta}(k+1) = W_{x\Delta}(k) + T_s[i_{xu}(k)v_{xu}(k) - i_{xl}(k)v_{xl}(k)] \quad (2.18)$$

$$\hat{W}_{x\Sigma}(k+1) = W_{x\Sigma}(k) + T_s[i_{xu}(k)v_{xu}(k) + i_{xl}(k)v_{xl}(k)]. \quad (2.19)$$

2.2.2 Cost function

The cost function is responsible for the evaluation of a candidate control action in terms of several specified control objectives, normally in the form of weighted sum of tracking errors of the related control quantities. It defines the optimal performance of the system.

Considering only current tracking

In order to employ the MPC technique, the cost function is introduced as

$$J_i = p_1|i_x^* - \hat{i}_x|^h + p_2|i_{circ,x}^* - \hat{i}_{circ,x}|^h \quad (2.20)$$

taking into account the tracking errors of output current and circulating current which are the most important control objectives of an MMC. $p_{1,2} > 0$ denote the weighting factors and the variables with $*$ denote the corresponding references. h normally equals 1 or 2. The current references are determined by outer control loop according to the applications and/or operating conditions, which are considered here as given information and the investigation will be focused on the inner current control loop implemented with an MPC. In most of the cases, this outer loop can be implemented by the conventional field-oriented control (FOC) and voltage-oriented control (VOC) for motor drives and grid connected applications, respectively.

Considering arm energy regulation

To regulate the energy stored in the SM capacitors, the cost function can be defined as follows

$$J_w = p_3|W_{x\Delta}^* - \hat{W}_{x\Delta}|^h + p_4|W_{x\Sigma}^* - \hat{W}_{x\Sigma}|^h. \quad (2.21)$$

Normally, J_w is not applied alone, but as an auxiliary term together with J_i as

$$J_{iw} = J_i + J_w. \quad (2.22)$$

Other control objectives can also be included in the cost function, such as individual SM capacitor voltage ripple, switching frequency, active/reactive power, and so on, which are not the focus of the thesis.

2.2.3 Common MPC techniques for MMC

Commonly-adopted implementations of the MPC techniques can be outlined in Fig. 2.5. In a direct application of the conventional MPC principle, namely the FCS-MPC, to an MMC

as shown in Fig. 2.3, all possible switching states need to be evaluated, which amounts to 2^{6N} combinations of S_{xyz} [84]. If each phase is treated independently, this combination number can be reduced to 3×2^{2N}. Furthermore, if the total number of switched-on SMs of each phase is limited to N, this number can be reduced to $\frac{(2N)!}{(N!)^2}$ per phase [85]. However, all these techniques present extremely high calculation burden and are only feasible for an MMC with very low number of SMs.

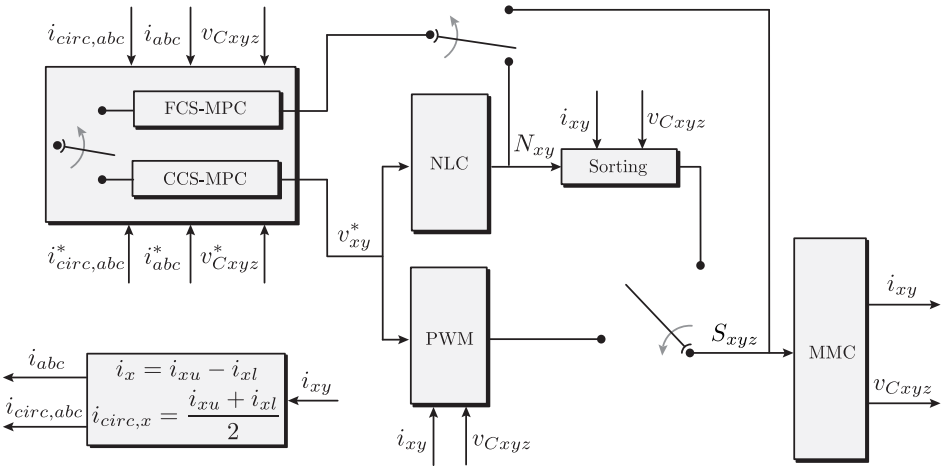


Figure 2.5 Commonly-used MPC control structure of an MMC.

To make the MPC more suitable for the MMC with reduced computational burden, the SM capacitor voltage balancing can be achieved by the conventional sorting scheme, and thus the MPC is employed to obtain solely the voltage level/insertion index for each arm [33]. Normally, for each phase, different combinations of insertion indexes of the upper and lower arms are compared in order to select the optimal one, leading to $(N+1)^2$ candidates per phase to be evaluated [34]. Several research works have dedicated effort to refine the candidates according to the operation [63–65, 86]. However, the resulting size of control set is still, at least, proportional to N, and moreover, with possibility of losing optimality of the original method proposed in [34]. Several solutions have been developed in [68, 87] which only need to evaluate 2-4 voltage level combinations regardless of N, but their potential limitations in current control have not been analyzed.

As an alternative of the FCS-MPC method, the CCS-MPC scheme derives the output voltage reference analytically and then applies the modulation stage to generate the switching signals [82, 83]. In the context of the MMC, several CCS-MPC techniques have been developed during the last years [88–90], which normally integrate the PWM scheme to generate the derived arm voltage reference, leading to a better regulated harmonic spectrum and a fixed switching frequency.

3 Variable Rounding Level Control

This chapter describes and validates a new control method named variable rounding level control (VRLC) as an improved version of the conventional NLC scheme which is made possible by adopting the MPC concept. The chapter is structured as follows. Section 3.1 introduces the conventional NLC-based control scheme of the MMC. Section 3.2 provides basic descriptions of the proposed VRLC method and section 3.3 explains the implementation of the VRLC strategy by applying an MPC technique. At last, the experimental evaluations are described and analyzed in section 3.4.

3.1 Conventional Control Structure of an MMC

As explained in section 2.1, considering the high switching losses and complex implementation structure of the PWM schemes in medium/high-voltage MMC-based applications, it is more reasonable to operate the MMC in such application scenarios with the conventional NLC method, which is included in the family of pseudomodulation strategies [58]. The conventional control structure including the pseudomodulation method is shown in Fig. 3.1. The AC side is configured as load connection in this chapter (for grid-connection configuration, feedforward terms of grid voltages need to be added to the output of PI current controllers).

As the first step of the conventional MMC controller structure, the three-phase phase currents (i_x) are transformed into the dq frame generating i_d and i_q being controlled by dedicated PI controllers. It is important to notice that i_d^* and i_q^* are determined according to the required nominal power to be delivered. Since this chapter focuses on the inner-control-loop design and modulation, the external controllers which are responsible for generating i_d^* and i_q^* are not shown.

On the other hand, the circulating current reference $i_{circ,x}^*$, being tracked by the use of dedicated controller, is normally assigned a DC value, which is equal to

$$i_{circ,x}^* = \frac{I_{dc}^*}{3} \tag{3.1}$$

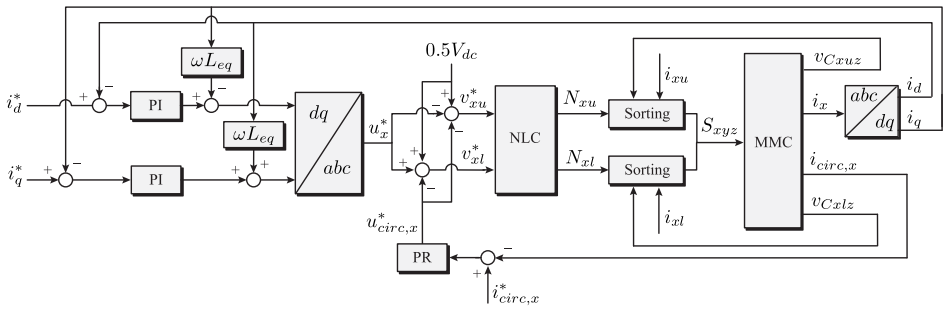


Figure 3.1 Diagram of the conventional phase current and circulating current control of the MMC, including the SM floating capacitor voltage balancing strategy.

where I_{dc}^* is determined such that $I_{dc}^* \cdot V_{dc}$ provides the sum of the active power of the AC side and the losses. The losses are difficult to be estimated especially those caused by the nonideality of the IGBTs. Therefore, an extra PI controller can also be introduced to better regulate the total energy of each converter phase (and also of both converter arms of each phase) which generates $i_{circ,x}^*$ [54].

Taking into account the MMC mathematical model introduced in section 2.2, for convenience of controller design, the internal AC output voltage of the converter considering the decoupled phase current model can be defined as

$$u_x = \left(\underbrace{\frac{1}{2}L_{arm} + L}_{L_{eq}} \right) \frac{di_x}{dt} + \left(\underbrace{\frac{1}{2}R_{arm} + R}_{R_{eq}} \right) i_x \tag{3.2}$$

and the circulating-current-related voltage drop across the arm inductor is defined as

$$u_{circ,x} = L_{arm} \frac{di_{circ,x}}{dt} + R_{arm} i_{circ,x} \tag{3.3}$$

In this thesis, the current-regulating voltages derived from the decoupled current models are denoted by u to be distinguished from those measurable voltage quantities denoted by v.

Considering expressions (2.5), (2.6), (3.2) and (3.3), the arm voltages can be derived as

$$v_{xu} = \frac{1}{2}V_{dc} - u_x - u_{circ,x} \tag{3.4}$$

$$v_{xl} = \frac{1}{2}V_{dc} + u_x - u_{circ,x}. \tag{3.5}$$

which provide the outline for the current control loop design of the MMC. The references of the arm voltages (v_{xu}^* and v_{xl}^*) can be obtained by replacing u_x and $u_{circ,x}$ with their corresponding references u_x^* and $u_{circ,x}^*$.

Once the references of the arm voltages (v_{xu}^* and v_{xl}^*) are generated, the NLC method is

applied to determine N_{xy}: in each sampling time the number of the switched-on SMs in each arm (or insertion index, arm voltage level) is easily determined by normalizing (by DC-link voltage V_{dc}) and rounding the arm voltage reference v^*_{xy} as follows

$$N_{xy} = \text{round}\left(\frac{v^*_{xy}}{V_{dc}/N}\right) \tag{3.6}$$

the result of which is then restricted to $0 \leq N_{xy} \leq N$ by a saturation block. It is important to mention that the above-mentioned phase/arm energy controllers are not necessary since the DC-link voltage (which is assumed constant) is used for normalizing the arm voltage reference, which guarantees the asymptotic stability of the system as analyzed in [91].

Though applying the NLC to an MMC highly reduces the switching losses, and moreover simplifies its hardware implementation avoiding the use of carrier signals [52, 60, 92], an error exists in the arm voltage generation due to the rounding operation, the maximum value of which is $0.5V_{dc}/N$ as can be inferred from (3.6). This error is tolerable only if N is large enough.

The gate signals for all SMs (indicated by S_{xyz}) are finally determined by a sorting strategy [18]. Specifically, the SMs with the lowest capacitor voltage are selected to be switched on if the arm current is positive (charging), and the SMs with the highest capacitor voltage are selected to be switched on if the arm current is negative (discharging). This sorting strategy balances the SM capacitor voltages in each MMC arm.

3.2 Proposed VRLC Strategy Basic Concept

The application of the NLC method to the MMC leads to a reduction in the switching losses compared with other carrier-based modulation techniques, while the resulting output waveforms present higher total harmonic distortion (THD) [58]. As mentioned before, the conventional NLC scheme introduces an arm-voltage-generating error up to $0.5V_{dc}/N$, which will degrade the control performance especially when N is not large.

Moreover, the NLC method leads to a high amplitude of circulating current and extra controllers have to be added to the MMC control structure as shown in Fig. 3.1. According to the operating principle of the NLC, the number of switched-on SMs for each phase ($N_{xu} + N_{xl}$) has to be kept as N in order to suppress the circulating current. However, unavoidable capacitor voltage ripples accumulate across the N switched-on SMs and the consequent mismatch between $v_{xu} + v_{xl}$ and V_{dc} are then applied to the arm inductors. This fact leads to an uncontrolled circulating current which can further jeopardize the quality of the output current also increasing the MMC losses. As a common practice, (3.6) can be modified through adjusting v^*_{xy}, in which case a PI or PR circulating current controller needs to be included [52, 53].

In this chapter, the PR controller [52] is adopted in the conventional control scheme to achieve the above mentioned circulating current regulation, as shown in Fig. 3.1. In order to obtain a good performance of phase current tracking while maintaining the circulating current regulated, both the PI and PR controllers in Fig. 3.1 have to be well designed.

However, the coordination of both groups of controllers is not a straight-forward task since multiple control parameters need to be tuned.

To mitigate these issues, a VRLC approach is proposed in this chapter as a modified version of the NLC technique. The entire VRLC scheme is outlined in Fig. 3.2. The reference arm voltages v^*_{xu} and v^*_{xl} are determined using expressions (3.4) and (3.5) similar to the conventional control scheme. However, instead of using PR controller, $u^*_{circ,x}$ is determined in an open-loop manner by applying expression (3.3) with the input reference $i^*_{circ,x}$. Then, as the core of the proposed control scheme, the insertion indexes N_{xy} determined by expression (3.6) are modified in order to enhance the output current quality and regulate the circulating current. Different rounding functions, namely floor() and ceiling(), are considered in each MMC arm as follows

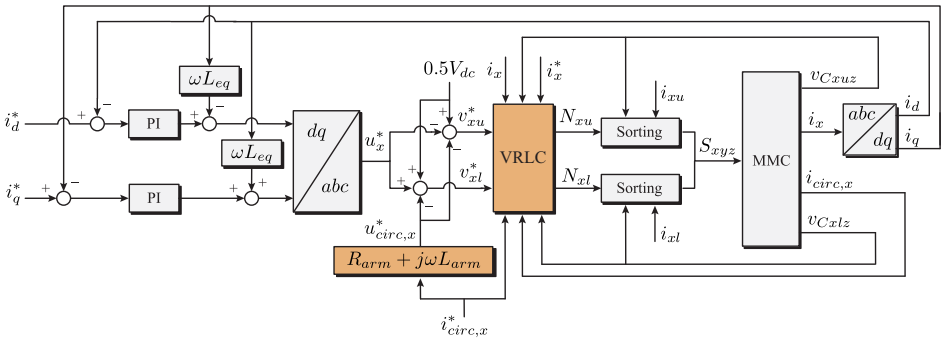


Figure 3.2 Structure of the control method highlighting the proposed new blocks compared with the conventional control structure shown in Fig. 3.1.

$$N_{xy} = \text{floor}\left(\frac{v^*_{xy}}{V_{dc}/N}\right)$$
$$N_{xy} = \text{ceiling}\left(\frac{v^*_{xy}}{V_{dc}/N}\right) \tag{3.7}$$

The floor() function rounds a real number to the largest integer that is not greater than the real number. The ceiling() function rounds a real number to the least integer that is not less than the real number. As an example, $\text{floor}(3.8) = 3$ and $\text{ceiling}(3.4) = 4$. In the VRLC method, each phase is treated independently and each arm selects its respective rounding function (floor or ceiling), thus leading to four possible combinations of rounding functions per phase. In each phase, the possible four combinations are further evaluated according to certain performance criterion and the optimal one is selected to be finally applied.

To facilitate understanding, an example of an arm voltage reference and its corresponding actual arm voltages (5 levels, $N = 4$) resulted from different rounding methods are illustrated in Fig. 3.3, where the capacitor voltage ripples are neglected and the rounding operations are applied periodically. It can be observed that the round function adopted by

the conventional method (Fig. 3.1) acts as a very rough candidate approximation and a large discrepancy exists between the induced arm voltage and reference. Even equipped with a circulating current controller, the intrinsically approximative feature of the round function makes the conventional scheme less accurate in voltage level determination. In comparison, the VRLC proposal carries out a periodical selection of rounding functions, leading to more voltage-level jumping required for current regulation.

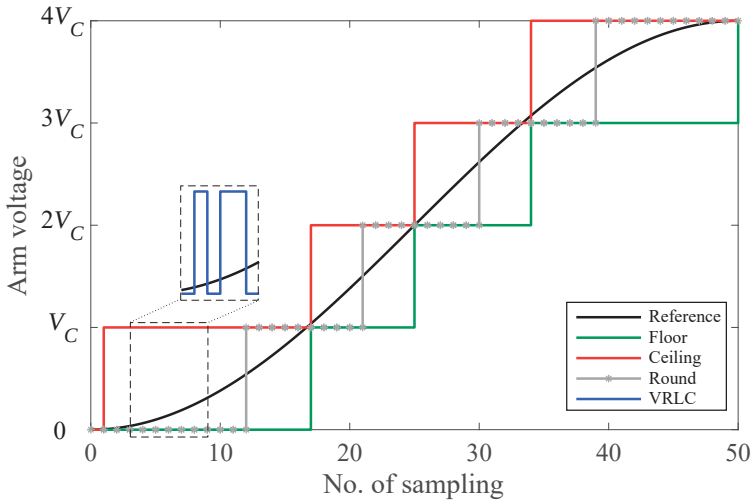


Figure 3.3 An example of the arm voltages resulted from different rounding methods.

Typical insertion-index waveforms of both the conventional method and the proposed VRLC scheme are illustrated in Fig. 3.4 (the system configuration and test results are detailed in section V) to exhibit the active voltage-level updating of the VRLC method. N_{au} and N_{al} are the insertion indexes of the upper and lower arms of phase-a, respectively. $N_a = (N_{al} - N_{au})/2$ and $N_{circ,a} = (N - N_{au} - N_{al})/2$ reflect the number of SMs employed for the regulation of phase current and circulating current, corresponding to u_a and $u_{circ,a}$, respectively. As can be observed, the proposed VRLC technique presents more voltage-level jumping than the conventional scheme in the arm voltages and current-regulating voltages.

3.3 Rounding Method Decision by Applying an MPC Strategy

A proper choice to undertake the evaluation and selection of the proper rounding function, as the basis of the proposed VRLC method, is to employ an MPC technique for each phase of the MMC. A schematic diagram of the VRLC-MPC strategy aiming at a proper selection of the rounding method for each arm in phase-x is provided in Fig. 3.5.

The effectiveness of the MPC has been verified in the literatures for a wide range of applications in power electronics [22, 33, 62–64, 68, 80, 85, 88]. To apply the MPC to an

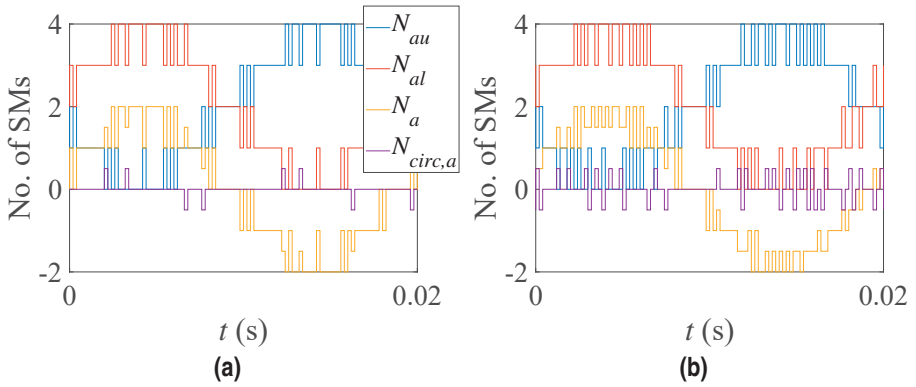


Figure 3.4 Insertion indexes of arm voltages and current regulations when using (a) conventional scheme (Fig. 3.1). (b) proposed scheme (Fig. 3.2).

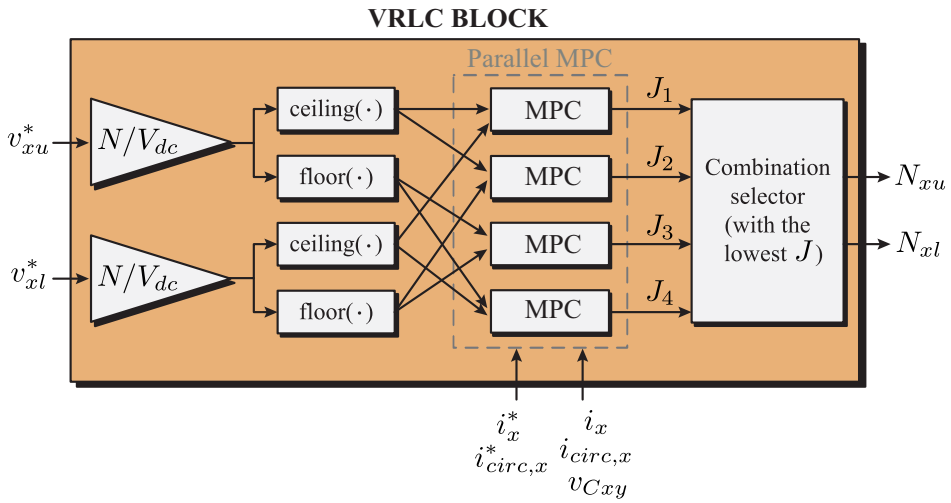


Figure 3.5 Control diagram of the VRLC method with the determination of N_{xy} by four MPC blocks working in parallel for each phase x.

MMC, the predictions of phase current and circulating current values can be carried out based on the mathematical model of the system, which is provided in section 2.2.

Once the electrical variables of the MMC are predicted applying one specific rounding-method combination, a cost function is applied as the selection criterion to finally determine the value of N_{xy}. As the target in this chapter is to control the phase current and circulating current, the cost function (2.20) is adopted with $h = 1$, considering the phase current and circulating current tracking errors of phase x as the control objectives. It is necessary to tune the weighting factors of both faced control targets. For simplicity, setting $p_1 = 1$, then only p_2 needs to be tuned. i^*_x and $i^*_{circ,x}$ are the corresponding references assigned

according to the outer loop controllers which are not the focus of the thesis. On the other hand, $\hat{i}_x$ and $\hat{i}_{circ,x}$ are the predicted current values using the discrete mathematical model derived in (2.16) and (2.17).

Since the SM capacitor voltages are balanced with the sorting scheme and the total energy can be regulated through the adjustment of I^*_{dc}, the cost function defined in (2.20) does not have to incorporate those terms of individual capacitor voltage ripples [62, 63]. In addition, since the nominal total DC-link voltage V_{dc} is used for normalization purposes in VRLC expressions (3.7), other extra terms for the arm energy regulation do not need to be included in the cost function [63, 91].

The delay of one sampling period exists unavoidably in any digital control system. It needs to be compensated otherwise may degrade the performance of the control system. As a merit of the MPC scheme, this delay can be easily compensated by applying an extra step of prediction [93]. The scheme of the proposed two-step horizon MPC method is represented in Fig. 3.6. For each sampling period from k to $k+1$, $\hat{i}_x(k+1)$ and $\hat{i}_{circ,x}(k+1)$ are predicted first based on the measurements of time instant k. Then, the prediction model is employed again to determine the control action to be applied at $k+1$ in order to optimize $\hat{i}_x(k+2)$ and $\hat{i}_{circ,x}(k+2)$. It is worth noting that in the second-step prediction, the SM capacitor voltage measurements of time instant k are adopted without being predicted since their dynamic is relatively slow. This delay compensation measure has been adopted by all the MPC methods in all the tests, of either experiments or simulations, throughout the thesis.

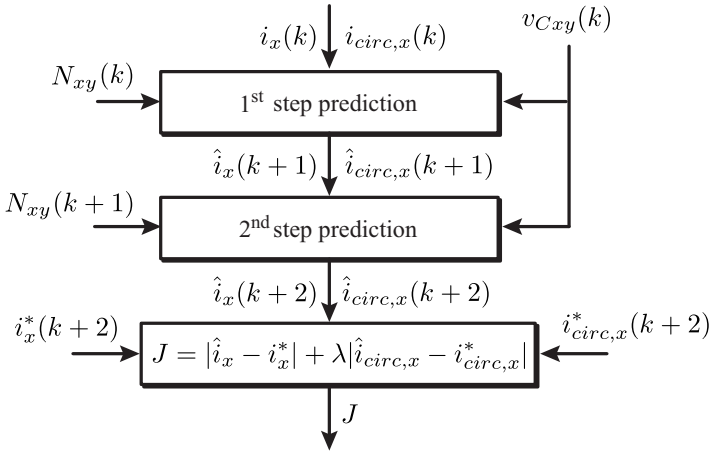


Figure 3.6 Flowchart of two-step horizon prediction MPC method.

After evaluating the cost function values corresponding to the four combinations of rounding functions in phase x, the combination that achieves the minimum value is selected to determine the N_{xy} values and then sent to the sorting algorithm to finally determine the switching signals S_{xyz}.

Remark 1: Compared with the conventional control scheme shown in Fig. 3.1, the proposed VRLC method is able to lead to a better decision of the arm voltage level (or

insertion index) considering both phase current tracking and circulating current regulating. Utilizing the information of system model, the current quality can be enhanced as a benefit of applying the MPC scheme. In addition, a flexible trade-off between both current-regulating tasks can be achieved with ease by simply commanding the weighting factor.

Remark 2: In the proposed VRLC technique, the total number of switched-on SMs in each phase (i.e. $N_{xu}+N_{xl}$) is $N-1$, N or $N+1$. In other words, every sampling time only three voltage levels are used to achieve the circulating current regulation. Thus, the proposed method is better suited for medium-voltage applications where the number of SMs of MMC is not too large, as the methods proposed in [68, 88, 94]. For high-power applications such as the HVDC transmission where hundreds of SMs per arm are involved, more voltage levels close to Nv^*_{xy}/V_{dc} can be considered, which is out of the scope of this chapter and is thus not detailed here.

Remark 3: It is important to notice that, different from the conventional MPC-based MMC control techniques which evaluate a large number of states per sampling period [62, 63, 85], the number of cost-function evaluations of the proposed VRLC approach is always four per phase, regardless of the number of SMs. Thus, the calculation burden is not heavy.

3.4 Experimental Analysis

To validate the effectiveness of the proposed strategy, several experimental tests are carried out on a three-phase MMC laboratory prototype with four SMs per arm controlled by a dSPACE 1007 platform. Details on experimental setup and control algorithm implementation are provided in Appendix A. The AC-side of the MMC is connected to a three-phase $R-L$ load and the most important parameters of the MMC system are summarized in Table 3.1.

Table 3.1 Parameters of the MMC laboratory setup.

DC-link voltage, V_{dc}	180 V
Number of SMs per arm, N	4
SM capacitance, C	1 mF
Arm inductance, L_{arm}	15 mH
Arm resistance, R_{arm}	0.5 Ω
Load inductance, L	15 mH
Load resistance, R	20.5 Ω
AC frequency, f	50 Hz
Sampling/control frequency, f_s	5.0 kHz

3.4.1 Steady-state performance

The steady-state performance of the VRLC control scheme shown in Fig. 3.2 has been evaluated. For comparison purposes, the conventional control scheme shown in Fig. 3.1 is also evaluated, implementing the circulating current PR controller described in [52]. In order to make a fair comparison, the first-step prediction for delay compensation is applied to the conventional control scheme as well. i_x^* is directly assigned a balanced sine with an amplitude of 3.7 A, which corresponds to an active power of 0.42 kW and a reactive power of 0.10 kVA. In order to display the circulating-current-regulating performance of the proposed method, the $i_{circ,x}^*$ is assigned a pure DC value of 0.86 A, which is selected for a smooth operation with the SM energy close to its nominal level.

The obtained results are shown in Fig. 3.7, Fig. 3.8, and Table 3.2. Figure 3.7a and Fig. 3.8a show the phase current, circulating current and arm currents of phase-a. Figure 3.7b and Fig. 3.8b show the arm voltages and phase voltage (v_a) of phase-a. Figure 3.7c and Fig. 3.8c show the capacitor voltage and the output voltage of an arbitrary SM ($au2$).

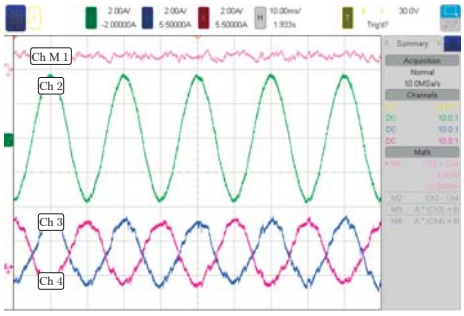
Table 3.2 Steady-state performance comparison of both methods including experimental and simulation results.

	Method	THD_{50} (%)	RMS (A)	f_{sw} (kHz)	f_s (kHz)
Exp.	Conv.	2.37	0.1631	1.01	5.0
	VRLC	1.90	0.1547	1.13	5.0
Sim.	Conv.	2.13	0.1566	1.09	5.0
	VRLC	1.67	0.1485	1.20	5.0
	Conv.	1.89	0.1537	1.22	5.7

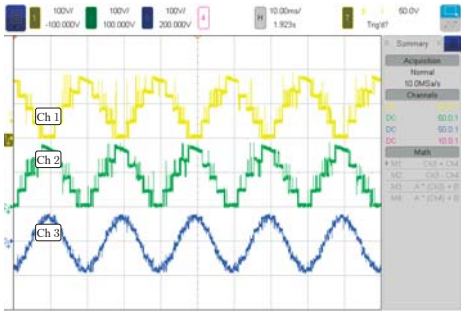
As summarized in Table 3.2, the phase current THD up to 50th harmonic order (THD_{50}) of the proposed VRLC method is lower than that obtained using the conventional method. Considering the low range of THD_{50}, the improvement is significant. In terms of the circulating current, both methods show similar RMS values of AC component of $i_{circ,a}$ (denoted by RMS in Table 3.2). Also, both control schemes achieve very similar results in terms of the capacitor voltage ripple and individual device switching.

Compared with the conventional NLC-based method, the proposed VRLC scheme shows more voltage level jumping, which reflects its active regulation of arm voltage in order to achieve a better current tracking (coinciding with Fig. 3.4). In this test, imposing a sampling frequency f_s equal to 5 kHz, the average switching frequencies of the SMs (f_{sw}) are 1.01 kHz and 1.13 kHz applying the conventional and the VRLC methods respectively.

For further examination of the above mentioned characteristics of the VRLC method, i.e. the significantly improved phase current quality and the slightly higher switching frequency (compared with the conventional scheme), the same steady-state tests are carried out also in simulation using the Matlab/Simulink environment. The corresponding simulation results are also summarized in Table 3.2, which are very similar with those obtained in the experiments.



(a)



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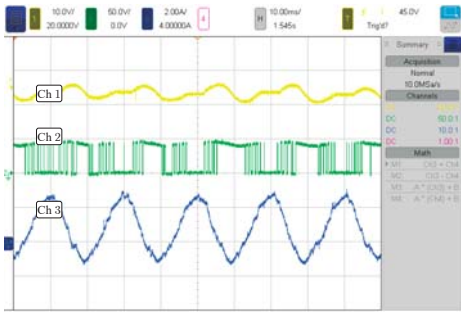
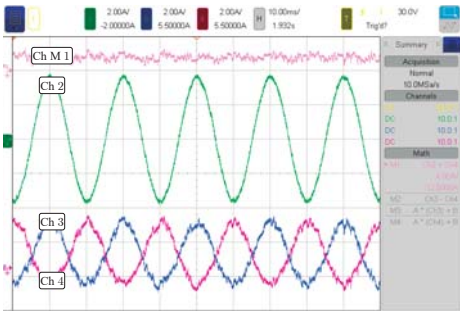
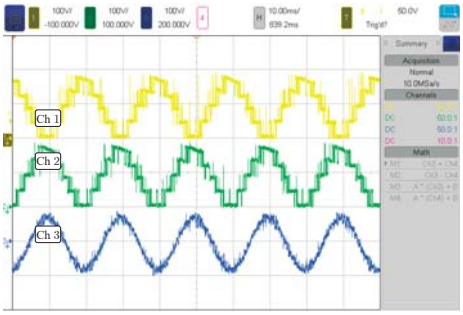


(c)

Figure 3.7 Steady-state performance of the conventional scheme. (a) CH2-4, M1: i_a, i_{au}, i_{al}, $i_{circ,a}$. (b) CH1-3: v_{au}, v_{al}, v_a. (c) CH1-3: v_{Cau2}, output voltage of SM $au2$, i_{au}.



(a)



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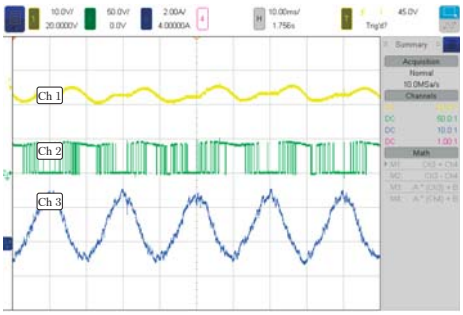


(c)

Figure 3.8 Steady-state performance of the proposed control scheme. (a) CH2-4, M1: i_a, i_{au}, i_{al}, $i_{circ,a}$. (b) CH1-3: v_{au}, v_{al}, v_a. (c) CH1-3: v_{Cau2}, output voltage SM $au2$, i_{au}.

In order to make a comparison of both methods with very similar average switching frequency, Table 3.2 also addresses the steady-state performance of the conventional method with increased sampling frequency. In this way, a sampling frequency of 5.7 kHz is imposed and the conventional method obtains very similar average switching frequency. Even forced to have the same average switching frequency, the VRLC technique outperforms the conventional scheme.

In terms of computational cost of control implementation on the dSPACE DS1007 PPC processor board, the MPC execution time is 2.6 μs and the PR controller execution time is 0.7 μs. But compared to the total calculation time of the whole control schemes (proposed: 78.0 μs, conventional: 76.2 μs), this difference is not critical.

3.4.2 Dynamic response

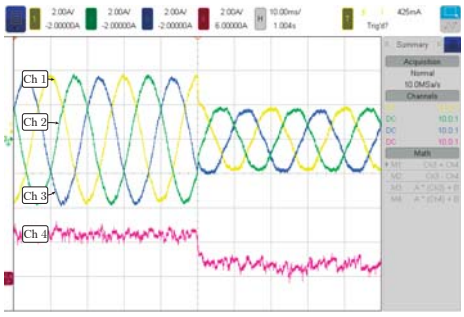
The dynamic performance of both schemes has been evaluated, where the amplitude of i_x^* is reduced to half (1.85 A) and $i_{circ,x}^*$ is reduced to one fourth (0.215 A) correspondingly. The obtained results are illustrated in Fig. 3.9 and Fig. 3.10 showing that both methods present a good dynamic response. It should be noted that the dynamic response of phase current mainly depends on the outer loop PI controllers in the dq frame. Thus, both methods exhibit similar performance. Nevertheless, the proposed control scheme shows better dynamic response of phase current as can be observed in Fig. 3.9b and Fig. 3.10b. In addition, the modulation index decreases from 0.86 to 0.43 during the transient. It can be clearly observed that with low modulation index, the phase current of the proposed method presents higher quality than the conventional control scheme as shown in Fig. 3.9a and Fig. 3.10a.

i_{dc} is shown in this test representing the same trend as the circulating current. It can be observed that the VRLC method exhibits very fast dynamic of i_{dc}, while the conventional technique shows slightly faster dynamic since the PR controller is used. Considering that the phase current tracking is the main control objective, it can be concluded in this test that the VRLC method presents preferable overall performance.

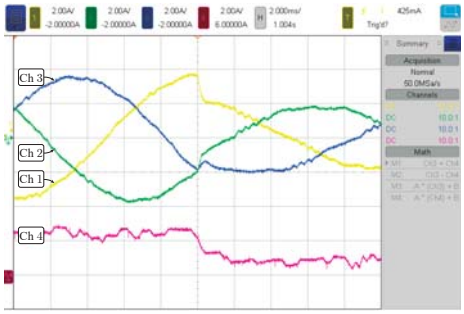
3.4.3 Harmonic injection of circulating current

The proposed control scheme can also track a circulating current reference with AC component. In this experiment, a second harmonic is selected as AC reference for the circulating current, which is designed to eliminate the second-order harmonic of the SM capacitor energy fluctuation [95]. Figure 3.11 shows the results, where the circulating current reference is a pure DC component for the first 100 ms and the second harmonic is added for the rest 100 ms. It can be observed that the second-order harmonic is well injected into the circulating current without deteriorating the output current. A detail of the effect of this second-order harmonic injection in the circulating current on the capacitor voltage regulation is shown in Fig. 3.12 where it can be clearly observed that the regulation is improved after applying the harmonic injection.

It is worth noting that during the harmonic injection of circulating current, the fluctuation of arm energy will change correspondingly, which may call for further regulation. In the proposed control scheme using the MPC, there are two steps of predictions, the first for delay compensation and the second for finite-control-set evaluation. For the average

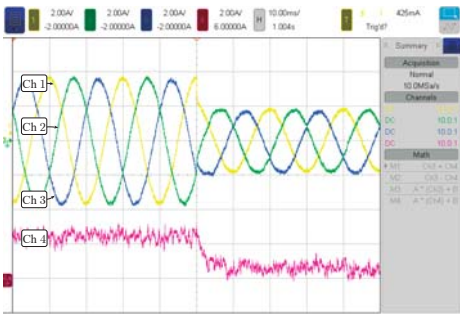


(a)

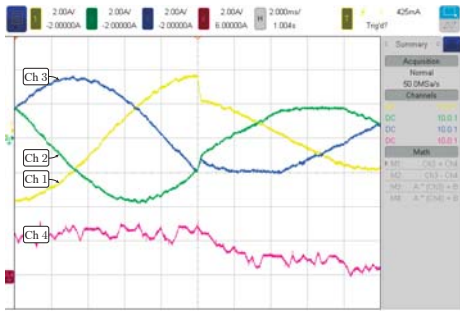


(b)

Figure 3.9 Dynamic performance of the conventional control scheme. (a) CH1-4: i_a, i_b, i_c, i_{dc}. (b) zoom-in of (a).



(a)



(b)

Figure 3.10 Dynamic performance of the proposed control scheme. (a) CH1-4: i_a, i_b, i_c, i_{dc}. (b) zoom-in of (a).

capacitor voltage (v_{Cxy}) in expression (2.8), the measurements ('m') v_{Cxyz} or the reference value ('r') V_{dc}/N can be used. This leads to four different options in the two-step prediction model: 'rm', 'mm', 'mr' and 'rr'.

Employing the reference ('r') value in either step of the prediction helps to regulate the arm energy (i.e., regulate the capacitor voltage close to the nominal value). Fig. 3.12 shows this effect. The whole experiment of 25 seconds is evenly divided into five parts of 5 seconds. Part 1 and 2 illustrate the same test shown in Fig. 3.11 but with a larger time span. Parts 2-5 correspond to the harmonic injection test with the implementation scheme of 'rm', 'mm', 'mr' and 'rr' respectively. It can be observed that the capacitor voltage ripples decrease after the harmonic injection of circulating current (parts 2-5) but during 'mm' part, the capacitor voltage is further from the nominal value (45 V) than other implementation methods. This shows the negative effect of the capacitor voltage ripples in the MPC control and the merit of using the nominal reference value in at least one of the prediction steps.

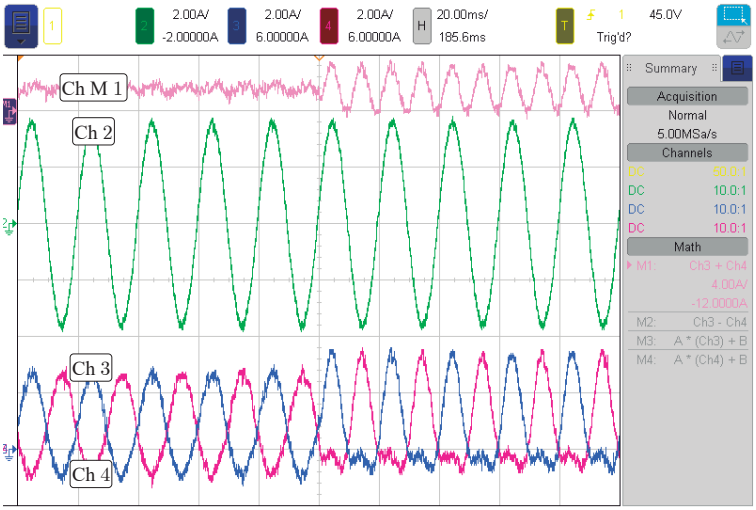


Figure 3.11 Injection of a circulating current with second harmonic. CH2-4, M1: i_a, i_{au}, i_{al}, $i_{circ,a}$.

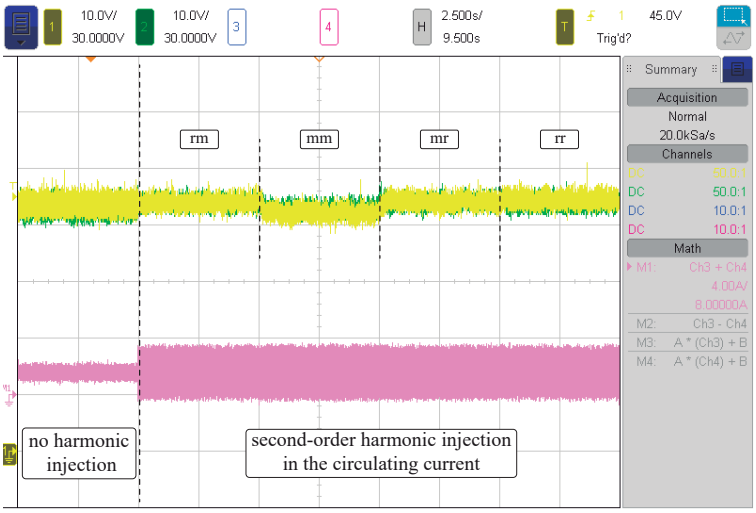


Figure 3.12 Capacitor voltage regulation during the injection of circulating current. CH1, 2, M1: v_{Cau1}, v_{Cal1}, $i_{circ,a}$.

3.4.4 Trade-off between different control objectives

The performance of an MPC method largely depends on the definition of the cost function and the selection of its weighting factors. In the case of the proposed MPC scheme, the weighting factor p_2 needs to be properly tuned. The tuning procedure can be done testing a range of values of p_2 considering the phase current THD_{50} and the RMS value of the

circulating current ripple. During the tests, the same experimental conditions as Fig. 3.7c are adopted.

The results are summarized in Fig. 3.13 and a clear trade-off between both control objectives is observed. The prediction model implementation mentioned before, namely 'rm', 'mm', 'mr' and 'rr', are considered. The 'rm' scheme is adopted for its superior current control performance with the lowest THD_{50} in Fig. 3.13a. Finally, p_2 is fixed to 0.5 in order to achieve good performance considering both control targets for all the experiments addressed in this section.

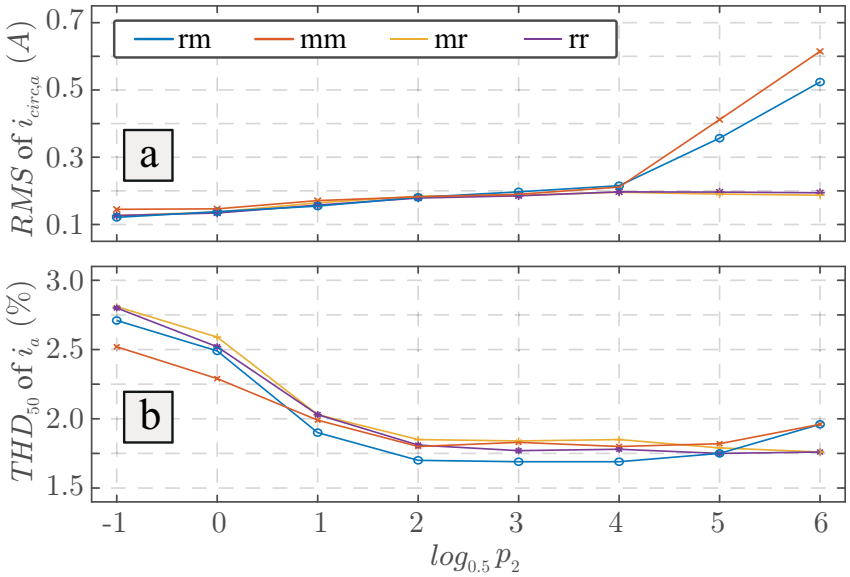


Figure 3.13 Steady-state performance of the VRLC-MPC method with different weighting factor values.

3.4.5 Discussions

Various experimental tests in this section have revealed the advantages of the proposed VRLC technique compared with the conventional NLC method: higher phase current quality with comparative or even lower circulating current ripple, higher dynamic of phase current tracking in transient condition, and more flexible trade-off between different current regulations. Fundamentally, these merits stem from the proper determination of control set defined by the VRLC proposal and the effective coordination between different control objectives enabled by the MPC scheme. Since the tracking errors of electrical variables can be predicted employing the discrete system model, and the importance of each individual control objective can be quantified by assigning the corresponding weighting factor within the cost function, the control action can be properly determined with ease.

The expenses of the above-mentioned advantages of the VRLC technique are the increased complexity and switching frequency. However, since the size of the finite control set of the MPC is only 4 per sampling time per phase, the increased implementation burden of the VRLC scheme is relatively trivial as verified in subsection V-A. As for the switching frequency, the slightly increased switching frequency (under the same sampling frequency) of the proposed method represents the necessary extra switchings for current-quality improvement, and further test results (summarized in Table 3.2) have shown the potential current improvement with even the same switching frequency with the conventional method.

The PWM scheme has not been considered in this chapter for its high implementation cost and high switching losses in the medium-voltage applications and distinct feature from the NLC/VRLC schemes. The VRLC technique has been proposed in this chapter as a solution for medium-voltage MMC systems whose number of voltage levels is relatively insufficient for the NLC method to achieve a satisfying waveform quality but relatively excessive for the PWM technique to be implemented with an affordable complexity. Considering the scenario of lower voltage range, the comparison between the VRLC and PWM schemes could be an interesting topic. The unique features of the PWM scheme are the equal switching losses of different power devices and concentrated harmonic spectrum of phase voltage/current. In comparison, the VRLC technique possesses the advantages of simple implementation, high dynamics, flexible coordination of different control targets, and easy delay compensation, etc.

4 Generalized VRLC-based MPC Techniques

In the previous chapter, the VRLC technique has been developed as an improved version of the NLC scheme. This chapter generalizes the VRLC concept as a new stream of MPC strategies and analyzes their current regulating capability. The chapter is organized as follows. Section 4.1 gives some general descriptions of the current control principles adopted in this chapter. Section 4.2 addresses the generalization of the VRLC strategy. Section 4.3 explains the potential negative influence of SM capacitor voltage ripples on the current controllability of the VRLC technique, which is supported by several derived analytical ripple expressions. Section 4.4 provides an analysis of the current regulating ability of the VRLC method, followed by several simulation tests in section 4.5 for validation.

4.1 Current Control of MMC

In this chapter, focus is given to the steady-state current control performance of the MMC as summarized below:

1. The studied MMC operates as a DC-AC interface, with the DC-link voltage V_{dc} assumed as constant and the AC side connected to the grid through an $R-L$ filter or with $R-L$ load connection to simplify the analysis.

2. The phase current of the AC side (i_x) is controlled to track its reference (i_x^*), and only the three-phase balanced sinusoidal waveforms are considered which correspond to specific commands of active power and reactive power.

3. The circulating current ($i_{circ,x}$) is controlled to track its reference ($i_{circ,x}^*$) which is set as a direct component given according to the power balance of both sides (DC side and AC side) of the MMC.

Considering the definition of u_x and $u_{circ,x}$ in (3.2) and (3.3), respectively, taking into account the approximation in (2.8), (2.5) and (2.6) can be rewritten as

$$\begin{aligned} u_x &= v_{Sx} + L_{eq}\frac{di_x}{dt} + R_{eq}i_x \\ &= \frac{-N_{xu}v_{Cxu} + N_{xl}v_{Cxl}}{2} \end{aligned} \tag{4.1}$$

$$\begin{aligned} u_{circ,x} &= L_{arm}\frac{di_{circ,x}}{dt} + R_{arm}i_{circ,x} \\ &= \frac{V_{DC}}{2} - \frac{N_{xu}v_{Cxu} + N_{xl}v_{Cxl}}{2}. \end{aligned} \tag{4.2}$$

As shown in Fig. 2.4b and 2.4c, the phase current model and circulating current model are independent of each other, thus a decoupled analysis of both current control problems can be achieved. It can be observed that both current models share similar structure. Basically, the control objectives are: generating N_{xu} and N_{xl} which make possible that

1. u_x approximates u_x^*, in order that i_x tracks i_x^*.
2. $u_{circ,x}$ approximates $u_{circ,x}^*$, in order that $i_{circ,x}$ tracks $i_{circ,x}^*$.

In the conventional solutions, these objectives are achieved by dedicated controllers (normally PI or PR controllers) in a decoupled way as shown in Fig. 2.2. Once u_x^* and $u_{circ,x}^*$ are obtained, v_{xy}^* can be determined by rewriting (3.4) and (3.5) as

$$v_{xu}^* = \frac{1}{2}V_{dc} - u_x^* - u_{circ,x}^* \tag{4.3}$$

$$v_{xl}^* = \frac{1}{2}V_{dc} + u_x^* - u_{circ,x}^*. \tag{4.4}$$

Then, for determining the insertion index of each arm, the arm voltage reference is simply normalized as

$$N_{xy}^* = \frac{v_{xy}^*}{V_C} = \frac{v_{xy}^* N}{V_{dc}}. \tag{4.5}$$

where $V_C = \frac{V_{dc}}{N}$ is the capacitor voltage reference defined for convenience. N_{xy}^* is a decimal which can be directly employed as input of carrier-based methods, or rounded to an integer if the pseudomodulation techniques are used.

When it comes to the FCS-MPC techniques, as shown in Fig. 2.3, the above objectives are achieved by evaluating different combinations of SM switching states (S_{xyz}) or arm voltage levels (N_{xy}), normally in a coupled manner owing to the use of cost function. In this chapter (and this thesis), the MPC is employed to determine only the insertion index of each arm (N_{xy}) that satisfies the above-mentioned current control requirements, and the SM capacitor voltages of the same arm are balanced by the sorting-and-selecting scheme originally proposed in [18].

4.2 Generalization of VRLC

4.2.1 General principles

As previously commented in section 2.2, commonly-used voltage-level-based MPC methods [33] compare all the $(N+1)^2$ or at least a large number of (proportional to N even if the control sets are refined) combinations of voltage levels of both arms of each converter phase, namely N_{xu} and N_{xl}, in order to achieve accurate tracking of i_x^* and $i_{circ,x}^*$. However, the corresponding calculation burden is heavy and turns unaffordable as the number of SMs of the MMC becomes very large. By contrast, the proposed VRLC-based MPC method introduced in the previous chapter only needs to evaluate 4 voltage level combinations per phase. This represents great advantage in terms of computational burden, as a result of the refined control sets (voltage level combinations). Since this refining effect is achieved by extra current controllers (PI phase current controllers in the dq frame), performance can be guaranteed.

Following this idea, the VRLC can be generalized as a stream of MPC methods whose control sets are refined by additional current controllers. This concept can be explained in the two-dimensional $N_{xu}-N_{xl}$ coordinate as illustrated in Fig. 4.1. At first, the arm voltage references v_{xy}^* determined by extra current control loops are normalized by (4.5), leading to a reference point (or vector) represented by $\mathrm{G}_*(N_{xu}^*,N_{xl}^*)$. Next, the 4 nearest candidates, G_1, G_2, G_3 and G_4, can be obtained from the VRLC scheme as refined candidates, which are then sent to the MPC module for cost function evaluation. Finally, the candidate that achieves the lowest cost function value is selected for further implementation as input of the capacitor voltage sorting modules, which then generate all the gate signals.

An important step of the above technique is the determination of v_{xy}^*, which can be determined by u_x^* and $u_{circ,x}^*$ as (4.3) and (4.4). In terms of the determination of u_x^*, the following current controllers can be considered

1. PI/PR: utilizing dedicated current controllers, e.g. PI controllers in the dq frame, or PR controllers in the abc or $\alpha\beta$ frame.
2. DB (deadbeat): employing deadbeat principle upon the discrete model of (4.1) aiming at making zero the tracking error at the next sampling instant (since the current models under investigation are first-order systems).
3. OL (open-loop): calculating u_x^* in an open-loop manner, i.e., substituting the analytical expression of i_x^*, e.g. $I\sin(\omega t-\gamma)$, into (4.1) without feedback of the instantaneous phase current measurements.

PI/PR and DB controllers are more accurate than OL controller. Compared with PI/PR controller, DB controller requires lighter calculation and is simpler in design since no control parameters are required. OL controller is the simplest but is rough in terms of current tracking. Characteristics of different current controllers are compared in Table 4.1.

In terms of the determination of $u_{circ,x}^*$, the above control options can be applied as well. Considering that the circulating current regulation is an auxiliary control objective and PI/PR controller presents relatively high complexity in both computation and controller

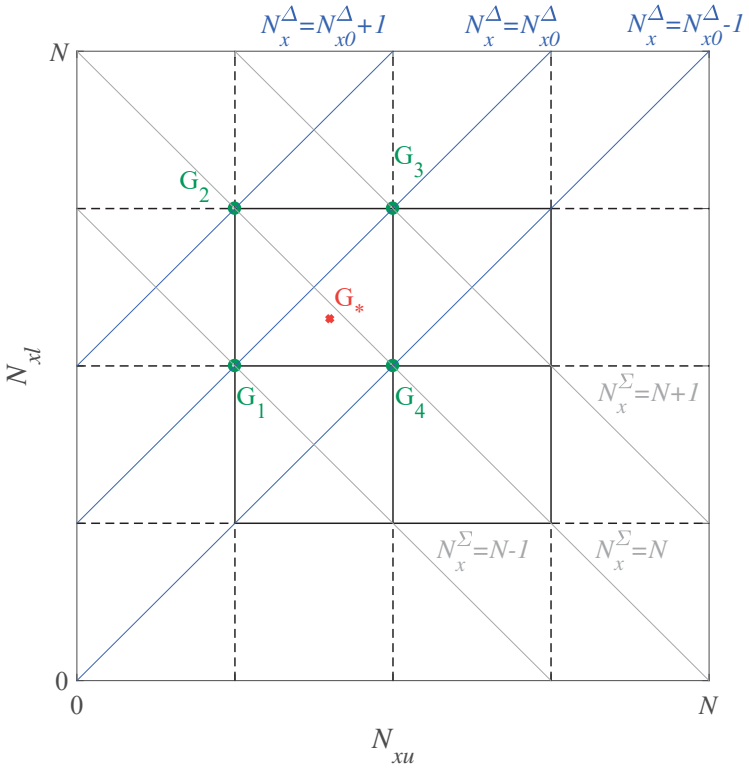


Figure 4.1 Principles of the VRLC technique.

Table 4.1 Characteristic comparison of different current controllers.

Principle	PI/PR	DB	OL
Control accuracy	High	High	Low
Computational cost	High	Medium	Low
Number of control parameters	2	0	0

design, this control option is not recommended for the generation of $u^*_{circ,x}$. Additionally, v^*_{xy} is just for control set refining and thus does not need to be determined very precisely, while the current quality can be further enhanced by the MPC module. Thus, DB and OL controllers can be employed for determining $u^*_{circ,x}$.

The control diagram of the generalized VRLC-based MPC techniques is illustrated in Fig. 4.2. Combinations of the above current controllers lead to 6 different strategies of the VRLC-MPC technique (neglecting the use of PI/PR controller for circulating current control as explained above). Specific choice among the 6 possibilities can be made considering the trade-off between current tracking performance, calculation burden and

design complexity taking into account the information summarized in Table 4.1. As an example, the strategy studied in chapter 3 adopts the PI controller for phase current control and the OL controller for circulating current control.

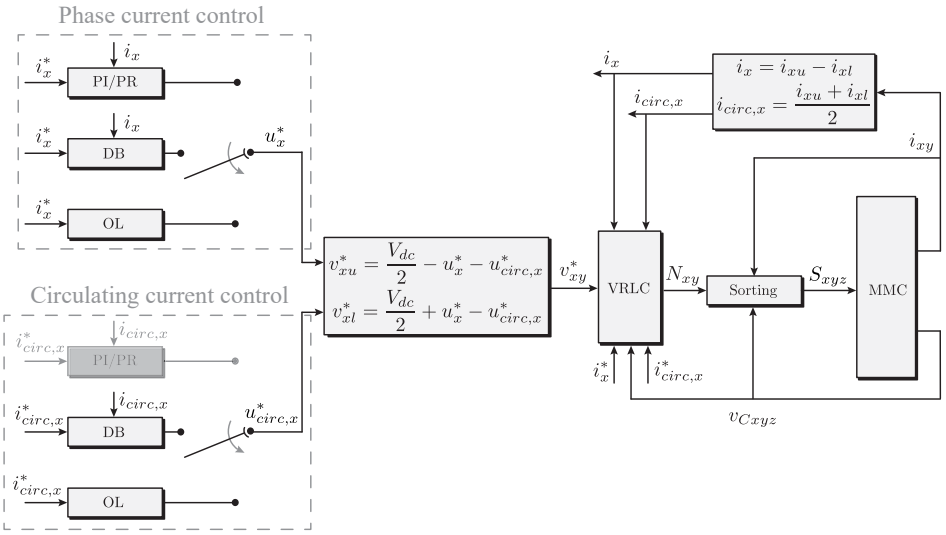


Figure 4.2 Diagram of the generalized VRLC-based MPC technique.

Since this chapter focuses on steady-state operation with $i^*_{circ,x}$ set as a constant value, for simplicity, applying the OL principle to (4.2), $u^*_{circ,x}$ can be set as

$$u^*_{circ,x} = i^*_{circ,x} R_{arm} \approx 0. \tag{4.6}$$

As for the determination of u^*_x, all the three principles will be analyzed for a comparative study.

4.2.2 Potential problems

It can be inferred from the previous subsection that the effectiveness of the proposed VRLC-MPC technique depends on proper determination of point G_* in Fig. 4.1, which can be influenced by two factors: the determination and normalization of v^*_{xy}. The former depends on the selection of current controllers (among PI/PR, DB and OL), and the later depends on whether capacitor voltage measurement or reference is used for normalization.

As in chapter 3, for simplicity, the cost function adopts J_i defined in (2.20) with $h = 1$. Correspondingly, V_C is adopted for voltage normalization in (4.5) as an implicit regulation of arm energy which guarantees asymptotic stability without extra arm energy control loop as proved in [91]. This control configuration is very simple but presents potential error in the determination of N^*_{xy}, which can be significant if the SM capacitor voltages have high ripples and their instantaneous values are far from the reference V_C. As a result, the

reference point G_* in Fig. 4.1 will locate in an improper square, and the refined candidates (G_1, G_2, G_3 and G_4) will lose effectiveness in current control.

To take the SM capacitor voltage ripples into account and achieve an accurate normalization of v^*_{xy}, the following two alternatives can be adopted:

1. Using capacitor voltage measurements for normalizing v^*_{xy}. In this case, additional arm energy control loops (based on PI or PR controllers) need to be included which generate the circulating current reference $i^*_{circ,x}$ for the cost function, or J_{iw} defined in (2.22) has to be selected as the cost function which include additional terms of arm energy regulation [63]. Both solutions increase the complexity in terms of calculation and parameter tuning. Moreover, measurements need to be realized with short time delay for feedback of capacitor voltages, which is difficult and/or costly for an MMC with high number of SMs [91].
2. Employing capacitor-voltage-ripple-estimation approach proposed in [59] which also guarantees stability implicitly. But this method is sensitive to the parameter of SM capacitance and needs a lot of online calculation.

Thus, the normalization scheme using V_C plus cost function J_i seems to be the most cost-effective option. Its only drawback is the potential negative influence from the capacitor voltage ripples which bring error to the control sets refined from the VRLC concept. However, if this error can be tolerated, effective control sets can still be derived even if G_* is not accurate. This issue will be addressed in the following sections.

4.3 Negative Effect of Capacitor Voltage Ripples

4.3.1 Analytical expressions of capacitor voltage ripples

To study the influence of capacitor voltage fluctuations on the performance of the proposed VRLC-MPC technique, the analytical expressions of capacitor voltage ripples are of help, which can be derived as follows.

Firstly, the following assumptions are made

$$u_x = U\sin(\omega t + \phi_x) \tag{4.7}$$

$$i_x = I\sin(\omega t + \phi_x - \gamma) \tag{4.8}$$

where $\phi_{a,b,c} = 0, -2\pi/3, 2\pi/3$ respectively, and the circulating current is regulated as a pure DC component satisfying

$$(V_{dc} - 2u_{circ,x})i_{circ,x} = \frac{UI\cos\gamma}{2}. \tag{4.9}$$

Neglecting the steady-state voltage drop across the arm resistance ($u_{circ,x} = i_{circ,x}R_{arm}$) which is insignificant, $i_{circ,x}$ can be obtained as

$$i_{circ,x} = \frac{UI\cos\gamma}{2V_{dc}}. \tag{4.10}$$

In addition, the modulation index is defined as

$$m = \frac{2U}{V_{dc}}. \tag{4.11}$$

Considering the above assumptions, definitions, and the mathematical model of the MMC provided in section 2.2, the following expressions of arm currents and voltages can be derived as

$$i_{xu} = \frac{mI\cos\gamma}{4} + \frac{I}{2}\sin(\omega t + \phi_x - \gamma) \tag{4.12}$$

$$i_{xl} = \frac{mI\cos\gamma}{4} - \frac{I}{2}\sin(\omega t + \phi_x - \gamma) \tag{4.13}$$

$$v_{xu} = \frac{1}{2}V_{dc} - U\sin(\omega t + \phi_x) \tag{4.14}$$

$$v_{xl} = \frac{1}{2}V_{dc} + U\sin(\omega t + \phi_x). \tag{4.15}$$

Neglecting the differences between the capacitor voltages of all SMs of the same arm, the average switching function of each SM of the corresponding arm can be calculated with a focus on the DC and fundamental-frequency components by normalizing the arm voltage with the DC-link voltage (similar to the assumption made in [51]) as

$$S_{xu} = \frac{v_{xu}}{V_{dc}} \tag{4.16}$$

$$S_{xl} = \frac{v_{xl}}{V_{dc}}. \tag{4.17}$$

Then, the equivalent current passing through the capacitor can be derived as

$$i_{xu}^{SM} = S_{xu}i_{xu} = \frac{I}{8}[m\cos(2\omega t + 2\phi_x - \gamma) + 2\sin(\omega t + \phi_x - \gamma) - m^2\cos\gamma\sin(\omega t + \phi_x)] \tag{4.18}$$

$$i_{xl}^{SM} = S_{xl}i_{xl} = \frac{I}{8}[m\cos(2\omega t + 2\phi_x - \gamma) - 2\sin(\omega t + \phi_x - \gamma) + m^2\cos\gamma\sin(\omega t + \phi_x)]. \tag{4.19}$$

Through integration of (4.18) and (4.19), the average SM capacitor voltage of upper/lower arm of phase x are obtained as

$$v_{Cxu} = \frac{1}{C}\int i_{xu}^{SM} = v_{Cxu}^{0} + \Delta v_{Cx}^{com} + \Delta v_{Cx}^{dif} \tag{4.20}$$

$$v_{Cxl} = \frac{1}{C}\int i_{xl}^{SM} = v_{Cxl}^{0} + \Delta v_{Cx}^{com} - \Delta v_{Cx}^{dif} \tag{4.21}$$

where v_{Cxu}^{0} and v_{Cxl}^{0} are the direct components which can be set as the reference value V_C for the ease of analysis, and the alternate components are decoupled as a common-mode

quantity and a differential-mode quantity defined as follows

$$\Delta v_{Cx}^{com} = \frac{Im}{16\omega C}\sin(2\omega t + 2\phi_x - \gamma) \tag{4.22}$$

$$\begin{aligned}\Delta v_{Cx}^{dif} &= \frac{I}{8\omega C}[-2\cos(\omega t + \phi_x - \gamma) + m^2\cos\gamma\cos(\omega t + \phi_x)] \\ &= -\frac{I}{4\omega C}\sqrt{\left(\frac{m^4}{4} - m^2\right)\cos^2\gamma + 1}\sin(\omega t + \phi_x + \gamma_1)\end{aligned} \tag{4.23}$$

where the initial phase angle γ_1 is defined as

$$\gamma_1 = \begin{cases} \arctan\left(\frac{2-m^2}{2}\cot\gamma\right), \gamma \in [0, \pi] \\ \arctan\left(\frac{2-m^2}{2}\cot\gamma\right) + \pi, \gamma \in [-\pi, 0) \end{cases} \tag{4.24}$$

Considering the fact that $m \in [0,1]$ (over-modulation conditions such as common-mode voltage insertion are not considered in this chapter) and $\cos^2\gamma \in [0,1]$, the corresponding amplitudes satisfy

$$\mathrm{AMP}(v_{Cx}^{com}) = \frac{Im}{16\omega C} \in [0, \frac{I}{16\omega C}] \tag{4.25}$$

$$\mathrm{AMP}(v_{Cx}^{dif}) = \frac{I}{4\omega C}\sqrt{\left(\frac{m^4}{4} - m^2\right)\cos^2\gamma + 1} \in [\frac{I}{8\omega C}, \frac{I}{4\omega C}] \tag{4.26}$$

indicating that the amplitude of the fundamental component of the capacitor voltage ripples is at least twice that of the double-frequency component.

4.3.2 Synthesized effect of capacitor voltage ripples

In order to analyze the effect of capacitor voltage ripples on current control, the controllable voltages driving the phase current and circulating current are rearranged respectively considering (4.20) and (4.21) as follows

$$\begin{aligned} u_x &= \frac{-N_{xu}v_{Cxu} + N_{xl}v_{Cxl}}{2} \\ &= \underbrace{\frac{N_x^{\Delta}V_C}{2}}_{\widetilde{u}_x} + \underbrace{\frac{N_x^{\Delta}\Delta v_{Cx}^{com} - N_x^{\Sigma}\Delta v_{Cx}^{dif}}{2}}_{\widetilde{u}_x} \end{aligned} \tag{4.27}$$

$$u_{circ,x} = \frac{V_{dc} - (N_{xu}v_{Cxu} + N_{xl}v_{Cxl})}{2} = \underbrace{\frac{V_{dc} - N_x^{\Sigma}V_C}{2}}_{\overline{u}_{circ,x}} \underbrace{\frac{-N_x^{\Sigma}\Delta v_{Cx}^{com} + N_x^{\Delta}\Delta v_{Cx}^{dif}}{2}}_{\widetilde{u}_{circ,x}} \tag{4.28}$$

where the sum and difference of upper/lower-arm insertion indexes are defined as

$$N_x^{\Sigma} = N_{xu} + N_{xl} \tag{4.29}$$

$$N_x^{\Delta} = -N_{xu} + N_{xl}. \tag{4.30}$$

$\overline{u}_x$ and $\overline{u}_{circ,x}$ are hypothetical terms that correspond to an MMC free of capacitor voltage ripples, while $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$ are terms induced by capacitor voltage ripples. Considering an ideal operation of the MMC in steady state, i.e., $\widetilde{u}_x = \widetilde{u}_{circ,x} = 0$, the proposed VRLC-MPC scheme with V_C-based arm voltage normalization should lead to the desired N^{Σ} and N^{Δ} as can be inferred from the definitions of $\overline{u}_x$ and $\overline{u}_{circ,x}$, respectively. However, considering the existence of $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$, error terms (denoted as $\widetilde{N}_x^{\Sigma}$ and $\widetilde{N}_x^{\Delta}$ respectively) will occur as

$$\widetilde{N}_x^{\Delta} = \frac{2\widetilde{u}_x}{V_C} \tag{4.31}$$

$$\widetilde{N}_x^{\Sigma} = \frac{-2\widetilde{u}_{circ,x}}{V_C}. \tag{4.32}$$

To investigate these errors, the analytical expressions of $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$ are required. Considering the ideal expressions of hypothetical terms as $\overline{u}_x = U\sin(\omega t + \phi_x)$ and $\overline{u}_{circ,x} = 0$, then, N_x^{Δ} and N_x^{Σ} can be obtained as

$$N_x^{\Delta} = \frac{2\overline{u}_x}{V_C} = mN\sin(\omega t + \phi_x) \tag{4.33}$$

$$N_x^{\Sigma} = \frac{V_{dc} - 2\overline{u}_{circ,x}}{V_C} = 0. \tag{4.34}$$

Substituting (4.33), (4.34) and the expressions of capacitor voltage ripples derived in (4.22) and (4.23) into (4.27) and (4.28), the analytical expressions of $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$ can be respectively obtained as

$$\begin{aligned}\widetilde{u}_x &= -\frac{NIm^2\cos\gamma}{16\omega C}\cos(\omega t + \phi_x) + \frac{NI(m^2+8)}{64\omega C}\cos(\omega t + \phi_x - \gamma) - \frac{NIm^2}{64\omega C}\cos(3\omega t + 3\phi_x - \gamma) \\ &= \frac{NI}{\omega C}\left[\underbrace{\frac{\sqrt{(m^2+8)^2 + (8m^4 - 64m^2)\cos^2\gamma}}{64}\cos(\omega t + \phi_x - \gamma_2)}_{u_{1x}} \underbrace{-\frac{m^2}{64}\cos(3\omega t + 3\phi_x - \gamma)}_{u_{3x}}\right]\end{aligned} \tag{4.35}$$

$$\begin{aligned}\widetilde{u}_{circ,x} &= -\frac{NIm\sin\gamma}{16\omega C} + \frac{NIm^3\cos\gamma}{32\omega C}\sin(2\omega t+2\phi_x) - \frac{3NIm}{32\omega C}\sin(2\omega t+2\phi_x-\gamma) \\ &= -\frac{NI}{\omega C}\left[\underbrace{\frac{m\sin\gamma}{16}}_{u_{0x}} + \underbrace{\frac{m\sqrt{9+(m^4-6m^2)\cos^2\gamma}}{32}\sin(2\omega t+2\phi_x-\gamma_3)}_{u_{2x}}\right]\end{aligned} \tag{4.36}$$

where

$$\gamma_2 = \begin{cases} \arctan\left(\frac{8+m^2}{8-3m^2}\tan\gamma\right), (8-3m^2)\cos\gamma \geq 0 \\ \arctan\left(\frac{8+m^2}{8-3m^2}\tan\gamma\right)+\pi, (8-3m^2)\cos\gamma < 0 \end{cases} \tag{4.37}$$

$$\gamma_3 = \begin{cases} \arctan\left(\frac{3}{3-m^2}\tan\gamma\right), (3-m^2)\cos\gamma \geq 0 \\ \arctan\left(\frac{3}{3-m^2}\tan\gamma\right)+\pi, (3-m^2)\cos\gamma < 0 \end{cases} \tag{4.38}$$

It is shown that, theoretically, $\widetilde{u}_x$ consists of a fundamental-frequency component and a triple-frequency component, while $\widetilde{u}_{circ,x}$ consists of a direct component and a double-frequency component. The complication of controlling an MMC lies partly in these undesired effects induced by the capacitor voltage ripples, which can have a bad impact on the control performance if not considered and compensated well when their amplitudes are large. Especially, if the arm voltage references are normalized by V_C, as the VRLC techniques studied in this chapter, these undesired effects of $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$, i.e., $\widetilde{N}_x^{\Sigma}$ and $\widetilde{N}_x^{\Delta}$ respectively, will be directly imposed on the normalization result N_{xy}^*. Therefore, special considerations have to be taken.

4.4 Analysis of Current Regulating Capability

4.4.1 Case study of VRLC

It can be inferred from (4.1), (4.2), (4.27) and (4.28) that N_x^{Δ} and N_X^{Σ} are directly related to the regulation of phase current and circulating current, respectively. As shown in Fig. 4.1, the selection among the 4 nearest candidates leads to three voltage levels for each current regulation: $N_x^{\Delta} \in \{N_{x0}^{\Delta}-1, N_{x0}^{\Delta}, N_{x0}^{\Delta}+1\}$ for phase current regulation, and $N_x^{\Sigma} \in \{N-1, N, N+1\}$ for circulating current regulation, where

$$\begin{aligned} N_{x0}^{\Delta} &= -\text{floor}(N_{xu}^*) + \text{floor}(N_{xl}^*) \\ &= -\text{ceiling}(N_{xu}^*) + \text{ceiling}(N_{xl}^*). \end{aligned} \tag{4.39}$$

During an ideal operation of the MMC, all the control decisions (N_{xu}, N_{xl}) determined by the intersection of $N_x^{\Delta} = N_{x0}^{\Delta}$ and $N_x^{\Sigma} = N$ (as an average control action though unrealizable) should always guarantee satisfying current regulation provided that the sampling and control frequency is high enough. However, considering the ripple terms $\widetilde{u}_x$ and $\widetilde{u}_{circ,x}$ resulted from the unavoidable SM capacitor voltage fluctuation, the normalization errors

$\widetilde{N}_x^{\Sigma}$ and $\widetilde{N}_x^{\Delta}$ need to be compensated by the selection of N_x^{Δ} and N_x^{Σ}, respectively, among three candidates each.

Phase current controllability

In terms of phase current tracking, if the PI/PR controller is adopted, the ripple term $\widetilde{u}_x$ which normally contains a fundamental-frequency component and a third-order harmonic as exhibited in (4.35) can be intrinsically considered by the controllers and thus compensated. But if the DB or OL controller is adopted, $\widetilde{u}_x$ cannot be compensated well due to the limited options of N_x^{Δ}. The DB controller suffers from this limitation to a less extent owing to the accurate generation of v_{xy}^*. In order that the VRLC-MPC method with the DB or OL controller can achieve well regulation of phase current considering the disturbance of $\widetilde{u}_x$, the adjustment of $\overline{u}_x$ of $\pm\frac{V_C}{2}$ (resulted from commanding N_x^{Δ} to $N_{x0}^{\Delta}\pm 1$) should be large enough to compensate the effect of $\widetilde{u}_x$. Taking in account (4.27), (4.29) and (4.30), the following equations should be satisfied to a large extent

$$\frac{V_C+\Delta v_{Cx}^{com}}{2}+\widetilde{u}_x^*>0 \tag{4.40}$$

$$\frac{-V_C-\Delta v_{Cx}^{com}}{2}+\widetilde{u}_x^*<0. \tag{4.41}$$

Actually, (4.40) and (4.41) are equivalent. To better express the above requirement, a positive real parameter τ is introduced to (4.40) as

$$\frac{V_C+\Delta v_{Cx}^{com}}{2}+\tau\widetilde{u}_x^*\geq 0. \tag{4.42}$$

Defining τ_{phs} as the maximum τ that makes (4.42) tenable, it can be inferred that τ_{phs} should be as large as possible in order to maintain the phase current controllability. In addition, it is worth noting that only one phase needs to be considered since the same value of τ_{phs} will be achieved in the other two phases. Considering (4.35), the following expression can be derived from (4.42) as

$$\frac{V_{dc}}{N}+\frac{I}{\omega C}[\Delta u_2^{com}+2\tau N(u_{1x}+u_{3x})]\geq 0 \tag{4.43}$$

where

$$\Delta u_2^{com}=\Delta v_{Cx}^{com}\frac{\omega C}{I}=\frac{m}{16}\sin(2\omega t-\gamma) \tag{4.44}$$

considering the information provided in (4.22).

Circulating current controllability

In terms of the circulating current regulation, since the PI/PR controller is not adopted, the corresponding current control requirement is necessary to be taken into account. Similar to the above analysis of phase current regulation, the following relations should be satisfied

to a large extent as

$$\frac{V_C+\Delta v_{Cx}^{com}}{2}+\widetilde{u}_{circ,x}^{*}>0 \tag{4.45}$$

$$\frac{-V_C-\Delta v_{Cx}^{com}}{2}+\widetilde{u}_{circ,x}^{*}<0. \tag{4.46}$$

Introducing the positive real parameter τ into (4.45) and (4.46), the following inequalities can be derived

$$\frac{V_C+\Delta v_{Cx}^{com}}{2}+\tau\widetilde{u}_{circ,x}^{*}\geq 0 \tag{4.47}$$

$$\frac{-V_C-\Delta v_{Cx}^{com}}{2}+\tau\widetilde{u}_{circ,x}^{*}\leq 0. \tag{4.48}$$

Similarly, defining τ_{circ} as the maximum τ that makes the relations in both (4.47) and (4.48) hold, it can be inferred that τ_{circ} should be at least larger than 1 in order to suppress the double-frequency circulating current. Considering (4.36), the following expressions can be derived from (4.47) and (4.48) as

$$\frac{V_{dc}}{N}+\frac{I}{\omega C}[\Delta u_2^{com}+2\tau N(u_{0x}+u_{2x})]\geq 0 \tag{4.49}$$

$$-\frac{V_{dc}}{N}+\frac{I}{\omega C}[-\Delta u_2^{com}+2\tau N(u_{0x}+u_{2x})]\leq 0. \tag{4.50}$$

From (4.43), (4.49) and (4.50), it can be inferred that the controllability of the VRLC-MPC technique depends largely on the value of N. Basically, a larger N means a smaller V_C (assuming a fixed value of V_{dc}) and the capacitor voltage ripples accumulated through more SMs, leading to poorer current controllability. Thus, the proposed analysis can be used to evaluate the feasibility of the VRLC scheme on a specific MMC system, or serve as designing criterion of an MMC system to be controlled by the VRLC-MPC technique if N can be configured as a design parameter. Given the desired rating and output characteristic of the MMC system (i.e. I, U, γ and ω), as well as the circuit parameters, the requirements of parameter N can be obtained which result in satisfying τ_{phs} and τ_{circ}. Generally, an upper bound of N can be determined as the solution.

Amplitude of current tracking ripples

On the other hand, the ripple amplitude of the phase current or circulating current tracking error can be estimated from the corresponding mathematical prediction model. For an accurate prediction (though slightly higher calculation cost as well), (4.1) and (4.2) are discretized employing the trapezoidal formula in this chapter (and only in this chapter) as

$$\hat{i}_x(k+1)=\frac{1}{\frac{2L_{eq}}{T_s}+R_{eq}}\left[\left(\frac{2L_{eq}}{T_s}-R_{eq}\right)i_x(k)-v_{Sx}(k)-v_{Sx}(k+1)\underbrace{-N_{xu}(k)v_{Cxu}(k)+N_{xl}(k)v_{Cxl}(k)}_{2u_x(k)}\right] \tag{4.51}$$

$$\hat{i}_{circ,x}(k+1)=\frac{1}{\frac{2L_{arm}}{T_s}+R_{arm}}\left[\left(\frac{2L_{arm}}{T_s}-R_{arm}\right)i_{circ,x}(k)+\underbrace{V_{dc}-N_{xu}(k)v_{Cxu}(k)-N_{xl}(k)v_{Cxl}(k)}_{2u_{circ,x}(k)}\right]. \tag{4.52}$$

The amplitude of phase current or circulating current tracking error (ripple) can be estimated from the variation of predicted current value per unit variation of $N_x^{\Delta}(k)$ or $N_x^{\Sigma}(k)$ in (4.51) and (4.52) respectively as

$$\delta_{phs}=\frac{V_C}{\frac{2L_{eq}}{T_s}+R_{eq}} \tag{4.53}$$

$$\delta_{circ}=\frac{V_C}{\frac{2L_{arm}}{T_s}+R_{arm}} \tag{4.54}$$

neglecting the capacitor voltage ripples. It is seen from (4.53) and (4.54) that larger value of V_C leads to larger current tracking ripples. Thus, N should be as large as possible for a better current quality once the requirements of current controllability are met.

4.4.2 Extension to other techniques

The proposed analysis can also be extended to other similar MPC methods which evaluate very few adjacent voltage levels [68,87,88]. As an example, the fast MPC (FMPC) method developed in [87] is illustrated in Fig. 4.3. Given $\mathrm{G}_*(N_{xu0},N_{xl0})$ being applied in the current sampling interval (i.e. the previous optimal control action), the candidates to be applied at the next sampling instant are itself (G_1) and those corresponding to the two adjacent voltage levels (G_2 and G_3): N_x^{Δ} can select its value from $\{N_{x0}^{\Delta}-2,N_{x0}^{\Delta},N_{x0}^{\Delta}+2\}$, while N_x^{Σ} is always maintained as N. The dependence of current controllability on N can be derived in a similar manner to the VRLC-MPC.

The $N+1$-level or $2N+1$-level modulation refer to the modulation technique with $N_x^{\Sigma}=N$ or $N_x^{\Sigma}\in\{N-1,N,N+1\}$, respectively [94]. Both modulation schemes present different characteristics of circulating current regulation. The $2N+1$-level modulation has been analyzed in the case of the proposed VRLC technique. In terms of the $N+1$-level modulation, if it is adopted as in [87, 94], it can be inferred from (4.28) that the circulating current can only be regulated by $\pm 2\Delta v_{Cx}^{dif}$ since N_x^{Σ} is fixed to N while N_x^{Δ} can be commanded to $N_{x0}^{\Delta}\pm 2$. However, the amplitude of $\Delta v_{Cx}^{dif}\frac{\omega C}{I}$ is normally much lower than that of Nu_2, making this scheme applicable only to MMC with very low number of SMs. As an example, considering an operating condition with $m=0.9$ and $\cos\gamma=0.95$, it can be obtained from (4.26) and (4.36) that the amplitudes of $2\Delta v_{Cx}^{dif}\frac{\omega C}{I}$ and u_{2x} are 0.3228 and 0.1283, respectively, which means that the circulating current may not be suppressed for $N\geq 3$ (though in reality this threshold may be larger owing to the influence of low-order harmonic contents in arm voltages/currents which are more significant when N is small). Thus, the $N+1$-level modulation is not preferable in terms of circulating current regulation.

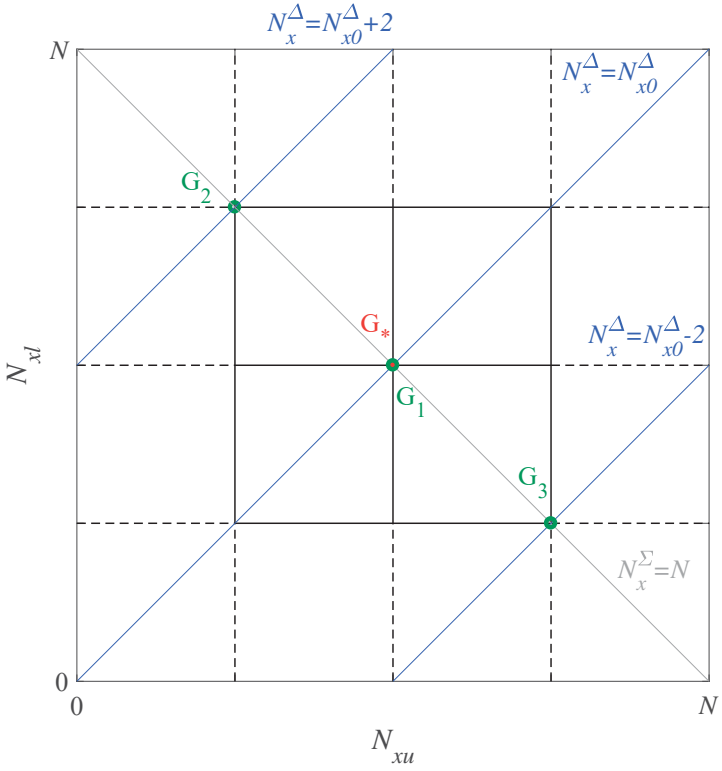


Figure 4.3 Principles of the FMPC method proposed in [87].

In addition, the proposed analysis can be applied to non-MPC techniques which use V_C for normalizing arm voltage references v_{xy}^*, such as the NLC method.

4.5 Simulation Results

To validate the effectiveness of the generalized VRLC-MPC techniques and the proposed analysis of current controllability, several simulation tests are carried out on a single-phase MMC-based system in the Matlab-Plecs environment. The output terminal is fed by an $R-L$ load. Related parameters are listed in Table 4.2.

The single-phase topology is adopted here and the power rating is scaled down compared with real applications. The steady-state performance is evaluated and the phase current reference is set with peak value of 10 A, leading to an operation with $m = 0.9042$, $\cos\gamma = 0.9987$. The number of SMs per arm is selected from $N = 12$ to 30 to study its influence on the current controllability of the VRLC-MPC method. Values of τ_{phs} and τ_{circ} of the studied operating condition with different parameter N are listed in Table 4.3 for reference. To maintain consistency with naming of variables, the single phase under study is denoted as phase-a.

Table 4.2 Parameters of the experimental MMC setup.

DC-link voltage, V_{DC}	670 V
Number of SMs per arm, N	12-30
SM capacitance, C	5 mF
Arm inductance, L_{arm}	6 mH
Arm resistance, R_{arm}	0.5 Ω
Load inductance, L	2 mH
Load resistance, R	30 Ω
AC frequency, f	50 Hz
Sampling/control frequency, T_s	20 kHz

Table 4.3 Value of τ_{phs} and τ_{circ} of the studied MMC system with different N.

N	12	14	16	18	20	22	24	26	28	30
τ_{phs}	4.7	3.4	2.6	2.1	1.7	1.4	1.1	1.0	0.8	0.7
τ_{circ}	5.6	4.1	3.2	2.5	2.0	1.7	1.4	1.2	1.0	0.9

The first group of steady-state phase current waveforms (blue curves), the corresponding references (red curves), and tracking errors of $N = 14$ are shown in Fig. 4.4. Different phase current controllers, namely PR (since PI controllers are not applicable for single-phase MMC), DB and OL are evaluated. The circulating current regulation adopts the OL controller for its simplicity as mentioned in section 4.2. The MPC method considering all the $(N+1)^2$ voltage level combinations [34] is evaluated as well (referred as Opt. for convenience). For a fair comparison, the same cost function J_i is employed by the Opt. method as well, which cannot guarantee stability in theory, is nevertheless adopted here as optimal performance reference (in terms of current tracking) since only the steady-state performance is evaluated. The circulating current waveforms of the above-mentioned methods are illustrated as well in Fig. 4.5. It can be observed that different methods show similar performance in terms of phase current tracking and circulating current regulation. The THD of different methods (for convenience, PR/DB/OL represents the proposed VRLC-MPC technique with the corresponding phase current controller) are, PR: 1.30%, DB: 1.26%, OL: 1.29%, and Opt.: 1.28%. The similar performance can find its explanation in Table 4.3: when $N = 14$, both $\tau_{phs} = 3.4$ and $\tau_{circ} = 4.1$ are large enough, which means that the accumulated capacitor voltage ripples can be easily compensated by proper selection of voltage levels according to the proposed analysis.

For comparison, the waveforms of phase current and circulating current when $N = 26$ are shown in Fig. 4.6 and 4.7, respectively. Compared with the case of $N = 14$, the circulating current waveform is suppressed well with lower amplitude as can be inferred from (4.54), which means $\tau_{circ} = 1.2$ is enough for suppressing the double-frequency

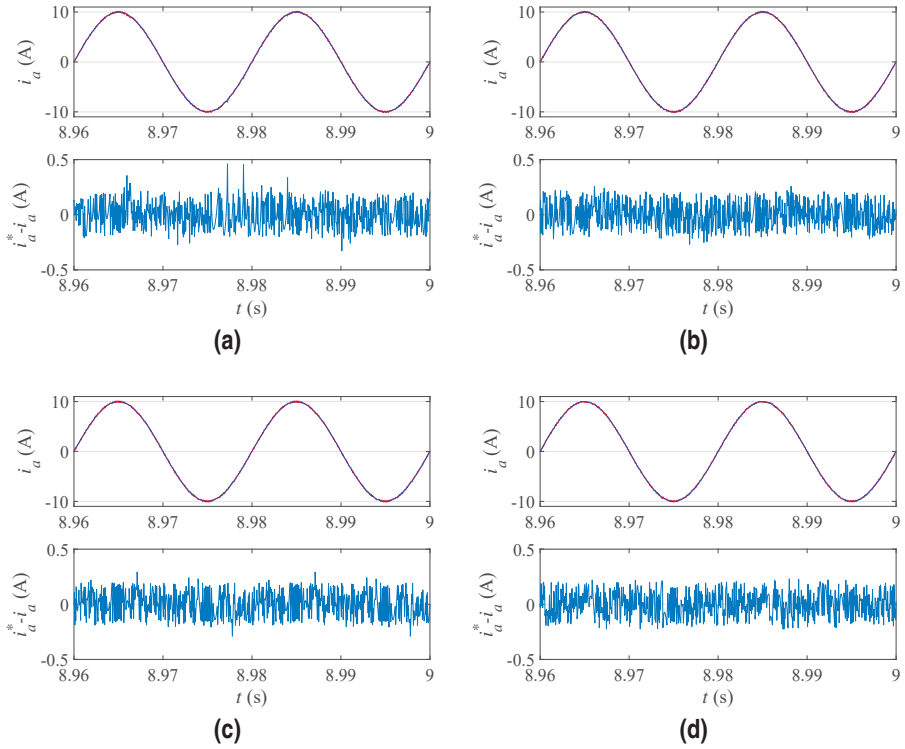


Figure 4.4 Phase current and tracking error ($N = 14$) of: (a) PR. (b) DB. (c) OL. (d) Opt.

fluctuation. However, different performance of phase current tracking shows among different MPC methods: apparent fundamental-frequency and triple-frequency components can be observed in the tracking error of VRLC-MPC method with OL scheme as a result of the decreased τ_{phs} (shown in Fig. 4.6c), which coincides with the analytical result derived in (4.35). The DB scheme presents the same problems but to a less extent. In contrast, the PR scheme shows reduced tracking error of phase current without apparent low-order harmonics similar to the Opt. reference method owing to the use of dedicated controller.

In terms of the circulating current regulation, poor performance can be caused if τ_{circ} is not sufficiently large. To illustrate this effect, circulating current waveforms of different values of N are shown in Fig. 4.8. With $\tau_{circ} = 1$ ($N = 28$) the circulating current can still be controlled well, while with $\tau_{circ} = 0.9$ ($N = 30$) a clear double-frequency component occurs because the one-level adjustment of N_Σ is not competent to compensate the ripple term of u_{2a} as derived in (4.36).

To further reveal the influence of parameter τ_{phs} and τ_{circ} on the current regulation of the MMC, phase current THD, 3rd harmonic content and circulating current ripple amplitude (RMS) of different MPC methods and different values of N are summarized in Fig. 4.9. Consistent to the previous analysis, as N increases (and thus τ_{phs}, τ_{circ}, δ_{phs} and δ_{circ}

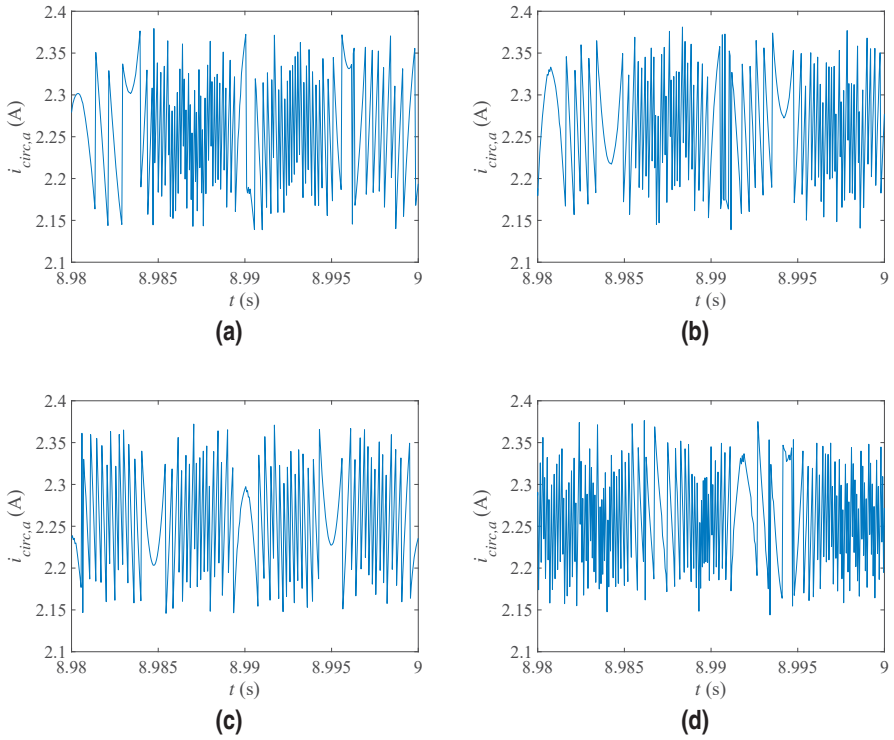


Figure 4.5 Circulating current ($N = 14$) of: (a) PR. (b) DB. (c) OL. (d) Opt.

decrease), a finer current regulation with lower amplitude of tracking error can be achieved provided that τ_{phs} and τ_{circ} are sufficiently large. However, as N continues to increase, τ_{phs} and τ_{circ} cannot meet the requirement for current regulation, and the VRLC-MPC method presents degraded performance. In terms of the circulating current, the amplitude increases when $N = 30$ for the VRLC technique in all three cases owing to the unsuppressed second harmonic. In terms of the phase current, THD and third harmonic content increase as N increases if OL principle is employed. The DB scheme shows increasing third harmonic content to a less extent while the THD is not much influenced (which can be explained by the fact that the worst-case value of τ_{phs} considered in this study is 0.7 that is not very low). The PR shows improved phase current quality as N increases since the ripple terms u_{1a} and u_{3a} are inherently compensated by the PR controller. As reference, the Opt. method shows immunity against the increasing value of N since all $(N+1)^2$ combinations of voltage levels are evaluated. However, its computational burden is much higher than the VRLC-MPC method which only evaluates 4 voltage level combinations and the VRLC-MPC technique shows comparable steady-state performance when τ_{phs} and τ_{circ} are large enough. Considering the possibility of increasing the sampling/control frequency owing to the reduced calculation, the VRLC-MPC is more recommended.

The proposed analysis of current controllability is based on the estimated information

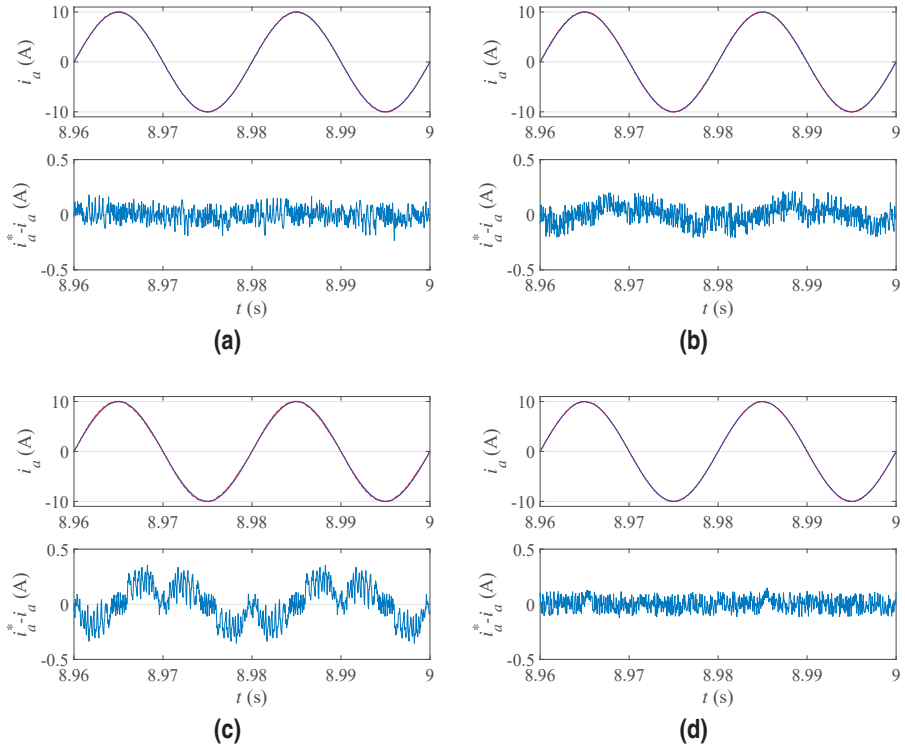


Figure 4.6 Phase current and tracking error ($N = 26$) of: (a) PR. (b) DB. (c) OL. (d) Opt.

of SM capacitor voltage ripples as addressed in section 4.3. For validation, the decoupled capacitor voltage ripples of the PR-based VRLC-MPC technique with $N = 26$ and the corresponding references are shown in Fig. 4.10. It can be observed that the fundamental- and double-frequency components match perfectly with the theoretical analysis. A little DC offset exists which is normal since v_{Cxu}^0 and v_{Cxl}^0 (in eq. (4.20) and (4.21)) do not necessarily have to equal V_C owing to the lack of explicit arm energy regulator. Considering that the offset is negligible and the ripple parts are more concerned, the conducted verification still holds valid.

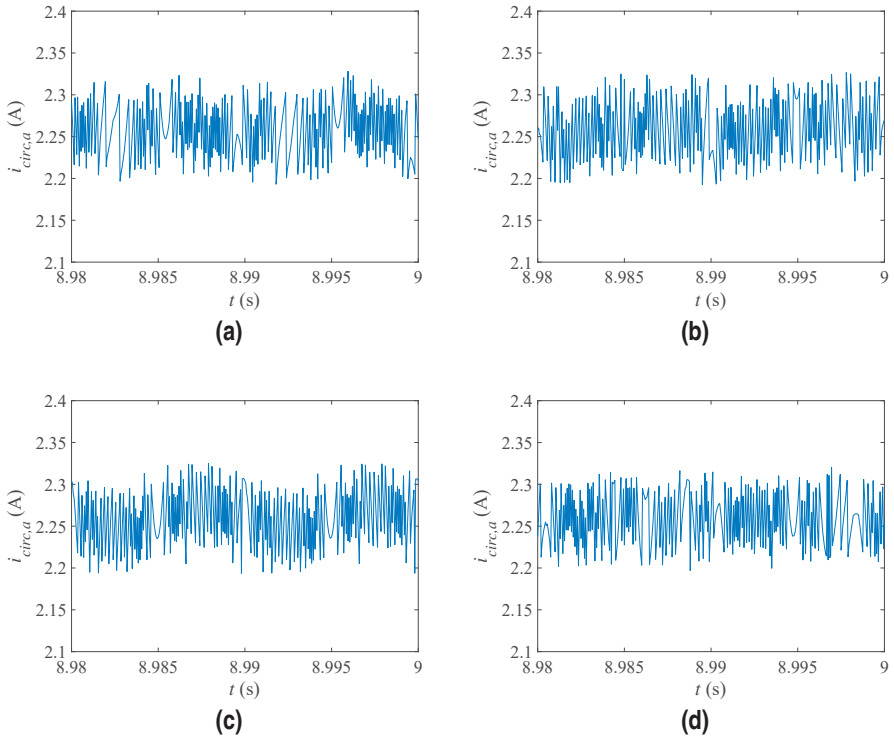


Figure 4.7 Circulating current ($N = 26$) of: (a) PR. (b) DB. (c) OL. (d) Opt.

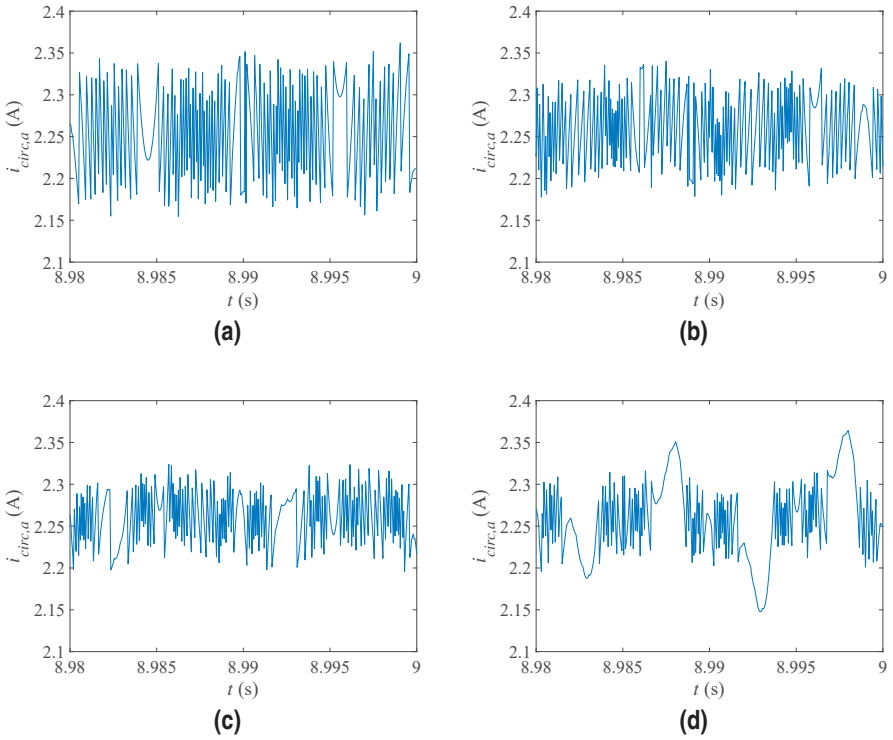


Figure 4.8 Circulating current of PR of: (a) $N = 16$. (b) $N = 22$. (c) $N = 28$. (d) $N = 30$.

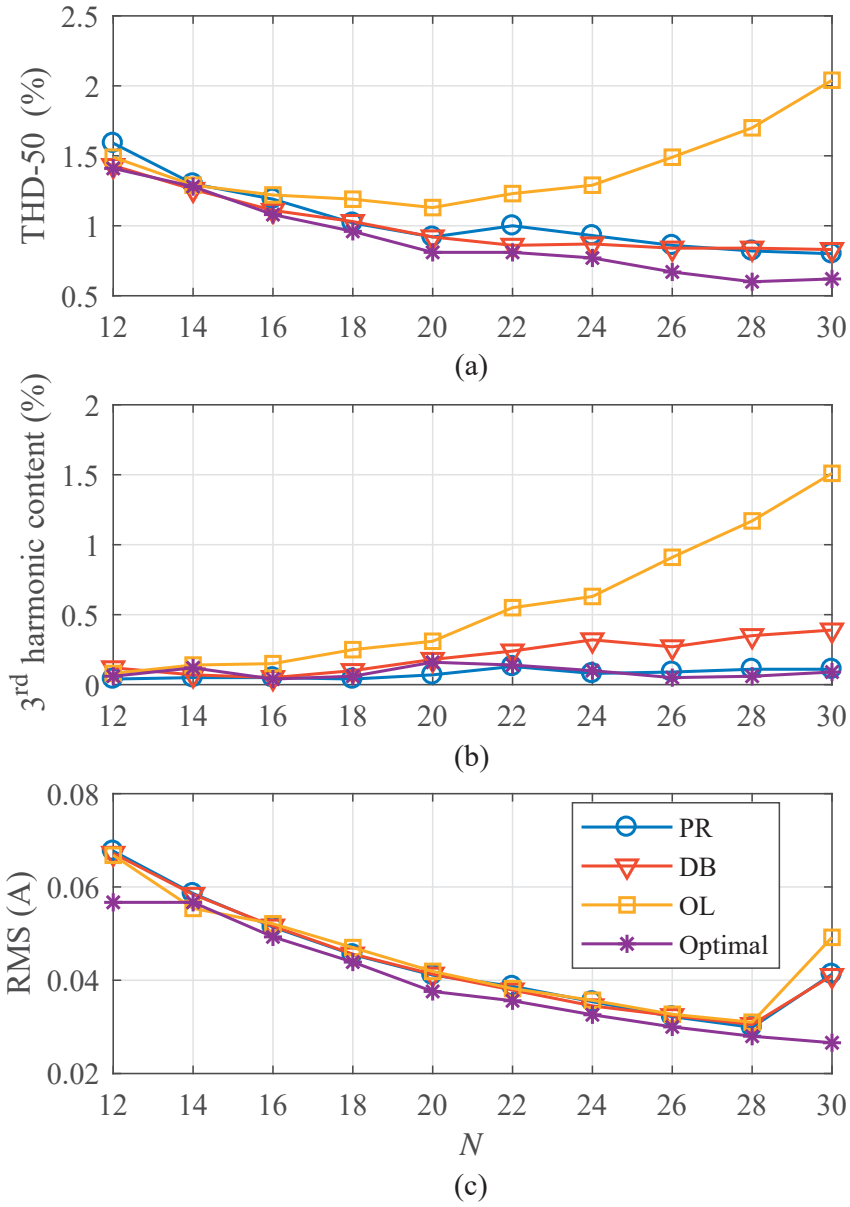


Figure 4.9 (a) THD-50 of i_a (b) Third harmonic content of i_a (c) RMS of $i_{circ,a}$.

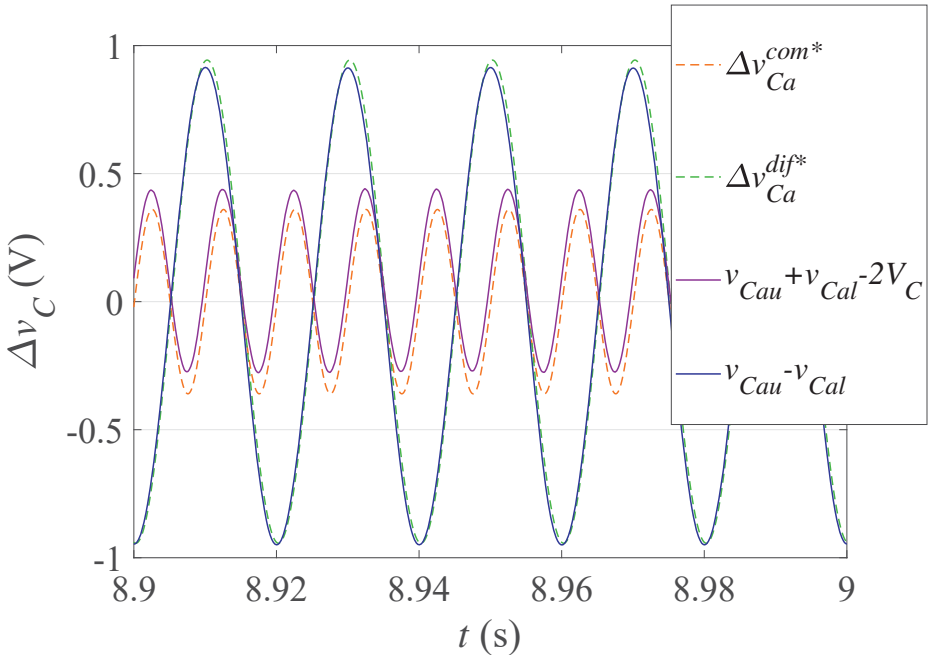


Figure 4.10 Decoupling of capacitor voltage ripples.

5 VRLC-MPC for MMC with Large Number of SMs

Benefitting from the analysis in the previous chapter, this chapter proposes a solution for applying the VRLC-MPC technique to an MMC with large number of SMs, while achieving enough current quality and reduced computational cost. This chapter is outlined as follows. Section 5.1 summarizes the challenges in the control of an MMC with large number of SMs. Section 5.2 proposes a solution based on SM grouping, which is validated by several simulation tests in section 5.3

5.1 Difficulties in Controlling an MMC with Large Number of SMs

In high-voltage MMC-based applications, such as HVDC transmissions, the number of SMs (N) is very high, up to several hundreds [17, 19]. For such MMC systems, the control and modulation methods face a lot of challenges, as very high volume of input and output signals need to be handled. Therefore, the involved computational burden has to be limited to an affordable level in order to achieve a high bandwidth, whichever control/modulation technique such MMCs apply.

Conventional MPC techniques exhibit their limitations in this scenario because within each control cycle, the number of cost function evaluations is at least proportional to N, leading to unaffordable computational burden even if the SM capacitor voltage balancing can be achieved by the simple sorting scheme. Thus, the only feasible MPC-based option is to evaluate the cost function for fixed number of times (normally no more than four per phase) for voltage level determination, such as the VRLC technique.

However, the VRLC method suffers from reduced controllability as explained in the previous chapter: as N increases, V_C becomes increasingly insufficient to suppress the ripple component of $\widetilde{u}_x$ or $\widetilde{u}_{circ,x}$ respectively defined in (4.35) and (4.36), and as a result the phase current or circulating current cannot be regulated well. PI or PR controllers can be employed to carry out the phase current tracking to mitigate the above problem.

However, the circulating current control is highly influenced by this phenomenon since DB or OL controller is used.

As mentioned in chapter 3, a possible solution is to evaluate more adjacent voltage levels as N increases, which, however, again increases the computational burden and design complexity.

In addition, even with properly-determined arm voltage levels, the capacitor voltage sorting is still very costly in implementation since N is large. Thus, the capacitor voltage balancing needs to be addressed in a decentralized manner [96].

5.2 Proposed MMC Operation applying a SM-grouping Scheme

5.2.1 General description

To solve the above-mentioned problems, the SMs within each arm can be grouped as illustrated in Fig. 5.1. Specifically, in the proposal, the N SMs in each arm are evenly divided into B groups of M SMs. All the M SMs of the same group always adopt the same switching signal. In this way, each SM group is equivalent to a virtual larger SM with scaled-down capacitance of C/M and scaled-up capacitor voltage reference of MV_C, as shown in Fig. 5.1. Since the gap between adjacent voltage levels is increased to M times its original value, the current controllability can be enhanced according to the analysis of the previous chapter. In this way, the control of an MMC with high number of SMs is transformed into the control of an MMC with low number of SMs, and the effectiveness of the VRLC method (and similar ones) can be guaranteed. Other benefits include simplified implementation and easy realization of distributed control of such large MMCs.

The concept of virtual SM or SM grouping has been discussed previously in [86, 96–98]. However, these methods are different from the proposed one. In [86] one group of each arm is permitted to switch on part of the SMs in order to approximate the arm voltage reference; in [97, 98] each SM group is modulated individually using the NLC technique; in [96] the number of switched-on SMs of each group keeps being updated for capacitor voltage and switching frequency balancing; etc.

5.2.2 Capacitor voltage balancing

It is worth noting that, in the proposed operation, the capacitor voltages of the virtual SMs (i.e. the sum capacitor voltage of each SM group) are sorted in the conventional way to achieve the balancing effect. Provided that the sampling frequency to achieve capacitor voltage balancing is high enough, the energy of each arm can still be evenly distributed among all SMs without much negative influence on the current control. The computational cost in terms of sorting can be reduced as well.

Ideally, the capacitor voltages of the SMs within the same group should be the same. However, in an actual case, the commonly-used aluminum electrolytic capacitors (AECs) gradually deteriorate as they age owing to electrolyte vaporization, resulting in decreased capacitance and increased equivalent series resistance [99]. Additionally, the inevitable tolerances of passive components, unequal losses among power devices, and imbalanced communication delay can also lead to unequal charging/discharging [100]. To solve this

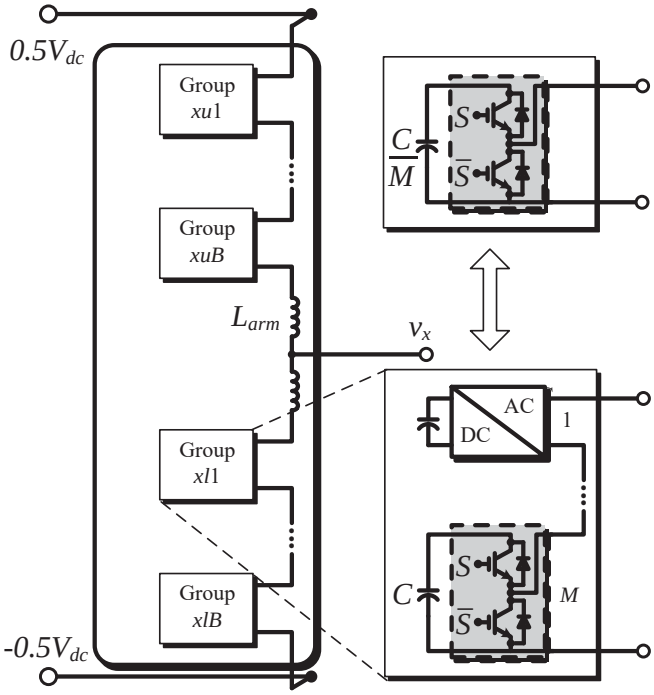


Figure 5.1 SM-grouping method.

problem, a capacitor-voltage-monitoring process can be designed: in case that some SM capacitor voltage has large deviation (larger than a specific threshold) from the average value of the group, extra regulation is required for the corresponding SM. One option is to select the outliers of each group and swap the outliers among different groups. A detailed design of this approach is out of the scope of this thesis. In the remainder of this chapter, all SMs are assumed to have exactly the same gate signals and capacitor voltage in order to simplify the analysis.

As analyzed above, significant reduction in calculation can be achieved by the proposed SM-grouping strategy. Further simplification in hardware infrastructure is another potential benefit. For instance, reduced number of voltage sensors are required if the capacitor voltages are monitored and balanced with only one voltage sensor for each group, leading to lower system cost and easier fault-tolerant operation [101, 102]. This possibility will be investigated as future work.

5.2.3 Design principles considering current controllability

The group size M is an important parameter for the design of the proposed SM-grouping scheme. This parameter can be designed with the help of the current control requirement analyzed in the previous chapter (in section 4.4). Considering the grouping configuration described above, and the definitions of τ_{phs} and τ_{circ} provided in section 4.4, phase current

controllability can be obtained from (4.43) as

$$\frac{MV_{dc}}{N}+\frac{I}{\omega C}[M\Delta u_2^{com}+2\tau_{phs}N(u_{1x}+u_{3x})]\geq 0 \tag{5.1}$$

and circulating current controllability can be obtained from (4.49) and (4.50) as

$$\frac{MV_{dc}}{N}+\frac{I}{\omega C}[M\Delta u_2^{com}+2\tau_{circ}N(u_{0x}+u_{2x})]\geq 0 \tag{5.2}$$

$$-\frac{MV_{dc}}{N}+\frac{I}{\omega C}[-M\Delta u_2^{com}+2\tau_{circ}N(u_{0x}+u_{2x})]\leq 0. \tag{5.3}$$

Considering the fact that M should be much lower than N for a high number of voltage levels (and thus voltage/current quality), the second terms in the above three inequalities can be neglected. Thus, (5.1) turns into

$$\frac{MV_{dc}}{N}\geq -\frac{2\tau_{phs}NI(u_{1x}+u_{3x})}{\omega C} \tag{5.4}$$

while (5.2) and (5.3) turn into

$$\frac{MV_{dc}}{N}\geq \pm\frac{2\tau_{circ}NI(u_{0x}+u_{2x})}{\omega C}. \tag{5.5}$$

Then, M can be designed according to phase current controllability as

$$M\geq \frac{2\tau_{phs}IN^2}{\omega CV_{dc}}\mathrm{AMP}(u_{1x}+u_{3x}) \tag{5.6}$$

and according to circulating current controllability as

$$M\geq \frac{2\tau_{circ}IN^2}{\omega CV_{dc}}[\mathrm{AMP}(u_{0x})+\mathrm{AMP}(u_{2x})]. \tag{5.7}$$

AMP represents the amplitude (peak value) of the corresponding input, which can be easily obtained from (4.35) and (4.36). Considering the information given in (4.36), the explicit solution of (5.7) can be derived as

$$M\geq \frac{\tau_{circ}IN^2m\left[2\sin\gamma+\sqrt{9+(m^4-6m^2)\cos^2\gamma}\right]}{16\omega CV_{dc}}. \tag{5.8}$$

τ_{phs} and τ_{circ} are given by the users, normally set a value much larger than 1. Then, the lower bound of M can be obtained from (5.6) and (5.8). Since larger M means high current tracking ripples as can be inferred from δ_{phs} and δ_{circ} defined in (4.53) and (4.54), respectively, the final value of M can be selected as small as possible once the requirements of (5.6) and/or (5.8) are met.

5.3 Simulation Results

Several simulation tests have been carried out to validate the proposed solution applied to a three-phase MMC system with 128 SMs per arm. Related parameters are summarized in Table 5.1. The DC side of the MMC is connected to a DC power supply and the AC side is connected to a three-phase grid. The controlling/sampling frequency is set as f_s=20 kHz for a high current quality.

Table 5.1 Parameters of the MMC system.

DC-link voltage, V_{dc}	128 kV
Grid voltage, peak value of v_{Sx}	69.8 kV
AC frequency, f	50 Hz
Number of SMs per arm, N	128
Nominal capacitor voltage, V_C	1 kV
SM capacitance, C	20 mF
Arm inductance, L_{arm}	40 mH
Arm resistance, R_{arm}	100 mΩ
AC side inductance, L	5 mH
AC side resistance, R	100 mΩ

5.3.1 Steady-state evaluation

The steady-state performance of the VRLC method, with the same implementation of chapter 3, is evaluated on the MMC simulation system. In other words, PI and OL principles are adopted to determine u_x^* and $u_{circ,x}^*$, respectively. For comparison, the conventional NLC technique is also applied but without circulating current controller. In this way, the only difference between both methods is the rounding function and thus permitting to observe whether the VRLC technique works effectively or not. Fig. 5.2 illustrates the test results of both techniques (without applying the SM-grouping concept). The converter works in inverter mode with an active power of 85.5 MW and a reactive power of 0 VA. Before 2.5 seconds, the MMC is operated with the conventional NLC scheme and the VRLC method is activated at 2.5 seconds. In both cases, the output current achieves very high quality resulted from the large number of voltage levels, without suffering from insufficient current control capability because the PI controllers are used. However, in both methods the circulating current presents a second-order harmonic with non-negligible amplitude. As expected, no improvement is observed by activating the VRLC technique because of the large number of SMs that limit the circulating current controllability.

To verify the effectiveness of the proposed SM-grouping method, the same test of Fig. 5.2 is done with the SMs of each arm organized in 16 groups with 8 SMs in each group ($B = 16, M = 8$). Since in simulation all the SMs are in exactly the same condition,

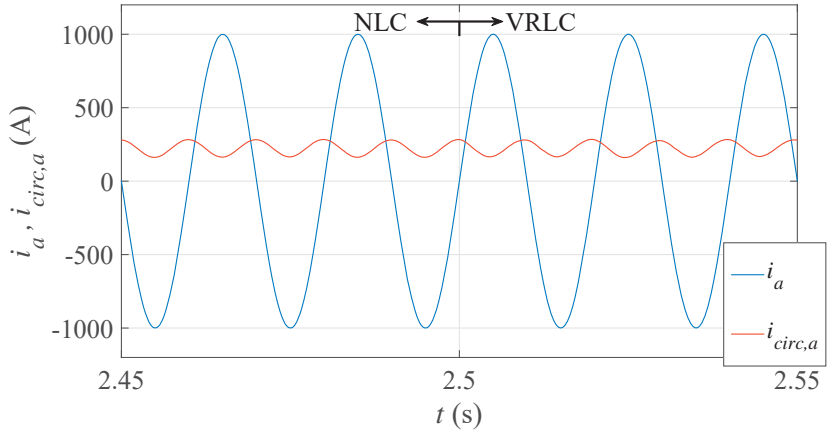


Figure 5.2 Phase current and circulating current of phase a applying NLC or VRLC to determine N_{xy} (both without SMs grouping).

the SM capacitor voltages of the same group are identical. Results are shown in Fig. 5.3, where it can be observed that after activating the VRLC method, the circulating current is correctly regulated with the major second-order harmonic component eliminated, thus validating the proposed solution.

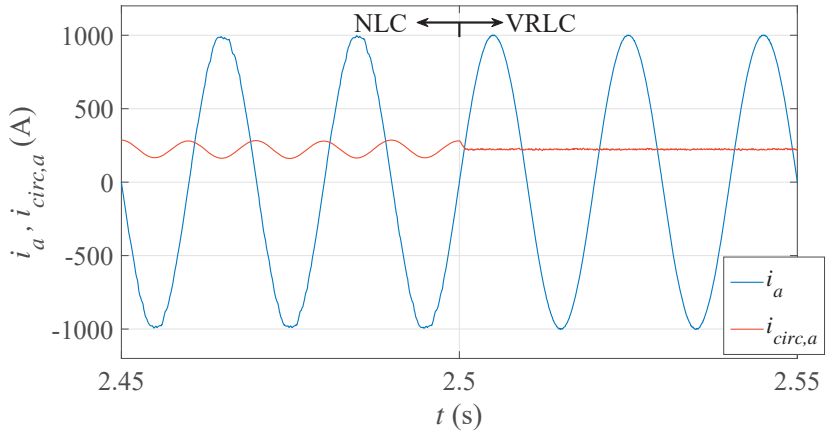


Figure 5.3 MMC with SM grouping ($M = 8$): phase current and circulating current of phase a applying NLC and VRLC techniques to determine N_{xy}.

Fig. 5.4 illustrates the waveforms of the arm voltage (v_{au}) and phase voltage (v_a) of the MMC controlled by the VRLC with/without SM-grouping. It can be observed that the number of arm voltage levels has decreased applying the SM-grouping scheme (from 129 levels to 17 levels theoretically), while in terms of the phase voltage, the grouping scheme

does not introduce too much negative influence and the phase voltage still presents high quality.

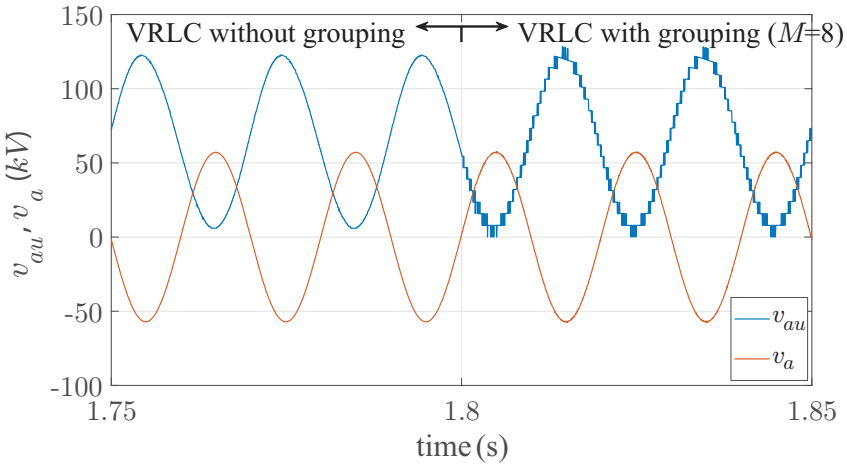


Figure 5.4 Phase voltage and upper arm voltage of the MMC applying the VRLC method without and with SMs grouping (M=8).

The performance of the proposed SM-grouping technique highly depends on the parameter M. To investigate this effect, the above-described steady-state test is evaluated for both the NLC and the VRLC techniques with different values of M in terms of the THD of the phase current and the RMS value of the AC component of the circulating current. Results are summarized in Fig. 5.5. The case of $M = 1$ corresponds to the original MMC without SM grouping. Generally, as M increases, the VRLC presents increasing improvement of phase current quality and circulating current suppression over the conventional NLC technique applying the same number of groups, as a result of the increased current control capability quantified by τ_{phs} and τ_{icirc}. However, it should be noticed that applying the SM grouping concept, as the MMC behaves as an MMC with less number of SMs, the quality of the output waveforms is lowered. This represents a trade-off between current controllability, power quality, and computational cost.

As commented previously, the performance of the VRLC does not always get improved when M is increased. As can be observed in Fig. 5.5, if M is too large, the performance in terms of both control objectives becomes worse. This is because as M increases, τ_{phs} and τ_{circ} increase but δ_{phs} and δ_{circ} increase as well, while δ_{phs} and δ_{circ} basically determines the ripple amplitude of the corresponding current tracking error. To illustrate this effect, the circulating current waveforms applying the VRLC method with $M = 4, 8, 16, 32$ are shown in Fig. 5.6 for comparison. As can be observed, when $M = 4$, the second-order harmonic circulating current cannot be suppressed well since τ_{circ} is small. As M increases, the second-order harmonic content in the circulating current is better controlled but with increasing ripple amplitude because of the increased δ_{circ}. Therefore, a trade-off needs to be considered.

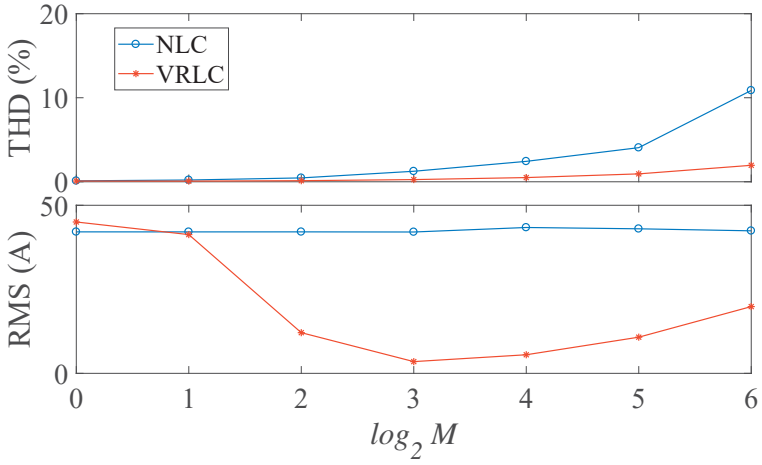


Figure 5.5 Steady-state performance comparison in terms of: THD of i_a (upper) and RMS of the AC component of $i_{circ,a}$.

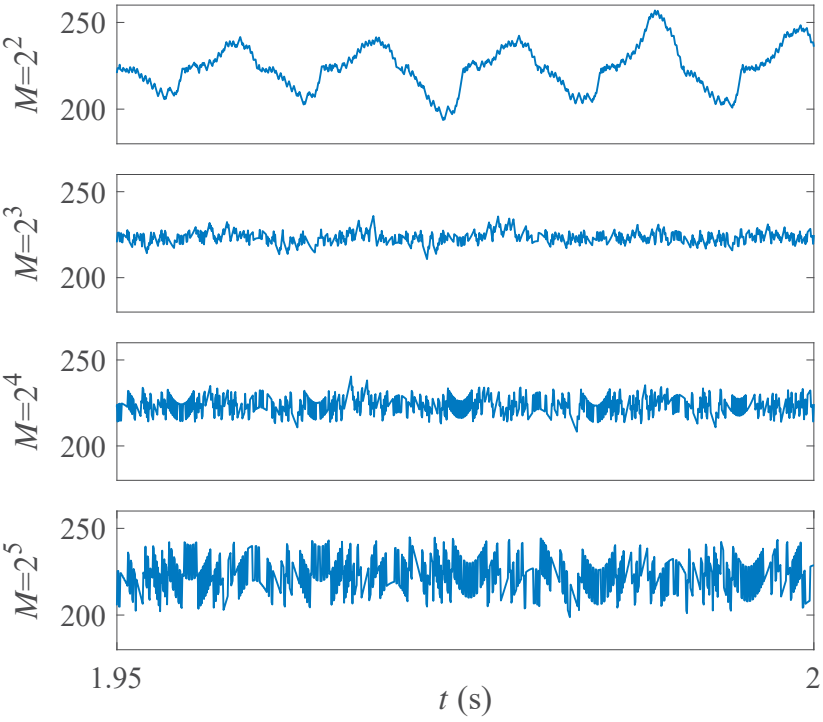


Figure 5.6 Waveforms of circulating current ($i_{circ,a}$) of VRLC under different M.

To quantify the circulating current regulating ability, τ_{circ} with different values of M are summarized in Table 5.2, which coincide with the results shown in Fig. 5.6 where the circulating current is uncontrolled with $M = 4$ and well regulated with $M = 8, 16, 32$.

Table 5.2 Value of τ_{circ} of the studied MMC system with different M.

$log_2 M$	0	1	2	3	4	5	6
τ_{circ}	0.4	0.7	1.4	2.8	5.7	11.4	22.7

5.3.2 Dynamic evaluation

Poor dynamic response may be another drawback of the MPC-controlled MMC with large number of SMs if very limited number of voltage levels are evaluated, which can also be mitigated by the proposed SM-grouping solution. In the case of the VRLC method, since it contains a control loop of phase current controllers (PI controllers in the dq frame), the phase current dynamic is less vulnerable to the high value of N. However, as for the circulating current control, this issue needs especially to be dealt with.

The dynamic response of the MMC is tested by applying a reversal of active power reference at 1.805 seconds. The obtained results are shown in Fig. 5.7 and Fig. 5.8 in terms of the phase-a circulating current and phase current, respectively. The conventional NLC scheme without SM grouping and the VRLC technique with $M = 1, 8, 16, 32$ are evaluated. As can be observed, the VRLC without SM grouping (M=1) shows the worst dynamic (almost the same with the NLC without SM grouping). As M increases, the dynamic response of the VRLC scheme becomes faster, especially in terms of the circulating current as shown in Fig. 5.7. On the other hand, in terms of the phase current, different methods show slight difference because of the existence of the phase current control loop as explained previously (but still becomes faster as M increases as shown in Fig. 5.8). It is worth noting that the VRLC with $M = 8$ shows non-negligible amplitude of harmonic circulating current during the first several cycles during transient, though it achieves well-controlled circulating current with low ripple amplitude in the steady-state test. Thus, from Table 5.2, it can be inferred that $\tau_{circ} = 2.8$ ($M = 8$) is enough for steady-state circulating current control yet not sufficient for transient conditions. Taking all the simulation results into account, the VRLC with $M = 16$ seems to be the best option for the tested MMC with the parameters summarized in Table 5.1. During system design stage, M can be determined by substituting a proper value of τ_{circ} (for instance $\tau_{circ} = 4$) into (5.8), then selecting the minimum proper integer that satisfies this requirement.

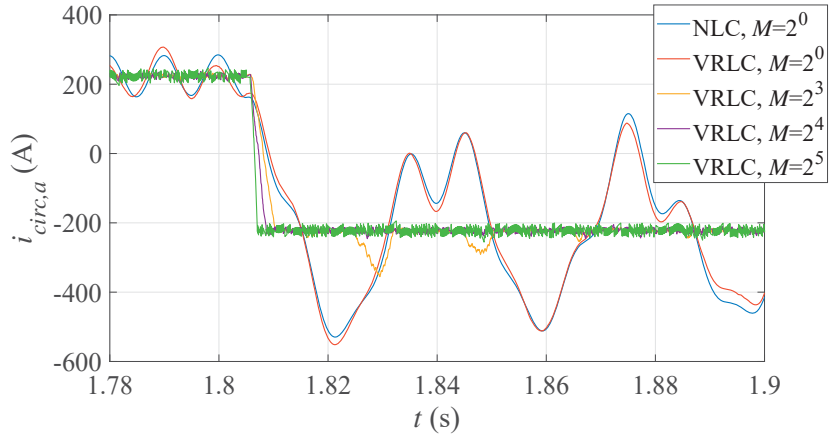


Figure 5.7 Dynamic performance in terms of circulating current response.

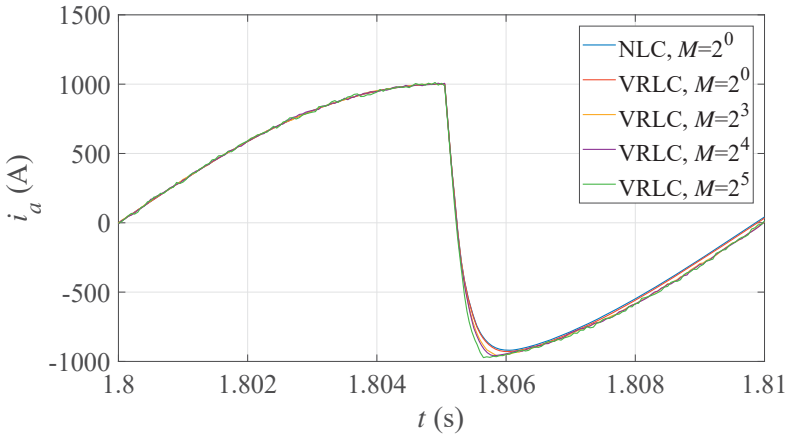


Figure 5.8 Dynamic performance in terms of phase current response.

6 VRLC-MPC Employing Quadratic Programming

In this chapter, the FCS-MPC and the CCS-MPC techniques are both considered to develop a joint control method to operate the MMC. The core step is to determine the arm voltage references by optimizing a constrained quadratic programming problem structured from the cost function. The chapter is arranged as follows. Section 6.1 derives the constrained optimization problems from the system models and the cost functions. The solutions are provided in section 6.2. Section 6.3 addresses the determination of arm voltage levels and gate signals. Then, section 6.4 and 6.5 provide the experimental and simulation validation with comparative analysis based on the results.

6.1 Formulation of Optimization Problem

As the first step of the proposed technique, the cost functions (2.20), (2.21), and (2.22) introduced in chapter 2 need to be rearranged into optimization problems. In this chapter, the quadratic cost function ($h = 2$) is investigated.

6.1.1 Cost function reformulation

Considering only current tracking

Firstly, the cost function (2.20) (which considers only current tracking) is reformulated. Applying (2.16) and (2.17) into (2.20), the cost function can be expressed as a function of $v_{xu}(k)$ and $v_{xl}(k)$ as

$$J_i(v_{xu}(k),v_{xl}(k)) = p_1 g_1^2[v_{xu}(k) - v_{xl}(k) + f_1(k)]^2 + p_2 g_2^2[v_{xu}(k) + v_{xl}(k) + f_2(k)]^2 \quad (6.1)$$

where

$$g_1 = \frac{T_s}{L_{arm} + 2L} \tag{6.2}$$
$$g_2 = \frac{T_s}{2L_{arm}}$$

and $f_{1,2}(k)$ are defined as

$$f_1(k) = 2v_{Sx}(k) + (R_{arm} + 2R)i_x(k) + \frac{i_x^*(k+1) - i_x(k)}{g_1} \tag{6.3}$$
$$f_2(k) = 2R_{arm}i_{circ,x}(k) - V_{dc} + \frac{i_{circ,x}^*(k+1) - i_{circ,x}(k)}{g_2} \tag{6.4}$$

For the sake of simplicity, setting

$$\lambda_1 = p_1 g_1^2, \lambda_2 = p_2 g_2^2 \tag{6.5}$$

then (6.1) can be reformed as

$$J_i(v_{xu}(k), v_{xl}(k)) = \lambda_1[v_{xu}(k) - v_{xl}(k) + f_1(k)]^2 + \lambda_2[v_{xu}(k) + v_{xl}(k) + f_2(k)]^2. \tag{6.6}$$

Considering arm energy regulation

Similar to J_i, J_w of (2.21) can be arranged into the following form

$$\begin{aligned} J_w(v_{xu}(k), v_{xl}(k)) &= \lambda_3[i_{xu}(k)v_{xu}(k) - i_{xl}(k)v_{xl}(k) \\ &+ f_3(k)]^2 + \lambda_4[i_{xu}(k)v_{xu}(k) + i_{xl}(k)v_{xl}(k) + f_4(k)]^2 \end{aligned} \tag{6.7}$$

where

$$\lambda_3 = p_3 T_s^2, \lambda_4 = p_4 T_s^2 \tag{6.8}$$

and

$$f_3(k) = \frac{W_{x\Delta}(k) - W_{x\Delta}^*(k+1)}{T_s} \tag{6.9}$$
$$f_4(k) = \frac{W_{x\Sigma}(k) - W_{x\Sigma}^*(k+1)}{T_s}. \tag{6.10}$$

Then, from (2.22), the formulation of J_{iw} can also be obtained adding (6.6) and (6.7) together.

6.1.2 Optimization problem

Within the frame of the MPC, the cost function (either J_i or J_{iw}) has to be minimized to achieve optimal performance. In the previously proposed MPC schemes, the minimization of the cost function is realized by evaluating different voltage levels of $v_{xy}(k)$ in an exhaustive manner, leading to a considerable computational cost. As an alternative,

the cost function can be minimized employing numerical optimization techniques. Thus, optimization problems need to be formulated.

Case of J_i

Considering optimizing J_i, it can be inferred from (6.6) that the cost function reaches the minimum (zero) when and only when the following equations are satisfied

$$v_{xu}(k) - v_{xl}(k) + f_1(k) = 0 \tag{6.11}$$
$$v_{xu}(k) + v_{xl}(k) + f_2(k) = 0 \tag{6.12}$$

leading to the global solution as

$$v_{xu\_0}(k) = -\frac{f_1(k) + f_2(k)}{2},\ v_{xl\_0}(k) = \frac{f_1(k) - f_2(k)}{2}. \tag{6.13}$$

To gain a further insight into the cost function, (6.6) is altered into the following matrix form. For simplicity, the time instant k is not explicitly indicated. Throughout the chapter, all variables denote those of time instant k unless otherwise stated.

$$J_i(\boldsymbol{v}_{xy}) = \boldsymbol{v}_{\boldsymbol{xy}}^T \boldsymbol{Q_i} \boldsymbol{v}_{xy} + 2\boldsymbol{c_i}^T \boldsymbol{v}_{xy} + d_i \tag{6.14}$$

where the related variables are defined as follows

$$\boldsymbol{Q_i} = \begin{bmatrix} q_{i1} & q_{i2} \\ q_{i2} & q_{i3} \end{bmatrix} = \begin{bmatrix} \lambda_1 + \lambda_2 & -\lambda_1 + \lambda_2 \\ -\lambda_1 + \lambda_2 & \lambda_1 + \lambda_2 \end{bmatrix} \tag{6.15a}$$
$$\boldsymbol{c_i} = \begin{bmatrix} c_{i1} \\ c_{i2} \end{bmatrix} = \begin{bmatrix} \lambda_1 f_1 + \lambda_2 f_2 \\ -\lambda_1 f_1 + \lambda_2 f_2 \end{bmatrix},\ \boldsymbol{v}_{xy} = \begin{bmatrix} v_{xu} \\ v_{xl} \end{bmatrix}. \tag{6.15b}$$

Since

$$\det(\boldsymbol{Q_i}) = 4\lambda_1\lambda_2 > 0, \tag{6.16}$$

$\boldsymbol{Q_i}$ is positive definite. Therefore, (6.14) is strictly convex with at most one minimum point [103], and (6.14) represents an elliptic paraboloid in orthogonal coordinates $(v_{xu}, v_{xl}, J_i(v_{xu}, v_{xl}))$ as shown in Fig. 6.1. The contour lines of J_i are a series of ellipses with the same center point (v_{xu_0}, v_{xl_0}), the same eccentricity, and the same major/minor axis with equation of (6.11)/(6.12). As the weighting factor λ_2 increases relative to λ_1, the elliptic paraboloid is stretched along the axis of (6.12).

However, the arm voltage is bounded as

$$0 \le v_{xy}(k) \le v_{dcxy}(k) = \sum_{z=1}^{N} v_{Cxyz}(k). \tag{6.17}$$

Thus, the unconstrained solution (6.13) cannot be adopted directly. Since the constrains are linear, the optimization problem to be solved is a typical quadratic programming problem, which can be formulated as

$$\min_{\boldsymbol{v}_{xy}} J_i(\boldsymbol{v}_{xy}), \quad \text{subject to } \boldsymbol{A}\boldsymbol{v}_{xy} \preceq \boldsymbol{b} \tag{6.18}$$

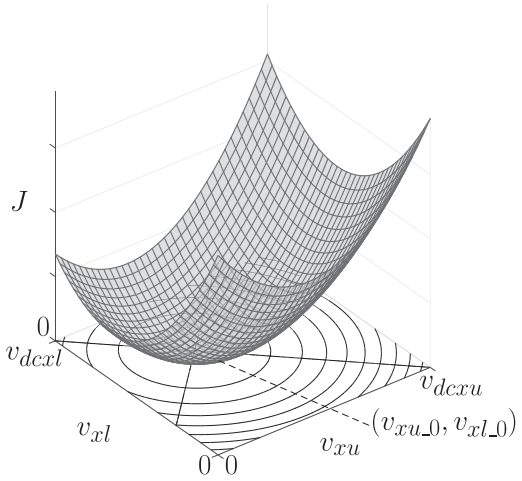


Figure 6.1 Geometrical interpretation of the elliptic paraboloid in orthogonal coordinates.

where

$$\boldsymbol{A} = \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \end{bmatrix}^T \tag{6.19a}$$

$$\boldsymbol{b} = \begin{bmatrix} v_{dcxu} & v_{dcxl} & 0 & 0 \end{bmatrix}^T. \tag{6.19b}$$

Case of J_{iw}

Similar to (6.14) and (6.15), J_w can be rearranged into the matrix form as

$$J_w(\boldsymbol{v}_{xy}) = \boldsymbol{v}_{\boldsymbol{xy}}^T \boldsymbol{Q}_{\boldsymbol{w}} \boldsymbol{v}_{xy} + 2\boldsymbol{c}_{\boldsymbol{w}}^T \boldsymbol{v}_{xy} + d_w \tag{6.20}$$

where

$$\begin{aligned} \boldsymbol{Q}_{\boldsymbol{w}} &= \begin{bmatrix} q_{w1} & q_{w2} \\ q_{w2} & q_{w3} \end{bmatrix} \\ &= \begin{bmatrix} i_{xu}^2(\lambda_3+\lambda_4) & i_{xu}i_{xl}(-\lambda_3+\lambda_4) \\ i_{xu}i_{xl}(-\lambda_3+\lambda_4) & i_{xl}^2(\lambda_3+\lambda_4) \end{bmatrix} \end{aligned} \tag{6.21a}$$

$$\boldsymbol{c}_{\boldsymbol{w}} = \begin{bmatrix} c_{w1} \\ c_{w2} \end{bmatrix} = \begin{bmatrix} i_{xu}(\lambda_3 f_3 + \lambda_4 f_4) \\ i_{xl}(-\lambda_3 f_3 + \lambda_4 f_4) \end{bmatrix} \tag{6.21b}$$

From (2.22), (6.14) and (6.20), J_{iw} can be derived as

$$J_{iw}(\boldsymbol{v}_{xy}) = \boldsymbol{v}_{\boldsymbol{xy}}^T \boldsymbol{Q}_{iw} \boldsymbol{v}_{xy} + 2\boldsymbol{c}_{\boldsymbol{iw}}^T \boldsymbol{v}_{xy} + d_{iw} \tag{6.22}$$

where

$$\boldsymbol{Q}_{iw} = \begin{bmatrix} q_{iw1} & q_{iw2} \\ q_{iw2} & q_{iw3} \end{bmatrix} = \boldsymbol{Q}_i + \boldsymbol{Q}_w \tag{6.23a}$$

$$\boldsymbol{c}_{iw} = \begin{bmatrix} c_{iw1} \\ c_{iw2} \end{bmatrix} = \boldsymbol{c}_i + \boldsymbol{c}_w \tag{6.23b}$$

The problem to be optimized is

$$\min_{\boldsymbol{v}_{xy}} J_{iw}(\boldsymbol{v}_{xy}), \quad \text{subject to } \boldsymbol{A}\boldsymbol{v}_{xy} \preceq \boldsymbol{b}. \tag{6.24}$$

Since

$$\det(\boldsymbol{Q}_{iw}) = 4\lambda_1\lambda_2 + 4i_{xu}^2 i_{xl}^2 \lambda_3\lambda_4 + i_x^2(\lambda_1\lambda_3 + \lambda_2\lambda_4) + 4i_{circ,x}^2(\lambda_1\lambda_4 + \lambda_2\lambda_3) > 0. \tag{6.25}$$

The optimization problem (6.24) is a positive-definite quadratic programming problem as (6.18).

6.2 Solving for Arm Voltage References using Quadratic Programming

6.2.1 Rigorous solution

Solution of J_i

As mentioned above, the global solution of the unconstrained version of (6.18) can be obtained as (v_{xu_0}, v_{xl_0}) determined from (6.13). As an equivalent measure, (v_{xu_0}, v_{xl_0}) can be obtained from

$$\nabla J_i(\boldsymbol{v}_{xy\_0}) = 2(\boldsymbol{Q_i}\boldsymbol{v}_{xy\_0} + \boldsymbol{c_i}) = \boldsymbol{0}. \tag{6.26}$$

Considering the constraints, several techniques are available such as the active-set, interior-point or first-order methods, which normally require multiple steps of iterations and/or solutions of a linear system of equations [104]. Since the feasible set of (6.18) is only two-dimensional, the solution can be derived explicitly from geometrical interpretation.

According to the constraints of (6.18), the Euclidean plane of (v_{xu}, v_{xl}) can be divided into 9 regions as shown in Fig. 6.2. Apparently (v_{xu_0}, v_{xl_0}) is not the solution of (6.18) when it falls outside region I (the feasible region). In that case, the optimization problem (6.18) is equivalent to looking for the first point in region I that touches the elliptical contour lines expanding from the center (v_{xu_0}, v_{xl_0}). To solve (6.18), the 9 regions shown in Fig. 6.2 can be divided into three types: I, II and III. For each group, the procedures of obtaining the solution are explained as follows:

1. (v_{xu_0}, v_{xl_0}) falls into region I:
   In this case, the solution of (6.18) is (6.13), as shown in Fig. 6.2.
2. (v_{xu_0}, v_{xl_0}) falls into region II:
   Region II-1 is studied here as an example because the other three regions (II-2,3,4)

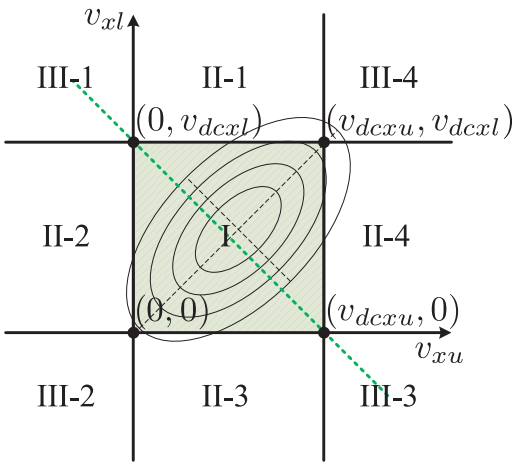


Figure 6.2 Geometrical interpretation: 9 regions where the unconstrained solutions fall.

are similar. In this situation, the optimum of (6.18) lies on segment AB and can be divided into three cases as illustrated in Fig. 6.3.

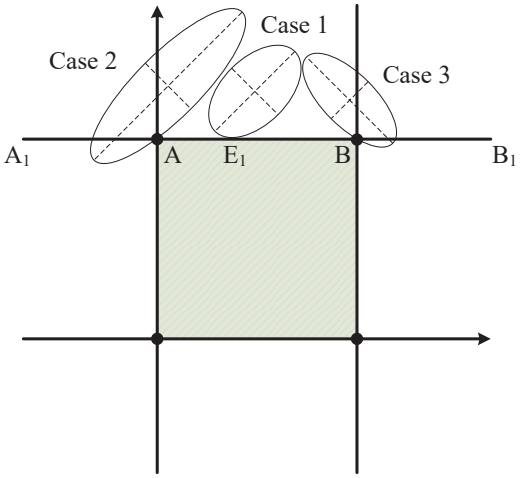


Figure 6.3 Solution for Regions II.

Firstly, the point E_1 on the segment A_1B_1 that first touches the expanding contours (i.e., the tangent point) is obtained by solving

$$\left.\frac{\partial J_i}{\partial v_{xu}}\right|_{v_{xl\_E1}=v_{dcxl}} = 2(q_{i1}v_{xu\_E1} + q_{i2}v_{dcxl} + c_{i1}) = 0 \tag{6.27}$$

leading to

$$v_{xu\_E1} = -\frac{q_{i2}V_{dcxl} + c_{i1}}{q_{i1}} \tag{6.28}$$

which specifies the coordinate of E_1 as (v_{xu_E1}, v_{dcxl}). Then, the solution of (6.18) can be achieved as follows:

a) Case 1: if E_1 is on AB ($0 \leq v_{xu\_E1} \leq v_{dcxu}$), the solution is E1.

b) Case 2: if E_1 is on AA_1 ($v_{xu\_E1} < 0$), the solution is A.

c) Case 3: if E_1 is on BB_1 ($v_{xu\_E1} > v_{dcxu}$), the solution is B.

3. (v_{xu_0}, v_{xl_0}) falls into region III:
Region III-1 is studied here as an example because the other three regions (III-2,3,4) are similar. In this situation, the optimum of (6.18) lies on segment AB or AC and can be divided into five cases as illustrated in Fig. 6.4.

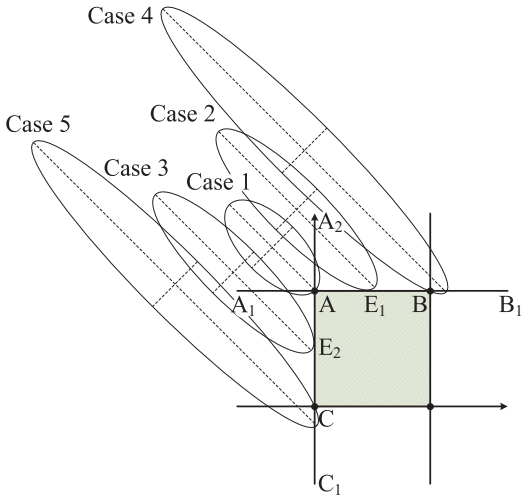


Figure 6.4 Solution for Regions III.

Firstly, the tangent points on the line A_1B_1 and A_2C_1 that first touch the expanding contour lines are obtained as E_1 and E_2 in a similar manner with the case of region II. Then, the solution of (6.18) can be achieved as follows:

a) Case 1: if E_1 is on AA_1 and E_2 is on AA_2, the solution is A.

b) Case 2: if E_1 is on AB, the solution is E_1.

c) Case 3: if E_2 is on AC, the solution is E_2.

d) Case 4: if E_1 is on BB_1, the solution is B.

e) Case 5: if E_2 is on CC_1, the solution is C.

Solution of J_{iw}

The solution of (6.24) can be obtained in a similar manner since it presents an objective function with the same constraints and structure introduced in (6.18). Similar to (6.26), the global optimal solution (without constraints) should satisfy

$$\nabla J_{iw}(\boldsymbol{v}_{xy\_0}) = 2(\boldsymbol{Q}_{iw}\boldsymbol{v}_{xy\_0} + \boldsymbol{c}_{iw}) = \mathbf{0} \tag{6.29}$$

leading to

$$\boldsymbol{v}_{xy\_0} = \begin{bmatrix} v_{xu\_0} & v_{xl\_0} \end{bmatrix}^T = -\boldsymbol{Q}_{\boldsymbol{iw}}^{-1}\boldsymbol{c}_{iw}. \tag{6.30}$$

Then, the procedures described above for solving (6.18) can be repeated for (6.24).

Complete solutions

The rigorous solutions of (6.18)/(6.24) are provided in the Table 6.1 (for region I and II) and Table 6.2 (for region III), where the corresponding subscript of *i*/*iw* will be added to the related variables depending on the applied cost function.

Table 6.1 Proposed rigorous solutions of (6.18)/(6.24) in region I and II.

Region of (v_{xu_0}, v_{xl_0})	Coordinates of E_1,E_2	Case	If	Solution
I	-	-	-	(v_{xu_0}, v_{xl_0})
II-1	$E_1(-\frac{q_2 v_{dcxl}+c_1}{q_1}, v_{dcxl})$	1	$0 \le v_{xu\_E1} \le v_{dcxu}$	(v_{xu_E1}, v_{dcxl})
		2	$v_{xu\_E1} < 0$	$(0, v_{dcxl})$
		3	$v_{xu\_E1} > v_{dcxu}$	(v_{dcxu}, v_{dcxl})
II-2	$E_2(0, -\frac{c_2}{q_3})$	1	$0 \le v_{xl\_E2} \le v_{dcxl}$	$(0, v_{xl\_E2})$
		2	$v_{xl\_E2} < 0$	$(0,0)$
		3	$v_{xl\_E2} > v_{dcxl}$	$(0, v_{dcxl})$
II-3	$E_1(-\frac{c_1}{q_1}, 0)$	1	$0 \le v_{xu\_E1} \le v_{dcxu}$	$(v_{xu\_E1}, 0)$
		2	$v_{xu\_E1} < 0$	$(0,0)$
		3	$v_{xu\_E1} > v_{dcxu}$	$(v_{dcxu}, 0)$
II-4	$E_2(v_{dcxu}, -\frac{q_2 v_{dcxu}+c_2}{q_3})$	1	$0 \le v_{xl\_E2} \le v_{dcxl}$	(v_{dcxu}, v_{xl_E2})
		2	$v_{xl\_E2} < 0$	$(v_{dcxu}, 0)$
		3	$v_{xl\_E2} > v_{dcxl}$	(v_{dcxu}, v_{dcxl})

In terms of implementation, the above-described scheme of region assignation and solution determination can be well designed to minimize the involved calculation cost. The corresponding flowchart with the least possible calculation is outlined in Fig. 6.5.

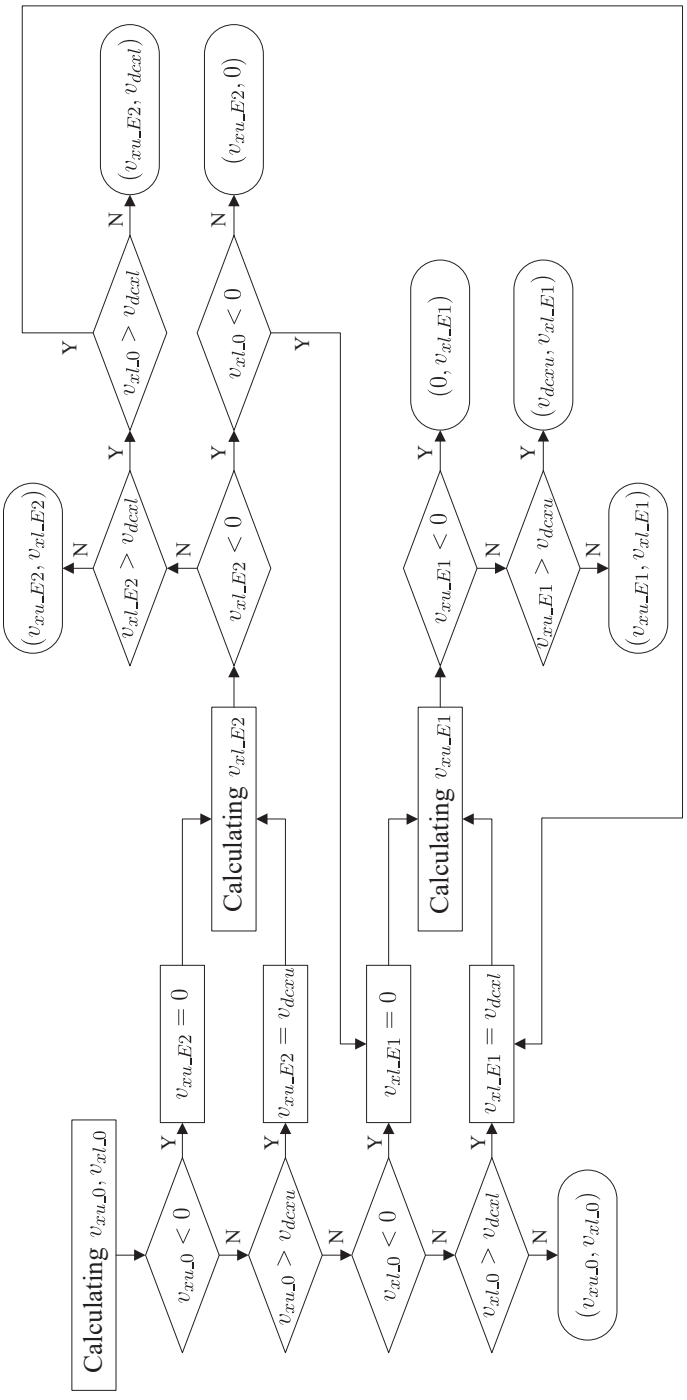


Figure 6.5 Flowchart of region-search and solution-determination scheme.

Table 6.2 Proposed rigorous solutions of (6.18)/(6.24) in region III.

Region of (v_{xu_0},v_{xl_0})	Coordinates of E_1,E_2	Case	If	Solution
III-1	$E_1(-\frac{q_2 v_{dcxl}+c_1}{q_1},v_{dcxl})$ $E_2(0,-\frac{c_2}{q_3})$	1	$v_{xu\_E1}<0$ $v_{xl\_E2}>v_{dcxl}$	$(0,v_{dcxl})$
		2	$0\le v_{xu\_E1}\le v_{dcxu}$	(v_{xu_E1},v_{dcxl})
		3	$0\le v_{xl\_E2}\le v_{dcxl}$	$(0,v_{xl\_E2})$
		4	$v_{xu\_E1}>v_{dcxu}$	(v_{dcxu},v_{dcxl})
		5	$v_{xl\_E2}<0$	$(0,0)$
III-2	$E_1(-\frac{c_1}{q_1},0)$ $E_2(0,-\frac{c_2}{q_3})$	1	$v_{xu\_E1}<0$ $v_{xl\_E2}<0$	$(0,0)$
		2	$0\le v_{xu\_E1}\le v_{dcxu}$	$(v_{xu\_E1},0)$
		3	$0\le v_{xl\_E2}\le v_{dcxl}$	$(0,v_{xl\_E2})$
		4	$v_{xu\_E1}>v_{dcxu}$	$(v_{dcxu},0)$
		5	$v_{xl\_E2}>v_{dcxl}$	$(0,v_{dcxl})$
III-3	$E_1(-\frac{c_1}{q_1},0)$ $E_2(v_{dcxu},-\frac{q_2 v_{dcxu}+c_2}{q_3})$	1	$v_{xu\_E1}>v_{dcxu}$ $v_{xl\_E2}<0$	$(v_{dcxu},0)$
		2	$0\le v_{xu\_E1}\le v_{dcxu}$	$(v_{xu\_E1},0)$
		3	$0\le v_{xl\_E2}\le v_{dcxl}$	(v_{dcxu},v_{xl_E2})
		4	$v_{xu\_E1}<0$	$(0,0)$
		5	$v_{xl\_E2}>v_{dcxl}$	(v_{dcxu},v_{dcxl})
III-4	$E_1(-\frac{q_2 v_{dcxl}+c_1}{q_1},v_{dcxl})$ $E_2(v_{dcxu},-\frac{q_2 v_{dcxu}+c_2}{q_3})$	1	$v_{xu\_E1}>V_{dc}$ $v_{xl\_E2}>V_{dc}$	(v_{dcxu},v_{dcxl})
		2	$0\le v_{xu\_E1}\le v_{dcxu}$	(v_{xu_E1},v_{dcxl})
		3	$0\le v_{xl\_E2}\le v_{dcxl}$	(v_{dcxu},v_{xl_E2})
		4	$v_{xu\_E1}<0$	$(0,v_{dcxl})$
		5	$v_{xl\_E2}<0$	$(v_{dcxu},0)$

6.2.2 Simplified solution

Although the rigorous procedures do not involve complex calculations, (6.18) and (6.24) can be solved in a simpler manner to accelerate the implementation. During normal operation of the MMC, the sum of arm voltages of each phase should always be kept close to the DC-voltage as

$$v_{xu}+v_{xl}\approx V_{dc} \tag{6.31}$$

in order to avoid generating high circulating current. Thus, all (v_{xu_0},v_{xl_0}) should fall close to the diagonal line shown in Fig. 6.2 (the green dotted line) even if they are outside region I. In addition, the contour lines of the cost function are normally not extremely

long-and-narrow. Considering the above factors, a simplified solution of (6.18) and (6.24) can be obtained by simply passing the unconstrained solution through a saturation block as

$$v_{xy}^{*} = \begin{cases} 0 & v_{xy\_0} < 0 \\ v_{xy\_0} & 0 \leq v_{xy\_0} \leq v_{dcxy} \\ v_{dcxy} & v_{xy\_0} > v_{dcxy} \end{cases} \tag{6.32}$$

which is equivalent to the rigorous solution with $\lambda_1 = \lambda_2$ and $\lambda_3 = \lambda_4 = 0$, forcing the elliptic contour lines mentioned above to evolve into circular contour lines.

6.3 Determination of Arm Voltage Level and Gate Signals

From the references of arm voltages (denoted as v_{xy}^{*}) obtained from the proposed method, the SM gate signals are determined applying a specific modulation method, such as the phase-shift/level-shift PWM or the NLC. Since the objective of this thesis is to determine the optimal arm voltage level of the MMC, the VRLC scheme is adopted. It is worth noting that if J_i is employed without arm-energy regulating terms, $v_{dcxy} = V_{dc}$ has to be adopted as indirect capacitor voltage regulation for stability [63].

To facilitate the understanding, the above concept is illustrated in Fig. 6.6. The whole feasible region is divided by $(N+1)^2$ candidates into N^2 units. In the case of Fig. 6.6a, $v_{dcxy} = V_{dc}$ is adopted for normalization of v_{xy}^{*} and thus each unit is a square. In addition, J_i is adopted as the cost function leading to an angle of $\pi/4$ between the major/minor axis of the contour lines and the v_{xy} axis as inferred from (6.11) and (6.12). Therefore, it can be deduced that in this case, the final solution of N_{xy}^{*} can be obtained by just evaluating the four vertices of the unit where the unconstrained solution (the center of the elliptical contour lines) falls. The optimal candidate is marked by the red-star icon. It is important to mention that the optimal candidate obtained by the proposed technique is identical to that determined by the conventional MPC scheme [34], which however has to evaluate all the $(N+1)^2$ possible candidates.

In the case of Fig. 6.6b, the SM capacitor voltages are used for normalization of v_{xy}^{*}, and the N^2 units are thus rectangular but not necessarily square. In addition, J_{iw} is adopted as the cost function (with $\lambda_{3,4} \neq 0$), making the major/minor axis of the contour lines form an angle different from $\pi/4$ with the v_{xy} axis. In this case, the refined four-candidate-evaluation scheme adopted by the VRLC technique may not be applicable, and the solution may be outside the unit as shown in Fig. 6.6b.

In a real MMC implementation, however, $v_{dcxu} \approx v_{dcxl} \approx V_{dc}$ since the capacitor voltage ripples should be much lower than V_{dc}. Additionally, the incorporation of J_w for arm energy regulation is auxiliary and should not change the slope of the major/axis (of the contour lines) to a large extent. Therefore, the assumption of Fig. 6.6a can be made and the VRLC technique can be applied without sacrificing performance compared with the original method evaluating all $(N+1)^2$ candidates [34].

The last step is to select the individual switched-on SMs within each arm. The conventional sorting scheme [18] is employed to undertake the SM-capacitor-voltage-balancer (SM-CVB) task.

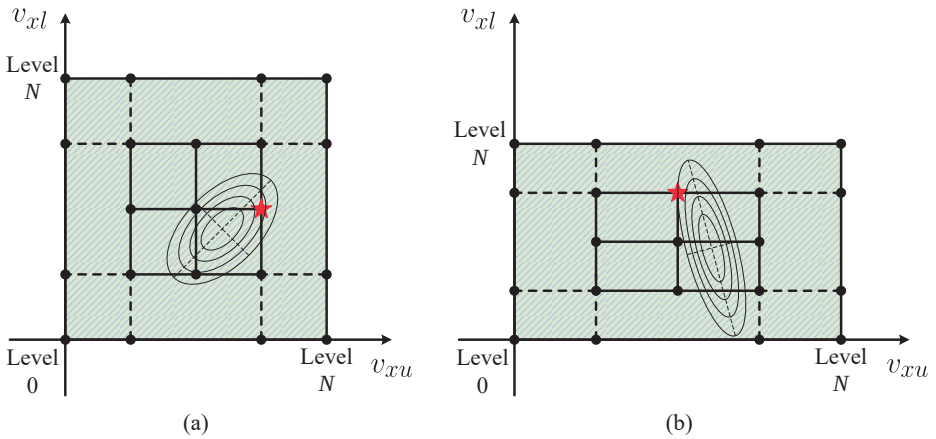


Figure 6.6 Determination of optimal arm voltage levels of (a) a normal case. (b) an abnormal case.

The entire control scheme of phase-x is outlined in Fig. 6.7, which starts from a set of given references since their determination is not the focus of this thesis. For a specified application, the proposed method can be easily integrated by simply introducing the corresponding outer-loop controllers that lead to the phase-current references i_x^*, such as the speed/torque and flux controllers in motor drive applications, active and reactive power controllers in grid-connected applications, etc. A detailed review of outer-loop-controller design can be found in [16]. In terms of the setting of circulating current reference $i_{circ,x}^*$, $i_{dc}/3$ or its DC component (determined based on the power balance of the MMC between its AC side and DC side) is commonly adopted [34, 65]. In addition, some harmonics can be included for various purposes [105]. For further enhancing the regulation of SM capacitor voltages, $i_{circ,x}^*$ can be given by extra arm voltage controllers [90].

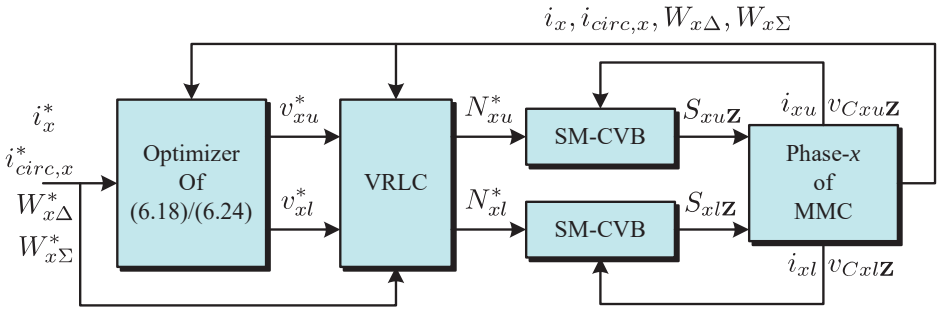


Figure 6.7 Block diagram of the entire proposed method ($\mathrm{Z} = \{1,2,...,N\}$).

The proposed technique can also be incorporated into abnormal operations. As an example, in case of unbalanced grid conditions, negative-sequence component needs to

be included in i_x^* to maintain a constant active- and reactive-power transfer and $i_{circ,x}^*$ is recommended to be set as a pure DC value (instead of $i_{dc}/3$ which contains ripples) for the regulation of zero-sequence and unbalanced circulating current [62, 88]. In addition, another issue in this scenario is that the common-mode voltage of the AC-side neutral point has to be considered in the phase-current model (2.5).

Remark: Since only four candidates are evaluated per phase per sampling period (regardless of N), the proposed method presents a significant advantage in terms of computational burden compared with the conventional FCS-MPC schemes which evaluate a great number of (at least proportional to N) candidates [34, 62–65]. Taking into account the calculation of v_{xy_0}, the worst-case implementation of Fig. 6.5 (both v_{xu_E1} and v_{xl_E2} are calculated) encompasses operations of 5 additions/subtractions, 8 multiplications, 4 divisions and 7 value comparisons. Additionally, every single evaluation of the cost function encompasses operations of 5 additions/subtractions, 8 multiplications and 1 value comparison. Thus, the proposed approach achieves much lower computational cost compared with the exhaustive MPC method. This advantage is achieved even if the MMC has a reduced number of SMs and becomes a critical issue when the number of SMs is large.

6.4 Experimental Analysis

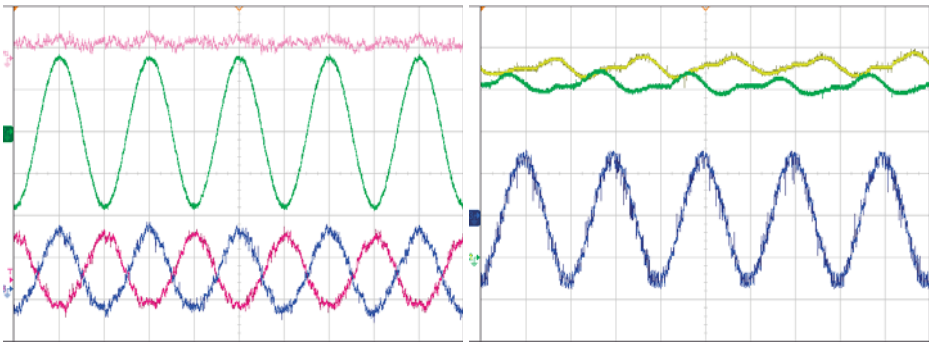
To evaluate the performance of the proposed method, the three-phase MMC setup (details on the MMC setup and control implementation are provided in Appendix A) is employed to conduct the experimental tests. All system parameters are the same as chapter 3 as summarized in Table 3.1.

6.4.1 Steady-state performance

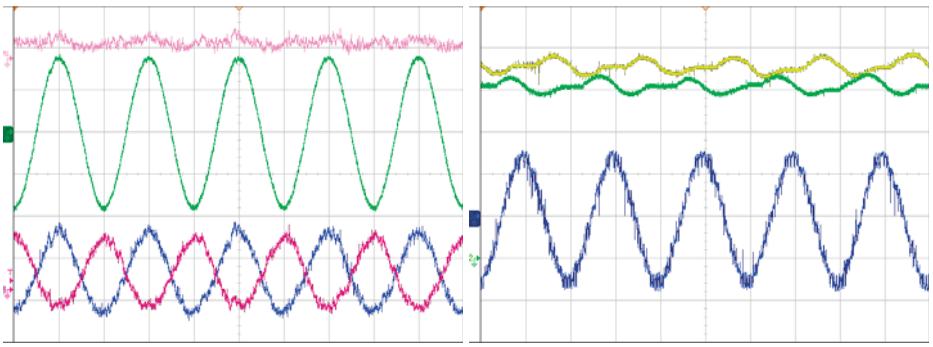
The steady-state tests are evaluated first. As chapter 3, i_x^* is assigned a balanced three-phase sinusoidal waveform with peak value of 3.7 A. $i_{circ,x}^*$ is set as a constant value of 0.86 A, which is determined manually (ideal DC reference [62] plus a slight adjustment accounting for the converter losses) instead of using a total-arm-energy controller [54] in order to observe the current tracking performance. $W_{x\Delta}^*$ is set as zero and $W_{x\Sigma}^*$ is set as $CN(V_{dc}/N - 0.8)^2$ considering the influence of IGBT voltage drop as 0.8 V.

The performance of the proposed techniques including both the rigorous and simplified solutions is shown in Fig. 6.8 and Fig. 6.9, while the emphasis is given to phase-a. For comparative purposes, the conventional FCS-MPC method [34] is also tested as an optimal-performance reference since it evaluates all $(N+1)^2$ insertion-index combinations in each phase. All tests in Fig. 6.8 evaluate the cost function J_i with $\lambda_1 = 1$, $\lambda_2 = 0.25$ while adopting $v_{dcxy} = V_{dc}$ for stability (though a perfect regulation of arm energy is not guaranteed as shown in the unbalanced capacitor voltage waveforms), and those in Fig. 6.9 evaluate the cost function J_{iw} with $\lambda_1 = 1$, $\lambda_2 = 0.25$, $\lambda_3 = 1 \times 10^{-3}$, $\lambda_4 = 1 \times 10^{-4}$.

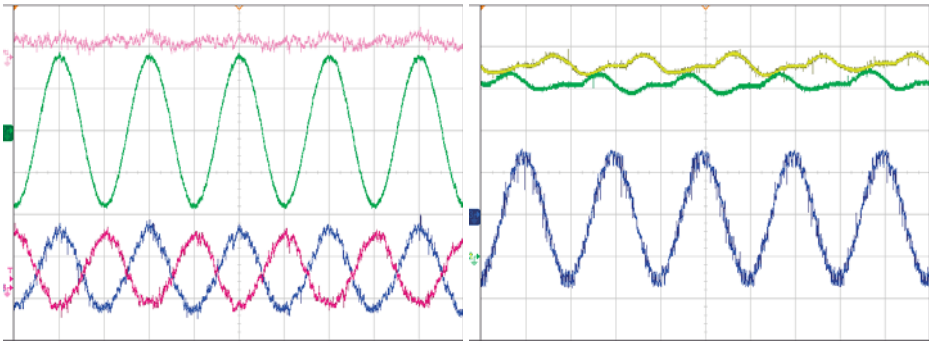
It can be observed that in both groups of tests, the proposed methods (both the rigorous and simplified solutions) exhibit similar performance with the conventional FCS-MPC method in terms of the phase current quality, circulating current ripple, and the waveforms of phase voltage and capacitor voltages. For a quantitative comparison, the THD (%, up to the 50th harmonic) of the phase current, the RMS value (A) of the circulating current



(a) Conventional method. **(b)** Conventional method.

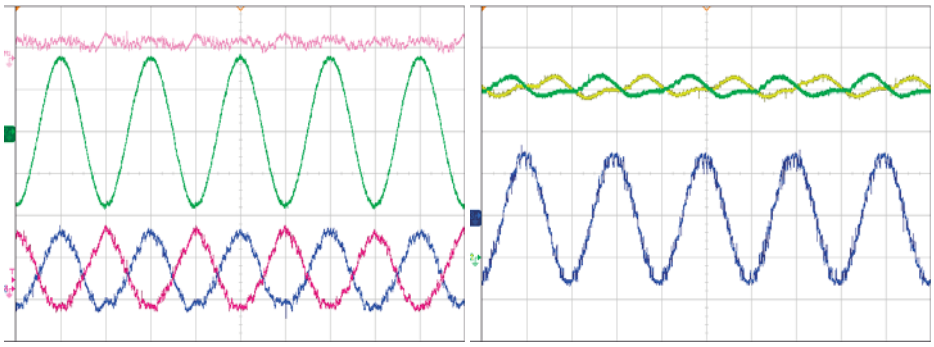


(c) Rigorous solution. **(d)** Rigorous solution.

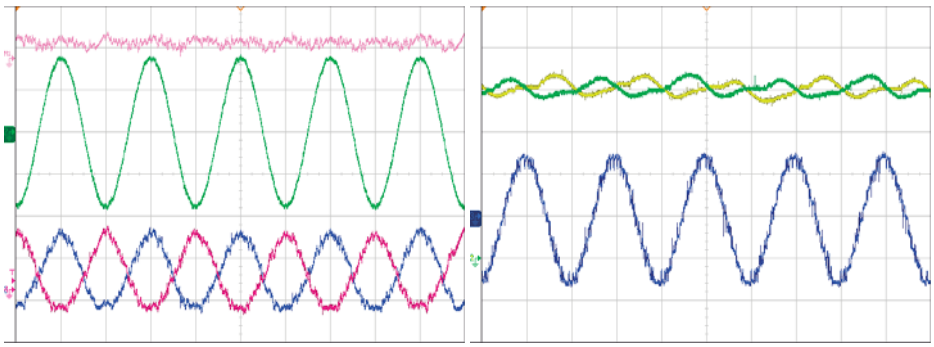


(e) Simplified solution. **(f)** Simplified solution.

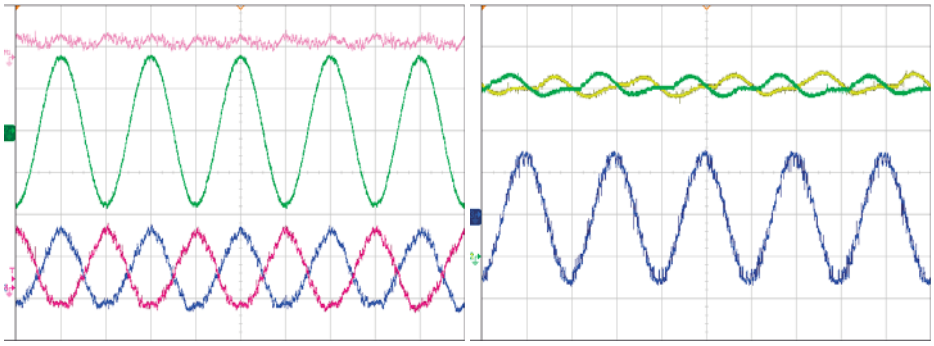
Figure 6.8 Steady-state performance of different methods using J_i (with $v_{dcxy} = V_{dc}$): (a)(c)(e) show i_a (green, 2.00 A/), $i_{circ,a}$ (pink, 2.00 A/), i_{au} (blue, 2.00 A/), i_{al} (red, 2.00 A/); (b)(d)(f) show v_{Cau2} (yellow, 10.0 V/), v_{Cal2} (green, 10.0 V/), v_a (blue, 50.0 V/); time (10.00 ms/).



(a) Conventional method. **(b)** Conventional method.



(c) Rigorous solution. **(d)** Rigorous solution.



(e) Simplified solution. **(f)** Simplified solution.

Figure 6.9 Steady-state performance of different methods using J_{iw}: (a)(c)(e) show i_a (green, 2.00 A/), $i_{circ,a}$ (pink, 2.00 A/), i_{au} (blue, 2.00 A/), i_{al} (red, 2.00 A/); (b)(d)(f) show v_{Cau2} (yellow, 10.0 V/), v_{Cal2} (green, 10.0 V/), v_a (blue, 50.0 V/); time (10.00 ms/).

ripple, and the average switching frequency (Hz) of all the SMs of phase-a applying the different methods are summarized in Table 6.3. More tests with different weighting factors are added for a more complete analysis. In all cases, both proposed solutions present almost identical results to the conventional exhaustive FCS-MPC method.

Table 6.3 Summary of steady-state performance of different methods in experimental tests.

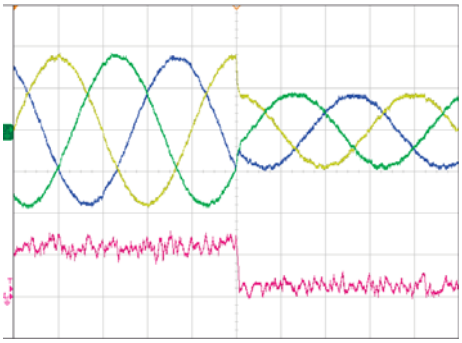
Cost function		J_i	J_{iw}		
Weighting factors		$\lambda_1 = 1$	$\lambda_1 = 1$ $\lambda_3 = 1 \times 10^{-3}$ $\lambda_4 = 1 \times 10^{-4}$		
		$\lambda_2 = 0.25$	$\lambda_2 = 0.25$	$\lambda_2 = 1$	$\lambda_2 = 4$
Conventional method	THD	1.81	1.57	2.02	2.87
	RMS	0.190	0.177	0.131	0.126
	f_{sw}	1196	1070	1081	1179
	$\boldsymbol{t}_{ex}$	**4.32**	**4.34**	**4.35**	**4.36**
Rigorous solution	THD	1.81	1.55	2.02	2.92
	RMS	0.187	0.175	0.130	0.123
	f_{sw}	1197	1069	1082	1180
	$\boldsymbol{t}_{ex}$	**1.49**	**1.50**	**1.49**	**1.49**
Simplified solution	THD	1.80	1.53	2.06	2.88
	RMS	0.192	0.173	0.126	0.126
	f_{sw}	1199	1069	1080	1178
	$\boldsymbol{t}_{ex}$	**1.45**	**1.44**	**1.45**	**1.45**

6.4.2 Dynamic response

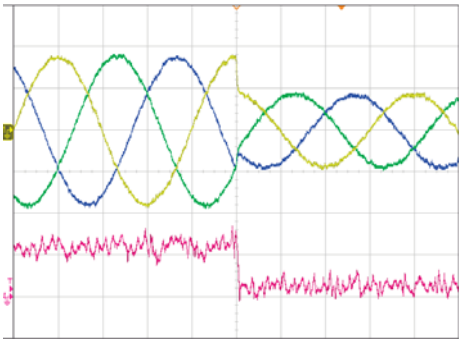
The dynamic performance of the above-mentioned methods is summarized in Fig. 6.10 (J_i) and Fig. 6.11 (J_{iw}). In the transient, the amplitude of i_x^* is reduced to half (1.85 A) and $i_{circ,x}^*$ is reduced to 0.215 A correspondingly. Fast dynamics in terms of phase currents and circulating current (reflected by the DC-link current i_{dc}) are achieved in all tests. Similar to the steady-state tests, both proposed solutions present similar results with the conventional exhaustive control scheme.

6.4.3 Computational burden analysis

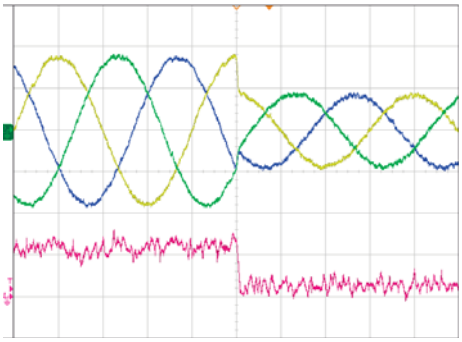
It is important to highlight that in terms of complexity, the proposed solutions involve much less computational burden than the conventional FCS-MPC scheme. The execution time (μs) of the determination of insertion indexes (neglecting the common part of the



(a) Conventional method.

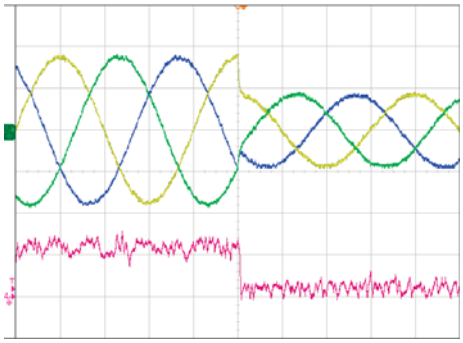


(b) Rigorous solution.

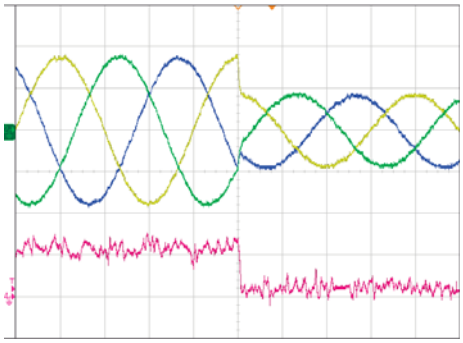


(c) Simplified solution.

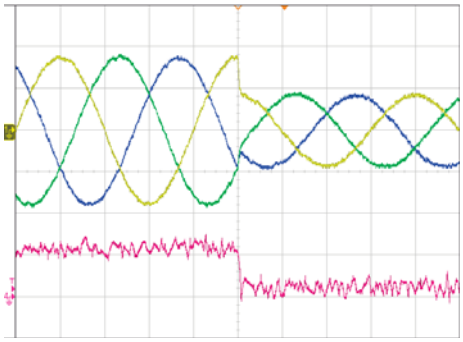
Figure 6.10 Dynamic performance of different methods using J_i (with $v_{dcxy} = V_{dc}$): i_a (yellow, 2.00 A/), i_b (green, 2.00 A/), i_c (blue, 2.00 A/), i_{dc} (red, 2.00 A/); time (5.000 ms/).



(a) Conventional method.



(b) Rigorous solution.



(c) Simplified solution.

Figure 6.11 Dynamic performance of different methods using J_{iw}: i_a (yellow, 2.00 A/), i_b (green, 2.00 A/), i_c (blue, 2.00 A/), i_{dc} (red, 2.00 A/); time (5.000 ms/).

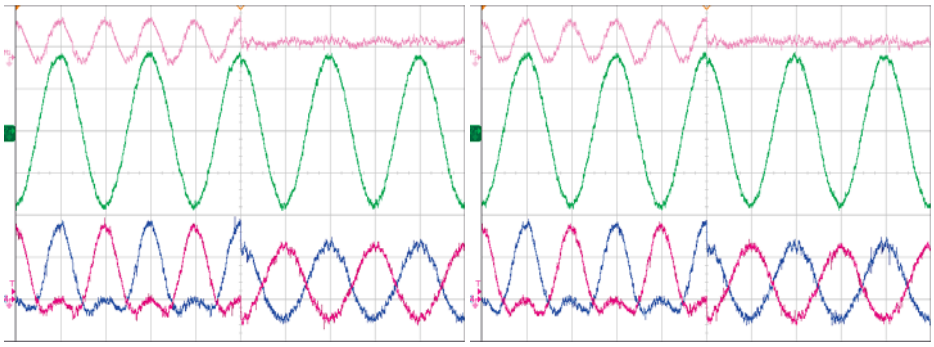
three methods such as calculating the matrix of cost function, delay compensation, etc.) of different tests are summarized in Table 6.3. Both proposed solutions present much lower computational cost than the conventional exhaustive technique, which coincides with the analysis of calculation time in section IV. In addition, it is important to notice that the proposed rigorous solution presents only slightly higher calculation than the simplified solution. In any case, the potential reduction of the computational burden of both proposed methods becomes significant considering the real MMC applications with much higher number of SMs. This would permit to increase the sampling frequency of the MMC leading to improved output waveform quality. Also, it would permit to define more complex cost functions including extra control terms to improve the MMC performance.

6.4.4 Advantage of rigorous solution

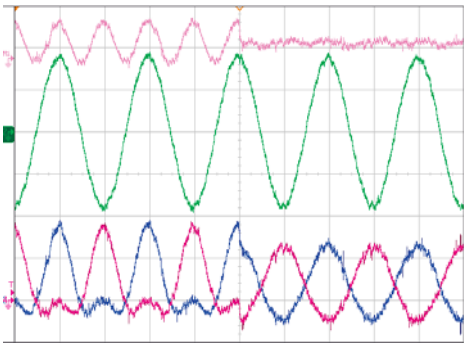
In all the tests above, both the rigorous and simplified solutions show a similar behavior. However, in certain conditions where the transient of circulating current is dramatic, the advantages of the rigorous solution can be observed. An example of harmonic injection of circulating current is investigated. Fig. 6.12 shows the performances of different methods with J_{iw} ($\lambda_1 = 1$, $\lambda_2 = 4$, $\lambda_3 = 5 \times 10^{-3}$, $\lambda_4 = 1 \times 10^{-3}$). A negative-sequence second harmonic is injected in the circulating current, which is eliminated from $i^*_{circ,x}$ during the transient. In steady state, all the three methods exhibit similar quality of circulating current injection. In the transient, all cases show fast dynamic, while a slightly higher distortion of i_a can be observed in Fig. 6.12a and Fig. 6.12b. To further investigate the transient, experimental data from dSPACE (ControlDesk) are employed and the insertion indexes along with the circulating current in reaction to the transient are illustrated in Fig. 6.13. From the zoom-in figures, it can be clearly observed that the rigorous solution and the conventional exhaustive FCS-MPC show faster dynamic than the proposed simplified solution. In Fig. 6.13a and Fig. 6.13b N^*_{au} increases one extra level compared with the result in Fig. 6.13c to adapt quickly to the transient. Thus, the proposed rigorous solution exhibits better performance than the simplified solution since the circulating current tracking is put in the first place.

6.4.5 Visualization of unconstrained solutions

For visualization, the distribution of all (v_{au_0}, v_{al_0}) of the proposed rigorous solution during different tests are illustrated in Fig. 6.14. It can be observed in Fig. 6.14a that all solutions fall close to the diagonal line in the steady state, including those outside region I. Thus, the weighting factors have little impact on the solution of v^*_{xy}. However, during transient of phase current and circulating current, as shown in Fig. 6.14b and Fig. 6.14c respectively, several outliers in region II and III appear which reflect the attempt of the system to adapt to the new reference during the transient. Thus, the proposed rigorous solution should be adopted as the preferred solution for a better dynamic and safer operation.

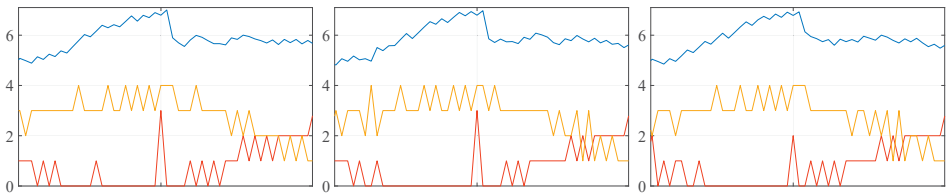


(a) Conventional method. **(b)** Rigorous solution.



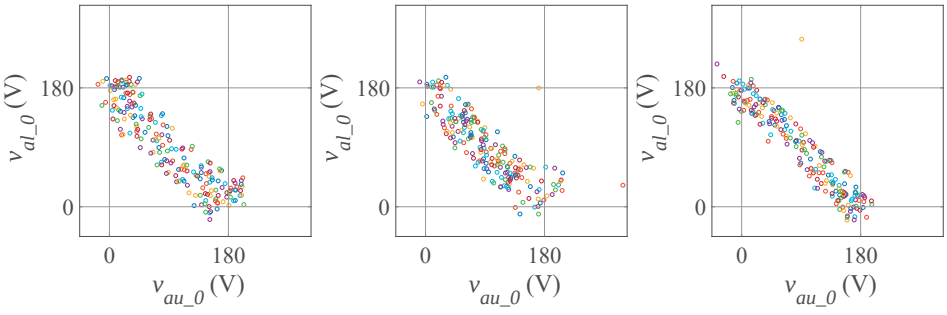
(c) Simplified solution.

Figure 6.12 Performance evaluation of different methods (using J_{iw}) in the circulating-current-injection tests: $i_{circ,a}$ (pink, 2.00 A/), i_a (green, 2.00 A/), i_{au} (blue, 2.00 A/), i_{al} (red, 2.00 A/); time (10.00 ms/).



(a) Conventional method. **(b)** Rigorous solution. **(c)** Simplified solution.

Figure 6.13 Zoom-in (0.01s) of the transient of Fig. 6.12 using the data from ControlDesk: $i_{circ,a}$ (blue), N^*_{xu} (red), N^*_{xl} (yellow).



(a) Test of Fig. 6.9(c). **(b)** Test of Fig. 6.11(b). **(c)** Test of Fig. 6.12(b).

Figure 6.14 Distribution of v_{au_0},v_{al_0} during 0.04 s of different tests.

6.5 Simulation Results of an MMC with $N = 200$

To evaluate the validity of the proposed strategy in a real-scale MMC system with large number of voltage levels, a simulation test of a grid-connected MMC with 200 SMs per arm (circuit parameters are almost the same to those summarized in Table 5.1 except for $N = 200$) is conducted with an sampling/control period of $T_s = 0.2$ s. Results are illustrated in Fig. 6.15 in terms of phase currents, circulating currents and phase-a arm energies (represented by total SM-capacitor voltage of arm). Only the rigorous solution with J_{iw} ($\lambda_1 = 1$, $\lambda_2 = 25$, $\lambda_3 = 2 \times 10^{-8}$, $\lambda_4 = 1 \times 10^{-9}$) is investigated since the other two methods (simplified solution and conventional MPC scheme) achieve very similar results and have been fully evaluated in the experimental section.

At first, the system operates smoothly in steady state with high-quality phase current (THD=0.18%), negligible circulating-current ripples and well-regulated arm energy. The converter works in rectifier mode with an active power of 85.5 MW and a reactive power of 0 VA. At 2.005 s, a transient condition is generated by reducing the peak amplitude of phase-current references to half, representing a step change of active-power command. It can be observed that the system presents very high dynamics and all control objectives are well regulated in a fast transition to the new steady state (with a phase-current THD of 0.35%). Thus, the feasibility of the proposed technique in a large-scale MMC is validated. It is worth emphasizing that even for a MMC with such high number of SMs, the proposed MPC technique still requires only 4 cost-function evaluations per phase per control cycle for the determination of arm-voltage levels.

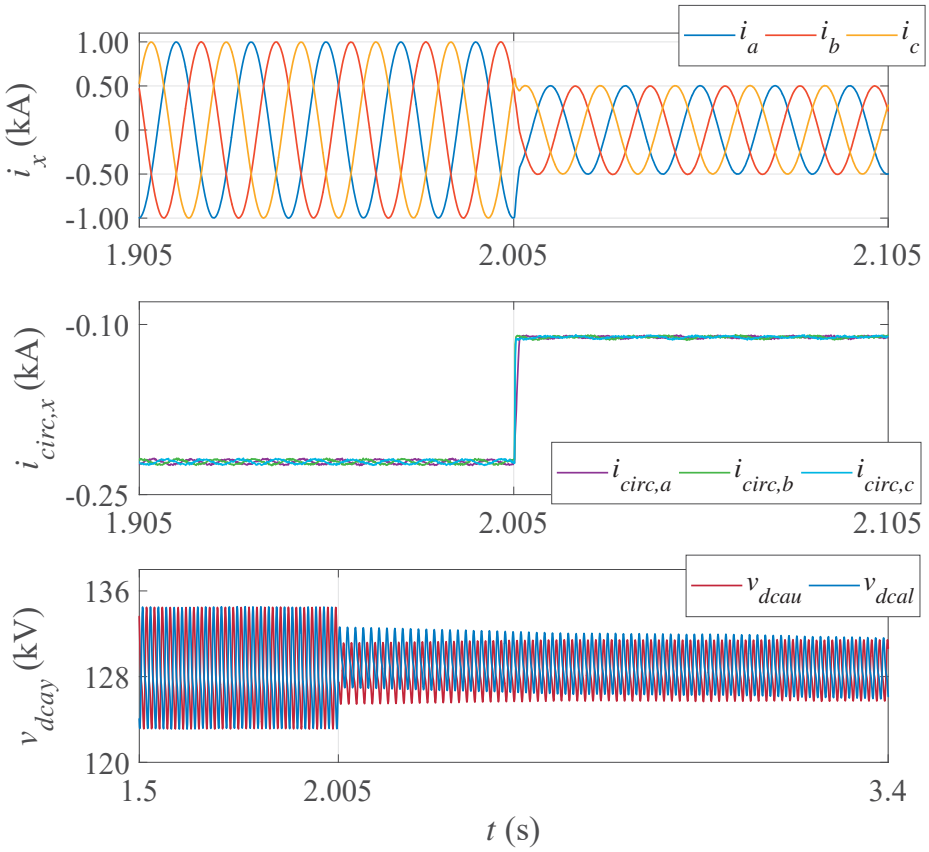


Figure 6.15 Simulation results of a grid-connected MMC in a dynamic test.

7 Conclusion and Future Work

7.1 Conclusion

In this thesis, the MPC technique has been employed to determine the arm voltage levels for an MMC operating as a DC-AC interphase for either grid- or load-connected applications, and the focus has been given to current control performance in terms of phase current and circulating current. To overcome the limitations of conventional MPC techniques regarding high computational cost, a VRLC technique has been proposed which considers only four voltage level combinations per phase per control period, regardless of the number of SMs of the MMC, while the SM capacitor voltage balancing is achieved by sorting-and-selecting scheme.

In chapter 3, the VRLC concept has been introduced which applies the floor() or the ceiling() function after normalizing the arm voltage references instead of the round function adopted by the traditional NLC technique, leading to four combinations in each phase which are then evaluated and selected employing the MPC strategy. As a result, the control performance of phase current and circulating current is superior compared with the traditional NLC scheme, while the simplicity in implementation is maintained, which has been verified by experimental results on a three-phase prototype: with the same sampling or switching frequency, the proposed VRLC technique seeks more active voltage level switching and better coordination of different control objectives for an enhanced current regulation with comparative computation complexity.

Then, in chapter 4, the VRLC technique has been generalized as a class of MPC techniques. Different current controllers, namely PI/PR, DB and OL, can be employed for determining arm voltage references, resulting in six feasible implementations of the VRLC-MPC technique. In each phase, the control sets are refined to only four nearest vectors which are subsequently evaluated by a well-defined cost function in the frame of the MPC. The current controllability issue owing to limited number of considered voltage levels and capacitor voltage ripples has been investigated, and the accumulated effect of capacitor voltage ripples on current regulations has been derived with explicit expressions, based on which the current control requirements are analytically provided. Both theoretical analysis and simulation results reveal that for the VRLC and similar MPC techniques with

very reduced control sets, if the number of SMs is not very large such that the current controllability is sufficient, the simpler DB or OL controller can be adopted leading to similar performance with that using PI/PR controller.

On the basis of the proposed analysis of chapter 4, a SM-grouping-based VRLC-MPC strategy has been developed in chapter 5 as a solution to overcome the loss of current controllability in an MMC with large number of SMs, which also brings convenience to system cost reduction and distributed control implementation. The group size has been analyzed as an important parameter with its influence on the performance of the system considering current regulating capability, amplitude of current tracking ripples, computation cost and system complexity, leading to the design principles of the proposed SM grouping scheme. Several simulation results on an MMC system with 128 SMs per arm have validated the effectiveness of the proposed solution.

At last, in chapter 6, a new method has been developed for a fast and effective determination of arm voltage references. Utilizing the predictions based on the discrete system model, the minimization of cost function is transformed into a constrained quadratic programming problem, and the arm voltage references can be obtained analytically following the proposed rigorous routines. Considering normal operation of the MMC, a simplified procedure has also been provided. Compared with the conventional FCS-MPC scheme that considers the entire feasible control set, the proposed method presents almost identical steady-state and dynamic performance but with much lower amount of calculation, as it has been verified by experimental and simulation test results.

In summary, the VRLC-based MPC strategies developed in this thesis open the possibility to apply the MPC methodology to an MMC with large number of SMs, overcoming the limitation of high computational cost without sacrificing performance.

7.2 Future Work

Based on the research results obtained in this thesis, future work of the author can be carried out in the following aspects:

- More in-depth comparison between the VRLC technique and the conventional PWM scheme in medium-low voltage range where both methods present similar switching frequency and comparable complexity in implementation.
- Experimental validation of the current controllability analysis proposed in chapter 4, and its extension to the analysis of other similar methods.
- System design of the SM-grouping scheme proposed in chapter 5, considering imbalanced charging/discharging of individual SM capacitor voltages, possible cost reduction through using lower number of capacitor voltage sensors, etc.
- Application of the PWM technique to accurately generate the arm voltage references determined by the method described in chapter 6, and comparing its performance with the VRLC-based arm voltage approximation.
- Extension of the VRLC-based strategies to specific applications, such as the HVDC, STATCOM, motor drive, etc.

- Application of the proposed techniques to unbalanced grid or load conditions or DC fault conditions.
- Incorporation of more control objectives into the cost function, such as switching frequency, common-mode voltage, etc.
- Extended application of the proposed VRLC methods to other multilevel converter topologies, such as the CHB with large number cells.

Appendix A
Experimental Setup

This appendix gives the related information about the experimental MMC prototype and hardware implementation of the control algorithm.

A.1 MMC Setup

Throughout the thesis, all the experiments are carried out in the three-phase MMC setup shown in Fig. A.1. The inductance value of arm inductors is 15 mH and the capacitance value of SM capacitors is 1 mF. DC-side of the MMC is directed connected to a DC voltage source and the AC-side is fed with a three-phase balanced $R-L$ load. The MMC occupies two cabinets, each contains 12 full-bridge SMs which are arranged into 4 SMs per arm (6 arms). Each SM is configured as half bridge.

A.2 Control Implementation

The dSPACE 1007 is employed for the control of the MMC setup. All the control tasks including the capacitor voltage sorting are implemented by the dSPACE DS1007 PPC processor board. In order to reduce the computational burden, the sorting algorithm is realized in a pseudo-sorting way by comparing those 4 SM capacitor voltages of each arm in two groups and enumerating all the cases. The control method is realized in C language codes. "ControlDesk 5.6" software is employed to realize the real-time control commanding and variable monitoring.

The DS1007 PPC processor board executes the real-time application based on a dual-core Freescale P5020 processor with 2 GHz CPU clock. The dual-core processor allows one to implement a real-time application on one processor core or on both processor cores. The one-core configuration has been adopted by the experiments of this thesis. More details about the processor board can be found in http://www.freescale.com and search for ”P5020”.

The DS2002 Multi-Channel A/D Board is used for receiving the current/voltage measurements from sensors to the dSPACE. The DS2002 Multi-Channel A/D Board provides

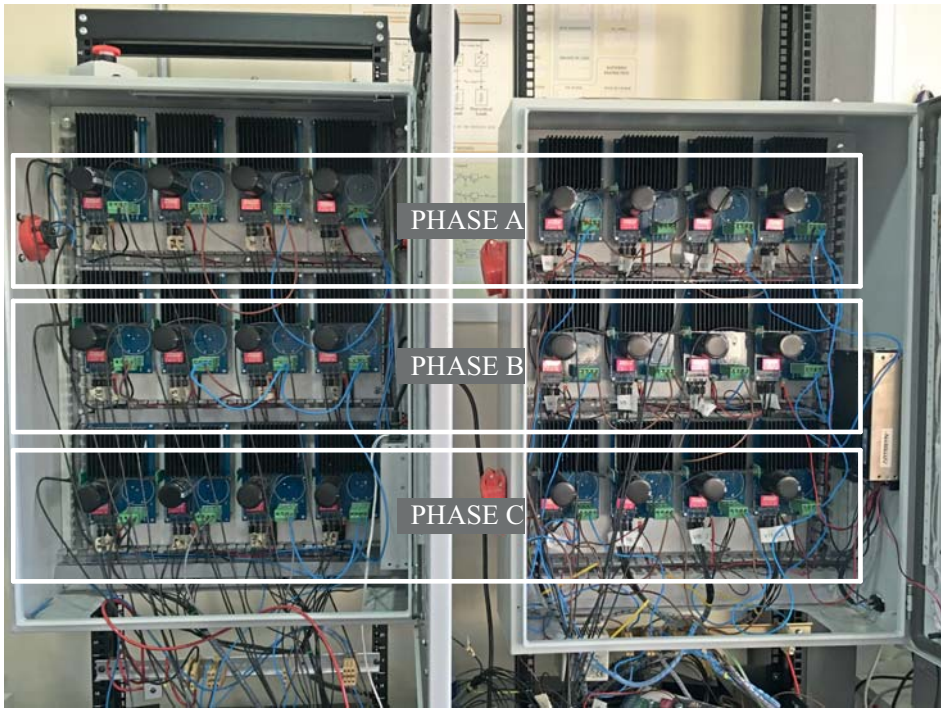


Figure A.1 The experimental setup (left/right cabinet: upper/lower arms)..

two independent A/D converters, each including 16 multiplexed inputs that can be used for conversion of analog signals. 30 of the total 32 channels are occupied for measurements of 24 SM capacitor voltages and 6 arm currents. Each capacitor voltage is scaled down first by a voltage divider circuit (with a scaling factor of 1/40) on the SM board, and then sent via cable to the DS4003 I/O Board after passing through an optical isolation unit.

The DS4003 Digital I/O Board is used for outputting gate signals. The DS4003 Digital I/O Board provides 96 digital I/O lines grouped into three I/O ports of 32 bits, each with handshake and strobe signals. 24 bits are occupied, 1 bit for each SM describing the corresponding switching state (S_{xyz}). In addition, two FPGA boards (one Spartan 3AN and one Spartan 3E) together with two communication boards are employed for generating the pair of complementary gate signals for both IGBTs of the same SM and transforming the gate signals (emitted from the digital I/O board) to optical signals, which are then sent to those cells through optical fibers.

List of Figures

List of Tables

Bibliography

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. Prats, "The age of multilevel converters arrives," *IEEE industrial electronics magazine*, vol. 2, no. 2, 2008.

[2] D. Gielen, F. Boshell, D. Saygin, M. D. Bazilian, N. Wagner, and R. Gorini, "The role of renewable energy in the global energy transformation," *Energy Strategy Reviews*, vol. 24, pp. 38–50, 2019.

[3] K. Riahi, F. Dentener, D. Gielen, A. Grubler, J. Jewell, Z. Klimont, V. Krey, D. McCollum, S. Pachauri, S. Rao *et al.*, "Energy pathways for sustainable development," 2012.

[4] A. Qazi, F. Hussain, N. A. Rahim, G. Hardaker, D. Alghazzawi, K. Shaban, and K. Haruna, "Towards sustainable energy: a systematic review of renewable energy sources, technologies, and public opinions," *IEEE Access*, vol. 7, pp. 63 837–63 851, 2019.

[5] IEA, "Global share of total energy supply by source, 2018, iea, paris," https://www.iea.org/data-and-statistics/charts/global-share-of-total-energy-supply-by-source-2018, 2020.

[6] S. Kouro, J. I. Leon, D. Vinnikov, and L. G. Franquelo, "Grid-connected photovoltaic systems: An overview of recent research and emerging pv converter technology," *IEEE Industrial Electronics Magazine*, vol. 9, no. 1, pp. 47–61, 2015.

[7] F. Blaabjerg and K. Ma, "Wind energy systems," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2116–2131, 2017.

[8] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galván, R. C. PortilloGuisado, M. M. Prats, J. I. León, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: A survey," *IEEE Transactions on industrial electronics*, vol. 53, no. 4, pp. 1002–1016, 2006.

[9] I. Sanz, M. Moranchel, E. J. Bueno, and F. J. Rodriguez, "Analysis of medium voltage modular multilevel converters for facts applications," in *IECON 2016-42nd Annual Conference of the IEEE Industrial Electronics Society*. IEEE, 2016, pp. 6459–6464.

[10] S. Kouro, J. Rodriguez, B. Wu, S. Bernet, and M. Perez, "Powering the future of industry: High-power adjustable speed drive topologies," *IEEE industry applications magazine*, vol. 18, no. 4, pp. 26–39, 2012.

[11] A. Nabae, I. Takahashi, and H. Akagi, "A new neutral-point-clamped pwm inverter," *IEEE Transactions on industry applications*, no. 5, pp. 518–523, 1981.

[12] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Transactions on industrial electronics*, vol. 57, no. 7, pp. 2197–2206, 2009.

[13] T. Meynard and H. Foch, "Multi-level choppers for high voltage applications," *EPE journal*, vol. 2, no. 1, pp. 45–50, 1992.

[14] M. Schweizer and J. W. Kolar, "Design and implementation of a highly efficient three-level t-type converter for low-voltage applications," *IEEE Transactions on Power Electronics*, vol. 28, no. 2, pp. 899–907, 2012.

[15] P. Barbosa, P. Steimer, J. Steinke, M. Winkelnkemper, and N. Celanovic, "Active-neutral-point-clamped (anpc) multilevel converter technology," in *2005 European Conference on Power Electronics and Applications*. IEEE, 2005, pp. 10–pp.

[16] J. I. Leon, S. Vazquez, and L. G. Franquelo, "Multilevel converters: Control and modulation techniques for their operation and industrial applications," *Proceedings of the IEEE*, vol. 105, no. 11, pp. 2066–2081, 2017.

[17] H.-J. Knaak, "Modular multilevel converters and hvdc/facts: A success story," in *Proceedings of the 2011 14th European conference on power electronics and applications*. IEEE, 2011, pp. 1–6.

[18] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Power Tech Conference Proceedings, 2003 IEEE Bologna*, vol. 3. IEEE, 2003, pp. 6–pp.

[19] A. Nami, J. Liang, F. Dijkhuizen, and G. D. Demetriades, "Modular multilevel converters for hvdc applications: Review on converter cells and functionalities," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 18–36, 2014.

[20] M. Espinoza-B, R. Cárdenas, J. Clare, D. Soto-Sanchez, M. Diaz, E. Espina, and C. M. Hackl, "An integrated converter and machine control system for mmc-based high-power drives," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2343–2354, 2018.

[21] A. Marzoughi, R. Burgos, and D. Boroyevich, "Optimum design guidelines for the modular multilevel converter in active front-end applications: Considerations for passive component reduction," *IEEE Power Electronics Magazine*, vol. 5, no. 2, pp. 56–65, 2018.

[22] Z. Gong, X. Wu, P. Dai, and R. Zhu, "Modulated model predictive control for mmc-based active front-end rectifiers under unbalanced grid conditions," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2398–2409, 2019.

[23] S. Kenzelmann, A. Rufer, D. Dujic, F. Canales, and Y. R. De Novaes, "Isolated dc/dc structure based on modular multilevel converter," *IEEE Transactions on power electronics*, vol. 30, no. 1, pp. 89–98, 2014.

[24] X. Zhang and T. C. Green, "The modular multilevel converter for high step-up ratio dc–dc conversion," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 8, pp. 4925–4936, 2015.

[25] T. Soong and P. W. Lehn, "Evaluation of emerging modular multilevel converters for bess applications," *IEEE Transactions on Power Delivery*, vol. 29, no. 5, pp. 2086–2094, 2014.

[26] L. Baruschka and A. Mertens, "Comparison of cascaded h-bridge and modular multilevel converters for bess application," in *2011 IEEE Energy Conversion Congress and Exposition*. IEEE, 2011, pp. 909–916.

[27] G. Zheng, Y. Chen, and Y. Kang, "A modular multilevel converter (mmc) based solid state transformer (sst) topology with simplified energy conversion process and magnetic integration," *IEEE Transactions on Industrial Electronics*, 2020.

[28] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: modular multilevel converter versus cascaded h-bridge solutions," *IEEE Industrial Electronics Magazine*, vol. 10, no. 4, pp. 6–19, 2016.

[29] S. P. Teeuwsen, "Modeling the trans bay cable project as voltage-sourced converter with modular multilevel converter design," in *2011 IEEE Power and Energy Society General Meeting*. IEEE, 2011, pp. 1–8.

[30] A. Dekka, B. Wu, R. L. Fuentes, M. Perez, and N. R. Zargari, "Evolution of topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 4, pp. 1631–1656, 2017.

[31] Siemens, "Principles of modular multilevel converter topology," https://assets.new.siemens.com/siemens/assets/api/uuid:852447ab-debe-4199-843b-4e256a22ddf7/%20GH150M2CWhitePaper.pdf.

[32] ABB, "A new statcom modular multilevel converter technology," https://search.abb.com/library/Download.aspx?DocumentID=9AKK107045A6778&LanguageCode=en&DocumentPartId=&Action=Launch&DocumentRevisionId=A, 2017.

[33] A. Dekka, B. Wu, V. Yaramasu, R. L. Fuentes, and N. R. Zargari, "Model predictive control of high-power modular multilevel converters–an overview," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2018.

[34] M. Vatani, B. Bahrani, M. Saeedifard, and M. Hovd, "Indirect finite control set model predictive control of modular multilevel converters," *IEEE Transactions on Smart Grid*, vol. 6, no. 3, pp. 1520–1529, 2015.

[35] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana, "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," *IEEE transactions on power electronics*, vol. 30, no. 1, pp. 4–17, 2015.

[36] M. A. Perez, J. Rodriguez, E. J. Fuentes, and F. Kammerer, "Predictive control of ac–ac modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 7, pp. 2832–2839, 2011.

[37] M. Glinka and R. Marquardt, "A new ac/ac multilevel converter family," *IEEE Transactions on Industrial Electronics*, vol. 52, no. 3, pp. 662–669, 2005.

[38] M. I. Daoud, A. A. Elserougi, A. M. Massoud, R. Bojoi, A. S. Abdel-Khalik, and S. Ahmed, "Zero-/low-speed operation of multiphase drive systems with modular multilevel converters," *IEEE Access*, vol. 7, pp. 14 353–14 365, 2019.

[39] G. P. Adam and B. W. Williams, "Half-and full-bridge modular multilevel converter models for simulations of full-scale hvdc links and multiterminal dc grids," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 2, no. 4, pp. 1089–1108, 2014.

[40] R. Zeng, L. Xu, L. Yao, and B. W. Williams, "Design and operation of a hybrid modular multilevel converter," *IEEE Transactions on power electronics*, vol. 30, no. 3, pp. 1137–1146, 2014.

[41] D. Karwatzki and A. Mertens, "Generalized control approach for a class of modular multilevel converter topologies," *IEEE Transactions on Power Electronics*, vol. 33, no. 4, pp. 2888–2900, 2017.

[42] M. M. Merlin, T. C. Green, P. D. Mitcheson, D. R. Trainer, R. Critchley, W. Crookes, and F. Hassan, "The alternate arm converter: A new hybrid multilevel converter with dc-fault blocking capability," *IEEE transactions on power delivery*, vol. 29, no. 1, pp. 310–317, 2013.

[43] M. Diaz, R. Cardenas, M. Espinoza, F. Rojas, A. Mora, J. C. Clare, and P. Wheeler, "Control of wind energy conversion systems based on the modular multilevel matrix converter," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8799–8810, 2017.

[44] L. Baruschka and A. Mertens, "A new three-phase ac/ac modular multilevel converter with six branches in hexagonal configuration," *IEEE Transactions on Industry Applications*, vol. 49, no. 3, pp. 1400–1410, 2013.

[45] F. Khera, C. Klumpner, and P. Wheeler, "Experimental validation of a quasi z-source modular multilevel converter with dc fault blocking capability," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 2019.

[46] V. Spudić and T. Geyer, "Model predictive control based on optimized pulse patterns for modular multilevel converter statcom," *IEEE Transactions on Industry Applications*, vol. 55, no. 6, pp. 6137–6149, 2019.

[47] A. F. Cupertino, J. V. M. Farias, H. A. Pereira, S. I. Seleme, and R. Teodorescu, "Comparison of dscc and sdbc modular multilevel converters for statcom application during negative sequence compensation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2302–2312, 2018.

[48] H. Akagi, "Classification, terminology, and application of the modular multilevel cascade converter (mmcc)," *IEEE Transactions on power electronics*, vol. 26, no. 11, pp. 3119–3130, 2011.

[49] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Transactions on industrial electronics*, vol. 53, no. 5, pp. 1398–1409, 2006.

[50] R. Lizana, M. A. Perez, D. Arancibia, J. R. Espinoza, and J. Rodriguez, "Decoupled current model and control of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 9, pp. 5382–5392, 2015.

[51] Q. Song, W. Liu, X. Li, H. Rao, S. Xu, and L. Li, "A steady-state analysis method for a modular multilevel converter," *IEEE Transactions on Power electronics*, vol. 28, no. 8, pp. 3702–3713, 2012.

[52] S. Li, X. Wang, Z. Yao, T. Li, and Z. Peng, "Circulating current suppressing strategy for mmc-hvdc based on nonideal proportional resonant controllers under unbalanced grid conditions," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 387–397, 2015.

[53] Q. Tu, Z. Xu, and J. Zhang, "Circulating current suppressing controller in modular multilevel converter," in *IECON 2010-36th Annual Conference on IEEE Industrial Electronics Society*. IEEE, 2010, pp. 3198–3202.

[54] A. Antonopoulos, L. Angquist, and H.-P. Nee, "On dynamics and voltage control of the modular multilevel converter," in *2009 13th European Conference on Power Electronics and Applications*. IEEE, 2009, pp. 1–10.

[55] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Analysis and operation of modular multilevel converters with phase-shifted carrier pwm," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 268–283, 2015.

[56] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 297–310, 2015.

[57] R. Darus, G. Konstantinou, J. Pou, S. Ceballos, and V. G. Agelidis, "Comparison of phase-shifted and level-shifted pwm in the modular multilevel converter," in *Power Electronics Conference (IPEC-Hiroshima 2014-ECCE-ASIA), 2014 International*. IEEE, 2014, pp. 3764–3770.

[58] J. I. Leon, S. Kouro, L. G. Franquelo, J. Rodriguez, and B. Wu, "The essential role and the continuous evolution of modulation techniques for voltage-source inverters in the past, present, and future power electronics," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 5, pp. 2688–2701, 2016.

[59] L. Angquist, A. Antonopoulos, D. Siemaszko, K. Ilves, M. Vasiladiotis, and H.-P. Nee, "Open-loop control of modular multilevel converters using estimation of stored energy," *IEEE transactions on industry applications*, vol. 47, no. 6, pp. 2516–2524, 2011.

[60] P. M. Meshram and V. B. Borghate, "A simplified nearest level control (nlc) voltage balancing method for modular multilevel converter (mmc)," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 450–462, 2015.

[61] L. Lin, Y. Lin, Z. He, Y. Chen, J. Hu, and W. Li, "Improved nearest-level modulation for a modular multilevel converter with a lower submodule number," *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5369–5377, 2016.

[62] J.-W. Moon, J.-S. Gwon, J.-W. Park, D.-W. Kang, and J.-M. Kim, "Model predictive control with a reduced number of considered states in a modular multilevel converter for hvdc system," *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 608–617, 2015.

[63] F. Zhang, W. Li, and G. Joós, "A voltage-level-based model predictive control of modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 5301–5312, 2016.

[64] P. Guo, Z. He, Y. Yue, Q. Xu, X. Huang, Y. Chen, and A. Luo, "A novel two-stage model predictive control for modular multilevel converter with reduced computation," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2410–2422, 2019.

[65] B. Gutierrez and S.-S. Kwak, "Modular multilevel converters (mmcs) controlled by model predictive control with reduced calculation burden," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 9176–9187, 2018.

[66] F. Deng and Z. Chen, "Voltage-balancing method for modular multilevel converters switched at grid frequency," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 5, pp. 2835–2847, 2014.

[67] K. Ilves, L. Harnefors, S. Norrga, and H.-P. Nee, "Predictive sorting algorithm for modular multilevel converters minimizing the spread in the submodule capacitor voltages," *IEEE Transactions on power electronics*, vol. 30, no. 1, pp. 440–449, 2014.

[68] J. Huang, B. Yang, F. Guo, Z. Wang, X. Tong, A. Zhang, and J. Xiao, "Priority sorting approach for modular multilevel converter based on simplified model predictive control," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4819–4830, 2018.

[69] Y. Jin, Q. Xiao, C. Dong, H. Jia, Y. Mu, B. Xie, Y. Ji, S. K. Chaudhary, and R. Teodorescu, "A novel submodule voltage balancing scheme for modular multilevel cascade converter-double-star chopper-cells (mmcc-dscc) based statcom," *Ieee Access*, vol. 7, pp. 83 058–83 073, 2019.

[70] Z. Li, R. Lizana, S. Sha, Z. Yu, A. V. Peterchev, and S. M. Goetz, "Module implementation and modulation strategy for sensorless balancing in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 9, pp. 8405–8416, 2018.

[71] Y. Deng, Y. Wang, K. H. Teo, M. Saeedifard, and R. G. Harley, "Optimized control of the modular multilevel converter based on space vector modulation," *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 5697–5711, 2017.

[72] M. Aleenejad, H. Mahmoudi, S. Jafarishiadeh, and R. Ahmadi, "Fault-tolerant space vector modulation for modular multilevel converters with bypassed faulty submodules," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2463–2473, 2018.

[73] G. Konstantinou, M. Ciobotaru, and V. Agelidis, "Selective harmonic elimination pulse-width modulation of modular multilevel converters," *IET Power Electronics*, vol. 6, no. 1, pp. 96–107, 2013.

[74] A. Perez-Basante, S. Ceballos, G. Konstantinou, J. Pou, J. Andreu, and I. M. de Alegría, "(2n+ 1) selective harmonic elimination-pwm for modular multilevel converters: A generalized formulation and a circulating current control method," *IEEE Transactions on Power Electronics*, vol. 33, no. 1, pp. 802–818, 2017.

[75] A. Christe and D. Dujic, "Virtual submodule concept for fast semi-numerical modular multilevel converter loss estimation," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 7, pp. 5286–5294, 2017.

[76] F. Hahn, M. Andresen, G. Buticchi, and M. Liserre, "Thermal analysis and balancing for modular multilevel converters in hvdc applications," *IEEE Transactions on Power Electronics*, vol. 33, no. 3, pp. 1985–1996, 2017.

[77] J. Li, G. Konstantinou, H. R. Wickramasinghe, and J. Pou, "Operation and control methods of modular multilevel converters in unbalanced ac grids: A review," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 1258–1271, 2018.

[78] X. Shi, B. Liu, Z. Wang, Y. Li, L. M. Tolbert, and F. Wang, "Modeling, control design, and analysis of a startup scheme for modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 11, pp. 7009–7024, 2015.

[79] Y. Zhang, H. Wang, Z. Wang, F. Blaabjerg, and M. Saeedifard, "Mission profile-based system-level reliability prediction method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 7, pp. 6916–6930, 2019.

[80] S. Vazquez, J. Rodriguez, M. Rivera, L. G. Franquelo, and M. Norambuena, "Model predictive control for power converters and drives: Advances and trends," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 2, pp. 935–947, 2017.

[81] S. Vazquez, J. I. Leon, L. G. Franquelo, J. Rodriguez, H. A. Young, A. Marquez, and P. Zanchetta, "Model predictive control: A review of its applications in power electronics," *IEEE industrial electronics magazine*, vol. 8, no. 1, pp. 16–31, 2014.

[82] S. Vazquez, C. Montero, C. Bordons, and L. G. Franquelo, "Design and experimental validation of a model predictive control strategy for a vsi with long prediction horizon," in *Industrial Electronics Society, IECON 2013-39th Annual Conference of the IEEE*. IEEE, 2013, pp. 5788–5793.

[83] S. Mariéthoz and M. Morari, "Explicit model-predictive control of a pwm inverter with an lcl filter," *IEEE Transactions on Industrial Electronics*, vol. 56, no. 2, pp. 389–399, 2009.

[84] J. Böcker, B. Freudenberg, A. The, and S. Dieckerhoff, "Experimental comparison of model predictive control and cascaded control of the modular multilevel converter," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 422–430, 2015.

[85] J. Qin and M. Saeedifard, "Predictive control of a modular multilevel converter for a back-to-back hvdc system," *IEEE Transactions on Power delivery*, vol. 27, no. 3, pp. 1538–1547, 2012.

[86] P. Liu, Y. Wang, W. Cong, and W. Lei, "Grouping-sorting-optimized model predictive control for modular multilevel converter with reduced computational load," *IEEE Transactions on Power Electronics*, vol. 31, no. 3, pp. 1896–1907, 2015.

[87] Z. Gong, P. Dai, X. Yuan, X. Wu, and G. Guo, "Design and experimental evaluation of fast model predictive control for modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 6, pp. 3845–3856, 2015.

[88] H. Mahmoudi, M. Aleenejad, and R. Ahmadi, "Modulated model predictive control of modular multilevel converters in vsc-hvdc systems," *IEEE Transactions on Power Delivery*, vol. 33, no. 5, pp. 2115–2124, 2017.

[89] A. Mora, M. Urrutia, R. Cárdenas, A. Angulo, M. Espinoza, M. Diaz, and P. Lezana, "Model-predictive-control-based capacitor voltage balancing strategies for modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2432–2443, 2018.

[90] J. Wang, X. Liu, Q. Xiao, D. Zhou, H. Qiu, and Y. Tang, "Modulated model predictive control for modular multilevel converters with easy implementation and enhanced steady-state performance," *IEEE Transactions on Power Electronics*, 2020.

[91] L. Harnefors, A. Antonopoulos, S. Norrga, L. Angquist, and H.-P. Nee, "Dynamic analysis of modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 60, no. 7, pp. 2526–2537, 2013.

[92] M. Guan, Z. Xu, Q. Tu, and W. Pan, "Nearest level modulation for modular multilevel converters in hvdc transmission [j]," *Automation of Electric Power Systems*, vol. 2, p. 012, 2010.

[93] P. Cortes, J. Rodriguez, C. Silva, and A. Flores, "Delay compensation in model predictive current control of a three-phase inverter," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 1323–1325, 2012.

[94] M. Vasiladiotis, A. Christe, and T. Geyer, "Model predictive pulse pattern control for modular multilevel converters," *IEEE Transactions on Industrial Electronics*, vol. 66, no. 3, pp. 2423–2431, 2018.

[95] J. Pou, S. Ceballos, G. Konstantinou, V. G. Agelidis, R. Picas, and J. Zaragoza, "Circulating current injection methods based on instantaneous information for the modular multilevel converter," *IEEE Transactions on Industrial Electronics*, vol. 62, no. 2, pp. 777–788, 2014.

[96] B. Xia, Y. Li, Z. Li, G. Konstantinou, F. Xu, F. Gao, and P. Wang, "Decentralized control method for modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 34, no. 6, pp. 5117–5130, 2018.

[97] Y. Zhou, D. Jiang, P. Hu, J. Guo, Y. Liang, and Z. Lin, "A prototype of modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 7, pp. 3267–3278, 2013.

[98] M. Alharbi and S. Bhattacharya, "Scale-up methodology of a modular multilevel converter for hvdc applications," *IEEE Transactions on Industry Applications*, vol. 55, no. 5, pp. 4974–4983, 2019.

[99] D. Ronanki and S. S. Williamson, "Failure prediction of submodule capacitors in modular multilevel converter by monitoring the intrinsic capacitor voltage fluctuations," *IEEE Transactions on Industrial Electronics*, vol. 67, no. 4, pp. 2585–2594, 2019.

[100] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade pwm statcom with star configuration," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1041–1049, 2007.

[101] R. Picas, J. Zaragoza, J. Pou, S. Ceballos, and J. Balcells, "New measuring technique for reducing the number of voltage sensors in modular multilevel converters," *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 177–187, 2015.

[102] L. Peng and Z. Wang, "Grouping capacitor voltage estimation and fault diagnosis with capacitance self-updating in modular multilevel converters," *IEEE Transactions on Power Electronics*, 2020.

[103] J. Nocedal and S. J. Wright, *Sequential quadratic programming*. Springer, 2006.

[104] J. L. Jerez, P. J. Goulart, S. Richter, G. A. Constantinides, E. C. Kerrigan, and M. Morari, "Embedded online optimization for model predictive control at megahertz rates," *IEEE Transactions on Automatic Control*, vol. 59, no. 12, pp. 3238–3251, 2014.

[105] V. Arredondo, M. A. Perez, and J. R. Espinoza, "Capacitor voltage ripple control based on decoupled power analysis in mmc," in *2017 11th IEEE International Conference on Compatibility, Power Electronics and Power Engineering (CPE-POWERENG)*. IEEE, 2017, pp. 544–549.