IMSE-CNM Instituto de Microelectrónica de Sevilla

CSIC Consejo Superior de Investigaciones Científicas — Universidad de Sevilla

Doctoral Thesis

Low-Power Artifact-Aware Implantable Neural Recording Microsystems for Brain-Machine Interfaces

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PROPUESTA DE TESIS DOCTORAL
PARA LA OBTENCIÓN DEL GRADO DE
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ACRONYMS

ADC Analog-to-Digital Converter.

AFE Analog Front-End.

ALS Amyotrophic Lateral Sclerosis.

AP Action Potentials.

ARL Auto-Ranging Loop.

ASAR Adaptive Stimulation Artifact Rejection.

ASIC Application Specific Integrated Circuit.

AZ Autozero.

BCIs Brain-Computer Interfaces.

BLE Bluetooth Low-Energy.

BMIs Brain-Machine Interfaces.

CCO Current-Controlled Oscillator.

CDS Correlated Double Sampling.

CIC Cascaded Integrator–Comb.

CM Common-Mode.

CMFB Common-Mode Feedback.

CMRR Common-mode Rejection Ratio.

CS Charge-Sampling.

CT Continuous-Time.

DAC Digital-to-Analog Converter.

DBS Deep Brain Stimulation.

DM Differential-Mode.

DSL DC Servo Loop.

DT Discrete-Time.

ECoG Electroencephalographic.

EEG Electroncephalogram.

FIR Finite-Impulse-Response.

FPGA Field-Programmable Gate Array.

HB LNA High-Bandwidth LNA.

HPF High-Pass Filter.

IA Instrumentation Amplifier.

IBL Impedance Boosting Loop.

IC Integrated Circuit.

IIR Infinite-Impulse-Response.

IRN Input-referred Noise.

LFP Local Field Potentials.

LMS Least Mean Square.

LNA Low-Noise Amplifier.

LSB Least Significant Bit.

LUT Look-Up Table.

MSB Most Significant Bit.

NEB Noise Equivalent Bandwidth.

NEF Noise Efficiency Factor.

NLMS Normalized Least Mean Square.

OS ADC Oversampled ADC.

OSR Oversampling Ratio.

OTA Operational Transconductance Amplifier.

PBS Phosphate Buffered Saline.

PGA Programmable Gain Amplifier.

PR Pseudoresistors.

PSD Power Spectral Density.

PSRR Power Supply Rejection Ratio.

SAR Successive Approximation Register.

SC Switched-capacitor.

SNR Signal-to-Noise Ratio.

TDD Time-Division Demultiplexing.

TDM Time-Division Multiplexing.

THD Total Harmonic Distortion.

VCO Voltage-Controlled Oscillator.

VS Voltage-Sampling.

WIS Windowed Integration Sampling.

RESUMEN

La neurociencia encargada de investigar sobre cómo se implementan las funciones cerebrales complejas a nivel celular requiere de interfaces de captación neuronal *in vivo*, incluyendo electrodos y circuitos de adquisición de señal con la mayor capacidad de observación y mayor resolución espacial. La tendencia de los dispositivos de captación de señal neuronal a emplear sondas de gran número de canales o mallas 2D con puntos de medición densamente espaciados para registrar grandes poblaciones neuronales dificulta el ahorro de recursos. Las especificaciones de bajo ruido y bajo consumo de la interfaz de registro del *front-end* analógico suelen requerir una gran ocupación de silicio, lo que hace que el problema sea aún más difícil. Un enfoque común para aliviar esta carga de consumo de área se basa en las técnicas de multiplexación por división de tiempo en las que la electrónica de lectura se comparte, parcial o totalmente, entre los canales preservando la resolución espacial y temporal de las grabaciones. En este enfoque, los elementos compartidos tienen que operar en un intervalo de tiempo más corto por canal, y la ocupación del área se reduce a cambio de mayores frecuencias de funcionamiento y anchos de banda. Como resultado, el consumo de energía sólo se ve ligeramente afectado, aunque otras métricas de rendimiento como el ruido en banda, el *crosstalk* o el *CMRR* pueden verse degradadas, especialmente si todo el circuito de lectura está multiplexado en la interfaz del electrodo. Además, estas interfaces de registro neural suelen emplearse en dispositivos neurales de bucle cerrado que también incluyen circuitos de estimulación. Las grandes interferencias, o artefactos, evocadas por la estimulación hacen necesario el desarrollo de técnicas y arquitecturas que garanticen que el sistema de detección es capaz de registrar la señal neuronal de interés en presencia de estos artefactos.

En esta tesis se revisan, en primer lugar, las diferentes alternativas de implementación reportadas para los sistemas de captación neuronal multiplexados en el tiempo, incluyendo técnicas de detección de artefactos, se analizan sus ventajas e inconvenientes y se sugieren estrategias para mejorar el rendimiento. A continuación, basándose en la revisión presentada, esta tesis presenta un front-end de señal mixta de alto rango dinámico, baja potencia y bajo ruido para la adquisición de potenciales de campo locales o señales electroencefalográficas con implantes neuronales invasivos. El sistema incorpora multiplexación temporal de 32 canales en la interfaz del electrodo para ahorrar superficie y

ofrece la posibilidad de codificar espacialmente las señales para aprovechar las grandes correlaciones entre canales adyacentes. El circuito también implementa un algoritmo de auto-regulación de señal mixta accionada por voltaje que permite atenuar las grandes interferencias en el dominio digital al tiempo que preserva la información neuronal, aumentando así eficazmente el rango dinámico del sistema y evitando la saturación. Un prototipo, fabricado en un proceso CMOS estándar de 180 nm, ha sido verificado experimentalmente *in vitro* y muestra un ruido integrado referido a la entrada en la banda de 0.5–200 Hz de 1.4 μV_{rms} para un ruido de punto de unos 85 nV/$\sqrt{Hz}$. El sistema consume 1.5 μW por canal con una alimentación de 1.2 V y obtiene un rango dinámico de 71 dB + 26 dB (con compresión de artefactos), sin penalizar otras especificaciones críticas como el *crosstalk* entre canales o los ratios de rechazo de modo común y de alimentación.

Esta tesis está dividida en siete capítulos. En el primero se introduce el objetivo de este trabajo. El capítulo 2 presenta las consideraciones de diseño de los dispositivos multi-canal para la captación de señales neuronales junto con una comparación del estado del arte. El tercer capítulo ofrece un resumen de las técnicas y arquitecturas empleadas para paliar las largas interferencias durante la adquisición de señal y el capítulo 4 muestra una revisión de la técnica de multiplexación por división de tiempo. Por último, el capítulo 5 describe el microsistema de registro neuronal de baja potencia de 32 canales, y el capítulo 6 ofrece sus resultados experimentales. El último capítulo aborda las conclusiones y los trabajos futuros.

ABSTRACT

Neuroscience research into how complex brain functions are implemented at cell level requires in vivo neural recording interfaces, including microelectrodes and read-out circuitry, with increased observability and spatial resolution. The trend in neural recording interfaces towards employing high-channel-count probes or 2D meshes with densely spaced recording sites for recording large neuronal populations makes it harder to save on resources. The low-noise, low-power requirement specifications of the Analog front-end (AFE) recording interface usually require large silicon occupation, making the problem even more challenging. One common approach to alleviating this area consumption burden relies on time-division multiplexing techniques in which read-out electronics are shared, either partially or totally, between channels while preserving the spatial and temporal resolution of the recordings. In this approach, shared elements have to operate over a shorter time slot per channel, and area occupation is thus traded off against larger operating frequencies and signal bandwidths. As a result, power consumption is only mildly affected, although other performance metrics such as in-band noise, crosstalk, or CMRR may be degraded, particularly if the whole read-out circuit is multiplexed at the electrode interface. Furthermore, these neural recording interfaces are usually employed in closed-loop neural devices which also include stimulation circuits. The large interferences, or artifacts, evoked by stimulation arise the need for the development of techniques and architectures to ensure that the sensing system is capable of recording the neural signal of interest in the presence of these artifacts.

In this thesis, we firstly review the different implementation alternatives reported for time-multiplexed neural recording systems, including artifact-aware techniques, analyze their advantages and drawbacks, and suggest strategies for improving performance. Then, based on the presented review, this thesis presents a high dynamic range, low-power, low-noise mixed-signal front-end for the recording of local field potentials or electroencephalographic signals with invasive neural implants. It features time-multiplexing of 32 channels at the electrode interface for area saving and offers the ability to spatially delta encode signals to take advantage of the large correlations between nearby channels. The circuit also implements a mixed-signal voltage-triggered auto-ranging algorithm which allows attenuating large interferers in the digital domain while

preserving neural information, thus effectively increasing the dynamic range of the system while avoiding the onset of saturation. A prototype, fabricated in a standard 180 nm CMOS process, has been experimentally verified *in-vitro* and shows an integrated input-referred noise in the 0.5–200 Hz band of 1.4 μV_{rms} for a spot noise of about 85 nV/$\sqrt{Hz}$. The system draws 1.5 μW per channel from 1.2 V supply and obtains 71 dB + 26 dB (with artifact compression) dynamic range, without penalizing other critical specifications such as crosstalk between channels or common-mode and power supply rejection ratios.

This thesis is divided into seven chapters. In the first one, the aim of this work is introduced. Chapter 2 presents the design considerations of multi-channel neural recording devices along with a state-of-art comparison. The third chapter offers an overview of techniques and architectures to overcome the large interference signals in neural recording and Chapter 4 provides a review of the time-division multiplexing technique. Finally, Chapter 5 describes the 32-channel low-power neural recording microsystem, and Chapter 6 provides its experimental results. The last chapter addresses the conclusions and future works.

CHAPTER 1

INTRODUCTION

Over the years, researchers have been exploring the electrical activity in groups of neurons to find out how this is related to brain disorders and diseases. The study of the electrical response in different cortical regions is consolidated as a powerful tool for a variety of clinical applications. Hence, neural recording techniques entailed an evolution in the diagnose of the most common neural diseases such as Parkinson, epilepsy or Alzheimer . These sensing methods combined with neural stimulation are used as therapies for the treatment of many of those neural diseases and disorders [19, 20]. For instance, the Deep Brain Stimulation (DBS), which can be considered as a kind of pacemaker for the brain, monitoring and keeping the neural activity under control, has proven its efficacy in treating Tourette's syndrome, chronic pain, and major depression.

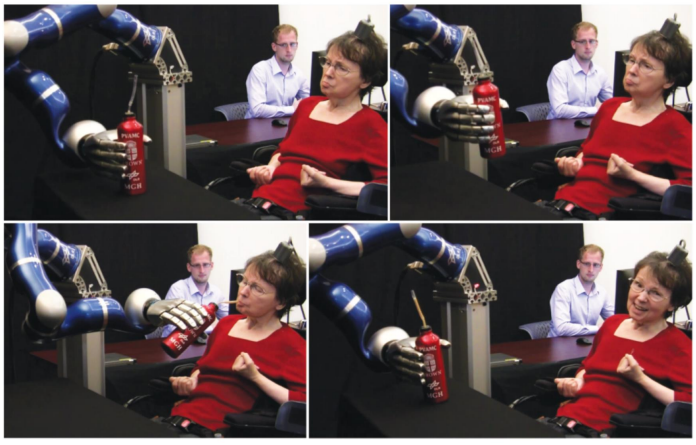


Figure 1.1: Patient employing a brain-machine interface to drink from a bottle [1].

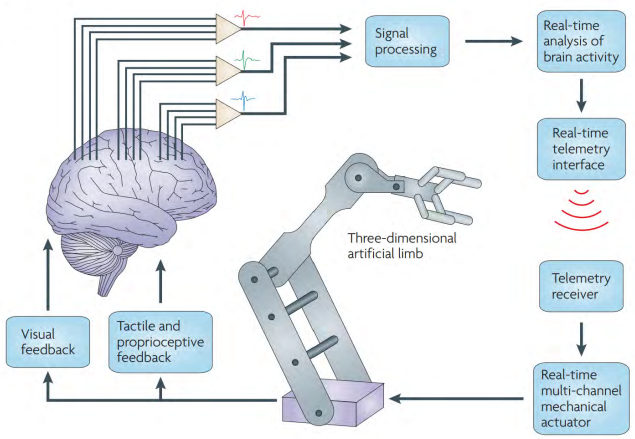


Figure 1.2: Flow diagram of the operation of a BMI [2].

On the other hand, Brain Machine Interfaces (BMIs), or Brain Computer Interfaces (BCIs), (Figure 1.1) emerged as a potential therapy to restores motor control in disabled patients such as those suffering from Amyotrophic Lateral Sclerosis (ALS) [21], stroke and cerebral palsy or spinal cord injury. The development of these multidisciplinary interfaces has also lead to the restoration of locomotion and the control of robotic prostheses [22, 23]. The operation principle of the BMIs is disclosed in Figure 1.2 [2]. The recorded data from the neural sensing circuitry is processed, analyzed and transmitted to a control unit which sends a control signal to a mechanical actuator (such as a prosthesis). The response of the sensors located in the actuator is sent back as a feedback signal to the neural system via a stimulator, thus closing the loop. This, along with the aforementioned medical applications, leads to the need for continuous development of neural recording devices and techniques, specially intended for bidirectional interfaces.

1.1 Neural Recording Techniques and Signals

The different neural recording techniques can be classified in function of their observation level (see Figure 1.3). Each level represents an anatomical site where signals are recorded. Each technique presents different constraints in terms of invasiveness, mobility, longevity, scalability or stability.

Firstly, Electroncephalogram (EEG) is a non-invasive method exploiting the sensing of the averaged activity of millions of neurons. In this technique, the electrode array is placed at the scalp, about 2 cm above the cortex and each electrode records the neural activity of about 4 cm. Although this detection method is widely adopted by neuroscientists, the provided resolution might not be sufficient for many other applications where more spatial resolution is required [24].

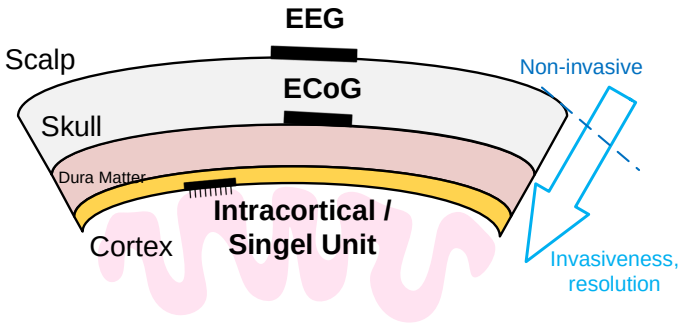


Figure 1.3: Neural recording techniques in function of their invasiveness level.

Electroencephalographic (ECoG) provides the less invasive intracranial recording approach resulting in a spatial resolution from 0.2 to 10 mm [25]. This constitutes a medium point between EEG and intracortical implants in terms of the resolution-invasiveness trade-off, providing a powerful recording technique without producing neural damage. One of the most common clinical applications of ECoG is related to seizure detection in epilepsy treatments.

Finally, single unit recording constitutes the most invasive sensing method in which intracortical implanted electrodes capture the extracellular activity from the cortex. This provides the highest achievable spatial resolution, capable of recording the activity and potentials of a single neuron. These measurements are useful for BMIs because this information contains, for instance, the motor commands in the primary motor cortex or cognitive signals in the posterior parietal cortex [26].

In these invasive recording techniques, two main signals are captured: Local Field Potentials (LFP)s and Action Potentials (AP)s. The LFPs comprises the combination of synaptic and network activities within a local brain region [27]. These neural signals are mainly characterized by their low-frequency oscillations (up to 500 Hz) [28] and low-amplitude (tens of μV to few mV) and can be classified in delta waves (0.5-3 Hz), theta waves (4-6 Hz), alpha waves (8-14 Hz), beta waves (15-38 Hz), gamma waves (38-100 Hz) and fast waves (100-500 Hz). Among the applications of these waves, BMIs based on LFP recording have demonstrated to suffer less from biocompatibility issues [26]. The information contained in LFPs has also shown to be useful for decoding of the onset and intensity of acute pain [29], the cognitive processes including attention, memory and perception or the mechanisms related to sensory processing [30].

In contrast to the LFPs, spikes or APs represent the response of a single neuron. While their amplitude is similar to that of LFPs, their frequency components start at about 500 Hz and can reach up to 5-10 kHz. The spike sensing applications are numerous and mostly related to neurological diseases [10]. For instance, one of the most widespread uses involves epilepsy and relies on seizure prediction [31].

Table 1.1 summarizes the main characteristics of neural recording techniques and the acquired neural signals [25].It is worth observing how low-frequency signals present a Power Spectral Density (PSD) similar to 1/f. This spectral distribution has been exploited by data compression algorithms [32] and by low-noise design processes [33].

Table 1.1: Neural Recording Techniques Comparison

	EEG	ECoG	Intracortical	
			LFP	AP
Bandwidth	0.5-50Hz	0.5-500Hz	0.5-500Hz	0.5-10kHz
Amplitude	1-10μV	1-100μV	0.01-1mV	0.01-1mV
PSD	1/f	1/f	1/f	Constant
Spatial resolution	3-5cm	0.2-10mm	0.1-1mm	0.1-1mm
Invasive	No	High	Highest	Highest
Neural damage	No	No	Yes	Yes
Area coverage	Whole Brain	~cm^2, whole brain	~mm^2	~mm^2

1.2 Thesis Contributions

This work provides two main contributions to the field of neuroscience, related to implantable neural recording microsystems.

Firstly, a complete review of multi-channel neural recording interfaces is presented. This review not only includes neural front-ends but also contains considerations related to the electrode interface and its integration along with the Analog Front-End (AFE). Analyses have been also provided in order to evaluate the impact of these techniques on the overall performance of the sensor. Neural sensing architectures have been reviewed and classified together with the new trends in the design of neural recording devices, specially intended for area and power saving. An exhaustive state-of-art comparison including more than 50 high-performance neural front-ends is provided to ease the evaluation of each different architecture.

Time-division multiplexing has been studied due to its promising results in terms of area and power saving over the last years. A classification of recording structures regarding the location of the multiplexer in the signal path is introduced along with the advantages and disadvantages of applying this technique at the electrode interface.

The presence of large interference signals in bidirectional interfaces has been addressed through the examination of different techniques and architectures. The presented artifact-aware front-ends offer promising solutions to overcome this issue for differential and common-mode artifacts.

This study of neural recording techniques has led to the design of a 32-channel low-noise, high-dynamic range recording front-end, which constitutes

the second main contribution of this thesis. This CMOS prototype intended for LFPs or ECoG recording is based on a novel alternative to overcome the noise issues regarding time-division multiplexing architectures. A new low computational cost artifact-aware technique is proposed to largely increase the dynamic range of the system, which makes this design suitable for its integration in a low-power bidirectional interface. Finally, a compression technique that relies on the spatial correlation of the neural signal is also employed to reduce the input range and the raw data to process and transmit. The prototype has been *in-vitro* verified providing state-of-art specifications, specially interesting in terms of input-referred noise and dynamic range.

1.3 Thesis Outline

This thesis is structured as follows:

- Chapter 2 presents the design considerations of multi-channel neural recording interfaces along with a brief review of high-performance neural recording architectures. Furthermore, an exhaustive state-of-art revision of neural front-ends is also provided at the end of this Chapter.
- Chapter 3 introduces the problem related to the large interference signals evoked by stimulation in bidirectional interfaces and disclosed some of the most significant reported artifact-aware techniques and architectures.
- Chapter 4 reviews the main advantages and drawbacks of the time-division multiplexing technique in neural recording front-ends. Moreover, a classification of the different architectures depending on the location of the multiplexer along with a state-of-art comparison is provided. Finally, the benefits and disadvantages of multiplexing at the electrode interface have been analyzed.
- Chapter 5 presents a 32-channel low-noise CMOS prototype of a neural recording front-end. Detailed design analyses, specially those regarding the noise contribution have been also included in this Chapter.
- Chapter 6 shows the experimental results of the prototype presented in the previous chapter. Herein, the Integrated Circuit (IC) is firstly electrically characterized and, then, verified by in vitro measurements. A brief discussion about the obtained results during this work is addressed at the end of this Chapter.
- Finally, Chapter 7 presents the conclusions of this work and highlights the contributions of this thesis. Future research works are also disclosed.

While the first 4 Chapters mainly constitute an exhaustive review of the reported multi-channel artifact-aware neural recording devices, Chapters 5 and 6

present and verify a CMOS prototype of a low-power artifact-aware implantable neural recording microsystem intended for low-amplitude low-frequency signals acquisition whose major applications are related to brain-machine interfaces.

CHAPTER 2

MULTI-CHANNEL NEURAL RECORDING INTERFACES

Closed-loop neural prostheses have largely proven their effectiveness in treating brain disorders [19, 20] and in their application in BMIs [23, 21]. To develop such therapies and devices, the spatial resolution of neural recording interfaces needs to be increased. In recent years, therefore, and in line with the well-known Moore's law for transistor count scaling in dense integrated circuits, we have seen gradual increases in the number of simultaneous recording channels incorporated into neural interfaces, either by penetrating probe shanks or through the use of surface 2D microelectrode meshes. The number of active sites in probe shanks, for example, has increased from about 100 in the most advanced systems available a decade ago to the approximately 3,000 simultaneously recorded channels reported nowadays. Similarly, the density of recording channels has risen from some 5-6 channels/mm^2 to more than 80 channels/mm^2 in the current state-of-the-art. Figure 2.1 illustrates how the number of simultaneously recorded neurons has largely incremented over the years [3].

Figure 2.2 shows the most commonly used electrodes in multi-channel neural recording devices: i) Utah intracortical electrode array [4, 34] (Figure 2.2 (a)); ii) parallel microwire arrays [5] (Figure 2.2 (b)); and iii) probes on silicon [35, 6] (Figure 2.2 (c)). While the Utah intracortical electrode array and the microwire arrays are able to capture the information from various neurons in a specific region of the brain, the probes on silicon are usually employed to record the activity in a specific spot. In these electrodes, the base houses the main CMOS signal conditioning circuitry and the shank is mainly made up of pixels and the interconnecting wires between the pixels and the base. These pixels

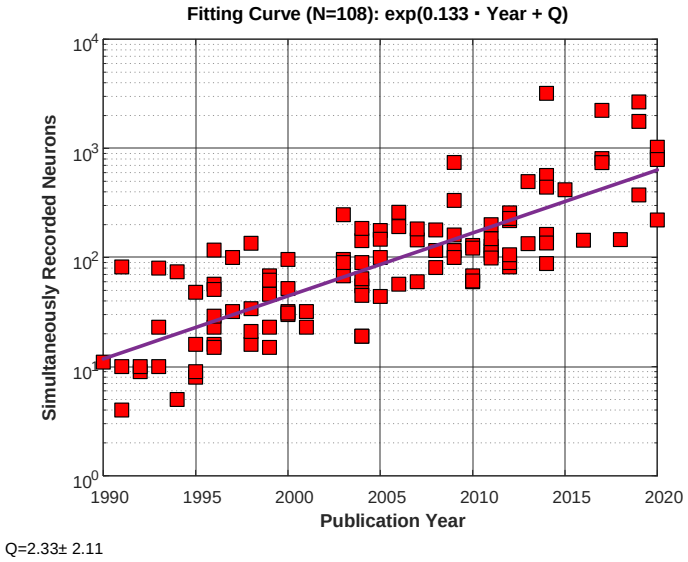


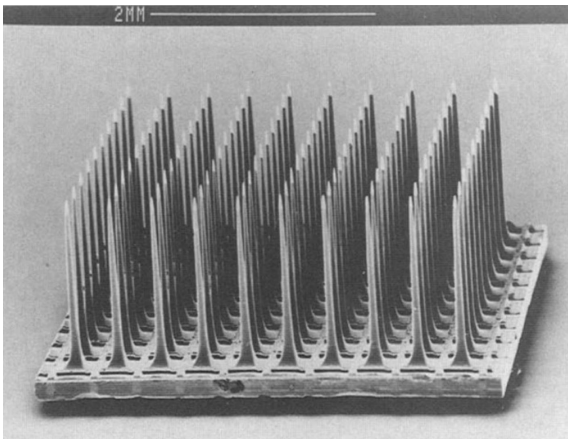
Figure 2.1: Number of simultaneously recorded neurons over the years [3].

are the minimum recording unit in neural probes and comprise electrodes and interconnection wires. They may also include active devices such as switches or amplifiers.

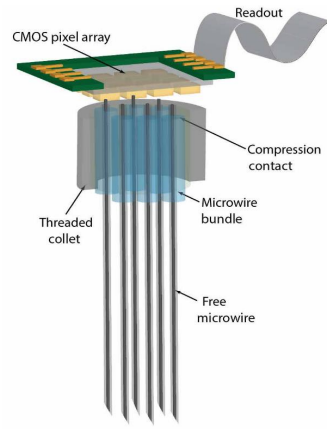
The conventional multi-channel neural sensor interface is shown in Figure 2.3. The M-channel electrode array is connected by the interconnection wires to the neural recording IC. It is worth commenting that other main blocks of the neural recording IC, such as the power management, are not included in the Figure. In this architecture, each electrode is recorded by an independent AFE, which amplifies, filters and converts to the digital domain the neurological signals. The AFE usually comprises a Low Noise Amplifier (LNA), also known as Instrumentation Amplifier (IA), which generally embeds a bandpass filter, a Programmable Gain Amplifier (PGA) which maximize the output swing of the analog signal and an Analog-to-Digital Converter (ADC). Then, the data from the M parallel readout channels is serialized, digitally processed and wirelessly transmitted to an external unit. In the case of standalone closed-loop systems, this wireless transmission is not required and the processed data is directly transmitted to the stimulator.

2.1 Considerations for multi-channel Neural Recording Systems

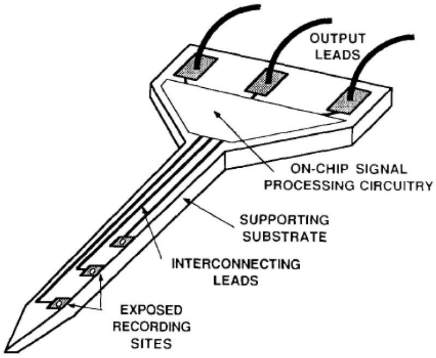
Implantable devices for neural sensing have to satisfy some design constraints from the point of view of medical safety and to ensure the longevity of the implant. Firstly, the system will function inside the human body, therefore



(a)



(b)



(c)

Figure 2.2: Electrode devices for multi-channel neural recording systems. (a) Utah intracortical electrode array [4]. (b) Example of microwire array-based device [5]. (c) Example of probe on silicon [6].

the used materials must be biocompatible [36]. The form factor of the device has to be minimized to avoid producing perturbations in the body where it is placed and it can not increase the temperature above 1°C to not damage the neural tissue [37]. This point is directly related to the power consumption of the system. Finally, the recorded data has to be sent to the external processing unit by wireless transmission to avoid employing wires across the skull and the brain surface.

The electrodes, in addition to be biocompatible, have to be minimized to maximize the spatial resolution of the implant, which leads to an increment in the number of sensing channels. However, the impedance of each electrode (Z_e), which also depends on the electrode material and the environment where the electrodes are allocated, is inversely proportional to the area of the electrode. For instance, for intracortical electrode arrays, the electrode impedance at low frequencies can reach up to tens of MΩ [17]. Herein, the thermal noise contri-

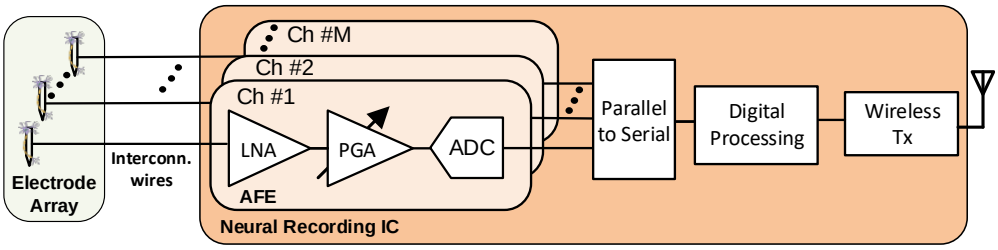


Figure 2.3: Conventional multi-channel neural recording sensor interface.

bution of the electrodes which is proportional to their impedance, can strongly degrade the noise performance of the system. This establishes a trade-off between noise and area when selecting/designing the electrode interface. Due to the low magnitude of the neural signals, the recording front-end plus the noise contribution of the electrodes have to provide an Input-referred Noise (IRN) below 10 μV_{rms} to obtain high enough Signal-to-Noise Ratio (SNR) to properly record and process the neural activity. The demanded SNR will depend on the specific application of the neural device.

Increasing the number of sensing channels while maintaining the size of the electrode interface could involve a smaller gap between the interconnection wires, increasing the crosstalk between channels. This turns the electrical crosstalk into one of the most significant scaling limitations of multi-channel recording devices. For neural applications, the crosstalk level has to be below 1% of the recorded signal level to make it negligible compared with the background noise [6].

Neural front-ends present design constraints which are related to the electrodes properties, characteristics of the neural signals, multi-channel scaling limits and the aforementioned implantable device needs. In terms of the electrode properties, to avoid signal attenuation of more than the 10 %, the input impedance of the AFE has to be at least 50 times larger than the electrode impedance [38]. This results in an input impedance requirement of about hundreds of M Ω. Moreover, electrodes also present mismatch problems regarding to the fabrication non-idealities. This increases the effect of large Common-Mode (CM) interferences at the input of the system, demanding of a high Common-mode Rejection Ratio (CMRR) to palliate this problem. Additionally, an offset rejection mechanism is required to avoid the saturation of the signal path due to the DC offset of tens of mV evoked by the contact between the electrode and the tissue [39].

Low power is one of the main features of neural recording devices because of: i) the need to avoid feeding the implant with large batteries, demanding energy harvesting schemes or large coils in wireless inductive links; ii) avoid increasing the brain tissue heating. In this regard, scaling the number of channels could compromise the miniaturization, security and longevity of the implant, making the power consumption one of the most critical specifications of the front-end.

In high-channel recording devices, the number of simultaneous recording electrodes is restricted by the interconnection wires, the size of the active silicon area, and the number of parallel read-out channels. The form factor requirement of employed AFE, demands silicon areas of less than 0.16 mm^2 per channel because an inter-electrode spacing of 400-μm provided a large enough spatial resolution [40]. Additionally, increasing the number of readout channels also scales the amount of raw data to be processed and transmitted, which can create a bottleneck on the recording interfaces and significantly increase the dynamic power consumption of the digital part [32]. Herein, compression algorithms have to be implemented to counteract this problem.

Finally, neural recording systems have to be able to handle large interferences, or artifacts, from dozens to hundreds of mV. This has special relevance for artifacts produced by stimulation current pulses in closed-loop interfaces [13, 41]. This increases the requirement of the input differential range that the system is able to tolerate without saturating the signal path (as detailed in Chapter 3). Stimulation artifact evokes a response of the brain (for instance, m-waves [42]) reaching up to a few of mV. This demands a larger dynamic range of the system.

Table 2.1 summarises the main requirements of multi-channel neural recording AFEs. Some of these needs can be relaxed regarding the employed electrode interface, the specifications of the complete recording device and the specific application of the system. The designer has to take into account the trade-offs between all presented specifications to meet all the design considerations without penalizing each other.

Table 2.1: Required Specifications for Multi-Channel Neural Recording AFEs

AFE specifications	Required value	Imposing constraint
Input impedance	>50 $\cdot Z_e$	Electrode impedance
CMRR	>60 dB	Electrode mismatch and CM interferences
DC offset rejection	>50 mV	DC offset from the electrodes
Low-noise	<10 μV_{rms}	Neural signal amplitude
Bandwidth	0.5-200/500 Hz for LFP 300-5/10 kHz for AP	Neural signal frequency
Power consumption per channel	<10 μ W	Reduce power supply circuitry and heating
Area per channel	<0.16 mm^2	Number recording channels
Maximum tolerable input signal	>20 mV_{pp}	Large interference signals
Dynamic range	>60 dB	Evoked signal from stimulation

2.2 Electrode-AFE interface

AFEs in multi-channel systems are usually placed relatively far from the recording electrodes. The interconnection wires between the electrode array and the AFEs severely limit the electrode density and reduce the efficiency of the device's area occupation. However, some silicon-based devices make it possible

to integrate one or more AFE stages along with the electrodes. The most suitable stage to be integrated adjacent to the electrodes is the IA. Therefore, the main advantages and disadvantages of employing or not this active circuitry along with the electrode have to be considered. These effects can be disclosed in its impact on the electrode crosstalk and its noise contribution to the system.

2.2.1 Crosstalk in Electrode-AFE Interfaces

The electrode crosstalk can be defined as the crosstalk from the electrode interface (including the active circuitry) to the input of the AFE.

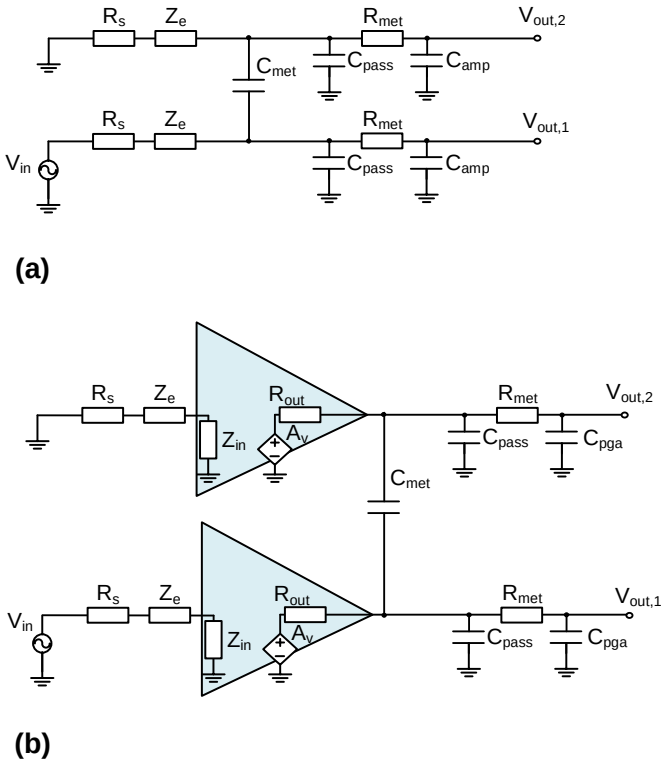


Figure 2.4: Equivalent circuit model for electrode crosstalk analysis (a) without active electrode-AFE interface. (b) with active electrode-AFE interface.

In multi-channel neural sensing devices, the space between adjacent electrodes and between interconnection wires is largely reduced while the dielectric layers below and above the electrodes remain constant. The coupling capacitance between electrodes thus increases because of the reduced space, thereby increasing the electrical crosstalk. A simplified scheme modeling crosstalk from electrodes to the AFE was proposed in [6] and further developed in [43, 44] (see Figure 2.4 (a)). It should be noted that [44] also shown that the switches placed at the electrode interface have a negligible effect on crosstalk, so this was not included in the model. For the AFE to be integrated within the neural

probe, the capacitive coupling between metal lines in the external wire [43] was also excluded. To further develop this approach, Figure 2.4 (b) shows a model including an amplifier adjacent to the electrodes, similar to [45]. The employed circuit elements with their corresponding values used to simulate the model (taken from [44, 43]) are described as follows:

- R_s is the spreading resistance encountered by the current propagating out into the fluid near to the electrode. It has been reported to be about 10 kΩ [43].
- Z_e represents the equivalent impedance of the electrode. This impedance is a frequency-dependent parameter because it is formed by a resistance in parallel with a capacitor. For the analysis purpose, which was carried out for a 1 kHz sine wave input signal, the value of Z_e has been set to 2 MΩ, corresponding to a 20 μm diameter Pt electrode.
- C_{met} describes the capacitive coupling between adjacent lines. It was estimated as 0.3 pF.
- C_{pass} is the estimated capacitance of the metal lines with the extracellular fluid. This value was set as 0.6 pF.
- R_{met} represents the equivalent resistance between the metal traces to the amplifier (PGA, in the case of the active electrode-AFE interface) input. Its value was about 180 Ω.
- C_{amp} (only for non-active electrode-AFE interfaces) models the input capacitance of the AFE and was set at about 10 pF.
- C_{pga} (only for active electrode-AFE interfaces) represents the input capacitance of the PGA and was taken as about 10 pF.
- Z_{in} (only for active electrode-AFE interfaces) is the input impedance of the IA. It was selected to be above 70 MΩ.
- R_{out} (only for active electrode-AFE interfaces) describes the output resistance of the amplifier next to the electrode. This value was set as 50 kΩ.

Crosstalk simulations, where crosstalk was defined as $V_{out,2}/V_{in}$, were carried out in standard CMOS 0.18 μm technology (Figure 2.5). Figure 2.5 (a) represents electrode crosstalk against electrode impedance. It can be observed how while in the active configuration crosstalk remained constant, for the passive electrode-AFE model it largely increases with the electrode impedance. For impedances above 6 MΩ, the electrical crosstalk theoretically surpasses the background noise of the recorded signals, significantly reducing the SNR. This imposed a severe constraint in terms of the size and the material of the electrodes. For the active electrode-interface scheme, crosstalk is affected by the

amplifier output resistance (see Figure 2.5 (b)). It can be seen how, for output resistance values up to hundreds of kΩ, crosstalk remained below 0.1 %. In practical implementations, however, it has been shown that reducing this output resistance is not trivial, due to the power and area limitations of the amplifier. In [45], for instance, crosstalk was about -45 dB, despite using such amplifiers. A new approach to the same design, but using amplifiers with reduced output resistance, improved crosstalk results up to -64.4 dB [35].

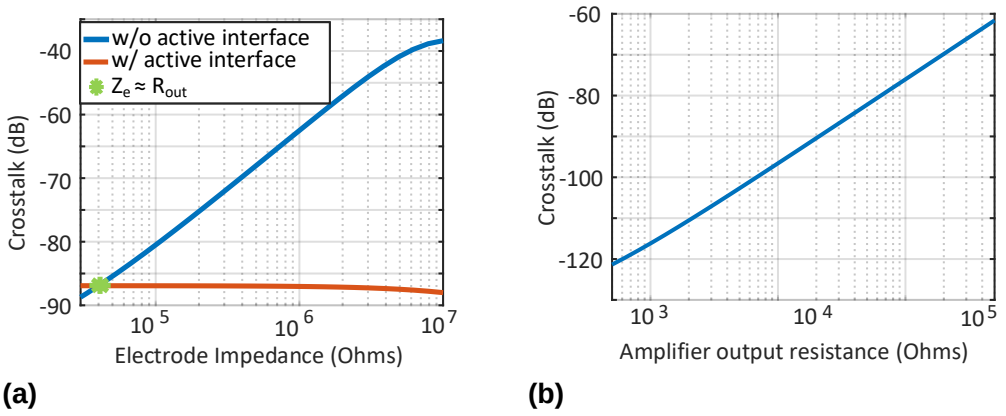


Figure 2.5: Electrode crosstalk against (a) electrode impedance with and without active electrode-AFE interface. (b) output resistance of the amplifier adjacent to the electrode.

2.2.2 Noise in Electrode-AFE interfaces

Integrating the IA in the electrode interface makes the power and area constraints of this stage even more restricted. These two design specifications are strongly related to the amplifier's noise contribution. Assuming a differential pair amplifier as shown in Figure 2.6 with $M1$ and $M2$, and $M3$ and $M4$ identical, the equivalent noise spectral density referred to the input will be given by:

$$N_{in}(f) = N_{th} + N_{1/f}(f) \tag{2.1}$$

where N_{th} and $N_{1/f}$ are the thermal and the flicker noise contributions of the amplifier, which can be obtained as [46]:

$$N_{th} = N_{th,M1} + N_{th,M3} = \frac{16kT}{3gm_1} + \frac{16kT}{3gm_3}\left(\frac{gm_3}{gm_1}\right)^2 \tag{2.2}$$

$$N_{1/f} = N_{1/f,M1} + N_{1/f,M3} = \frac{2K_p}{C_{ox}\ A_1\ f^a} + \frac{2K_n}{C_{ox}\ A_3\ f^a}\left(\frac{gm_3}{gm_1}\right)^2 \tag{2.3}$$

where k is the Boltzamnn constant, T is the temperature, gm_i is the transconductance of the $i-th$ transistor, C_{ox} is the gate-oxide capacitance, A_i is the

area of the $i-th$ transistor, and K_p, K_n and a are flicker parameters dependent on the specific fabrication process. To maximize the gain of the stage and minimize noise, the ratio gm_1/gm_3 is maximized. For simplification, we will assume $gm_1 >> gm_3$ so the noise components of transistor $M3-M4$, $N_{th,M3}$ and $N_{1/f,M3}$, will be neglected in the analysis.

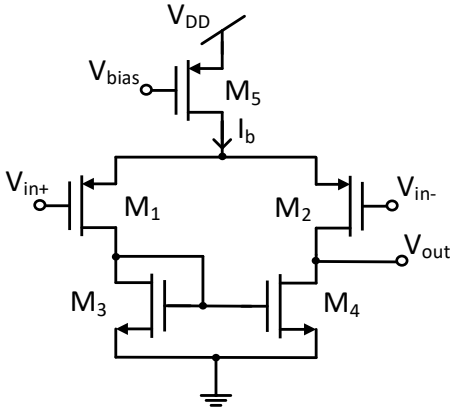


Figure 2.6: Differential-pair CMOS amplifier scheme.

In terms of thermal noise, neural devices have to be designed within the aforementioned limit of < 1 ºC of brain tissue heating [37]. The power consumption of active electrodes increases shank heating, and, therefore, the current through the IA, I_b, has to be minimized. With $gm_1 \propto I_b$, the thermal noise contribution of the active electrode-AFE interfaces would theoretically be larger than in passive interfaces. Nevertheless, as demonstrated by the finite element method simulations carried out in [35], this power limitation depends on the structure employed for the headstage. Up to 20 mW of power dissipation in the shank can be tolerated without increasing the temperature of the tissue by one degree. The amplifier's power consumption at the electrode interface and, consequently, the thermal noise contribution of this stage, will therefore be kept at the same level as in conventional AFE structures by properly designing the neural interface.

Reducing the area of the electrode interface makes it possible to increase the number of recording channels and, in turn, the recording density of the neural device. Keeping the electrode pitch constant (so as not to increase the electrode impedance), the active area will decrease with the size of the amplifier located in the electrode interface, establishing a trade-off between the CMOS area and the amplifier's flicker noise contribution. While no such huge impact has been reported in the action potential band [45], the effect of this noise becomes significant for LFP recording. Assuming that the input pair transistors will occupy a maximum of 50 % of the active area, this area-flicker noise trade-off can be quantified. Simulations were carried out and compared with the theoretical results (Figure 2.7). For these simulations, I_b was set at 2 μA and

the size of transistors $M3$, $M4$ and $M5$ was kept constant, ignoring their noise contributions. As can be seen in Figure 2.7, for small active areas, the IRN flicker noise for theLFP band is up to 20 times larger than in conventional topologies [47].

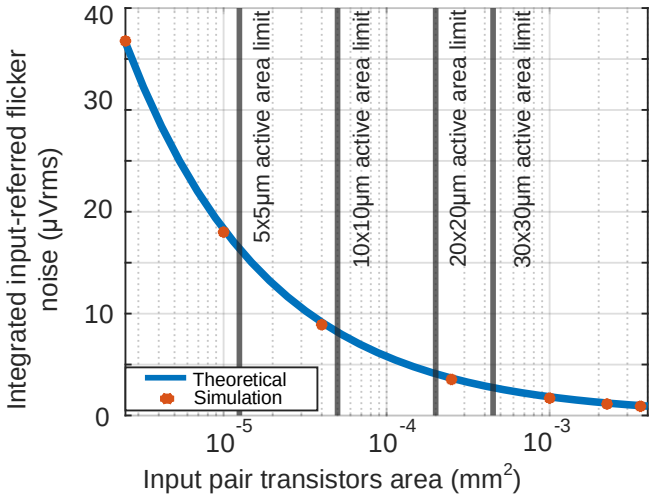


Figure 2.7: Integrated input-referred flicker noise contribution of the input differential pair against the area of the transistors.

2.3 Neural Recording Front-ends

Conventional architecture of neural recording front-ends was presented in Figure 2.3. Over the years this standard has gradually been adapted according to the requirements of each specific system and to optimize the performance of the circuit. Thus, five different high-performance approaches for neural front-ends have been simplified and illustrated in Figure 2.8.

The traditionally adopted AC coupled topology, also known as Continuous-Time (CT) AFE [10, 48, 32, 49], is shown in Figure 2.8 (a). The basic structure of the IA was presented in [50]. This topology obtains large input impedances by reducing the size of the input capacitors. To reject the input DC offset from electrodes a High-Pass Filter (HPF) is embedded within the IA. The pole of this filter is set by the input capacitors and a pair of feedback resistors. Using Pseudoresistors (PR) is a common technique for setting this pole at sub-Hz frequencies without penalizing the area of the AFE. However, these resistors present large temperature and process variations [51]. In terms of noise, IAs are usually made up of large area input transistors due to the lack of specific techniques for low-frequency noise rejection. Finally, these architectures are prone to saturation by input artifacts because of their high gain and large time constant.

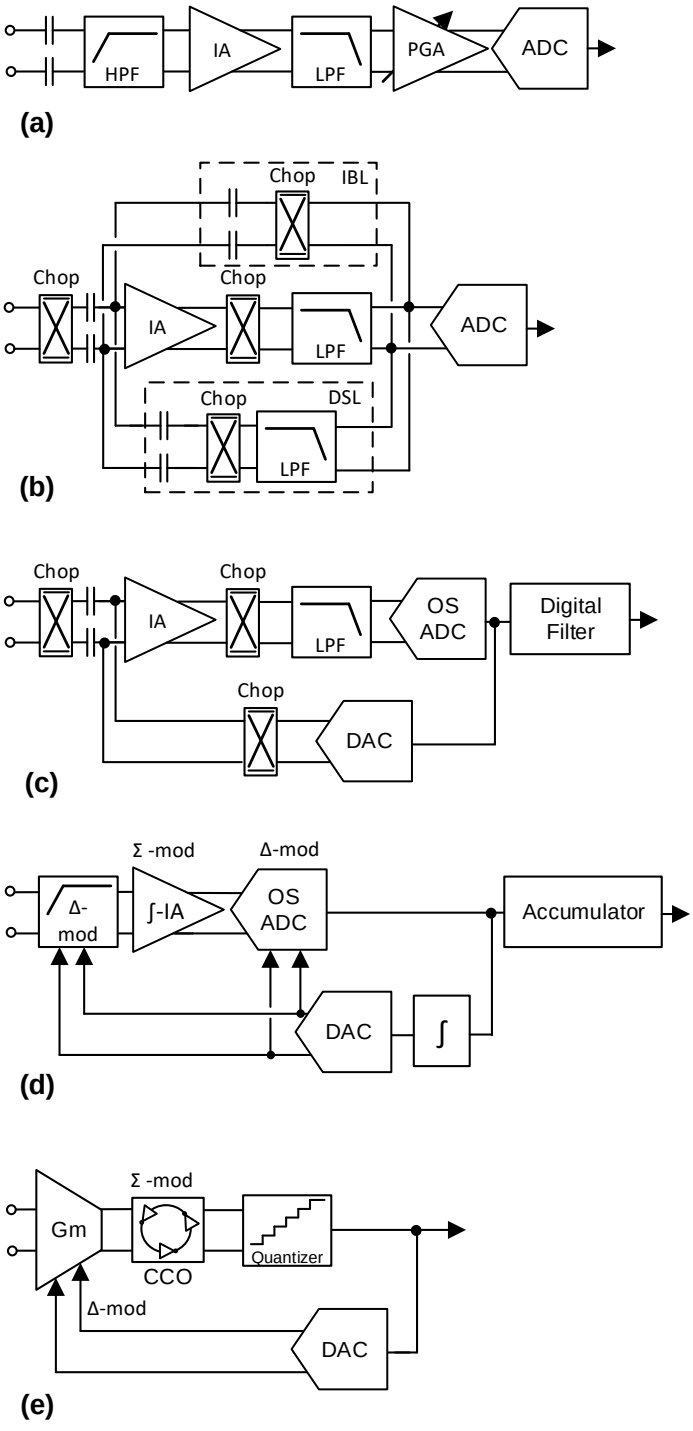


Figure 2.8: Block diagram of high-performance neural front-ends. (a) Continous-Time AFE toplogy. (b) Chopper-stabilized AFE topology. (c) DC coupled chopper-based Δ-AFE topology. (d) DC coupled $\Delta^2\Sigma$ AFE topology. (e) VCO-Based $\Delta\Sigma$ AFE topology

In recent years, chopper-stabilized AFE topologies, as shown in Figure 2.8 (b) and (c), have proven their efficiency in reducing the flicker noise component of the IA. In these architectures, the input impedance is inversely proportional to the chopping frequency and the input capacitor value. To boost this impedance, two main techniques have been reported: i) including an Impedance Boosting Loop (IBL) by means of a positive feedback network [52] (Figure 2.8 (b)), presenting large variations of the input impedance value due to process variations; ii) employing an auxiliary input path [47], penalizing the input-referred noise of the system. These DC-coupled topologies require a different mechanism to remove the input DC offset from the electrode. One widely adopted solution consists of employing a DC Servo Loop (DSL) (Figure 2.8 (b)) in the analog domain [47, 52, 53, 54] or in the digital domain [25] (not illustrated).

Another chopper-based approach relies on working with Δ-signals. In these structures, the input of the AFE is fed with the previous [41] or the predicted [55] value of the input signal (Figure 2.8 (c)) by employing a mixed-signal loop. An integral or accumulative stage is required in the analog or digital domain is required to reconstruct the signal (not shown in the figure). This technique also increases the dynamic range of the AFE at the cost of requiring an Oversampled ADC (OS ADC).

Besides conventional AFE topologies, some alternatives based on $\Delta^2\Sigma$ have been presented with promising results [56, 57] (Figure 2.8 (d)). A similar approach based on CT $\Delta\Sigma$ is reported in [39]. Some of these architectures are also known as ADC-direct schemes and do not present IAs. In these systems, the input signal is Δ-modulated, similar to Figure 2.8 (c). Then, during amplification the signal is Σ-modulated and, finally, Δ-modulated again in the analog-to-digital conversion, increasing the SNR. As in chopper-based AFEs, however, the input impedance depends on the modulation frequency. To improve that, a Δ-modulation opamp-less topology was presented in [58, 59] increasing the input impedance to the GΩs.

Voltage-Controlled Oscillator (VCO)-based circuits have recently proven to be an efficient low-power alternative to conventional AFEs [60] and low-frequency filters [61]. In these topologies, an AC-coupled input transconductance, G_m, converts the input voltage to current, which is translated to phase by a Current-Controlled Oscillator (CCO) and, finally, converted to the digital domain by a quantizer. Due to the open-loop nature of the AFE, for large input signals the G_m suffers from strong non-linearity, requiring an extra digital circuit calibration at the output of the quantizer. A different approach to implementing VCO-based front-ends is reported in [62, 63, 64] and shown in Figure 2.8 (e). To solve the dynamic range problem, a mixed-signal loop is employed to perform a $\Delta\Sigma$ loop. As in the previously presented topologies, these Δ-signals at the input eliminate the DC-offset from the electrodes and allow the G_m to work in the linear region for a larger input range. However, the low-frequency noise contribution of the G_m is not reduced and large input transistors are needed to keep it within the system's noise margins.

Table 2.2 summarizes the main advantages and drawbacks of the reported architectures. It is worth pointing out that C_{in} refers to the input capacitor value, f_{ch} is the chopper frequency and C_p is the parasitic input capacitor of the amplifier.

Table 2.2: High-Performance Neural Front-End Comparison.

	Continuous-Time	Chopper-stabilized	Chopper-Δ	Δ Σ	VCO - Δ Σ
Input impedance	$\frac{1}{2\pi C_{in} f}$	$\frac{1}{2\pi C_{in} f_{ch}}$ *	$\frac{1}{2\pi C_{in} f_{ch}}$	$\frac{1}{2\pi C_p f}$	$\frac{1}{2\pi C_{in} f}$
Main noise contributor	Flicker	Thermal	Thermal	Flicker / Thermal	Flicker
High-pass Filter	Embedded within the IA	Analog/Digital DSL	Δ-modulation	Δ-modulation	Δ-modulation
Pros	High and accurate gain Input impedance	Flicker reduction	Flicker reduction Area and power saving	Input impedance DC offset removal Area and power saving	Input impedance DC offset removal Area and power saving
Cons	Flicker contribution Area Dynamic range	Input impedance Limited DC offset removal	Input impedance	Flicker contribution	Linearity Flicker contribution

* Without IBL.

2.3.1 State-of-art Comparison

A state-of-art comparison of the employed LNA topologies is shown in Figure 2.9 and 2.10. Herein, Figure 2.9 (a) illustrates the Noise Efficiency Factor (NEF) against the area per channel. Note that the green-red scale of the symbols shown indicates the IRN value of each reported scheme, the green ones being the lowest IRN values and the red ones the highest IRN values. In Figure 2.9 (b), all the front-ends presented in Section 2.3 are denoted as digitally-assisted except for those shown in Figure 2.8 (a). It can be seen how chopper-stabilized LNAs offer the lowest IRN at the cost of increasing the area per channel. Proposed solutions based on $\Delta\,\Sigma$ AFEs and mixed-signal feedback offer some of the best performances in terms of noise and area per channel. Figure 2.10 (b) compares the LNA supply current with the normalized IRN. In this comparison, CT LNAs show better results than digitally-assisted front-ends, due to their employment of low-power analog blocks instead of complex mixed-signal loops. Moreover, CT LNAs usually present higher bandwidths than digitally-assisted front-ends, especially those using the chopper-stabilization technique requiring high chopper frequencies.

Finally, Tables 2.3 and 2.4 summarises the state-of-art of neural recording AFEs. In these tables, the main specifications of the reported front-ends are compared in order to provide a clear view of the evolution of these devices over the years and the pros and cons of the presented architectures. It is significant to point out some considerations about the tables: i) most of the ac coupled / dc coupled topologies are CT topologies. ii) MS loop refers to mixed-signal loop. iii) CTSD represents continuous-time sigma-delta topologies. iv) Mux structures define Time-Division Multiplexing (TDM) AFEs (detailed in Section 4.3).

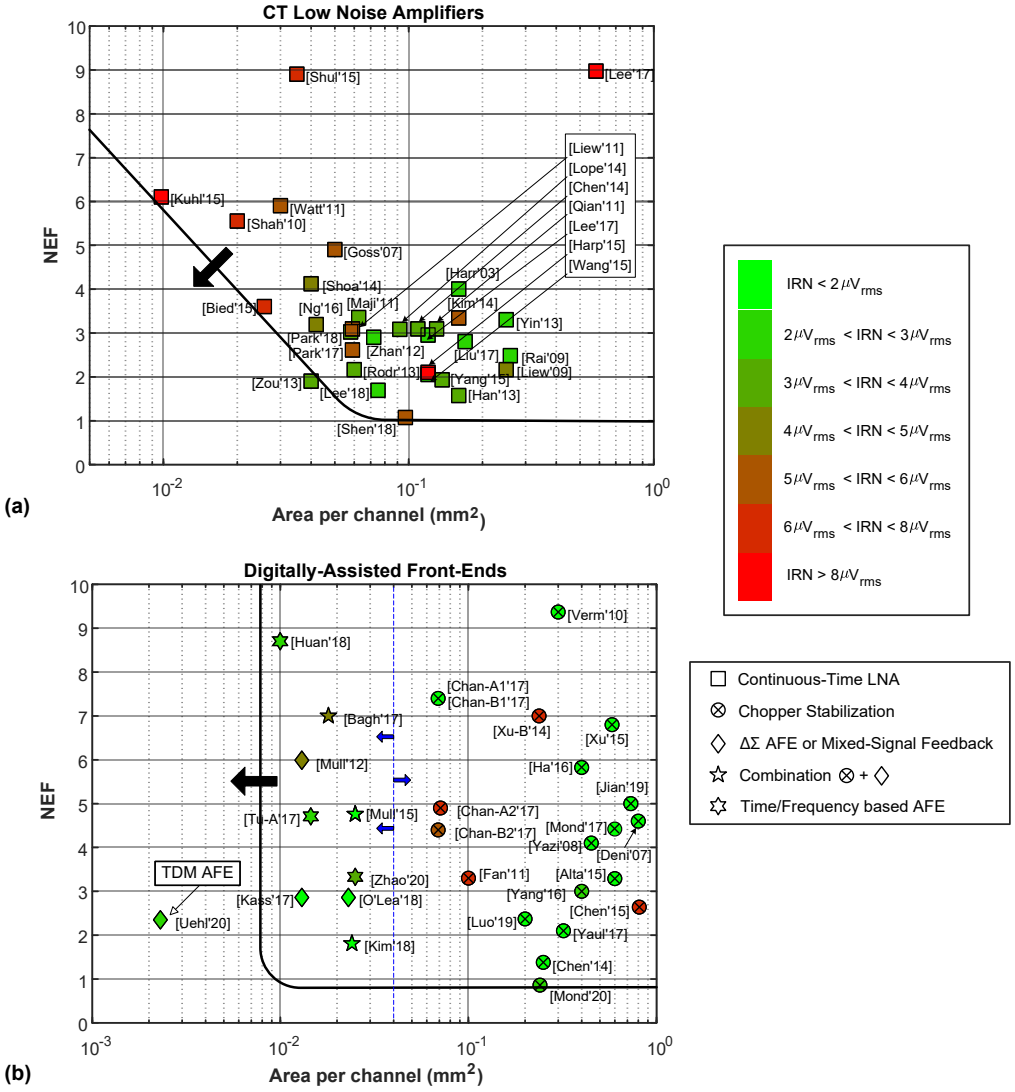


Figure 2.9: LNA's state-of-art NEF vs area per channel comparison.(a) CT LNAs. (b) Digitally-Assisted Front-ends.

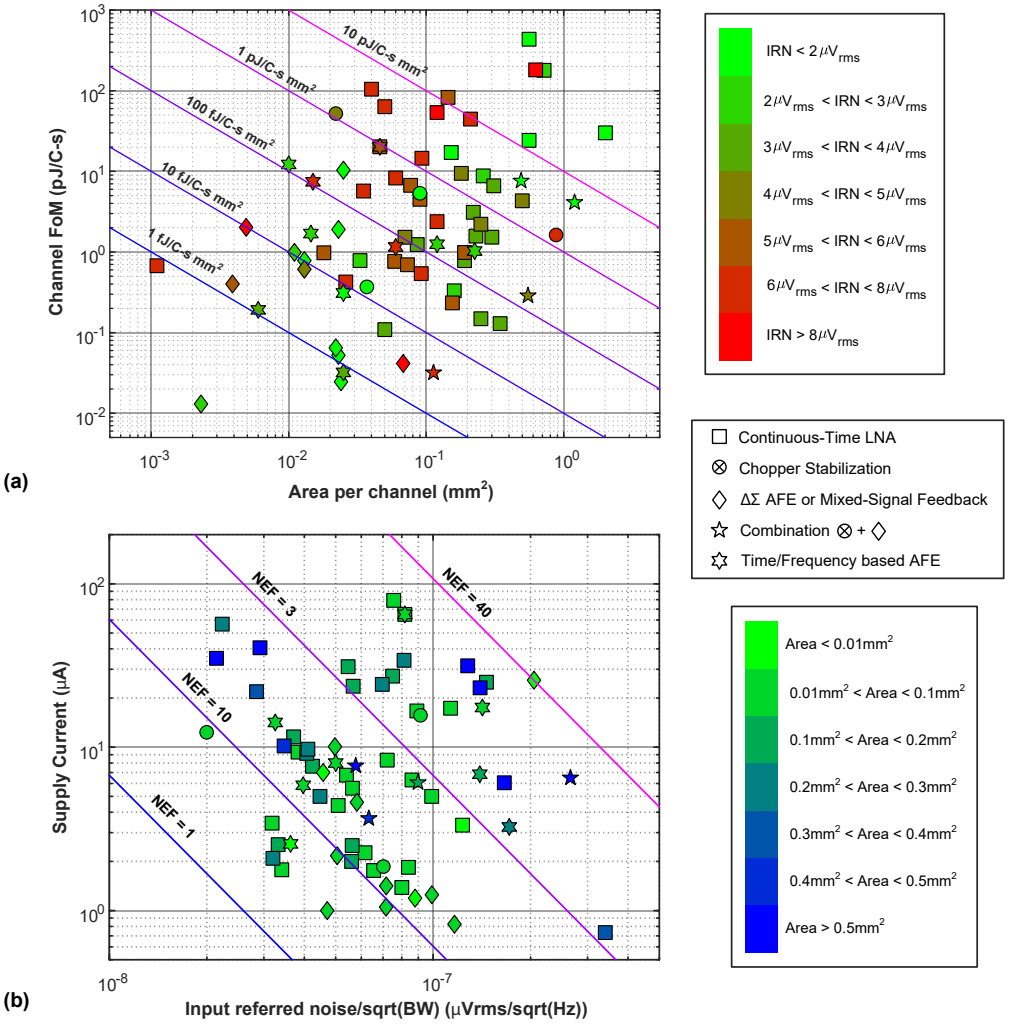


Figure 2.10: LNA's state-of-art (a) channel FoM vs area per channel comparison. (b) supply current vs normalized IRN comparison.

Table 2.3: State-of-art of Neural AFEs (1).

Reference	Year	Topology	Process (μm)	Application	Gain (dB)	Bandwidth (Hz)	Noise floor nV/(Hz)$^{1/2}$	IRN (μV_{rms})	Power (μW)	Supply (V)	Dynamic range (THD <1%) (dB)	NEF / PEF	Input range (mV)	THD 1% (mVpp)	CMRR (dB) / PSRR (dB)	DC offset rejection (mv)	Area (mm-sq)	Input impedance @ 1Khz (MΩ)
[50]	2003	ac coupled	1.5	LFP-AP	39.5	0.025-7.2k	21	2.2	80	5	69	4 / 80	-	16.7	83 / 85	full	0.16	7.96
[65]	2004	dc coupled	1.5	LFP-AP	39.3	0-9.1k	-	7.8	114.8	3	47.1	19.4 / 1129.08	-15 - 15	5	- / -	50	0.107	
[66]	2007	CT dc coupled	0.18	AP	49.52	98.4-9.1k	55	5.6	8.4	1.8	45	4.9 / 43.2	-	2.4	52.68 / 51.93	450	0.05	NA
[67]	2011	ac coupled	0.18	LFP-AP	49-66	350-11.7k	-	5.4	16.6	1.8	-	5.9 / 62.65	-	-	62 / 72	full	0.03	
[68]	2009	ac coupled	0.35	LFP-AP	45.7-60.5	217-7.8k	-	4.43	1.26	1	-	2.16 / 4.67	-	0.53 (full swing)	58 / 40	full	0.25	
[69]	2011	ac coupled	0.13	AP	48-54	40-7.5k	-	5.32	0.86	0.5	-	3.09 / 4.77	-	-	- / -	full	0.059	
[70]	2011	ac coupled	0.18	AP	39.4	10-7.2k	-	3.5	7.92	1.8	58.4	3.35 / 20.2	-	5.7	70.1 / 63.8	full	0.0625	7.96
[71]	2009	ac coupled	0.13	LFP-AP	38.3	23m-11.5k	-	2.2	12.5	1	-	2.48 / 6.15	-	1	63 / 63	full	0.26	
[72]	2012	ac coupled	0.13	LFP-AP	40	50m-10.5k	-	2.2	12.1	1	-	2.9 / 8.41	4	1	80 / 80	full	0.072	4
[73]	2013	ac coupled	0.6	LFP-AP	46	1-7.8k	-	2.83	60	3	-	3.3 / 32.67	-	-	50 / 60	full	0.25	
[74]	2010	ac coupled	0.35	LFP-AP	33	0.5-10k	-	6.08	8.4	3	-	5.55 / 92.40	-	-	60 / -	full	0.02	35.39
[75]	2014	ac coupled	0.18	AP	29.8	28-144k	-	4.2	8.4	1.2	-	4.12 / 20.37	-	2 (0.24% THD)	59.8 / -	full	0.04	
[76]	2011	ac coupled	0.6	Fast-ripples	39.4	0.36-1.3K	60	3.07	2.4	2.8	54	3.09 / 26.73	-	10	66 / 80	full	0.13	
[77]	2013	ac coupled	0.18	LFP-AP	49	0.25-(2.5-10)k	29	3.2	0.73	0.45	56	1.57 / 1.12	-	2.8 (0.53% THD)	73 / 80	full	0.16	
[78]	2013	ac coupled	0.18	LFP-AP	54.8-60.9	0.38-5.1k	40	4	0.81	1	-	1.9 / 5.6	-	0.9	60 / 70	full	0.04	7.96
[79]	2015	ac coupled	0.35	LFP-AP	32	0.1-10 to 500-10k	-	7.99	12.9	3	-	8.9 / 237.6	-	1 (0.8% THD)	60 / -	full	0.035	
[80]	2015	ac coupled	0.065	LFP-AP	26	10-1k to 3k-8k	-	7.5	1.2	1	-	3.6 / 12.9	-	-	- / -	full	0.0258	
[81]	2015	ac coupled	0.18	AP	26	140-20k	60	11.9	14.76	1.8	-	6.1 / 67	-	11	59.2 / 53.5	full	0.0098	
[82]	2015	ac coupled	0.35	LFP-AP	40.3	0.01-10k	-	2.81	9	2.5	63.7	2.05 / 10.50	3	4.3 (0.1%)	82 / 82	full	0.12	
[83]	2015	ac coupled	0.065	ECG	32	1.5-370	1400	26	0.0015	0.6	-	2.1 / 2.64	-	-	60 / 63	full	0.12	
[45]	2014	ac coupled	0.18	AP	30-72	300-6k	-	3.2	7.02	1.8	-	3.08 / 17.13	-	18	60 / 76	full	0.092	
[84]	2012	dc coupled MS loop	0.065	AP	32	300-10k	48	4.9	4.79	0.5	-	5.99 / 17.96	-	0.1 (2%)	75 / 64	20	0.013	1000
[25]	2015	chopper	0.065	ECoG. LFP	30	1-400	58	1.25	2.3	0.5	-	4.76 / 11.3	-	1 (0.4%)	88 / 67	50	0.025	28
[85]	2017	CT dc coupled	0.13	AP	44	20-15k	-	3	11	1	-	2.95 / 8.68	2.2	1 (0.8%)	- / 41	-200 - 100	0.12	61
[86]	2016	ac coupled	0.065	LFP-AP	52.1	1-8.2k	-	4.13	3.28	1	-	3.19 / 10.2	220	1.4	90 / 78	full	0.042	21
[9]	2014	ac-coupled	0.18	AP	54.2	0.0-5.7k	-	3.83	2.52	1	66	3.09 / 9.72	-	1.54 (0.2%)	65 / 67	-	0.109	NA
[87]	2017	chopper	0.18	LFP	57.8	0.0-670	36	0.94	0.79	0.2/0.8	-	2.1 / 1.6	2.1	1.6 (0.33%)	85 / 74	NA	0.32	100
[52]	2011	chopper	0.065	LFP	40	0.5-500	60	6.7	1.8	1	-	3.3 / 10.89	-	-	134 / 120	NA	0.1	30
[88]	2015	chopper	0.18	EEG. LFP	40	0.07-1k		0.9	1.62	1.8	-	3.29 / 19.49	-	-	97 / -	240	0.6	>500
[89]	2008	chopper	0.18	EEG. LFP	46	0.5-315/675	55	0.59	6.9	3	-	4.1 / 50.43	45	1.65	120 / 89	45	0.45	1000@1Hz
[90]	2015	(dc) chopper	0.18	EEG. LFP	36.9	0.5-100	60	0.65	13.32	1.8	-	6.8 / 83.23	0.5-1.2	-	102 / -	350	0.58	1000@1Hz
[91]	2018	chopper	0.04	EEG. LFP	30	2-150	145	1.85	3.8	0.6	-	14.71 / 129.83	400	-	87 / -	300	0.16	140.00
[92]	2015	chopper	0.065	LFP	51-96	0.5-250	253	6.52	0.017	0.6	48.6	2.64 / 4.18	-	0.5 (2.87%)	55 / 67	-	0.81	110.00
[93]	2007	chopper	0.8	LFP	50.5	0.05-120	100	1.1	2	1.8	-	4.6 / 38.1	-	5 (0.1%)	100 / -	50	0.8	8
[94]	2010	chopper	0.18	LFP	36	0.1-100	130	1.3	3.5	1	-	9.37 / 87.7969	-	-	60 / -	1000	0.3	700

Table 2.4: State-of-art of Neural AFEs (2).

Reference	Year	Topology	Process (μm)	Application	Gain (dB)	Bandwidth (Hz)	Noise floor nV/(Hz)$^{1/2}$	IRN (μV_{rms})	Power (μW)	Supply (V)	Dynamic range (THD <1%) (dB)	NEF / PEF	Input range (mV)	THD 1% (mVpp)	CMRR (dB) / PSRR (dB)	DC offset rejection (mv)	Area (mm-sq)	Input impedance @ 1Khz (MΩ)
[47]	2017	chopper	0.04	LFP	25.7	0.12-5k	80	1.8	2.8	1.2	81	7.4 / 65.71	40	40 (-76dB THD)	78 / 76	650	0.069	1600
[95]	2017	chopper	0.04	LFP-AP	25.7	0.12-5k	80	5.3	2.8	1.2	74	4.4 / 23.23	40	40 (-76dB THD)	78 / 76	650	0.069	1600
[39]	2018	chopper + CTSD	0.04	LFP	-	1-200	-	2.9	4.5	1.2	108.4	15.3 / 280.9	-	(102.5 SFDR)	81.2 / -	-	0.053	20
[96]	2015	ac-coupled	0.09	LFP-AP	58.7	0.49-10.5k	-	3.04	2.85	1		1.93 / 3.72	-	1(1.6%)	50 / 45	-	0.137	-
[97]	2017	chopper	0.13	LFP-AP	50.7-54	1-5k	-	5	9.9	1.2	-	7 / 58.8	50	1	65 / -	50	0.018	1000
[57]	2017	Sigma-Delta	0.13	LFP	-	0.01-500	-	1.13	0.63	1.2	-	2.86 / 9.81	-	-	90 / 95	rail-to-rail	0.013	1
[98]	2016	chopper	0.13	AP	45-71	1-7k	34	2.93	5.9	1.2	-	3 / 10.8	-	1	95 / -	-	0.4	100
[99]	2020	chopper	0.18	ECoG. LFP	36	0.1-240	158	2.84	0.0187	1.35	-	0.86 / 0.99	-	1000(-57dB THD)	95 / 68	-	0.24	87
[32]	2018	ac-coupled	0.18	LFP-AP	38.5	0.4-10.9k	-	3.32	3.05	0.5	-	3.02 / 4.56	-	3(74SFDR)	60 / -	-	0.058	20
[100]	2019	chopper + CTSD	0.18	LFP	40	0-1k	3.7	0.12	2160	1.8	-	5 / 44	10	-	134 /	100	0.73	1
[101]	2014	ac-coupled	0.18	LFP-AP	60	1-6.8k	-	5.4	0.88	0.5	-	3.34 / 5.57	-	-	- / -	-	0.16	-
[102]	2018	Sigma-Delta	0.065	LFP	5.95	1-500	44	0.99	0.8	0.8	92	1.81 / 2.62	-	-	81 / -	260	0.024	26
[103]	2018	Sigma-Delta	0.13	LFP	-	0.01-1k	-	1.6	1.26	1.2	70	2.86 / 9.8	rail-ro-rail	-	- / -	rail-ro-rail	0.023	-
[104]	2019	chopper	0.18	LFP	40	0.35-5.4k	39	0.65	3.24	1.8	-	2.37 / 10.11	-	5 (-61dB THD)	100 / -	50	0.2	440
[12]	2020	Mux Gm-C SAR	0.065	LFP	60	1-1k	80	2.78	2.98	2.5	96.27	2.35 / 13.80	110	-	76 / 82	-	0.0023	92
[105]	2018	ac-coupled	0.18	LFP-AP	25.6	4-10k	-	5.6	0.25	1	-	1.07 / 1.14	Inf	-	81 / 81	-	0.097	-
[106]	2018	chopper + CTSD	0.18	LFP	-	0-300	-	4.6	6.5	1	84.3	26.03 / 677.5	360	180 (104.7 SFDR)	84 / -	-	0.55	39
[107]	2018	chopper	0.065	EEG. LFP	40	0.5-250	-	4.5	5.4	1.2	-	3.59 / 15.46	-	-	110 / -	350	3.75	1000
[108]	2018	chopper T-ADC	0.065	LFP	-	0.1-500		2.2	3.2	0.6	51	8.7 / 45.41	47	62dB SFDR	77 / 65	47	0.01	500
[60]	2017	VCO-ADC	0.04	LFP	-	1-200	-	5.2	7	1.2	79	34.23 / 1406.0	50	-	66 / -	50	0.135	Inf
[109]	2017	chopper T-ADC	0.04	LFP-AP	-	0-5k	32	2.3	17	1.2	61.8	4.71 / 26.62	8	4 (70.8 THD)	97 / 91	-	0.0145	70
[110]	2017	chopper T-ADC	0.04	LFP	-	1-150	600	7.8	3.3	0.6	56	57.61 / 1991.3	150	40	60 / -	50	0.015	50
[111]	2019	VCO-ADC	0.04	LFP	-	1-250	100	2.2	8.2	1.2	81	14 / 235.2	100	-	- / -	100	0.12	Inf
[112]	2020	VCO-ADC	0.04	LFP-AP	-	0-10k	36	3.58	4.68	0.8	79	3.33 / 8.87	100	(91dB SFDR)	83 / 80	100	0.025	-

CHAPTER 3

ARTIFACT-AWARE TECHNIQUES FOR ANALOGUE/MIXED-SIGNAL NEURAL FRONT-ENDS

Some of the most common applications for neural recording systems require the implementation of a closed-loop sensor/actuator mechanism to interact with the brain and, hence, neural recorders have to co-exist with stimulators, often integrated on the same silicon die. Neural stimulation typically induces strong reactions (artifacts) in the tissue [113, 114, 115]. These artifacts may last for tens of milliseconds and may reach up to tens of mVs and depend on the stimulator architecture and performance, the stimulation waveform and the electrode configuration. Further, the amplitude of the artifacts increases with the proximity between the stimulation and the recording electrodes and, hence, the problem is more acute in dense multi-electrode arrays if both operations, stimulation and recording, are jointly implemented in the probe (as illustrated in Figure 3.1). These interferences not only corrupt the captured neural signals but it may also lead to the saturation of the recording front-end. An example of the PSD of a contaminated recorded LFP by a stimulation artifact is shown in Figure 3.2 [7]. It is worth seeing from Figure 3.2 how the spectral components of the stimulation artifact overlap the information contained by the LFP signal. Hence, in these closed-loop devices, neural recording systems not only should exhibit low noise, low power and low area occupation [10, 47] but they should also render tolerant to the large artifacts generated by the stimulation pulses. Together with neural stimulation, other large interfering signals may also contaminate recording, for instance, by sudden alterations of the tissue-electrode interface due to motions [47], [13]. As long as these interferences have a similar

effect on the recorded data as stimulation artifacts, in this work, we will regard both cases as artifacts and simply distinguish between CM and Differential-Mode (DM) artifacts, depending on the kind of perturbation received by the neural signal.

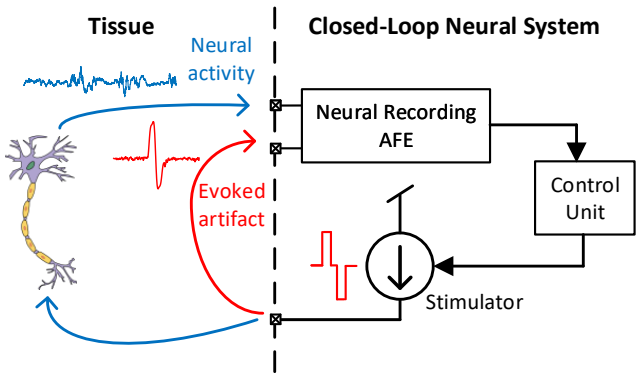


Figure 3.1: Simultaneous stimulation and recording in a closed-loop neural system.

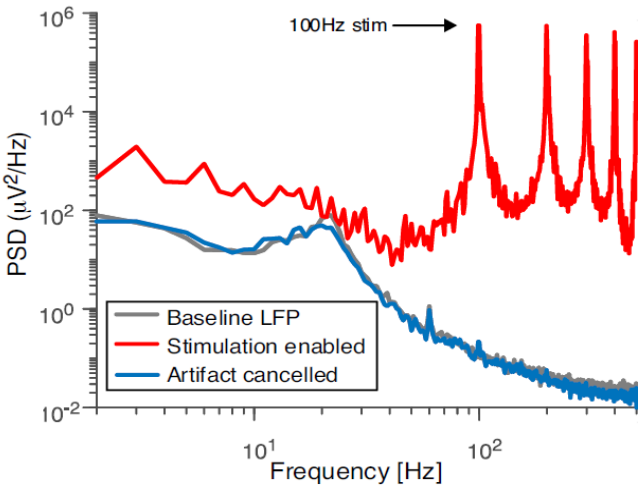


Figure 3.2: LFP signal contaminated by the stimulation artifact [7].

Figure 3.3 illustrates the amplitude and frequency ranges of neural signals (only LFPs and APs are shown) as compared to CM and DM artifacts [47]. As can be seen, while frequencies overlap, amplitude differences may be orders of magnitude different.

The use of fully-differential structures with large CMRR allows reducing the impact of CM artifacts. However, residual CM components in the differential signal path may still degrade system performance. To cope with this problem, CT [47] and Discrete-Time (DT) [11, 12] solutions applied at the input of the recording front-end have been proposed. DM artifacts are typically smaller than CM artifacts, however, their effect is more deleterious because they superpose

on the neural signal component which conveys useful information. DM artifacts could be handled by increasing the input dynamic range of the neural recorder and raising the resolution of the following ADC so as to convert both neural signals and artifacts. For example, the resolution of an DM intended for LFP recording should be increased from 10-12 bits to some 14-15 bits if artifacts have to be covered as well [14]. Obviously, this would significantly increase the area and power consumptions of the recording system and, for this reason, other artifact-aware front-end topologies have been recently proposed. In this work, we will make a brief review of these artifact-aware algorithms and structures and analyze their pros and cons.

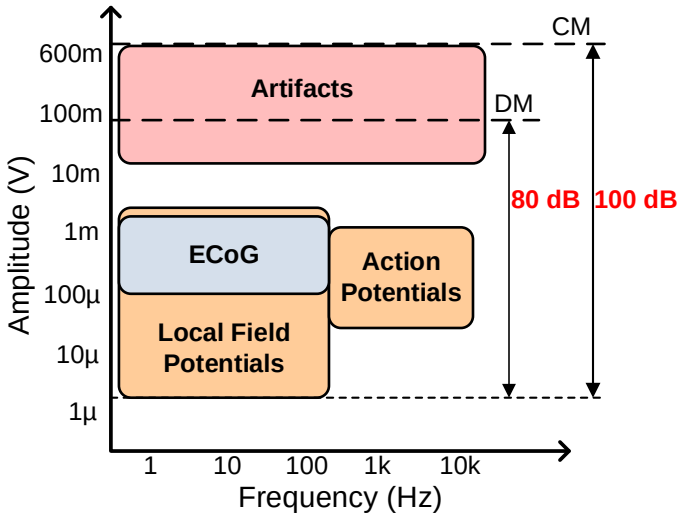


Figure 3.3: Specifications of recorded neural signals.

3.1 DM Artifacts-Aware Techniques

Artifact-aware topologies are aimed to relax the performance requirements of the neural recording system in terms of input dynamic range and/or converter resolution even when artifacts contaminate neural signals [116]. Some of these topologies are analyzed below and illustrated in Figure 3.4.

3.1.1 Channel Blanking

Figure 3.4 (a) illustrates the basic structure of the channel blanking technique [117]. The operation principle consists in disconnecting the recording channel from the tissue when an artifact is present. This disconnection has many alternatives: electrode disconnection, PGA isolation, high-pass pole shifting, etc. However, this only works when intentional stimulations are applied to the brain but it is useless for unpredictable interferers. Further, the technique carries out

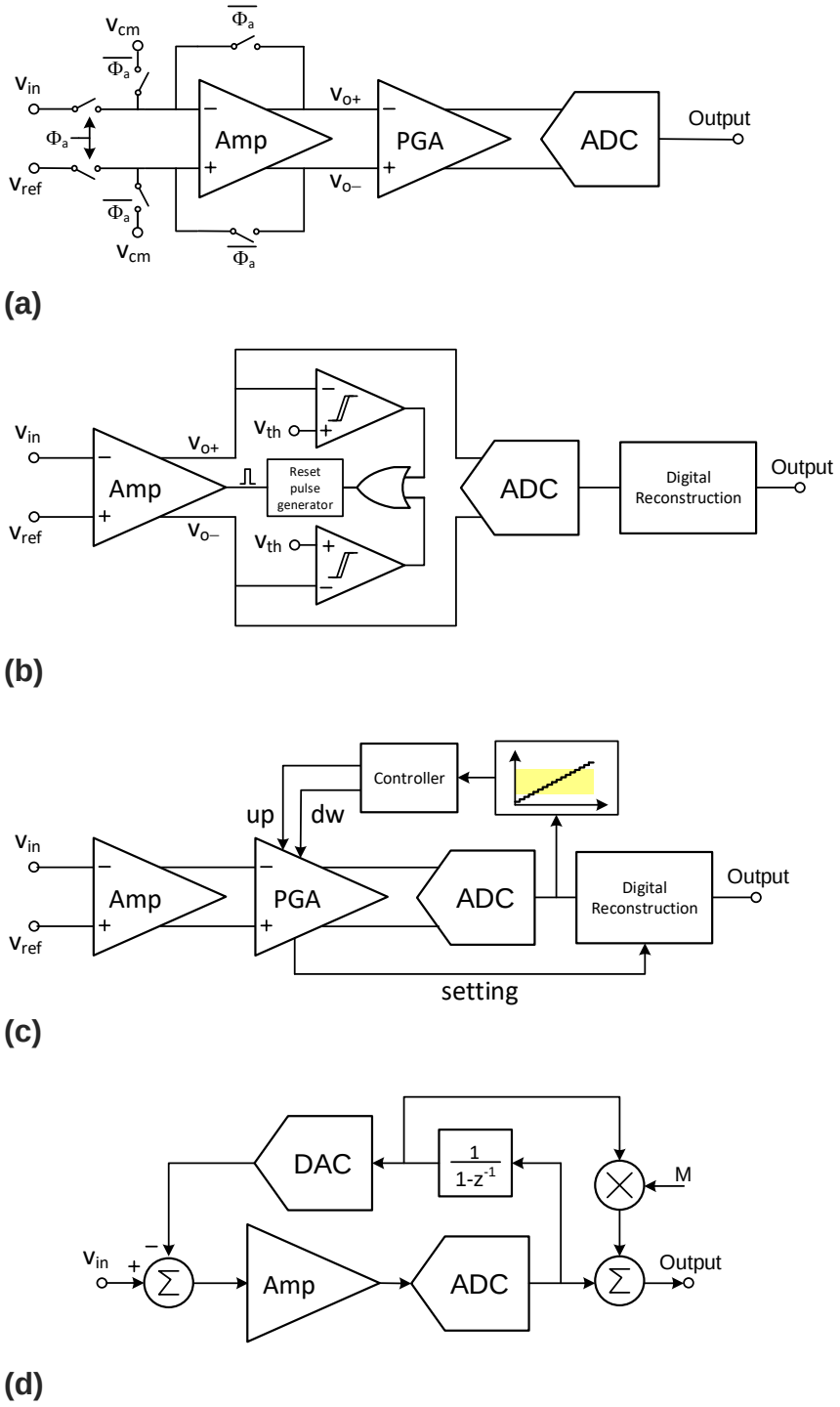


Figure 3.4: DM artifacts-aware techniques. (a) Channel blanking technique. (b) Signal Folding. (c) PGA tuning. (d) Δ-based technique.

a complete loss of information while the recording channel is disconnected. For

this reason, data reconstruction with interpolation techniques have been proposed [118]. Another potential problem is the long recovery time after blanking unless proper techniques are adopted [41, 119].

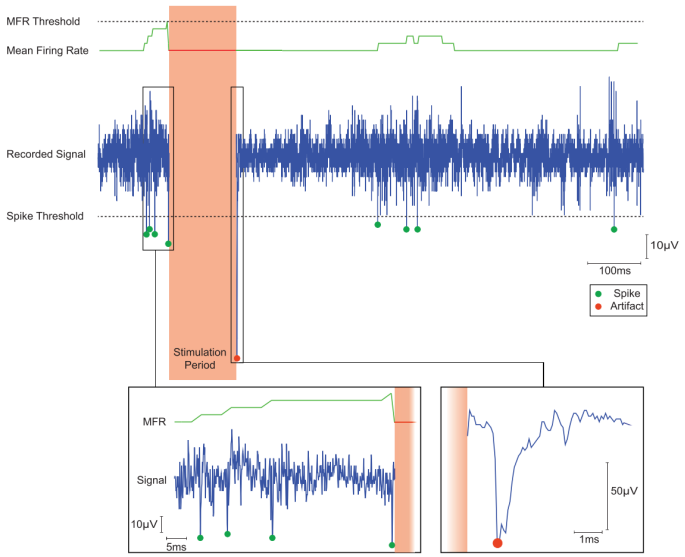


Figure 3.5: Example of the performance of the channel blanking technique [8].

An example of the performance of the channel blanking technique is shown in Figure 3.5 [8]. When the stimulation occurs, the recording path is disconnected from the input and the information is totally missed during that period.

3.1.2 Signal Folding

Another technique employed to avoid saturation in the front-end is signal folding [120, 9]. The operation principle is shown in Figure 3.4 (b). In this technique, the output voltage of the amplifier is compared with a fixed threshold voltage through a pair of comparators. If the magnitude of the output voltage is higher than this threshold a pulse resets the output node of the front-end amplifier to the nominal CM level. This way, saturation is avoided and the ADC requirements are relaxed. An example of the application of this technique is shown in Figure 3.6 [9]. It can be observed that without applying the signal folding technique (Figure 3.6 (a)) a 10-bit ADC is required to cover the whole range of the signal. When the signal folding technique is enabled, every time the signal surpasses the threshold voltage, the output is forced to the CM voltage. Herein, the input range of the ADC is reduced to 8 bits.

This technique demands a reconstruction method to recover the amplified signal when it is reset. Firstly, the derivative of the output signal is calculated and compared with a threshold to determine if a reset has occurred. Then, after discarding some data points after reset (due to the settling time of the amplifier), the missing signal is computed by polynomial interpolation of the derivative

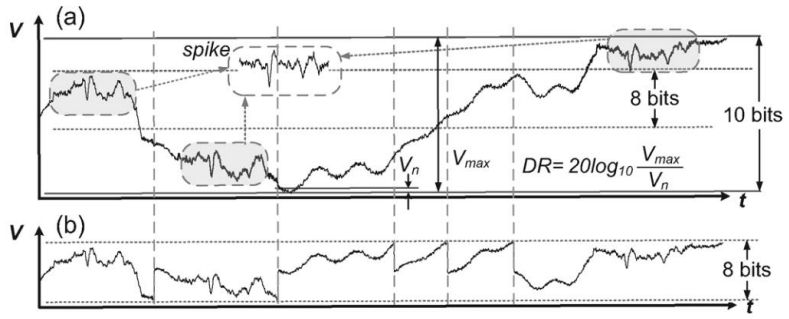


Figure 3.6: Example of the signal folding technique [9]. (a) Output signal (a) without applying the signal folding technique. (b) applying the signal folding technique.

signal. Finally, this interpolated signal is integrated to reconstruct the original output signal.

This topology shows two main shortcomings. On the one hand, samples after resetting are invalid due to the slow settling time of the amplifier. On the other, the reconstruction mechanism requires a correction algorithm which could involve an extra significant computational cost to the system.

3.1.3 PGA Tuning

In order to avoid saturation states due to artifacts, the gain of a PGA can be set [10], as shown in Figure 3.4 (c). In this technique, a capacitor bank is employed to set the gain of the PGA. The capacitor bank is controlled by a digital circuit which, depending on the amplitude of the signal at the output of the ADC, performs a dynamic adjustment of the amplification. This method allows the signal to fit in the ADC swing. Then, depending on this amplification, the signal is scaled and reconstructed in the digital domain. An application case of this technique is shown in Figure 3.7. It is worth observing how the PGA's control codes are being continuously updated to compress the output magnitude below a fixed range.

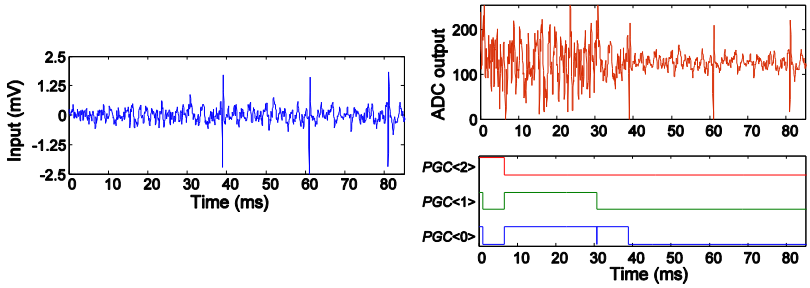


Figure 3.7: Example of the performance of the PGA tuning technique [10].

This method operates for all kinds of DM artifacts, as no disabling control is needed, and it may even address other recording problems such as the long-term degradation of the tissue-electrode interface. However, there are two main problems associated with this technique. First, it requires the PGA can be tuned over a wide amplification range, and it increases the complexity of the digital reconstruction circuit, which must scale the ADC output according to the gain value along the signal path. Second, the input-referred noise of the analog front-end and the PGA bandwidth changes with the gain setting.

3.1.4 Δ-based Techniques

Δ-based techniques are intended for reducing the ADC dynamic range requirements and for tolerating large input signals. Δ-based front-ends were previously presented in Chapter 2, Figure 2.8 (c) and (d). Two main techniques can be disclosed from these topologies: Δ-Encoding technique [11, 12] and Δ Σ modulation [57, 121]. Figure 3.4 (d) illustrates a Δ-Encoding front-end. The operation principle relies on tracking differences between successive samples at Nyquist rate (Δ-signals). This inherently places a high-pass pole at half the sampling frequency which compensates the typical 1/f spectral distribution of LFPs [32], thus, reducing the dynamic range requirements of the front-end. Further, large DM artifacts can be tolerated if they are slow enough. The performance of the Δ-Encoding technique is shown in Figure 3.8 [11, 12]. While without enabling the Δ-loop, the artifact saturates the signal path, when the technique is working the artifact is compressed to the input range of the ADC without losing information. It is worth commenting that this system also includes template-based artifact subtraction [11].

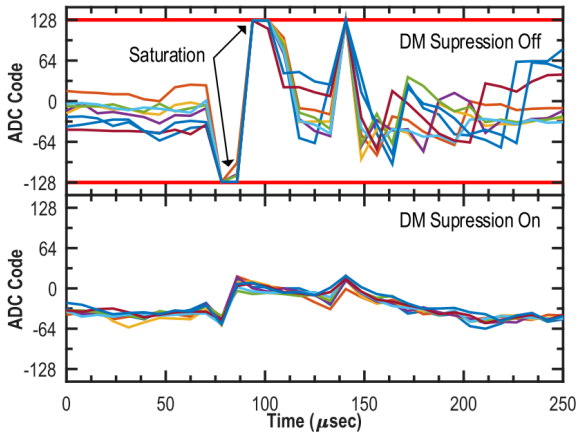


Figure 3.8: Example of the performance of the Δ-Encoding technique along with template-based artifact subtraction [11, 12].

Δ-signals are obtained at the input of the front-end amplifier by subtracting the current and previous samples, this latter regenerated through a Digital-to-

Analog Converter (DAC) from digital domain (see Figure 3.4 (d)). In order to reconstruct the signal, a scaled version of the DAC input and the ADC output are added together. The scaling factor M has to be calibrated to compensate for DAC transfer function nonidealities. As a drawback, the amplifier must have a wide bandwidth so that settling is possible between adjacent channels, potentially compromising noise performance due to aliasing and increasing power consumption.

In the case of the $\Delta\,\Sigma$ modulation, it can be considered as a straightforward extension of the Δ-Encoding technique, which follows similar operation principles combined with oversampling techniques for increasing the recorder dynamic range [57]. Examples using these topologies can be found in [57, 121, 122, 123].

3.2 CM Artifacts-Suppression Techniques

Fully-differential front-ends architectures providing high CMRR have been generally employed to cope with large CM interferences. However, for ultra low-power topologies, these artifacts can saturate the signal path or drastically change the operation point of the IA. Two reported techniques which mitigates this problem are illustrated in Figure 3.9.

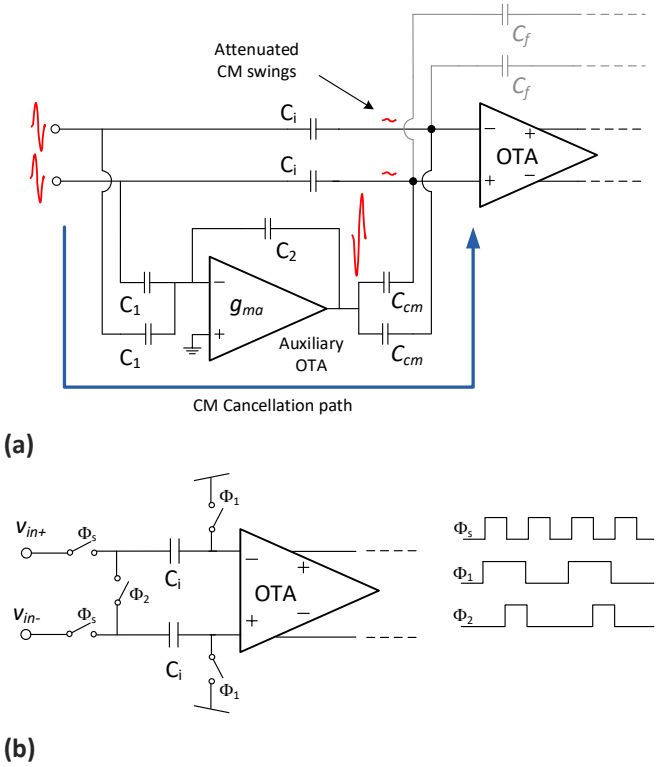


Figure 3.9: CM artifacts-suppresion techniques. (a) CM cancellation path. (b) SC CM cancellation scheme.

3.2.1 CM cancellation path

The CM cancellation path is shown in Figure 3.9 (a) [47]. In this technique, an auxiliary input path consisting of a capacitive feedback loop including a low-power Operational Transconductance Amplifier (OTA) computes the CM components of the input signal and subtracts from the input of the main OTA these components, largely canceling the CM interference. Herein, the capacitors of the auxiliary and the main path have to be properly scaled to maximize the suppression of the CM signal. Nevertheless, residual CM swings will remain at the input of the system mainly due to mismatch between capacitors. The main drawback of this suppression method is the increased IRN due to the noise contribution of the auxiliary OTA.

3.2.2 Switched-capacitor CM cancellation scheme

An alternative method to improve the CMRR which is specially interesting for open-loop front-ends relies on the employment of SC schemes which suppress the CM components from signals at the input of the front-end [11, 12]. First, as illustrated in Figure 3.9 (b), during ϕ_s and ϕ_1 the CM signal is sensed at the input capacitors. Then, when ϕ_1 and ϕ_2 are on, the switching scheme clears the DM components of the signal. At this point, with only ϕ_1 enabled, the signal is resampled and the CM components previously-stored are subtracted. It is worth observing that this technique is only valid if the switching scheme is fast enough to sense and subtract rapid CM variations.

On the other hand, including a switching scheme adds an inherent kTC noise at the input of the circuit which can increase the IRN of the front-end. Furthermore, the input impedance will be determined by the values of these input capacitors and the switching frequency. These considerations have to be taken into account when designing the scheme.

3.3 DM Artifacts-Suppression Techniques

The techniques discussed in the previous section are mainly intended for avoiding saturation in the neural recorders. However, neural activity, if not destroyed, still remains embedded in the artifact. For this reason, techniques able to suppress the artifact and recover the overlapped information are needed. These suppression techniques can use mixed-signal feedback or digital post-processing.

3.3.1 Artifacts Suppression Feedback Front-Ends

They are represented in Figure 3.10 (a). In this topology, artifact cancellation is performed at the input of the recorder amplifier, thus, avoiding the use of high-resolution ADCs. However, this is at the expense of some extra noise contribution by the DAC to the overall IRN of the recorder. To palliate this

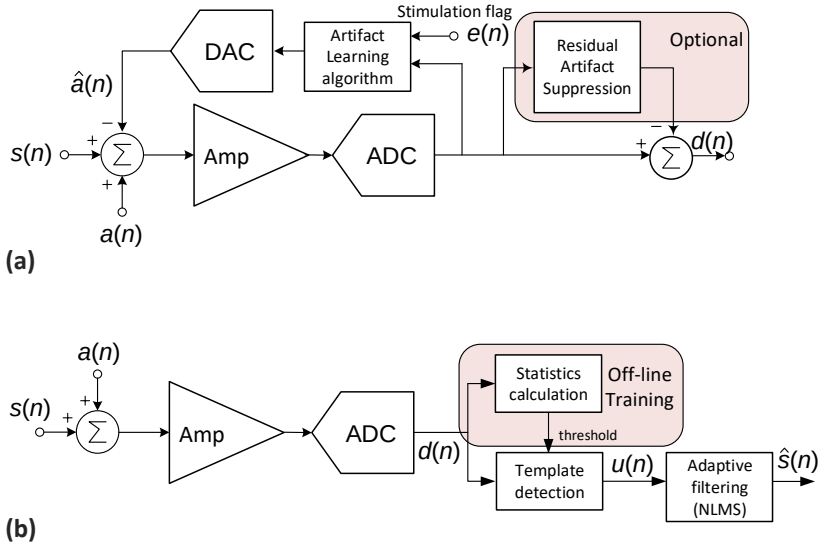


Figure 3.10: Artifacts-suppression techniques. (a) Artifacts suppression feedback front-ends. (b) Post-processing artifacts suppression front ends.

shortcoming, oversampling techniques can be used [25]. Furthermore, the clock of the circuit has to be fast enough to detect the artifact and inject the correction signal before the artifact saturates the signal path. Two of the most significant artifact suppression feedback techniques are the averaged template subtraction [124] and the adaptive stimulation filter [13].

In the first case, an artifact template is subtracted from the input of the recorder every time a new neural stimulation cycle turns on [124]. The template is calculated by means of a learning algorithm, based on recordings obtained from previous stimulation cycles. After template subtraction, a residual artifact waveform may persist in the signal path. To further enhance the artifact suppression, a post-processing digital circuit can be used to calculate the average amplitude of such residue and subtract it from the signal.

One of the main drawbacks of this approach is the high computational complexity cost and the need for offline training required for both generating the templates and calculating the artifact residues. Further, if there are substantial differences between the artifact and the stored template, the resulting residue can eventually saturate the signal path, unless a wide input range amplifier is used.

In the second case, an adaptive stimulation filter recreates the response of the neural tissue in order to subtract the artifact from the neural signal [13]. The approach takes advantage of the close correlation between the stimulation pulse, $e(t)$, and the neural tissue response, $b(t)$. Denoting by $s(t)$ and $a(t)$ the unaffected neural signal and the artifact, respectively, the recorded signal at instant n can be expressed as:

$$y(n) = s(n) + a(n) = s(n) + b(n) * e(n) \tag{3.1}$$

The objective is to generate a signal $\hat{a}(n) = \hat{b}(n) * e(n)$ such that, when subtracted to the input, gives an estimate

$$\hat{s}(n) = y(n) - \hat{a}(n) = s(n) + [b(n) - \hat{b}(n)] * e(n) \tag{3.2}$$

close to the original unaffected neural signal. The recreated response $\hat{b}(n)$ can be obtained through an adaptive filter where coefficients are updated by a Least Mean Square (LMS) learning algorithm [13]. This algorithm uses a steepest gradient descent approach to minimize errors in $\hat{s}(n)$. A simplified version of the LMS algorithm, the sign-sign LMS, facilitates hardware implementation by using a sign-bit signal representation as follows [125]:

$$\hat{b}(n) = \hat{b}(n-1) + \mu * [e(n) \times sgn(\hat{s}(n))] \tag{3.3}$$

Finally, Figure 3.11 illustrates the performance of the mixed-signal technique [13]. When the stimulation occurs without enabling the feedback cancellation block, artifacts largely contaminate the signal of interest. On the other hand, by applying the proposed scheme the artifacts are reduced with an attenuation of up to 24 dB.

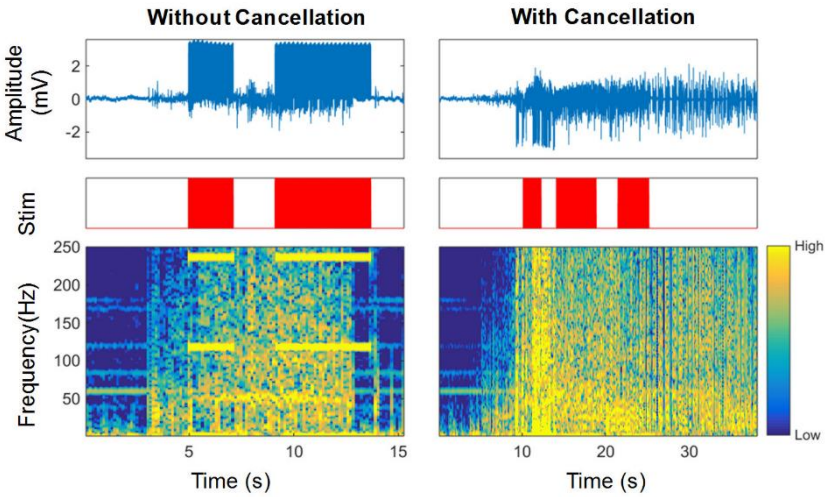


Figure 3.11: Example of the performance of a mixed-signal adaptive stimulation cancellation technique [13].

3.3.2 Post-Processing Artifacts Suppression Front-Ends

In these structures, artifacts are suppressed in digital domain with no feedback to the recorder front-end (Figure 3.10 (b)). This avoids any degradation in the noise performance, although, it demands a high dynamic range for the mixed-signal circuitry.

Herein, we will briefly review the blind ASAR proposed in [14], as a representative example of post-processing cancellation. Interestingly enough, the approach works with any arbitrary artifact with no prior knowledge about its structural and temporal shape. It relies on obtaining an artifact template $u(n)$ from an adjacent electrode. This template is detected when a threshold value, obtained from a previous statistics calculation phase in the absence of artifacts, is exceeded. If an artifact is detected in the recorded signal $y(n)$, the template $u(n)$ is applied to a Normalized Least Mean Square (NLMS) adaptive filter which updates the weighting factor, $w(n)$, as follows:

$$w(n) = w(n-1) + \frac{\mu}{||u(n)||^2 + \epsilon} u(n)^T [y(n) - u(n)w(n-1)] \tag{3.4}$$

where μ is the algorithm step-size and ϵ is a small positive parameter. To obtain a clean neural signal $\hat{s}(n)$, the estimated artifact is subtracted from the measured signal:

$$\hat{s}(n) = y(n) - u(n)w(n) \tag{3.5}$$

This approach obtains very fast convergence times and skips any modeling of the brain response in the presence of artifacts [14]. The effect of this technique is illustrated in Figure 3.12. Herein, up to 37 dB of artifact attenuation is achieved by applying this proposed method.

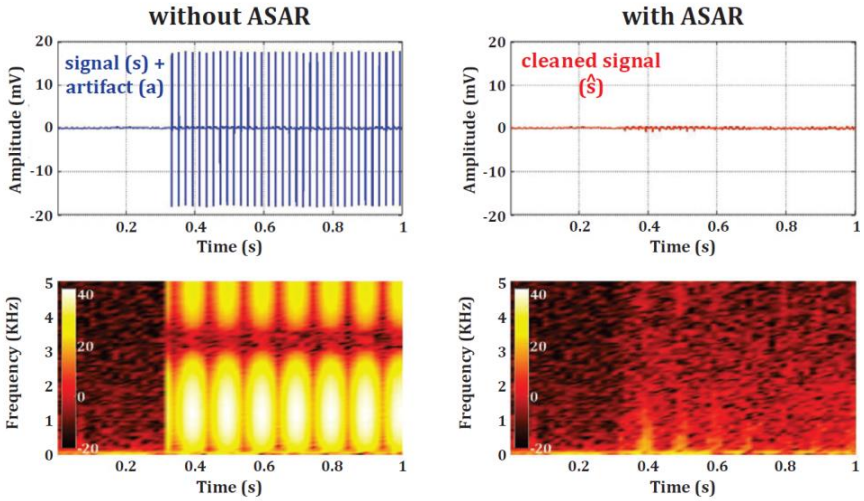


Figure 3.12: Example of the performance of the ASAR technique [14].

CHAPTER 4

TIME-DIVISION MULTIPLEXING IN NEURAL RECORDING FRONT-ENDS

As aforementioned in Chapter 2, form factor and power consumption are two of the main concerns in multi-channel neural recording interfaces. A technique that copes with these issues is the TDM technique. In this method, the same AFE block, or blocks, is shared among all the recording channels. The number of shared stages is, thereby, defined by the location of the multiplexer in the signal path.

The application of this technique at the electrode interface is a promising approach to further exploit the advantages of this method [126, 17, 18, 11, 12]. While in conventionally recording channels there is a one-to-one correspondence between electrodes and AFEs [47, 95, 103, 127] (Figure 4.1 (a)), in input TDM recording systems a single AFE is shared among all electrodes (Figure 4.1 (b)). This technique clearly reduces the area occupation per channel, which roughly scales down with the number of multiplexed electrodes thus leading to a noticeable area saving in multi-channel devices [12], and, eliminates the mismatch problem of these interfaces [86]. Nevertheless, this approach demands of AFEs with much larger bandwidth which may produce a significant increase of the in-band noise due to aliasing. This issue has to be carefully addressed when designing multiplexed front-ends.

4.1 Time-Divison Multiplexing

TDM is a widely employed technique in communication systems. The basic concept of TDM is illustrated in Figure 4.2: a clock-driven multiplexer converts M parallel input channels into a single output by splitting each input signal into

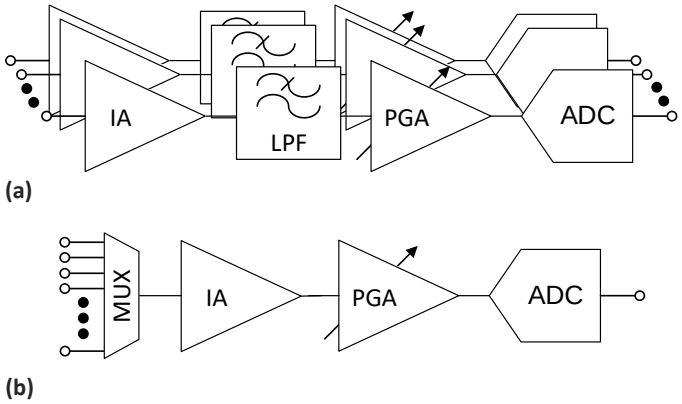


Figure 4.1: (a) Conventional neural recording front-ends for multiple channels. (b) Time-multiplexed neural recording front-end for multiple channels.

different time slots while keeping the same throughput rate per channel. Then, a demultiplexer performs the inverse operation, Time-Division Demultiplexing (TDD). Thus, this technique works essentially the same as the serial-parallel registers. After multiplexing, the signal from the M channels is shared by the same AFE block/s, reducing the number of instances of each multiplexed block by $M-1$. This results in area per channel saving, scaling with the number of multiplexed stages. When this technique is carried out in the analog domain by an analog multiplexer, the bandwidth of the subsequent block/s has to be at least M times larger than in non-multiplexed topologies, leaving the power consumption per channel about the same as in conventional architectures.

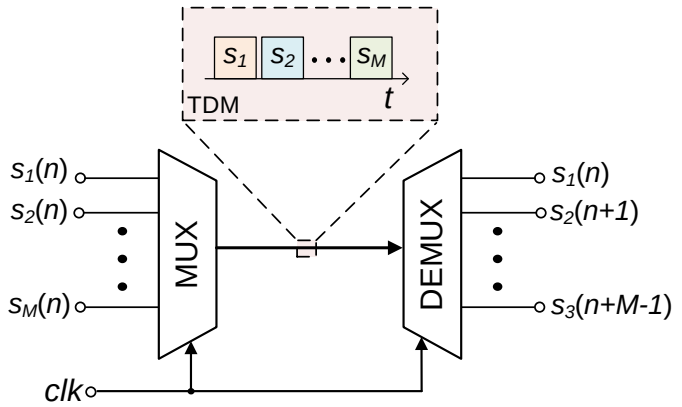


Figure 4.2: Time-division multiplexing technique.

This approach presents two major drawbacks: i) crosstalk in the analog multiplexer; ii) noise folding. Employing larger bandwidth blocks increases in-band noise, which will be folded into the baseband. Although anti-aliasing filters are used to deal with this spectral folding, if the multiplexer is located in one of the first stages of the AFE, this filter becomes more difficult to implement

and a different alternative has to be adopted. This problem is detailed in section 4.3.

4.1.1 Crosstalk in Time-Division Multiplexers

Crosstalk in TDM architectures can be seen as a noise source at the input of the analog multiplexer. This crosstalk can be disclosed in four different components: i) capacitive coupling between the input metal lines of the multiplexer; ii) the finite off-resistance of the switches; iii) time-adjacent channel crosstalk; iv) capacitive coupling through the parasitic capacitance of the transistor used as a switch. Firstly, the impact of the capacitive coupling can be avoided by applying layout techniques such as careful shielding of each input line. In the second case, the subthreshold conduction of the switches is negligible due to the large back-bias effect in low-voltage topologies. Thus, the off-resistance is in the order of hundreds of GΩ, avoiding the crosstalk between channels. The time-adjacent channel crosstalk reveals the multiplexer's ability to charge/discharge the load capacitors during the active period of a channel. If the multiplexer response is slow, a residual charge will appear between two time-adjacent channels, resulting in crosstalk noise. The on-resistance of the switches should therefore be designed to be as small as possible, in order to suppress this crosstalk source. Therefore, the first three crosstalk sources mentioned above can be neglected by properly designing the multiplexer.

The effect of the capacitive coupling through the parasitic capacitance of the transistor can have a real impact on the multiplexer output [128] and have to be analyzed. Figures 4.3 (a) and (b) present a transistor as a switch and its simplified model, respectively. In this model, R_{st} represents the state-resistance of the switch (R_{on} and R_{off} for the on-state and off-state, correspondingly) and C_{EQ} the equivalent parasitic capacitance of the switch (mainly comprising its drain-to-source capacitor and its drain-to-bulk and source-to-bulk capacitors). The crosstalk scheme for a M-channel multiplexer based on this simplified model is illustrated in Figure 4.3 (c). This model is developed to study the impact of the $M-1$ turned-off channels at the multiplexer output while a single channel is enabled. In Figure 4.3 (c), R_{ost} represents the output impedance of the stage feeding the multiplexer. In the case of multiplexing at the electrode interface, R_{ost} will mainly comprise the spreading resistance, R_s, and the electrode impedance, Z_e (Figure 4.3 (d)).

The crosstalk in the multiplexer is now defined as the effect of the $M-1$ turned-off channels at the output of the multiplexer V_{out}. Assuming $R_{off} >> C_{EQ}$ and $R_{on} << C_{EQ}$, this crosstalk, Cr_{MUX}, is given by:

$$Cr_{MUX}(dB) = 20\log_{10}\left(\frac{R_L}{R_{ost} + Z_{EQm} + R_L}\right) \tag{4.1}$$

with:

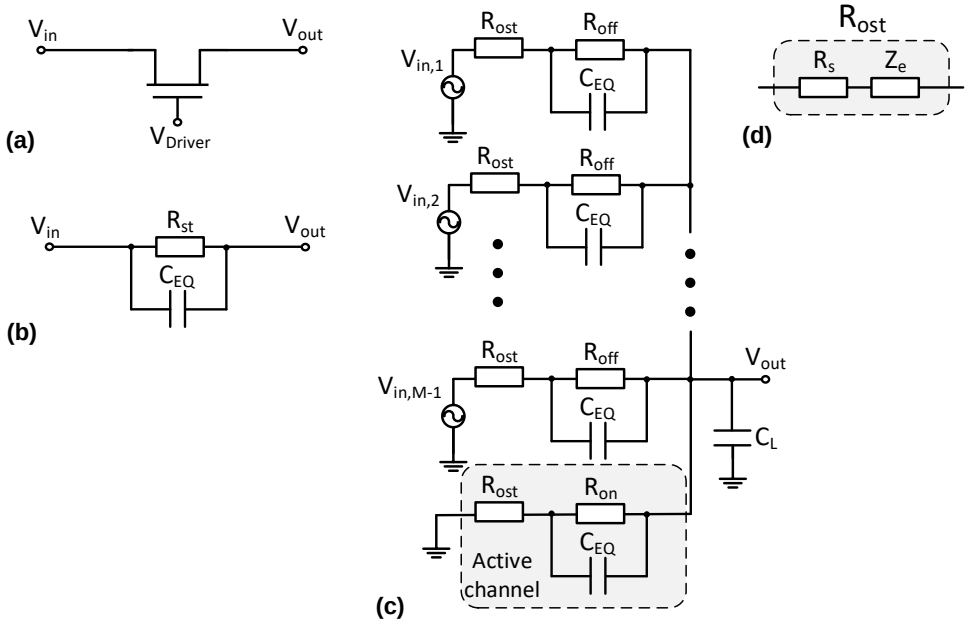


Figure 4.3: (a) MOSFET device as a switch. (b) Simplified equivalent circuit model for MOSFET as a switch. (c) Equivalent circuit model for crosstalk analysis of a M-channels multiplexer. (d) Equivalent impedance model for multiplexing at the electrode interface.

$$R_L = \frac{Z_{EQm}(R_{on} + R_{ost})}{Z_{EQm} + R_{on} + R_{ost}} \tag{4.2}$$

$$Z_{EQm} = \frac{1}{(M-1)\ j\ \omega\ C_{EQ}} \tag{4.3}$$

ω being the frequency of the input signal. Simulations were conducted to demonstrate the effectiveness of the model and the impact of the crosstalk at the output of the multiplexer (Figure 4.4). Figures 4.4 (a) (2-channel multiplexer) and (b) (64-channel multiplexer) illustrate crosstalk in AFEs with the multiplexer located at the electrode interface against the electrode impedance variations. On the other hand, Figures 4.5 (a) (2-channel multiplexer) and (b) (64-channel multiplexer) show the crosstalk in AFEs with the analog multiplexer before the PGA, against the IA's output resistance variations. Firstly, it can be observed that the effect of both variations increases with the number of multiplexed channels. Secondly, as the electrode impedance is usually larger than the output resistance of a conventional amplification stage, multiplexer crosstalk noise has major impact on topologies with multiplexing at the input of the AFE than in other multiplexed architectures. In the worst case, this crosstalk remains below -65 dB and can be further reduced by properly designing the multiplexer. The effect of multiplexer crosstalk is, therefore, lower than that of electrode crosstalk and

can be ignored as a source of noise in most analyses of multi-channel neural recording devices.

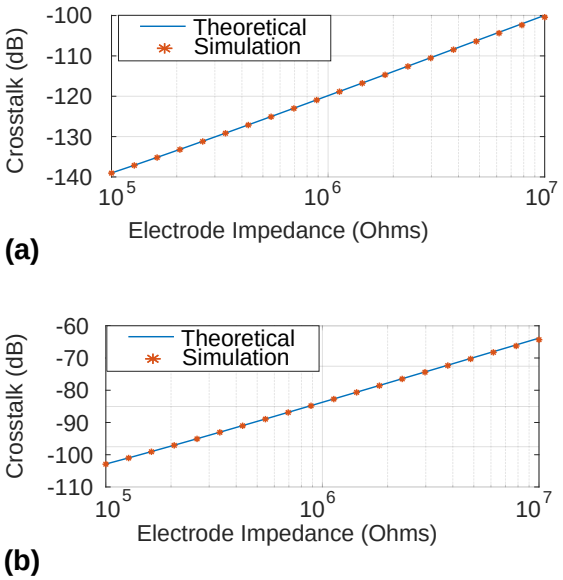


Figure 4.4: Multiplexer crosstalk for TDM at the electrode interface against electrode impedance for (a) a 2-channel multiplexer. (b) a 64-channel multiplexer.

4.2 Taxonomy of Multi-channel Neural Recording Multiplexed Systems

The neural front-ends presented in Section 2.3 can be multiplexed to reduce the area per channel of the device. Thereby, multi-channel neural recording AFE topologies can be classified by the position of the multiplexer in the signal path and, consequently, by the number of multiplexed blocks (Figure 4.6).

4.2.1 Non-Multiplexed AFE topology

In non-multiplexed AFE topology (see Figure 4.6 (a)), each channel is recorded by a low-rate low-power AFE. For M independent recording channels, M independent AFEs are required. Herein, all the front-ends presented in Section 2.3 are suitable for being implemented using this architecture.

The area limitations in the electrode interface make the integration of these AFEs along with the electrodes unfeasible. Moving the recording front-end far from the electrodes relaxes their size and power limitations. This enhances the design flexibility and allows the inclusion of additional on-chip functionality, such as data processing [10]. However, employing a complete AFE per channel increases the mismatch errors in multi-channel topologies [86].

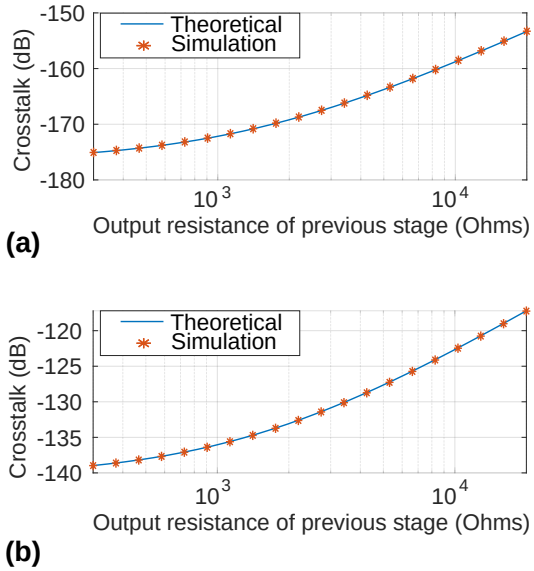


Figure 4.5: Multiplexer crosstalk for TDM before the PGA against the IA's output resistance for (a) a 2-channel multiplexer. (b) a 64-channel multiplexer.

In terms of the analog-to-digital conversion, despite using a low sampling frequency, the need for one ADC per channel requires a very careful design in order not to largely penalize the area and power consumption of the neural recording IC. Successive Approximation Register (SAR) ADCs have generally provided a suitable performance for this kind of topologies [41, 48, 34, 10]. After conversion, the signal is multiplexed, typically by using data serializers [32, 49]. In the digital domain, multiplexing is less prone to errors because the signal has higher noise margins and is more stable against crosstalk and other noise sources.

4.2.2 ADC Sharing & PGA Sharing AFE topologies

One of the most popular approaches for multi-channel architectures is to use a single ADC shared by all channels (Figure 4.6 (b)). Theoretically, this reduces the form factor and the power consumption of the IC in comparison with non-multiplexed AFEs. This topology is based on M parallel structures sharing a single ADC [67, 129, 130, 131, 78].

The electrical properties of the electrode-AFE interface for these architectures are the same as for non-multiplexed AFEs. In these topologies, the signal after amplification is directed towards the ADC by means of TDM. Increasing the sampling frequency increases the required power consumption of the ADC and its previous stage, even requiring driving buffers at the input of the converter [132].

Most of the topologies presented in Sec. 2.3 are suitable for being multiplexed

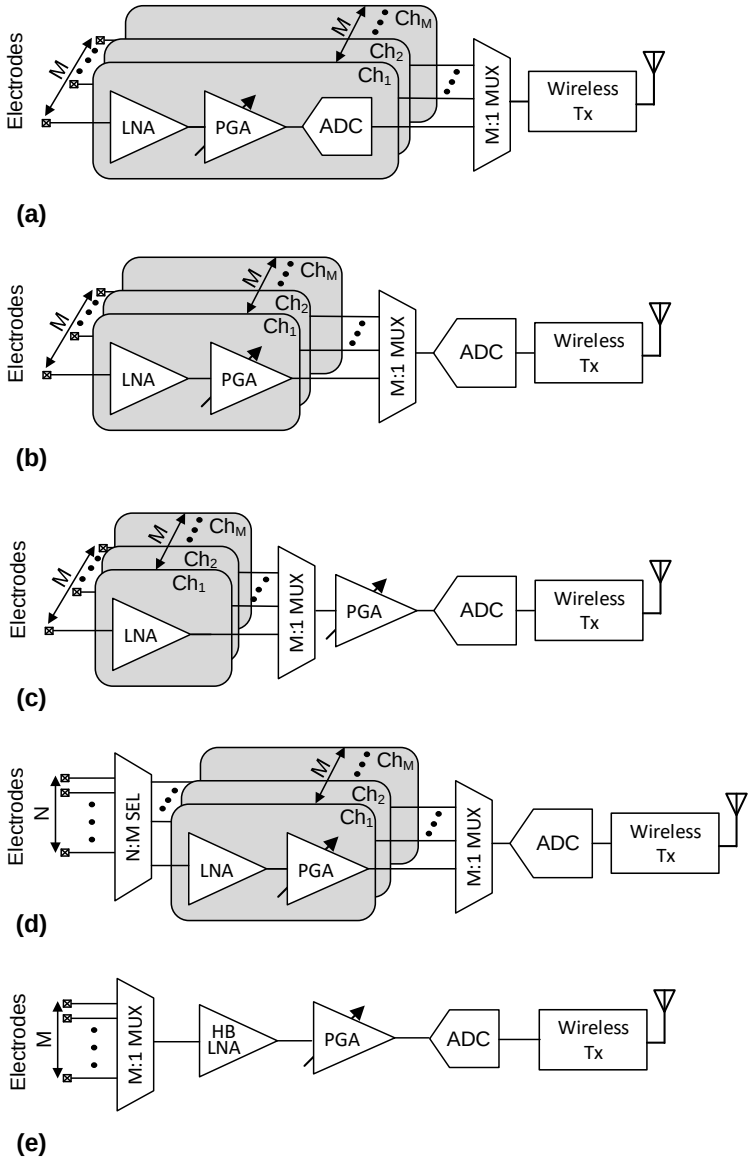


Figure 4.6: (a) Non-multiplexed AFE topology. (b) PGA sharing AFE topology. (c) ADC sharing AFE topology. (d) Switch array AFE topology. (e) Time-division-multiplexing AFE topology.

at the ADC stage. However, while chopper-stabilized AFE topologies demand an additional stage to properly settle the ADC, digitally-assisted architectures involve a considerable rise of power consumption. This is due to the need for oversampled blocks in addition to memory blocks which store the information of each channel to properly performing the mixed-signal operation.

A similar alternative to ADC sharing relies on sharing, not only the ADC but also the PGA for the M independent channels, as shown in Figure 4.6 (c)). In this topology, the input amplification stage can be integrated into the same

IC along with the rest of the AFE [133, 77, 134], or into the electrode interface, [8, 15, 135, 136].

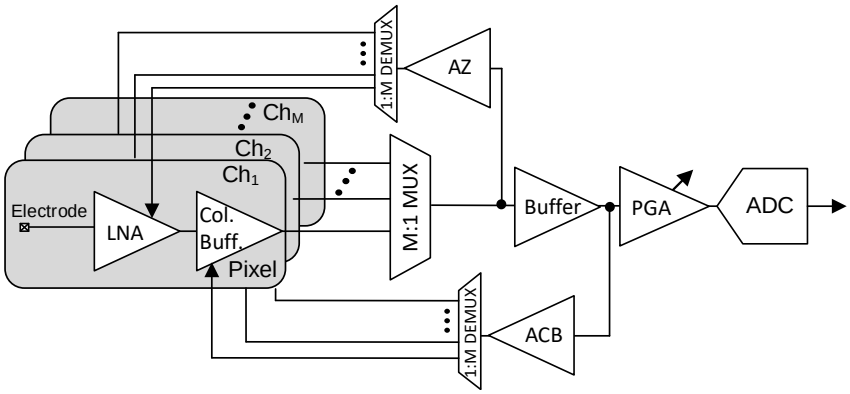


Figure 4.7: Simplified block diagram of the PGA sharing topology presented in [15].

An interesting application example of PGA sharing with the IAs within the electrode interface is reported in [15] and simplified in Figure 4.7. In this architecture, each pixel of the shank incorporates an open-loop amplifier, performing the function of the IA. To remove the DC offset without increasing the area of the pixel, an out-of-pixel Autozero (AZ) amplifier is shared by all the pixel's amplifiers through TDD. This proposed architecture implements two-stages column buffers: a pixel stage (with one column buffer per channel) and a base stage shared among all channels. The output of this multiplexed buffer is, then, fed into an amplifier (ACB) which mitigates the short channel effects by feeding the correction signal into each pixel's column buffer.

4.2.3 Switch Array AFE topology

All the previously introduced architectures allow full-frame read-out at the cost of reducing electrode density. To increase the number of electrodes, and, therefore, the spatial resolution of the probe, a switch-matrix can be within the electrode interface. In these architectures, also known as static multiplexing, for N electrodes, the switch-matrix only selects M of them (with $N > M$) and interconnects them with the M available read-out channels (AFEs), as illustrated in Figure 4.6 (d). After the amplification stages, the signal is commonly multiplexed as in ADC sharing topologies.

The switch-matrix comprises a large group of routing wires, switches, and a local memory such as an SRAM which stores the connection status of each electrode [137]. Herein, the area of the electrode interface is not significantly impacted. This architecture can also include amplifiers along with the electrodes [35, 138] or just the switch-matrix [139, 140, 16, 137]. A simplified example of a switch array AFE corresponding to the neural probe scheme reported in [16] is

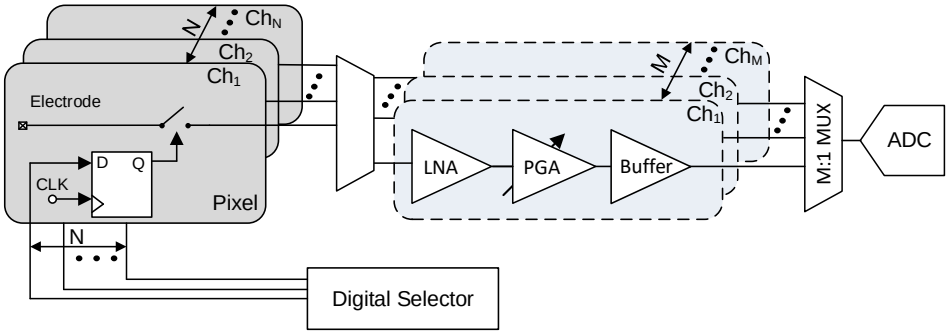


Figure 4.8: Simplified block diagram of the switch array AFE topology presented in [16]

shown in Figure 4.8. Note that the switch-matrix incorporates memories (flip-flops) which select the electrodes to record using a digital selector embedded into the base of the neural probe.

The required form factor defined by the number of readout channels restricts the possibilities of implementing some of the topologies of the Sec. 2.3. Furthermore, long-time constant feedback-loops (such as analog DSLs) have to be properly designed to not introduce crosstalk between channels when the switch-matrix changes between two electrodes.

One of the major issues concerning these structures is the selection of the electrodes to be read. One widely-used solution involves a process that firstly records the whole electrode matrix during different time slots. Then, the data is processed and some groups of electrodes are prioritized by applying an optimization algorithm (which could involve machine learning) based on the previously recorded signals and the main purpose of the recording. Another alternative presented in [35], divides the electrode matrix into a set of subgroups. In this proposal, the electrodes of each subgroup are selected pseudo-randomly, ensuring that all areas of the probe are covered.

4.2.4 Time-division multiplexing AFE topology

One new trend in multi-channel neural recording topologies is to place the multiplexer at the input of a single AFE (see Figure 4.6 (e)) which is shared by all channels. This reduces the area occupation per channel and ignores mismatch between recording channels (a further breakdown of the TDM AFE considerations and architectures is provided in Section 4.3). It is worth observing from Figure 2.9 (b) how the TDM AFE reported in [12] shows one of the most promising results in terms of area and NEF. The main drawback of these topologies relies on the requirement of a High-Bandwidth LNA (HB LNA) to fast-multiplex all the channels, which significantly increases the power consumption of the stage and the in-band noise due to aliasing [17].

4.2.5 Power-area State-of-art of Multi-channel Neural Recording Systems

Multi-channel neural recording systems presenting the TDM technique have been presented and classified. While a complete revision of the state-of-art of neural recording front-ends was presented in Section 4.2, Tables 2.3 and 2.4; Table 4.1 provides a brief revision of the state-of-art of multi-channel neural recording systems in terms of power consumption and area occupation. Herein, the main objective of this table is to illustrate the performance of each one of the presented TDM architectures. It can be observed that the best results are provided by non-multiplexed and TDM AFEs. In the case of the non-multiplexed AFEs, their design flexibility allows reducing the form factor and the power consumption of the system. On the other hand, multiplexing at the electrode interface allows us to obtain some of the best results in terms of area saving by far.

Table 4.1: Power-area State-of-art of Multi-channel Neural Recording Systems.

Reference	Year	Technology (nm)	Topology	Power/ch (μW)	Area/ch (mm^2)	#Electrodes	#Readout Channels	Additional info
[34]	2012	130	Non-Multiplexed	68	0.26	96	96	
[59]	2020	130	Non-Multiplexed	0.99	0.011	16	16	
[141]	2018	180	Non-Multiplexed	47	0.00049	144	144	Amplifiers within the electrode interface
[41]	2017	180	Non-Multiplexed	8	0.18	64	64	Area include Stimulation
[25]	2015	65	Non-Multiplexed	2.3	0.025	64	64	
[142]	2018	130	Non-Multiplexed	11.2	0.086	10	10	
[10]	2017	130	Non-Multiplexed	3.04	0.16	64	64	
[57]	2017	130	Non-Multiplexed	0.63	0.013	64	64	
[55]	2018	65	Non-Multiplexed	0.8	0.024	16	16	
[78]	2013	180	ADC sharing	10	0.28	100	100	
[130]	2014	130	ADC sharing	19	0.018	56	56	
[67]	2011	180	ADC sharing	10	0.01	32	32	
[80]	2015	65	ADC sharing	1.81	0.025	64	64	
[129]	2017	350	ADC sharing	73	0.3	64	64	
[134]	2009	350	PGA sharing	23	0.5	128	128	Include Wireless transmiter
[133]	2016	180	PGA sharing	2.5	0.1	16	16	Include Wireless transmiter
[136]	2013	180	PGA sharing	12.6	0.0033	1120	1120	Amplifiers within the electrode interface
[77]	2013	180	PGA sharing	0.8	0.25	100	100	
[15]	2018	180	PGA sharing	30	0.007	36	36	Amplifiers within the electrode interface
[15]	2018	180	PGA sharing	2.7	0.000625	512	512	Amplifiers within the electrode interface - Off-chip ADC
[137]	2010	600	Switch-Matrix	160	0.07	5120	126	Switch-matrix within the electrode interface
[16]	2019	130	Switch-Matrix	37.5	0.12	26400	384	Base/ch area - Switch-matrix within the electrode interface
[139]	2014	350	Switch-Matrix	37	0.033	966	1024	Only first amplification stage - Switch-matrix within the electrode interface
[35]	2017	130	Switch-Matrix	49	0.12	16384	384	Amplifiers within the electrode interface
[138]	2012	180	Switch-Matrix	2.2	0.001	16384	16384	Amplifiers within the electrode interface - Off-chip second Amplifiers and ADC
[12]	2020	65	TDM	3	0.0023	64	64	
[126]	2017	130	TDM	45	0.12	1356	1356	
[17]	2018	180	TDM	7	0.0039	20	20	

4.3 Review of Time-division-multiplexing AFEs

One of the first reported TDM AFEs was presented in [126]. In that work, the TDM technique was only employed for the amplifiers within the electrode interface, reducing the number of interconnection wires and increasing the electrode density of the neural probe. The AFE/electrode ratio, however, was still 1:1. Recently, new TDM systems have emerged which multiplexes the whole AFE [18, 12]. This kind of architecture aims to reduce the power and area of the whole recording interface, but here two major design issues arise: noise folding and DC offset from electrodes.

4.3.1 Noise folding in TDM AFEs

For a M-channel multiplexed recording device, the required sampling frequency can be set as:

$$f_s \geq M f_c = 2MB_w \tag{4.4}$$

being f_c the equivalent sampling frequency per channel and B_w the recording bandwidth. For conventional Voltage-Sampling (VS) techniques, assuming a single-pole low-pass response of the operational amplifier within the IA, the bandwidth requirement to settle the signal within f_s will be given by [17]:

$$f_b = \frac{\ln(\epsilon) f_s}{2\pi} = M\frac{\ln(\epsilon) f_c}{2\pi} \tag{4.5}$$

where ϵ is the tolerable dynamic settling error. For instance, ϵ must be <0.1 % to satisfy a 10-bit resolution constraint. A commonly adopted approach to characterize the noise performance of the systems is the Noise Equivalent Bandwidth (NEB). The NEB can be defined as the bandwidth of a brick-wall filter providing the same integrated noise power as that of an actual system. For a given system $H_e(f)$, its NEB can be calculated as [143]:

$$NEB = \int_0^{+\infty} \left| \frac{H_e(f)}{H_{e,max}} \right|^2 df \tag{4.6}$$

with $H_{e,max}$ being the maximum value of the system. For a TDM system employing voltage-sampling, $H_{TDM}(f)$, with an amplifier bandwidth set by 4.5, its NEB can be determined as:

$$NEB_{TDM} = \int_0^{+\infty} \left| \frac{H_{TDM}(f)}{H_{TDM,max}} \right|^2 df \approx \frac{\pi}{2} f_b = -f_s ln(\epsilon)/4 = -M f_c ln(\epsilon)/4 \tag{4.7}$$

From 4.7 it can be concluded that the NEB increases proportionally with the number of channels. For action potential recording, for example, the NEB in TDM AFEs is $3.5M$ higher than for conventional non-multiplexed AFE topologies [17]. Figure 4.9 illustrates the NEB vs the number of multiplexed channels

applying equation 4.7 for LFP signals (up to 200 Hz) and 10-bit resolution requirement. Accordingly, the system's noise will be undersampled and aliasing will occur, increasing the in-band noise power [126]. Figure 4.10 (a) conceptually shows this noise folding process. In an instantaneous sampling process (with the equivalent sampling frequency per channel equal to f_c), the output folded power spectral noise can be calculated by [144]:

$$S^S(f) = \frac{2NEB}{f_c} S_n \qquad -f_c/2 < f < f_c/2 \tag{4.8}$$

being S_n the white noise spectral density component. Herein, the NEB increment will proportionally increase the noise folded components.

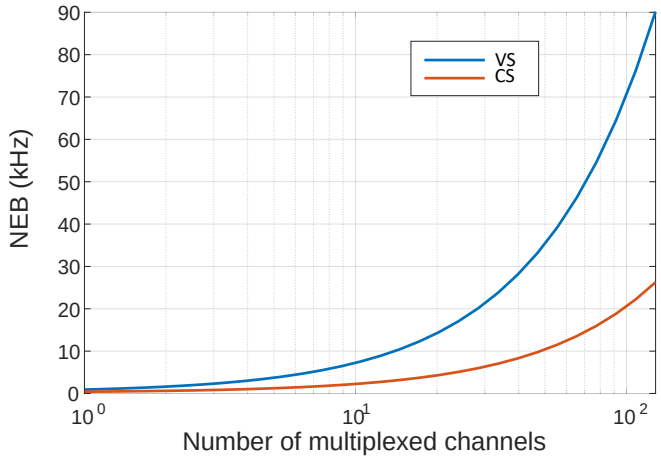


Figure 4.9: NEB against the number of multiplexed channels in VS-based and CS-based TDM AFEs

This problem applies not only to the noise from the recording electronics, but also to the noise from the electrodes. The noise power spectral density from the electrodes can be approached as [17]:

$$S_{el}(f) = 4kT\ Re[Z_e(f)] \tag{4.9}$$

where $Re[Z_e(f)]$ is the real part of the electrode impedance. By substituting 4.9 in 4.8, it can be easily noticed that the folded noise from electrodes will scale with the number of multiplexed channels. Therefore, the noise folding in TDM AFEs will strongly limit the scalability of the system. To solve this problem, the NEB of the front-end has to be reduced without sacrificing settling accuracy within the time allocated for channel sampling.

A promising technique to cope with this problem relies on implementing Charge-Sampling (CS) instead of voltage-sampling [11, 12, 126]. The Windowed Integration Sampling (WIS) solution proposed in [17] can be considered as a kind of charge-sampling technique. The main idea of this technique is based

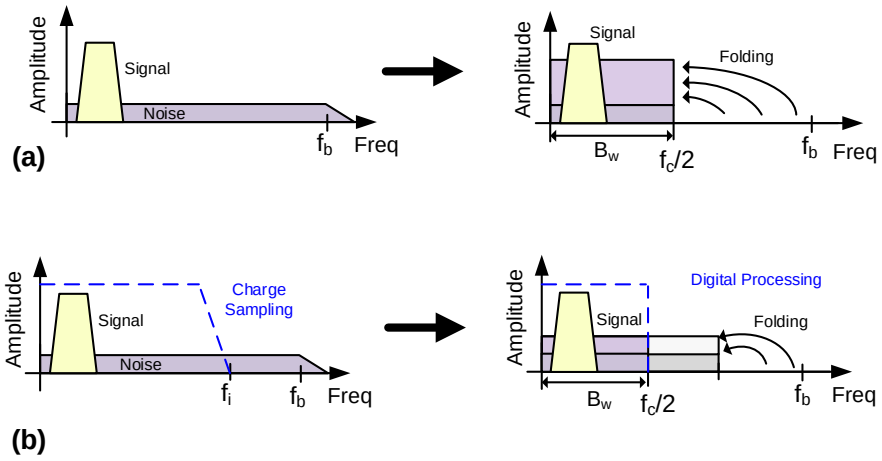


Figure 4.10: Noise folding problem in (a) VS-based multiplexing circuits. (b) CS-based multiplexing circuits

on integrating the signal during a period T_i, with $f_i = 1/T_i$ and $f_c < f_i < f_s$, and then sampling the last value. The NEB for charge-sampling architectures is then given by [17]:

$$NEB_{CS} = \frac{fs}{2} = -Mf_c/2 \tag{4.10}$$

It is worth noting from 4.10 and 4.7, that the NEB is reduced by $ln(\epsilon)/2$. Figure 4.9 illustrates how the NEB for CS-based topologies is significantly lower than for VS-based architectures when the number of multiplexed channels is large. Thus, high-frequency noise components are filtered (Figure 4.10 (b)) according to a $sync$ filter specification [145], reducing the noise folding effect. In terms of circuit implementation, this technique is performed by a transconductance G_m-cell driving a sample-and-hold capacitor, C_{int}. The DC gain of this architecture is given by:

$$CS_{DC} = \frac{G_m\ T_i}{C_{int}} \tag{4.11}$$

However, this technique has some significant drawbacks: i) the pole of the $sync$ filter and the DC gain of the architecture are very sensitive to clock jitter [145]; 2) process variations will have a high impact on the system's gain and time constant due to the employment of an open-loop structure; 3) low-frequency noise components are not reduced; 4) large CM signals could change the operating point of the G_m stage, which may lead to distortion or even saturation.

4.3.2 DC Offset from Electrodes in TDM AFEs

DC offset from electrodes is a recurrent problem in DC-coupled AFEs [47, 53, 52]. In most of the architectures employing an IA per channel, DC offset can be rejected using large time constant high-pass filtering stages. However, these analog filters are not suitable in rapid multiplexing systems, since the filtering would increase crosstalk between channels and would not be fast enough to reject large DC offset variations between channels. One solution to this problem relies on limiting the gain of the AFE and increasing the resolution of the ADC. However, this extra resolution, together with the high sample rate required for multiplexing, would make the ADC unsuitable for low-power designs.

High-pass filtering the signal through a mixed-signal loop has been adopted as an alternative approach to palliating this issue in DC-coupled topologies [25, 97]. In this method, a Finite-Impulse-Response (FIR) or Infinite-Impulse-Response (IIR) filter is fed into the input of the AFE by a DAC. While the filter can be designed to not penalize the system's power consumption and area occupation, the required DAC resolution has to be high enough not to increase the noise at the input of the AFE. The number of bits of the DAC will be then determined by the resolution of the ADC, the overall gain through the signal path, and the input-referred noise of the AFE. In most practical cases, a DAC of more than 16-bits is required, which strongly compromises the form-factor specification of the neural recording front-end. An adopted solution for implementing this high-resolution DAC is to employ a $\Delta\Sigma$ modulator [25, 97]. However, this method is not feasible for TDM AFEs because the required oversampling frequency will be multiplied by M , and this will significantly impact the power consumption of the digital part of the IC. An alternative to a high-resolution DAC would be to use a binary search algorithm, as proposed in [18]. This algorithm initially computes the DC offset codes for each channel and retains the correction values until a threshold condition occurs. At that instant, the binary search recalculates the correction value for each channel. By applying this method, DC offset drifts are palliated without increasing the input-referred noise of the AFE. Nevertheless, although the system range is ensured, there will be a residual offset at the output of the AFE, which must be filtered in the digital domain.

Another proposed solution is based on working with Δ-signals (as illustrated in Figure 2.8 (c) and (d)). In this approach, the system tracks differences between successive samples, high-pass filtering the input signal. After conversion, the signal has to be reconstructed in the digital domain using an integrator/accumulator. This technique can be transferred to TDM AFE topologies by employing registers to store the previously sampled value of each channel. One example of a TDM AFE that exploits this technique is reported in [11, 12].

4.3.3 Comparison of TDM AFE Architectures

Despite their promising results, to the best of the authors knowledge, TDM AFE topologies have not been researched in depth. In this subsection, two main reported TDM AFE architectures are detailed. Block diagrams of these neural front-ends are shown in Figure 4.11 and more detailed in Figure 4.12 and Figure 4.13. As illustrated in Figure 4.11, both structures are based on mixed-signal architectures for DC offset rejection.

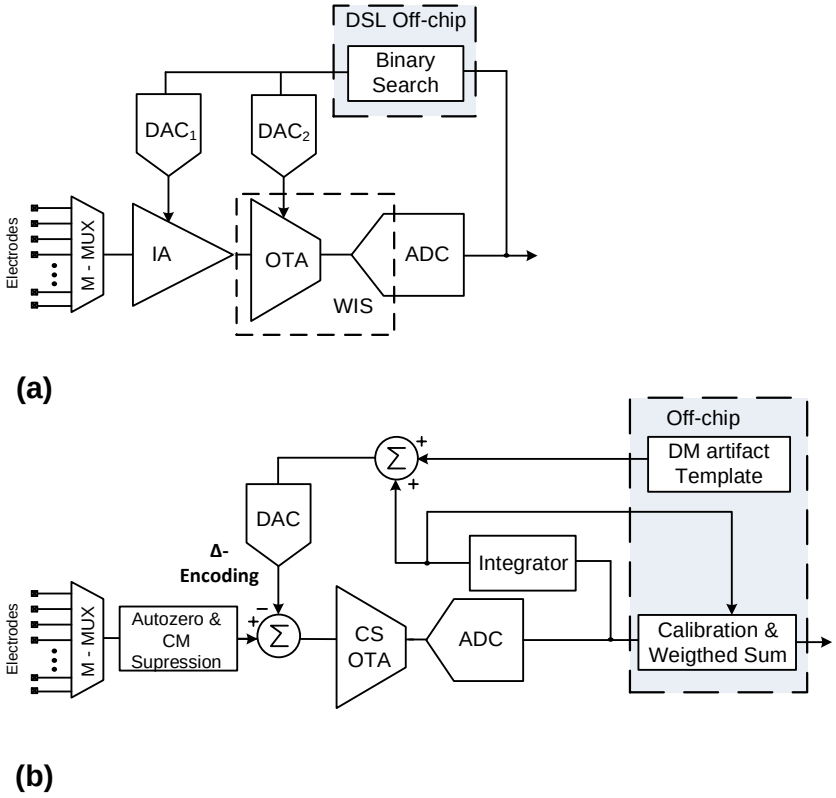


Figure 4.11: Block diagram of the reported TDM AFE topology in (a) [17, 18]. (b) [12].

The first architecture, reported in [17] and [18], is illustrated in Figure 4.11 (a) and detailed in Figure 4.12. In this proposed scheme, 20 channels are multiplexed. The IA comprises a capacitive feedback single-stage cascaded OTA whose gain is fixed by the ratio C_{in}/C_{fb}. This input stage is biased by a noisy bias network. Then, an open-loop OTA is employed as a G_m-cell along with the SAR ADC capacitors to implement the WIS filter and to further amplify the signal (Figure 4.12 (a)). This reduces the high-frequency noise components from the acquisition electronics and from the electrodes. The timing diagram of this operation is shown in Figure 4.12 (b). It can be seen that the integration period, T_i, lasts for most of the sampling period, T_s. After that, before the capacitors of the ADC are reset (ϕ_{rst}) and the input channel is changed, the conversion

phase, T_{conv}, takes place for only 11 % of the sampling period. This short-time conversion is carried out by an asynchronous converter. To remove the DC offset, a binary search algorithm is implemented externally by a Python script. This algorithm recomputes the 9-bit code each second to palliate the input DC offset. This is fast enough to compensate DC drifts at the input. The code is divided into 4-bits for DAC_1 and 5-bits for DAC_2 and maximizes the useful dynamic range of the system while reducing the ADC requirements. These both used DACs are embedded in the amplifier's structures.

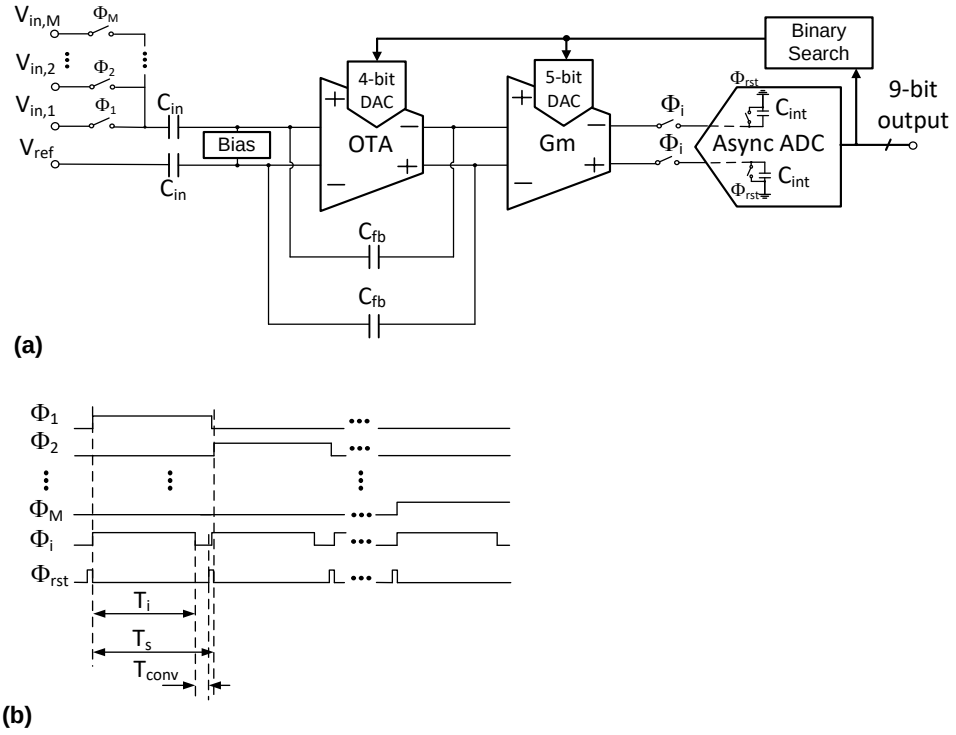


Figure 4.12: (a) Scheme of the TDM AFE proposed in [17, 18]. (b) Timing diagram of the presented scheme.

A Δ-Encoded TDM AFE was first presented in [11] and further developed in [12] (Figure 4.11 (b) and Figure 4.13). In this architecture, after the 64-channel input multiplexer, a switching scheme performs two main functions: i) autozeroing the inputs to reduce crosstalk between adjacent channels, and ii) largely suppressing the CM signals. This switching scheme (Figure 4.13 (a)) comprises the input capacitors, C_{in}, and the switches whose phases are ϕ_{AZ1}, ϕ_{AZ2} and ϕ_{TIE}. This switched architecture presents two operation modes. The first mode is intended for neural recording with the absence of large CM perturbations and its timing diagram is illustrated in Figure 4.13 (b). The second mode, triggered by the CM flag signal, largely suppresses the CM interferences. This mode was previously explained in Section 3.2 and its operation was simplified and shown in Figure (3.9 (b). It is worth pointing out that when the CM suppression is en-

abled, the performance of the system specially in terms of bandwidth and IRN is penalized [12]. After the switching scheme, an 8-bit capacitive DAC connected to the input node of the OTA then carries out the Δ-operation by subtracting the previous signal value to the current value, increasing the system's dynamic range. Afterwards, the Δ-signal is amplified by a charge-sampling amplifier consisting of an open-loop G_m-cell, capacitors C_L and switches (Figure 4.13 (a)). Note that the value of C_L is variable, mainly to set the gain of the charge-sampling topology and to palliate the ϕ_i clock variations. The timing diagram of this sampling operation is illustrated in Figure 4.13 (b). Once the signal is converted by an 8-bit SAR ADC, it can follow two paths: i) through the mixed-signal loop to perform the encoding technique; ii) to the sum and reconstruction block. In the mixed-signal path, the first stage is a user-programmable threshold block which determines the update quantity of the tracking signal to perform the Δ encoding. The update values, which can be -1, 0 or $+1$, are added to the previous tracking values, which are stored in a 64x8-bit register. This unit holds the correction data for each input channel, and, together with the tracking update value, performs an integration loop. The output signal from this loop feeds the DAC and is also scaled and added to the ADC output in order to reconstruct the signal. The output code thereby increases its resolution from 8 to 16 bits.

In both schemes, the input impedance is mainly defined by the input capacitors and the sampling frequency. Herein, these values along with the electrode-interface have to be carefully selected to not significantly increase the attenuation at the input of the system. This could compromise the scalability of the system, and, therefore, its spatial resolution. This scalability could be also degraded by the fact that both circuits demand external circuitry to properly operate. In the case of [17], it requires a computer to perform the DC offset removal and, in the case of [12], a Field-Programmable Gate Array (FPGA) is employed to tolerate large input DM signals.

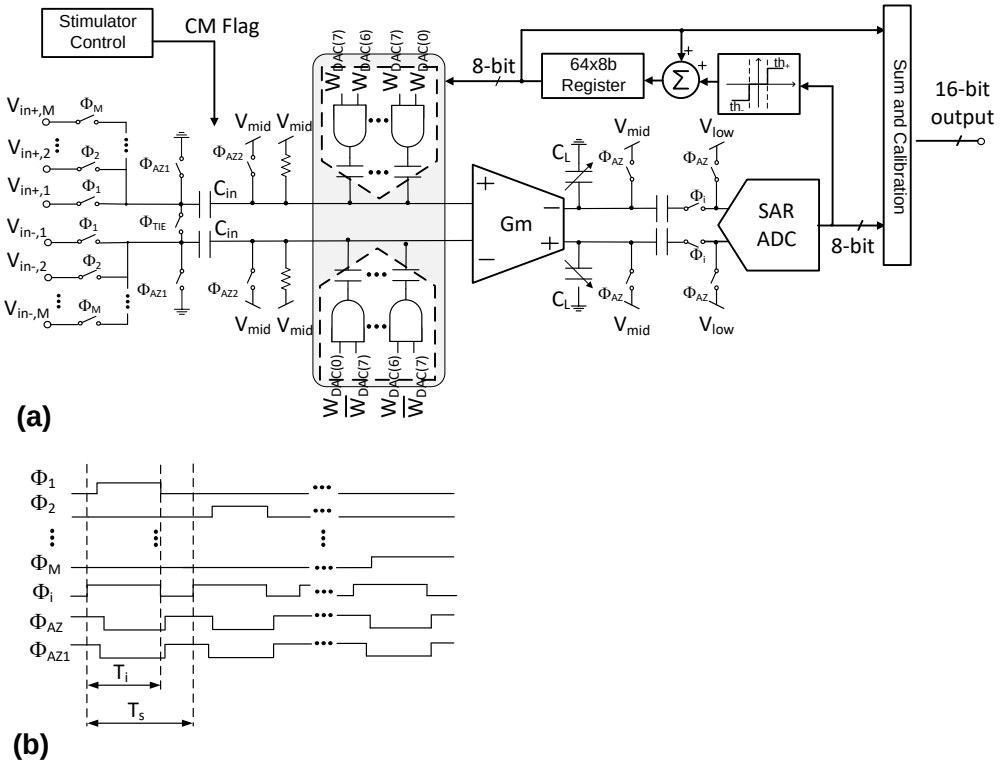


Figure 4.13: (a) Scheme of the TDM AFE proposed in [11, 12]. (b) Timing diagram of the presented scheme for no CM signals supression. Note that ϕ_{AZ2} and ϕ_{TIE} are not shown and open for the whole period.

CHAPTER 5

A 32-CH TIME-MULTIPLEXED ARTIFACT-AWARE NEURAL RECORDING SYSTEM

In the course of this work, the main considerations about designing multi-channel neural recording systems have been addressed. As aforementioned, most of the design constraints of neural recording devices are related to power consumption, area occupation and noise. Some techniques and architectures have been presented to improve these system's specifications. Here, TDM AFEs have demonstrated to be an auspicious alternative to conventional neural front-ends, specially increasing the area efficiency per channel. Moreover, for closed-loop systems in presence of large stimulation artifacts, the dynamic range and the maximum input tolerable signal have also emerged as key specifications in the design of these interfaces.

This chapter addresses the above problems and presents a 32-channel low-noise, high dynamic-range recording front-end, fabricated in a 180 nm standard CMOS technology. Focus has been on the recording of LFPs or ECoG signals. This extends earlier contributions in [146] and [116] with new experimental verifications, including measurements in saline, and additional theoretical analysis with emphasis in bandwidth and noise issues. The new prototype herein presented integrates a modified version of the converter in [147] and a new dedicated digital signal processor along with some minor modifications and corrections not included in our previous prototype [146]. The design follows a TDM recording strategy and uses two digital-feedback loops which provide robustness against large interferences with little impact on power consumption, area occupation or noise behavior. One loop implements a voltage-triggered

auto-ranging algorithm which allows to extend the effective dynamic range of the AFE to 71 dB + 26 dB; the other is a DC servo loop for electrode offset cancelling which extends the AFE input range to 300 mV_{pp}. Design considerations to not sacrifice other specifications such as crosstalk between channels, CMRR or input impedance are also presented. Furthermore, extended theoretical analyses have been carried out in order to describe the system's performance in terms of bandwidth and noise.

Compared to previous TDM front-end proposals with which this work presents similarities (only two to our best of knowledge, [17, 11, 12, 148]), our circuit uses a closed-loop amplification and filtering approach instead of charge-sampling techniques, it offers the possibility of applying both bipolar or monopolar sensing at the input multiplexer and it can delta encode neural signals between channels [32, 29] instead of tracking signal increments per channel. Additionally, our system offers two output modes (in one of them input signals are reconstructed including interferers, no matter their morphology or origin) and exploits the auto-ranging loop for handling differential-mode artifacts instead of adaptive filters [148].

5.1 System Overview

Figure 5.1 shows the block diagram of the proposed time-multiplexed neural recording system. The main core has been integrated in an Application Specific Integrated Circuit (ASIC) while some functions have been implemented in a micro-controller (μ-C, Rigado® BMD-350).

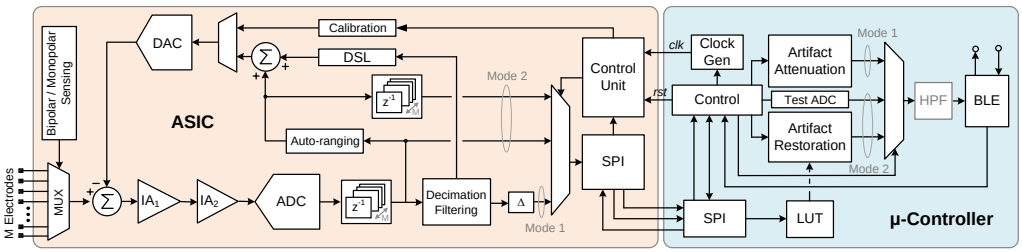


Figure 5.1: Block diagram of the proposed neural recording system.

After a switch matrix to multiplex M input neural signals, the ASIC comprises two cascaded fully-differential low-noise instrumentation amplifiers (IA_1 and IA_2) to sample, filter and amplify the signals captured by the electrodes. The multiplexer can be configured in two sensing modes, monopolar or bipolar, depending on whether signals are referred to a common reference or voltage differences between nearby electrodes are measured. Following amplification, a rail-to-rail SAR is used for taking signals into digital-domain. In this work, input signals are oversampled by a Oversampling Ratio (OSR) to reduce the in-band AFE IRN. The bandwidth of interest has been limited to $B_w \approx 200$ Hz.

Accordingly, the AFE sampling rate has been set to $f_s = 2MOSRB_w$ to satisfy the Nyquist rate criterion. All the time references are extracted from a master clock with frequency, f_m. For easy reference, Table 5.1 summarizes the main system frequencies and their notations.

Table 5.1: Summary of Frequency Parameters

Symbol	Description	Equivalent Value
f_m	Master clock frequency	2.5 MHz
f_s	Sampling frequency	$f_m/13 = 2 \cdot M \cdot OSR \cdot B_w$
f_b	Amplifier Bandwidth	$> f_s$
f_c	Sampling frequency per channel	f_s/M
f_{IA}	CDS Bandwidth	$f_c \approx f_{IA} < f_s/2$

Two feedback loops from the ADC memory are combined in a digital adder to drive the input of the first instrumentation amplifier by means of two DACs, one per differential terminal of the AFE. One loop, denoted as Auto-Ranging Loop (ARL), is used for the compression of large interferers, such as differential artifacts. The other feedback mechanism is a DSL for input offset rejection [25]. This loop is preceded by a decimation stage to filter signals down to baseband. Similar to [148], the ASIC control unit can enable an off-line calibration process to obtain the ADC outputs for all possible DAC input codes.

The ASIC features two output modes. In Mode-1, the decimated signal is transmitted through an SPI port. If monopolar sensing is enabled at the input multiplexer, the system gives the option to transmit increments between consecutive recordings. The purpose is to explore the possibility to losslessly reduce the word length of neuronal data, taking advantage of the large spatial correlation observed in LFP/ECoG signals captured from nearby electrodes. In bipolar sensing, decimated signals are inherently delta compressed and there is no need for further processing. For both sensing methods, output words are 14-b long. The second output mode, called Mode-2, is essentially used for verifying Mode-1 outcomes. In Mode-2, the output consists of two signals which are transferred through corresponding serial ports. One of the signals is the undecimated output of the SAR ADC (10-b) and the other is the sequence of the ARL codes (9-b). These codes are combined in the μ-C to losslessly reconstruct the input signal, including artifact, with 14-b resolution. An optional HPF has been also implemented in the μ-C for removing any residual DC component before data is transmitted through the Bluetooth Low-Energy (BLE) interface. For all the modes and rates, this HPF is a 6^{th}-order Butterworth IIR filters with cut-off frequency at 0.5 Hz.

5.2 Analog Front-End

5.2.1 Sensing and Coding

Figure 5.2(a) shows the schematics of the multiplexer at the interface with the electrodes. It consists of two sets of $M/2+1$ switches each connected to one AFE terminal. The switches are CMOS transmission gates implemented with low leakage thick oxide transistors. Although in this work $M = 32$, the approach is scalable to different configurations. Figure 5.2(a) also shows the different coding options available after the decimation and filtering stage in the proposed prototype (block Δ in Figure 5.1).

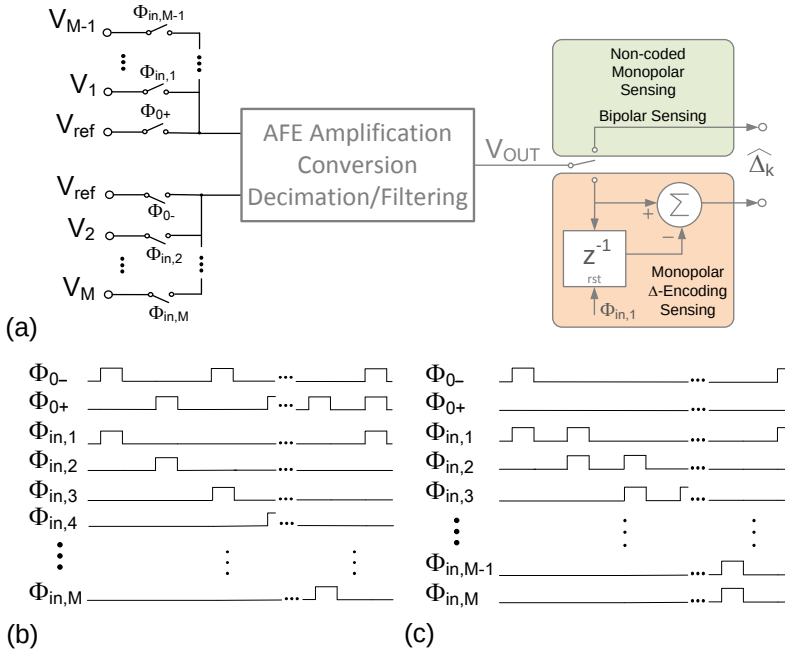


Figure 5.2: (a) Input multiplexer and spatial delta coding generation. Timing diagram of the (b) monopolar and (c) bipolar sensing modes.

As mentioned, the ASIC offers two electrode sensing options, monopolar or bipolar, which differ on how switches are pairwise-combined. Let us denote by $V_{i,j}(k)$ the k-th sample of the voltage difference between the i-th and the j-th nodes, where $i = 1,...,M$, and $k = 1,2,3...$ is a time index. Further, let us represent by $\hat{s}$ the amplified, converted, decimated and filtered version of sample s. In the monopolar sensing mode, based on the timing diagram of Figure 5.2(b), all the recording sites are referred to the reference electrode. If no delta encoding is selected, output samples are cyclically rendered according to

$$\widehat{\Delta_k} = (-1)^{i-1}\,\widehat{V_{i,ref}(k)} \tag{5.1}$$

where indexes i and k are linked by the expression

$$i = 1 + \mathrm{mod}(k-1, M) \tag{5.2}$$

Alternatively, a conventional delta encoder, formed by a register and an adder as shown in Figure 5.2(a), can be enabled to spatially encode signals in digital domain (only available in Mode-1). In this case, the sequence of coded outputs, $\widehat{\Delta_k}$, is

$$\widehat{\Delta_k} = (-1)^{i-1} \left(\widehat{V_{i,ref}(k)} - \widehat{V_{i-1,ref}(k-1)}\right) \tag{5.3}$$

where indexes i and k are again related by (5.2) and it is assumed that $V_{0,ref} = 0$. Note that for $i = 1$, the register of the delta encoder in Figure 5.2(a) is cleared and $\widehat{\Delta_k} = \widehat{V_{1,ref}(k)}$.

In the bipolar sensing mode, based on the timing diagram of Figure 5.2(c), voltages differences from adjacent recording sites are subsequently amplified. This effectively implements the spatial delta encoding paradigm in analog domain (available both in Mode-1 and Mode-2). In this case the encoded signals are given by,

$$\widehat{\Delta_k} = \widehat{(-1)^{i-1}\, V_{i,\,i-1}(k)} \tag{5.4}$$

where (5.2) holds again and it is assumed that $V_{1,0}(k) = V_{1,ref}(k)$ for $i = 1$. In this case, there is no need for any extra digital processing and $\widehat{\Delta_k}$'s are readily available after decimation and filtering.

Signals (5.3) and (5.4) can be easily decoded at the external hub so they are referred to the common reference electrode. This can be done by reverting the coding operation as

$$V^R_{i,ref}(k) = \sum_{j=m}^{k} (-1)^{i-1}\, \widehat{\Delta_j} \tag{5.5}$$

where $V^R_{i,ref}(k)$ is the decoded signal, $m = 1 + M\lfloor k/M \rfloor$, $\lfloor\cdot\rfloor$ represents the floor function and index i is given by (5.2).

5.2.2 Amplification and Filtering

In an M-channel multiplexed recording system, the sampling frequency f_s has to be $M\times$ faster than when a single channel is addressed to keep the same throughput rate per channel f_c, i.e., $f_s = M f_c$. This demands for an equivalent increase in the amplifier bandwidth f_b and, therefore, the AFE in-band noise raises due to spectral folding [126]. As the front-end amplifier typically dominates the noise behaviour of the whole system, noise folding due to multiplexing can indeed compromise the input-referred noise specifications in the bandwidth of interest. This was previously illustrated in Figure 4.10(a). To circumvent this problem, a mechanism is needed for reducing the NEB of the amplifier, so IRN specifications are satisfied, while ensuring the appropriate settling accuracy within the time T_s allocated for channel sampling [17]. This concern was fully detailed in Section 4.1. In this work, we address the problem through the combination of narrow-band Correlated Double Sampling (CDS) amplification (to reduce flicker noise and counteract the excess of thermal noise

due to multiplexing) and ADC oversampling (to filter out part of the folded noise generated by the CDS technique itself).

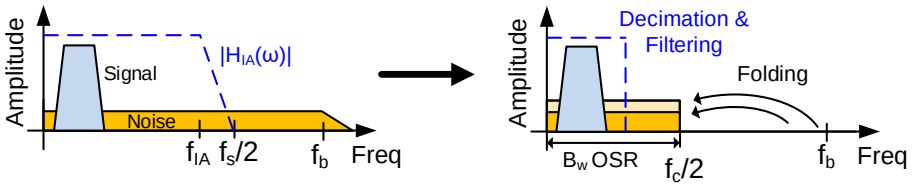


Figure 5.3: Noise folding in multiplexing circuits applying a narrow-band CDS architecture.

Figure 5.4(a) shows the schematics of the first CDS instrumentation amplifier, IA_1 in Figure 5.1 [149, 150], and the first row of Figure 5.4(b) shows the associated timing diagram. In this diagram, numbers indicate the master clock periods, T_m, comprising each phase and arrows indicate charge transfers from one block to another in the main AFE signal path. The circuit operates at a sampling frequency f_s and the pulses in Figures 5.2(b-c) are aligned to the clock phase Φ_1. The second amplifier, IA_2, uses the same circuit structure (excluding the positive feedback loop formed by capacitors C_{ib} and the two input DACs) but different phases – see the second row of Figure 5.4(b). Given the small bandwidth of neural signals compared to f_s, no continuous-time anti-aliasing filter precedes the ADC. In this proposed system, the ADC is a 10-b version of the charge-redistribution SAR topology used in [147]. The ADC is oversampled by $OSR = 16$ and uses 13 cycles of the master clock for completing each conversion: 2 cycles are used for signal sampling, 10 cycles for data conversion and one cycle for discharging internal capacitors, as shown in the third row of Figure 5.4(b). In this design, the converter achieves 58.2 dB SNDR at Nyquist frequency and consumes about 3.5 μW.

The positive feedback loop in Figure 5.4(a) (only for IA_1) is used for boosting the input impedance of the AFE [52]. In practice, the capacitors C_{ib} are implemented with 2-b capacitive banks to palliate variations due to mismatch and parasitics.

The DACs in IA_1 are used for closing the digital feedback loops in Figure 5.1. Each DAC is implemented with an 8-b binary-weighted capacitive array. Only one DAC injects charge at a time. Accordingly, the programming word W, which combines the ARL and DSL correction codes W_A and W_{DSL}, respectively, consists of 9-b: one for selecting the active branch and the rest for specifying the magnitude (w_p or w_n). Unit capacitors have been sized for an input-referred voltage correction range of ±150 mV at less than 0.56 mV step. The ratio between the total DAC capacitance per branch C_{DAC} and the input capacitance C_{in}, has been set below 1/4 to reduce the thermal noise contribution of the DAC to the overall IRN [151]. The reference voltage of the DACs, V_{BG} amounts 0.6 V.

In order to reduce the crosstalk between channels and offer a time-invariant

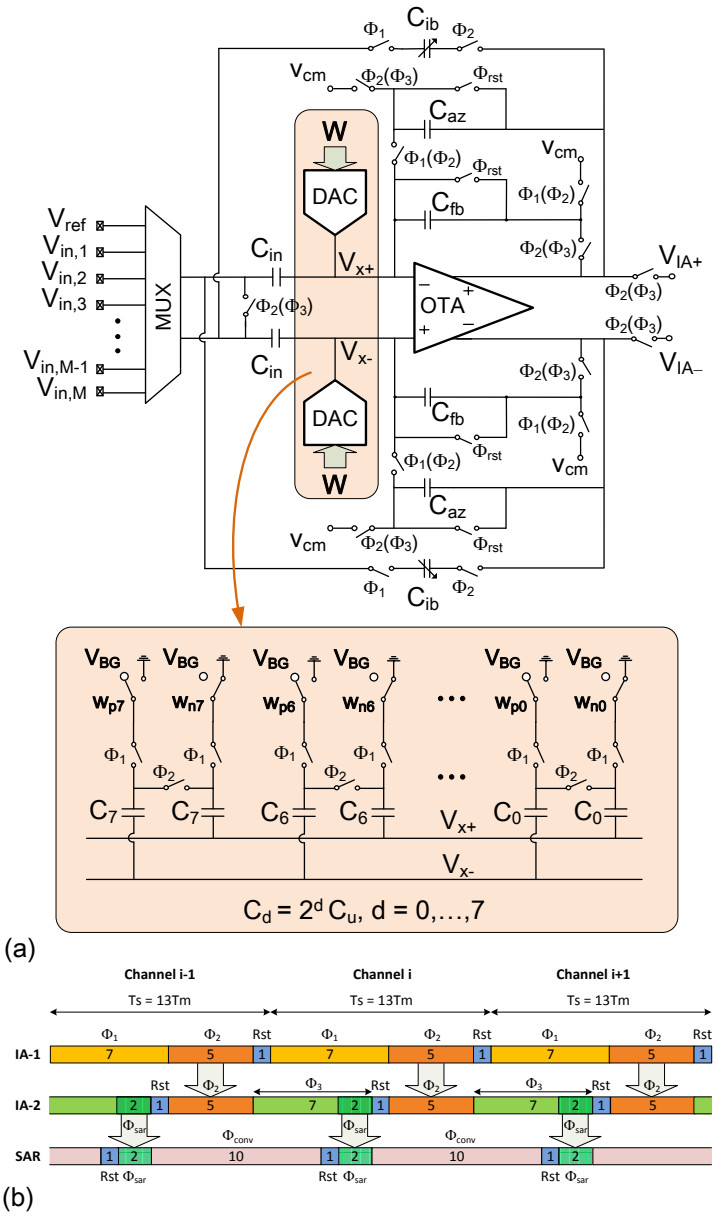


Figure 5.4: (a) Instrumentation amplifier IA_1. The inset shows the schematic of the two 8-b DACs used for closing the feedback loops in Figure 5.1. Amplifier IA_2 uses the same structure, excluding the input multiplexer, capacitors C_{ib} and DACs. Unparenthesised clock phases hold for IA_1, while parenthesized phases are for IA_2. (b) Timing diagram of the amplifiers and the SAR ADC.

input impedance, a short reset pulse Φ_{rst} after the amplification phases of IA_1 and IA_2 is used for clearing their respective feedback, C_{fb}, and the auto-zero, C_{az}, capacitors (Figure 5.4(b)). According to simulations with an electrode-tissue model for a typical Pt electrode [152], the crosstalk decreases quite significantly from -27 dB to -85 dB through the reset of these capacitors. A similar

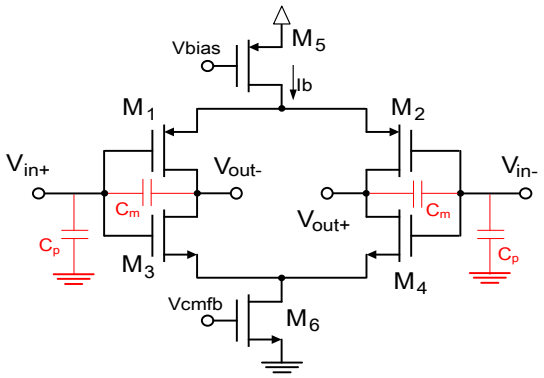


Figure 5.5: Current-reuse OTA topology used in the instrumentation amplifiers.

resetting of the input capacitors, C_{in}, reduces crosstalk by 3 dB but at the cost of degrading linearity and noise and, hence, the option was discarded.

Both IA_1 and IA_2 employ the same current-reuse topology for the OTAs, shown in Figure 5.5. In both cases, input transistors are biased in weak-inversion, however, while in the first amplifier these transistors are large to reduce the flicker noise contribution of the OTA, they are significantly smaller in the second amplifier to reduce parasitics. The OTAs use switched-capacitor Common-Mode Feedback (CMFB) circuits, because of their high linearity and low power consumption. For both amplifiers, the OTA transconductance is large enough so the dynamic settling errors during their respective sampling and amplification phases are lower than 0.1 % for 10-bit accuracy. Figure 5.6 shows the settling error of IA1 in terms of frequency. For the system sampling frequency f_s, the error remains below the desired 0.1 %. Moreover, Figure 5.7 illustrates the settling behavior at the output of IA_2 during its amplification phase Φ_3. The time scale is expressed in units of the master clock period, T_m. Under large voltage excursions, the circuit is able to drive the SAR ADC within the tolerable accuracy margins, as shown in the inset.

Taking into account parasitics, finite gain and bandwidth effects, as well as the non-negligible gate-to-drain capacitances C_m of the OTA (Figure 5.5), the magnitude of the transfer function, $H_{IA}(\omega)$ for both amplifiers takes the form:

$$|H_{IA}(\omega)| = \sqrt{\frac{N_0^2 + N_1^2 + 2N_0N_1\cos(\omega T_s)}{D_0^2 + D_1^2\cos(\omega T_s) + D_2^2\cos(2\omega T_s)}} \tag{5.6}$$

where parameters N_h and D_h, $h = 0,...,2$ can be expressed in terms of circuit parameters. Equation (5.6) is represented for different gain settings in Figure 5.8. The plots, obtained for IA_1, are normalised with respect to the ideal dc gain, $G_{IA} = C_{in}/C_{fb}$. Only the input capacitance has been varied; the feedback capacitance has been kept fixed. For all the configurations, the circuit complies with the settling requirements of the ADC.

Figure 5.8 shows that the amplifier bandwidth, f_{IA}, decreases as G_{IA} in-

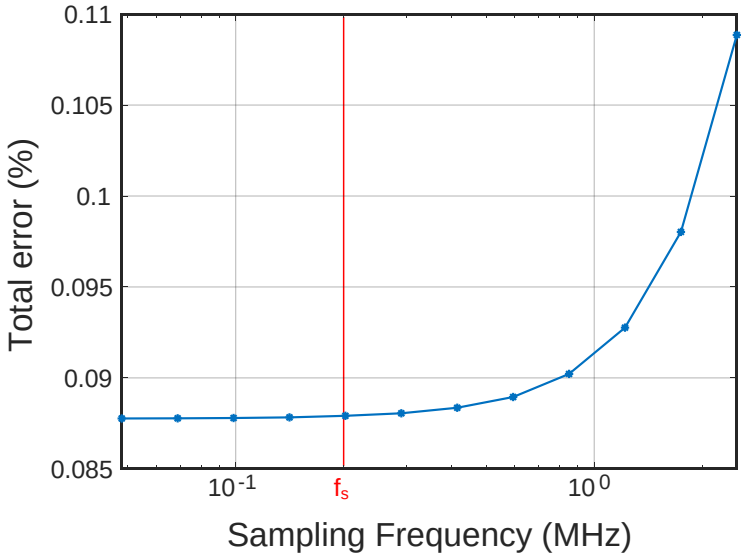


Figure 5.6: Total settling error of the IA_1 against the sampling frequency.

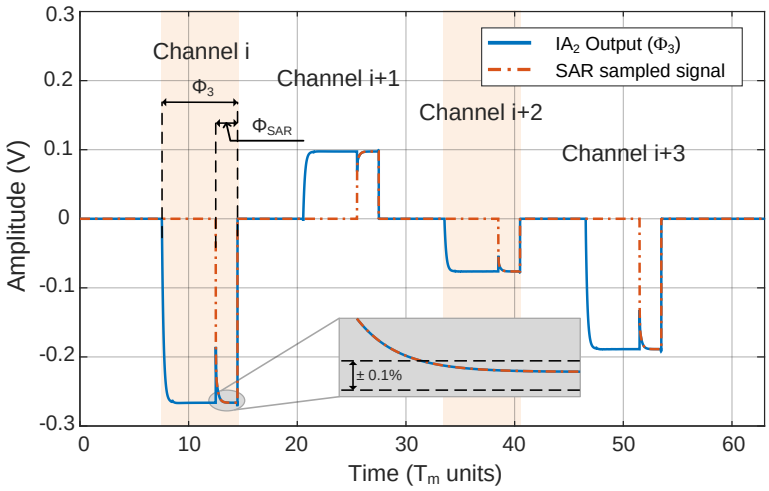


Figure 5.7: Illustration of the output of IA_2 along with timing information. Time unit T_m is the period of the master clock. A similar settling behavior is also observed with IA_1, although with smaller voltage excursions.

creases and it can be made more than one decade smaller than $f_s/2$, thus confirming its narrow-band feature [150]. Additionally, the topology is parasitic-insensitive and exhibits reduced sensitivity to the finite OTA gain [150]. In this work, the dc gain of IA_1 has been chosen so that f_{IA} is close to f_c. The gain of IA_2, with much lower impact on noise performance, has been adjusted, taking into account aspects such as the minimum detectable signal or the input range of the AFE. The pverall AFE dc gain is $G_{AFE} = 200$.

The output-referred noise spectral density of the first IA (simulation and

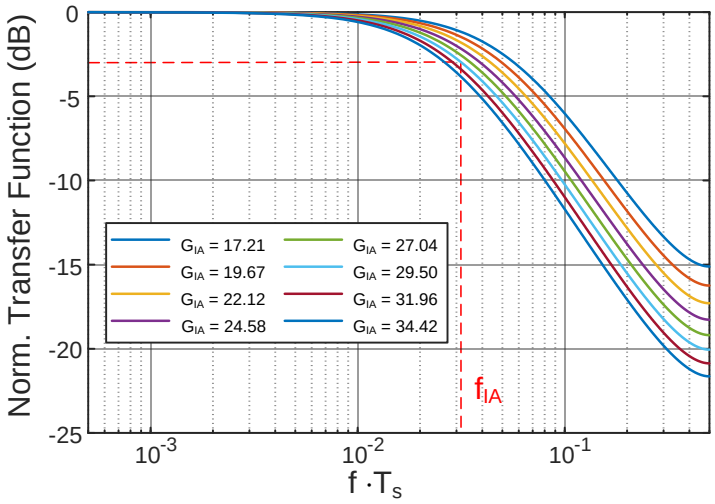


Figure 5.8: Normalised transfer function of the CDS instrumentation amplifier for different gain settings. The IA_1 bandwidth is marked in red.

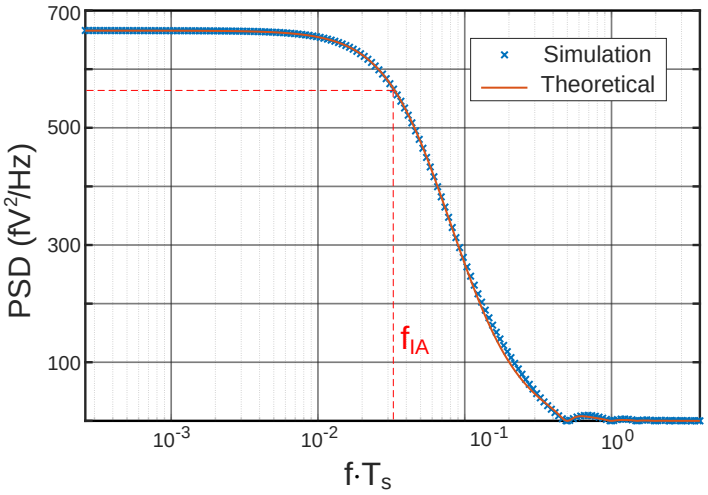


Figure 5.9: Output noise spectral density comparison between simulation results and the proposed model.

experimental results show that more than 80% of noise comes from this stage), taking only into account the white noise contribution from the OTA (this represents more than 94% of the total noise generated by IA_1), can be approximated as [153, 154]:

$$S_{IA}(\omega) = 4\,\mathrm{sinc}^2(\omega T_s/2)\; S_{CDS}(\omega) \tag{5.7}$$

where $\mathrm{sinc}(x) \equiv \sin(x)/x$ and $S_{CDS}(\omega)$ is a spectral density factor which depends on this particular CDS topology (see Appendix A for calculation details). This expression takes into account the folded noise components inherent of CDS techniques. The noise folding factor $N_f \approx \pi f_b / f_s$, where f_b is the OTA band-

width, is essentially defined by the requested settling accuracy and amounts about 7 for IA_1 in this design. Figure 5.9 plots $S_{IA}(\omega)$ for IA_1 using both electrical simulations and equation (5.7). The discrepancy between the plots is lower than 2% in the range from 1 Hz to $4/T_s$, thus confirming the accuracy of the model. Note that the $4\,\mathrm{sinc}^2(\omega T_s/2)$ factor in (5.7), which accounts for the hold operation of the amplifier, provides additional anti-aliasing filtering to the narrow-band amplifier. The side lobes of the noise spectral density are more than 2 orders of magnitude smaller than the spectral density in the passband. The noise equivalent bandwidth is approximately given by $\pi f_{IA}/2$ (assuming a first-order roll-off model), and, hence, similar to the sampling frequency per channel. This allows attenuating the out-of-band noise folded components arising from time multiplexing as illustrated in Figures 5.3(c-d). Hence, the approach effectively reduces the integrated input-referred noise compared to the case in Figure 5.3(b), while power consumption, essentially determined by settling considerations, remains at approximately the same level [17]. Note also that, once in digital domain, the decimation and filtering stage reduces the quantization noise of the ADC and filter out the thermal noise beyond the bandwidth of interest. Hence, the in-band noise power is actually divided by the oversampling ratio, thus palliating the noise folding due to the CDS operation. Furthermore, assuming the same noise folding factor, the OTA bandwidth increases with the oversampling ratio, what decreases the OTA noise floor and, hence, the overall folded noise compared to a non-oversampled system. This is at the cost of additional power and area consumption; however these increments are averaged by the number of channels multiplexed, as will be shown in the next subsection.

It is also worth remarking this combined strategy of narrow-band signal acquisition and oversampling not only holds for the OTA noise but also for the noise from the multiplexed electrodes. Using the microwire array model reported in [17], simulations from extracted layout were run to evaluate the noise contribution of the electrodes ($M = 32$) and the in-band input-referred noise was lower than 3 μV_{rms} in Mode-1, similar to the results presented in [17] with windowed integration sampling techniques.

5.2.3 Scalability

Figures 5.10 and 5.11 illustrate the scalability of the proposed analog front-end, including the ADC, in terms of the number of multiplexed channels (from 16 to 128) and the sampling rate per channel (from 6- to 30 kS/s), respectively. While the former analysis is performed in Mode-1, the latter considers Mode-2 operation. In both cases, changes in power and area consumption, as well as, in-band IRN, have been the metrics used for assessing scalability. In all the analysed configurations, the OTA structure of Figure 5.5, the capacitances in Figure 5.4, the oversampling ratio OSR, and the supply voltage have been preserved as in the current design; however, OTAs have been resized to guarantee operation in

weak inversion.

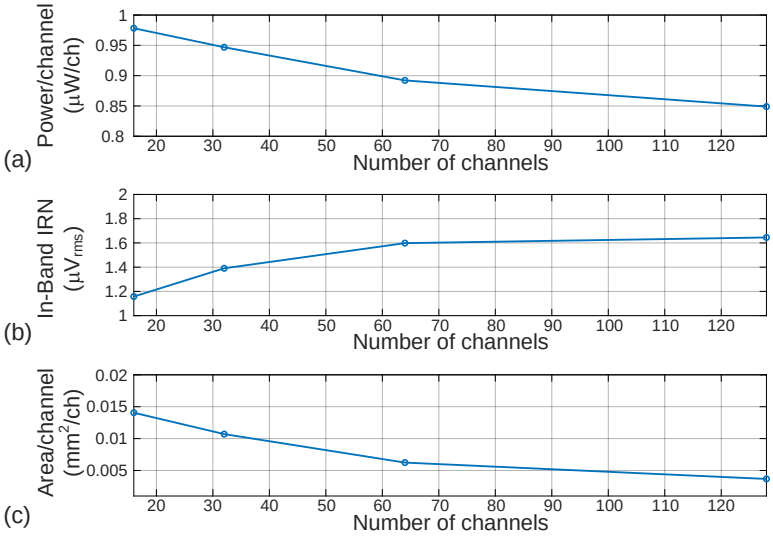


Figure 5.10: System scalability in terms of the number of multiplexed channels: (a) Power consumption per channel; (b) in-band IRN; and (c) area per channel occupation (only analog circuitry).

The OTA power consumption in IA_1 and IA_2 has to increase with the number of multiplexed channels to meet with bandwidth requirements. This is observed in Figure 5.10(a) where the power consumption per channel remains fairly constant with M. Deviations are due to the impact of OTA parasitics (in particular, the gate-to-drain capacitances C_m) on the feedback factor, β_q, of the OTAs – see Appendix A. Further, as the power consumption of the OTAs increases, the intrinsic in-band thermal noise floor of the IAs decreases, thus, partially compensating for the noise folding due to channel multiplexing, for the same settling accuracy. This is illustrated in Figure 5.10(b) where only a mild increase in IRN is observed with the number of multiplexed sites. Finally, it is observed that, although the OTA dimensions have to scale with their power consumption to keep input transistors in weak inversion, the total area occupation per channel of the analog circuitry (only 10 % of the total active area) actually decreases, as shown in Figure 5.10(c).

Similar arguments hold if the sampling rate per channel is increased for the recording of action potentials, typically at 30 kS/s [10]. As shown in Figure 5.11(a) and (c), the power consumption and the area occupation per channel increase with the recording bandwidth. However, increasing the recording bandwidth can only be done by increasing OTA bandwidths which, in turn, decreases the noise thermal floor and, thereof, the rms value of the aliased noise components due to multiplexing. Accordingly, the in-band IRN decreases with the recording bandwidth as illustrated in Figure 5.11(d).

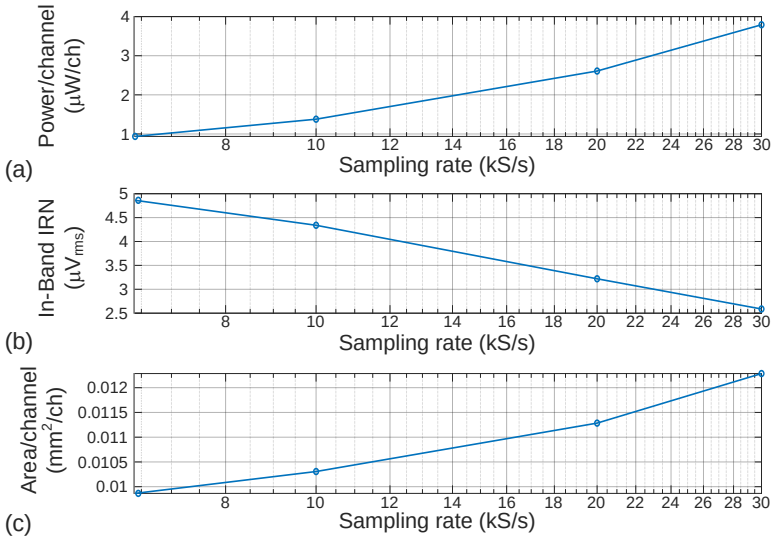


Figure 5.11: System scalability in terms of bandwidth: (a) AFE power consumption per channel; (b) in-band IRN; and (c) area per channel occupation (only analog circuitry).

5.3 Digital Processing

The samples converted by the SAR ADC are demultiplexed in digital domain by cyclically filling a 32-location memory block using a 5-b counter for address selection. This effectively decreases the sampling rate per channel to f_c. As shown in Figure 5.1, the stored codes, V_{ADC}, are then serially transferred to either the auto-ranging block or the DC servo-loop, this latter via a decimation and filtering circuit which is implemented by a 2nd-order Cascaded Integrator–Comb (CIC) filter (see Figure 5.12).

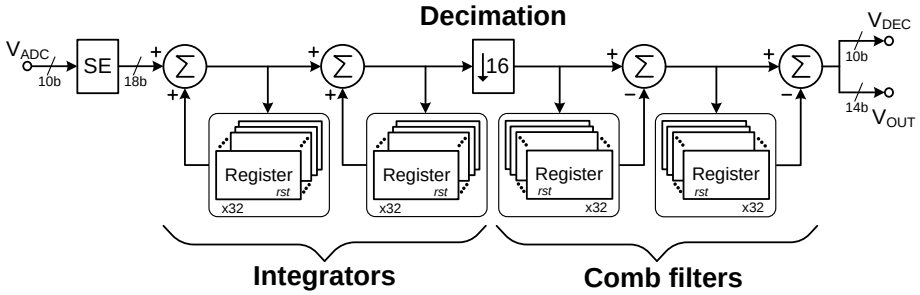


Figure 5.12: Block diagram of 2nd-Order CIC filter with decimation.

5.3.1 DC Servo Loop

The purpose of the DSL is twofold: (i) to limit the offset at the input of the front-end IA and (ii) to place a high-pass pole in the AFE transfer function. The

proposed architecture is shown in Figure 5.13 and consists of two main elements; a digital integrator and a binary search algorithm block, both operating serially over the 32 multiplexed channels. The former has been preferred for filtering instead of high-order FIR/IIR structures as they require larger area occupation and may even lead to stability problems [155]. Similar to [17], a binary search block has been chosen for driving the DACs instead of ΣΔ modulators [25, 97]. Because of the TDM operation, such modulators would require large oversampling frequencies and/or high-order topologies, which would demand large power consumption and area occupation. In the proposed approach, the DSL output code is only updated when necessary (for instance, if offset drifts are detected), avoiding the onset of potential oscillations at the AFE input.

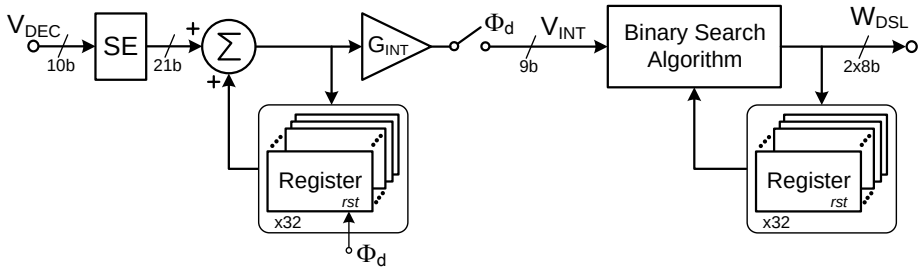


Figure 5.13: Block diagram of the Binary Search DC Servo Loop.

The gain factor, G_{INT}, of the integrator has been chosen as the largest integer power of 2 satisfying [155]

$$f_{hp} \leq \frac{B_w}{\pi} \ln\left(\frac{1}{1 - R_C\, G_{DC}\, G_{INT}}\right) \tag{5.8}$$

where f_{hp} is the intended frequency for the high pass pole of the AFE transfer function (in the proposed design $f_{hp} = 0.5$ Hz), G_{DC} is the DC gain of the AFE feedforward path and R_C is the ratio between the total DAC capacitance, i.e., $C_{tot} = C_u(2^8 - 1)$, and the input capacitor, C_{in}. In this design, G_{INT} must be at least 1/6000 so it has been rounded off to $1/2^{13}$ for easy implementation through bit shifting.

The integrator accumulates the V_{DEC} values (extended to 21-b to avoid overflows) provided by the decimation and filtering stage. Every $T_d = 2^9/B_w$ period (aprox. 3 seconds long) at instances of pulses Φ_d, the output of the integrator, V_{INT}, is transferred to the binary search block and then it is initialized to 0 to start a new count.

Either at start up or on-demand through a reset operation, the binary search block solves the binary words of the input DACs, W_{DSL}, sequentially from Most Significant Bit (MSB) to Least Significant Bit (LSB), based on the V_{INT} values provided by the integrator. As is conventional, every bit is decided at each iteration based on the sign of V_{INT}. During the process, the auto-ranging block is disabled so it does not interfere in the binary search. Once the search is

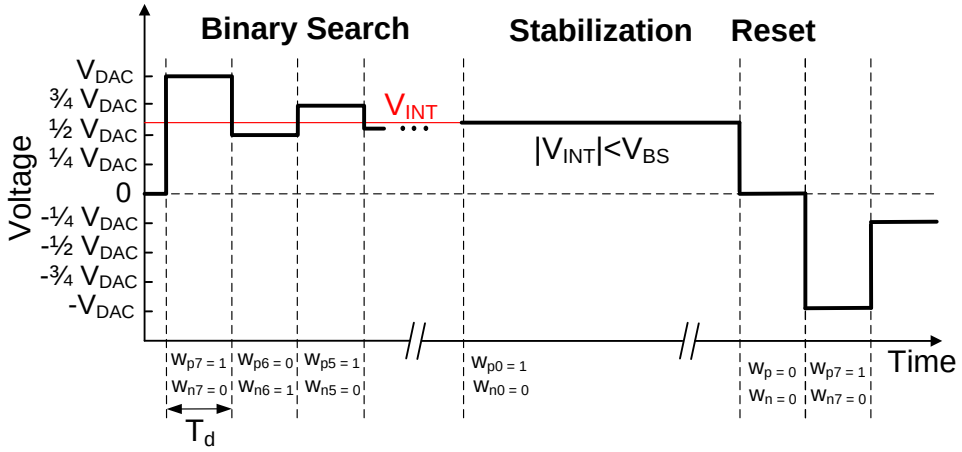


Figure 5.14: Illustration of the different operation modes of the binary Search block.

completed, the block assesses that the following V_{INT} instances verify $|V_{INT}| < V_{BS}$, where V_{BS} is a threshold value corresponding to the maximum tolerable offset at the AFE input. In this design, $V_{BS} = V_{LUT}(2_{10})$, i.e., the ADC code stored in the LUT after calibration corresponding to 2 DAC LSBs. If the condition is met, W_{DSL} preserves its previous values, otherwise, it is incremented or decremented by 1 DAC LSB to compensate for potential DC drifts as large as 0.4 mV/s (this is 25% larger than the drift rates experimentally measured in [18]). This mechanism provides dc baseline stabilization.

5.3.2 Auto-Ranging Loop

The purpose of the ARL is to make the recording system tolerant to undesired high amplitude interferers or artifacts. More specifically, the feedback loop avoids the onset of saturation in the AFE main signal path whenever the input signal exhibit variations below 40 V/s and, in case of faster transitions, it provides mechanisms for quick recovery into non-saturated system operation. This is particularly relevant in monopolar sensing mode where signals are acquired with respect to a common reference and may exhibit larger voltage swings than in bipolar mode.

The ARL operation is triggered when the input neural signal, contaminated by the interferer, exceeds threshold voltages, $\pm V_{th}$, beyond the useful signal range. In this work, V_{th} amounts 2.5 mV_p; much larger than the peak amplitude of LFP/ECoG signals which is typically below 1 mV_p [25]. If the input signal surpasses these limits, the ARL block generates voltage increments which are added or subtracted at the AFE input to take the signal back to the $\pm V_{th}$ range. Similar auto-ranging procedures were proposed in [55, 9]. Along this operation, no attempt is made to distinguish between neural signals and interferers, as the ARL block does not rely on the use of complex filtering stages or template-based mechanisms for artifact detection and suppression [12].

The block diagram of the ARL circuit is shown in Figure 5.15. First, a dead zone operator with bounds at $\pm V_{th}$ is applied in the incoming V_{ADC} signal to obtain

$$V_Z(l) = \begin{cases} V_{ADC}(l) - V_{th} & , V_{ADC}(l) > V_{th} \\ 0 & , |V_{ADC}(l)| \leq V_{th} \\ V_{ADC}(l) + V_{th} & , V_{ADC}(l) < -V_{th} \end{cases} \tag{5.9}$$

where l is a time index at a clock rate f_c. Any $V_Z(l)$ outside the dead zone is deemed to be affected by a high amplitude interferer. Then, the auto-ranging block generates the correction code

$$W_A(l) = \begin{cases} W_A(l-1) - \alpha V_Z(l) & , V_Z(l) \neq 0 \\ W_C(l-1) & , V_Z(l) = 0 \end{cases} \tag{5.10}$$

which is fed back to the AFE input (Figure 5.1).

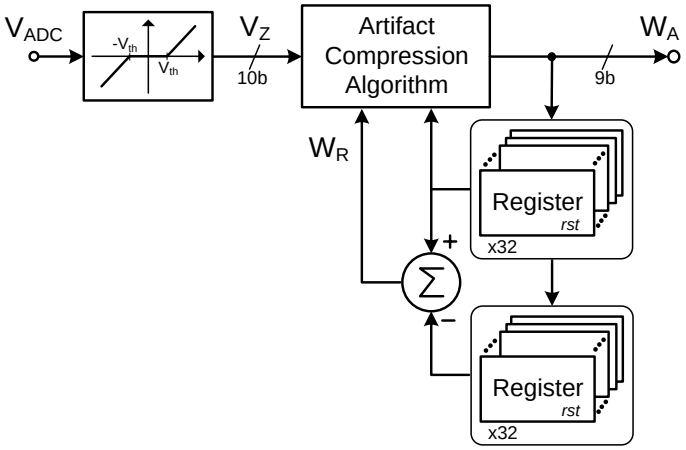


Figure 5.15: Block diagram of the auto-ranging circuit.

If $|V_{ADC}(l)| > V_{th}$, the correction code $W_A(l)$ aims to take the next V_{DAC} instance back, or at least closer, to the dead zone. No overflow is permitted, i.e., the magnitude of $W_A(l)$ is limited by an all-ones word. The scaling factor α is nominally given by the voltage gain from the DAC input to the ADC output as,

$$\alpha = \frac{V_{BG}}{V_{DD}} \frac{2}{R_C \, G_{DC}} \tag{5.11}$$

where the factor 2 accounts for the 1-b difference between the DAC and ADC resolutions. In practice, α has been rounded to the nearest power of 2 so scaling can be simply implemented through bit shifting.

If $|V_{ADC}(l)| \leq V_{th}$, two cases can be distinguished; either there is no artifact or an artifact is ongoing but V_{ADC} is comprised within the dead zone. Accordingly, variable W_C in (5.10) is given by,

$$W_C(l) = \begin{cases} 0 & , |W_R(l)| \leq W_{BS} \\ W_A(l) & , |W_R(l)| > W_{BS} \end{cases} \tag{5.12}$$

where W_{BS} amounts 2 DAC LSBs and the control variable $W_R(l)$ to decide between both states is simply given by the W_A increment, $W_R(l) = W_A(l) - W_A(l-1)$. From (5.12), if the accumulated value of $W_R(l)$ remains below a given tolerable offset deviation W_{BS}, it means that the artifact has concluded and $W_C(l) = 0$. Otherwise, $W_C(l)$ takes on the current correction code $W_A(l)$. This is done to avoid that a potentially large residual offset is held at the AFE input. In Figure 5.15, the control variable W_R is serially calculated per channel by taking the difference between corresponding positions of two daisy-chain memories, one for $W_A(l)$ and the other for $W_A(l-1)$.

The correction codes W_A are transferred to the AFE DACs at a rate f_s to voltage shift input samples and compress, within the dead zone limits, the high-amplitude input signal formed by the superposition of the neural record and the interferer (no matter its morphology or origin). These auto-ranged input samples pass through the AFE direct signal path to obtain the system outputs. In mode-1 operation, the neural information in the band of interest can be recovered after decimation and filtering, although contaminated by the filtered residues of the interference and the ARL voltage compensation. These residues are due to the limited quantization of the DAC and, in sum, account for the finite attenuation of the artifact. Such attenuation depends on the amplitude and frequency content of the interference. In both cases, the larger the values, the higher the attenuation because the larger are the differences between the neural signal of interest and the artifact. This is illustrated in the 3D plot of Figure 5.16 which shows the achievable attenuation versus the frequency and amplitude of the interference when the system is configured in monopolar sensing mode with no delta encoding. In this plot, input signals are formed by the superposition of two tones: a 2 $\mathrm{mV_{pp}}$ tone at 30Hz emulating useful neural signal and a variable tone, representing the artifact, with amplitude larger than 3 $\mathrm{mV_{pp}}$ (for triggering the auto-ranging mechanism) and frequency lower than half the sampling rate per channel, f_c. Note that the attenuation is smaller in the baseband and grows significantly for larger frequencies, particularly for high amplitude interferers. Larger attenuations could be accomplished by narrowing the dead zone, however, this is at the expense of increasing the activity of the auto-ranging loop and, therefore, its power consumption. Similarly, the attenuation could be improved for low frequency interferers by increasing the scaling factor α; however, this increases the chance for saturation at higher frequencies. For all the artifact configurations in Figure 5.16, the tone at 30Hz is recovered with eventual artifact-induced perturbations which, in any case, do not take the output signal out of the threshold limits. This will be illustrated in Chapter 6.

In Mode-2, input signals are fully reconstructed, including artifacts, by reverting in digital domain the correction codes W_A previously injected at the AFE input. To this end, the V_{ADC} values corresponding to each possible W_A code have to be determined, taking into account not only the DAC nonidealities (mainly due to capacitor mismtach) but also any deviation in the AFE signal

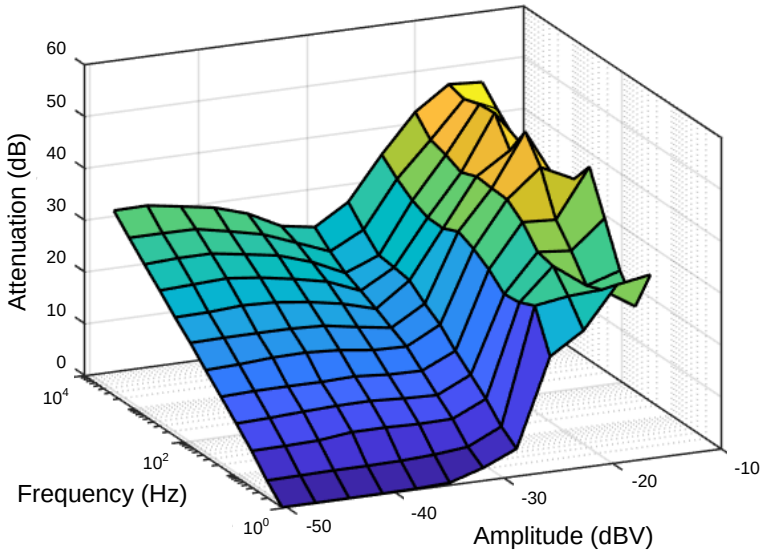


Figure 5.16: Attenuation of sinusoidal artifact versus tone frequency.

path. This vector mapping is obtained through an off-line calibration process in which the DAC is externally driven by a ramp sequence sweeping all W_A values. The process does not modify any circuit in the AFE nor use any extra technique; it just stores in a 9×10 Look-Up Table (LUT) the ADC-converted versions of the referred deviations. Based on these values, the losslessly restoration of the input voltage at instant l, $V_R(l)$, including uncompressed artifacts, can straightforwardly be obtained as,

$$V_R(l) = V_{ADC}(l) + V_{LUT}[W_A(l-1)] \tag{5.13}$$

where the last term represents the voltage stored in the LUT for the correction code W_A.

CHAPTER 6

EXPERIMENTAL RESULTS AND DISCUSSION

Figure. 6.1(a) shows a die photograph of the ASIC, fabricated in a standard 180 nm CMOS process. Its total active area is 0.70 mm^2. Figure 6.1(b) shows both sides of the test PCB. The ASIC, together with the μ-C and the electrode connector, is placed at the top (picture on th left), while a battery is located at the bottom (picture on the right). The power supply of the ASIC, provided by a voltage regulator connected to the battery, is 1.2 V.

6.1 Electrical Characterization and System Validation

Powered by the battery, in Mode-1, the ASIC consumes 48 μW so the power consumption per channel is 1.5 μW/ch. The power budget, dominated by the first IA, is illustrated in the pie chart of Figure 6.2. In Mode-2 for artifact restoration, the power consumption raises to 82 μW due to the increased data transfer rate to the μ-C.

Figures 6.3-6.6 show measurements for single input channel characterization. Unless otherwise stated, the ASIC was configured in Mode-1, using monopolar sensing mode without delta encoding and the output was taken directly from the decimation stage with no extra processing. Channel #1 was indistinctly taken for analysis – no meaningful differences were observed for the other channels. In all cases, the reference was connected to ground.

Figure 6.3(a) shows the transfer function of the AFE, obtained by applying input tones of 1 mV_{pp} amplitude at different frequencies (solid dots in the figure).

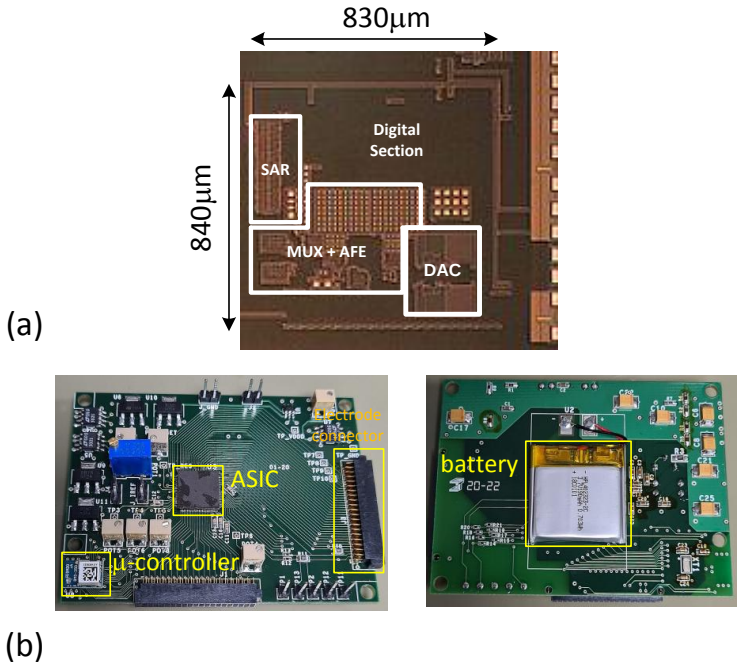


Figure 6.1: (a) Die photograph of the ASIC prototype. (b) PCB for the testbench.

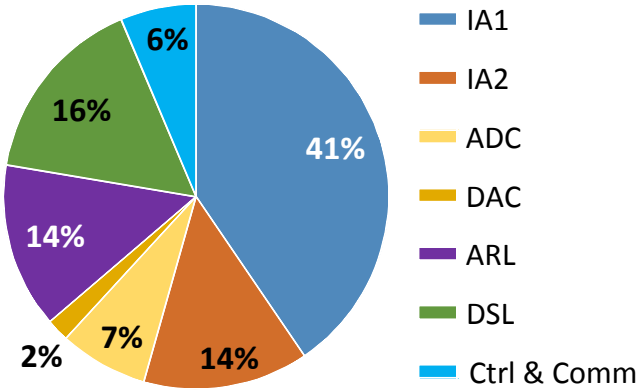


Figure 6.2: System's power budget.

The bandpass characteristic is bounded by the 0.5 Hz one-pole roll-off due to the DSL integrator and the 200 Hz cut-off frequency of the CIC filter at the decimation stage. The gain in the passband is 45 dB. The input referred noise of the front-end is illustrated in Figure 6.3(b). It was measured by shorting channel #1 and the reference and referring the decimated codes back to the AFE input. The noise floor in the passband is 85 nV/$\sqrt{\text{Hz}}$ for a total in-band rms input-referred noise of 1.4 μV_{rms}. This includes the kT/C noise from the input DAC capacitors which contribute less than 0.2 μV_{rms} to the total IRN, regardless of the DAC settings (see Figure 6.4). The noise generated by the DAC voltage reference is negligible compared to the DAC switching noise. Taking into account the $1/f^2$ spectral content of LFP and ECoG signals [156] and the fact

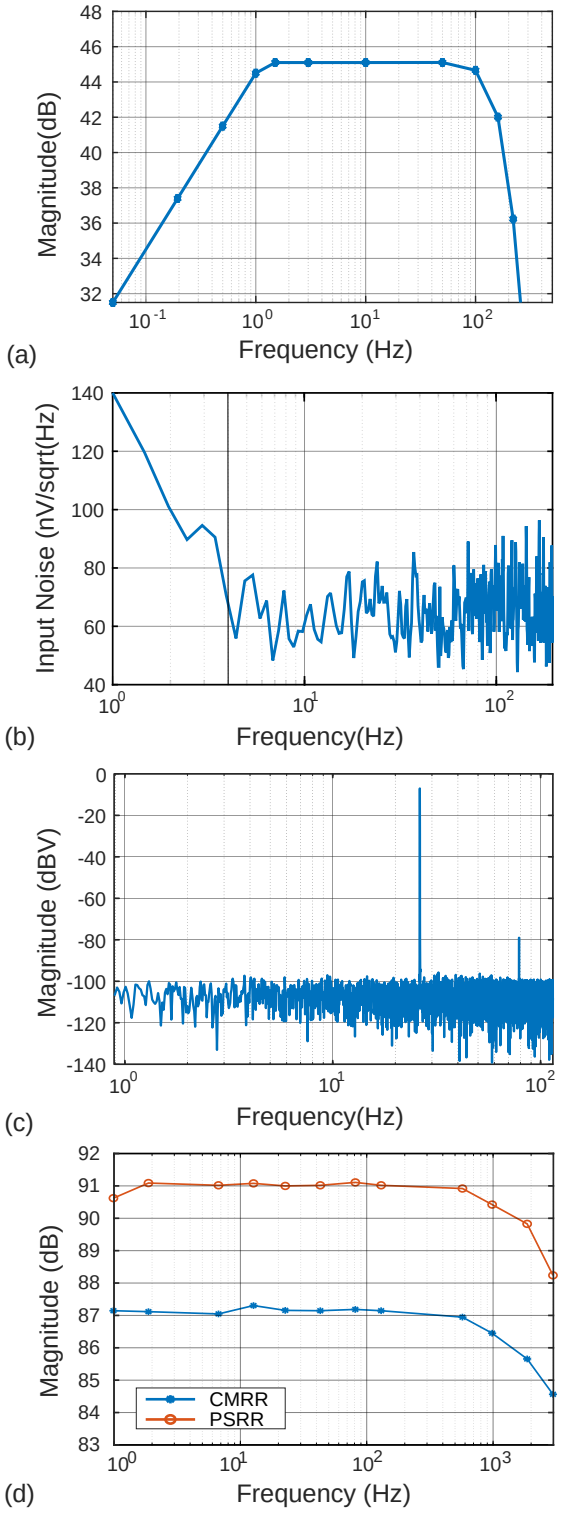


Figure 6.3: (a) Measured AFE transfer function. (b) Input referred noise of the AFE. (c) Output spectrum of the AFE with input tone of $5mV_{pp}$ at 27Hz. (d) CMRR and PSRR.

that power peaks are typically observed in the alpha and beta frequency bands [157, 158], the linearity of the AFE was evaluated in these bands. Figure 6.3(c) shows the measured output referred spectrum for a 5 mV_{pp}, 27 Hz tone in beta band. It shows a Total Harmonic Distortion (THD) of 75 dB. Figure 6.3(d) shows the experimental measurements of the CMRR and the Power Supply Rejection Ratio (PSRR). In this case, measurements were taken from the output of the ADC (Mode-2), without decimation and filtering. In the CMRR case, a set of 5 mV_{pp} tones with a common mode of 200 mV was applied to the input and reference electrodes at the same time. As shown, the CMRR amounts 87 dB in the passband. Measurements also demonstrate a common-mode input range as large as 600 mV_{pp}. For PSRR measurement, the regulated power suply was replaced by a 20 mV_{pp} tone superposed to V_{DD}. Approximately a PSRR of 91 dB is obtained.

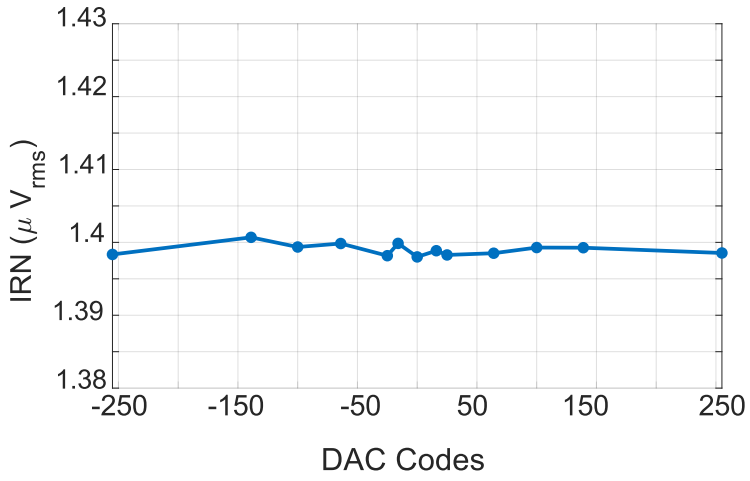


Figure 6.4: Measured AFE input-referred noise for different DAC settings.

The equivalent input impedance, Z_{in}, of channel #1 was measured w/ and w/out multiplexing using an input signal of 1 mV_{pp} at 100 Hz. Before multiplexing, Z_{in} was obtained for all the possible settings of the capacitive bank, C_{ib}, in the IBL around amplifier IA1 (see Figure 5.4). The measured values were: 41-, 71-, 104- and 64- MΩ. The system was then operated in TDM with the highest Z_{in} configuration to evaluate the input impedance of channel #1 again. It was observed that Z_{in} slightly decreased to 100 MΩ. This decrease is attributed to the leakage currents of the switches in OFF state. According to simulations, the input impedance without IBL is only 800 kΩ, so there is about 100 × improvement in Z_{in} when IBL is used.

To illustrate the auto-ranging block operation a 67 Hz, 1 mV_{pp} input tone was superposed to a large 100 mV_{pp} pulse train [55]. The output signals obtained by the recording system in both operation modes (in two independent tests) are shown in Figure 6.5. In Mode-1, Figure 6.5(a) shows that, after a short transient, the filtered and decimated output wave tracks the full-swing signal excursions

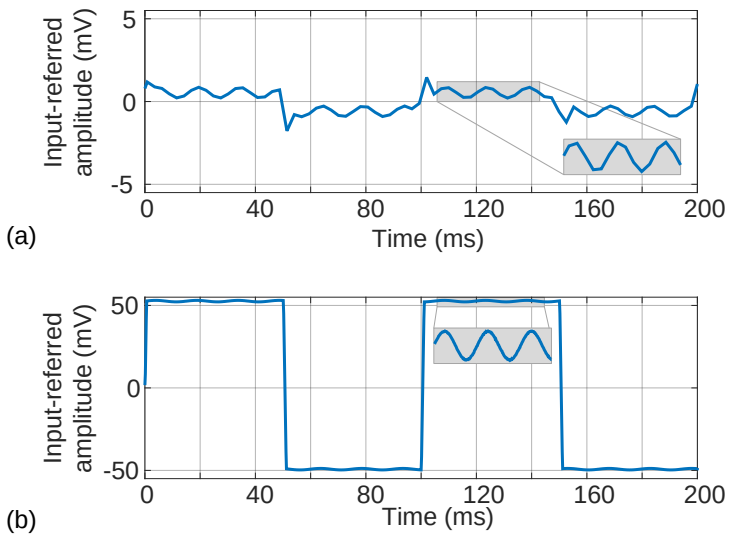


Figure 6.5: Measured transient response to large input signal (a) after filtering and decimation (Mode-1). (b) after signal reconstruction (Mode-2).

without saturation. In Mode-2, Figure 6.5(b) shows the reconstructed output signal after the deterministic decoding of the ARL word. In this case, no transient is observed and the time resolution is larger, however, this is at the expense of a higher noise level because the ARL output is not decimated.

Figure 6.6 shows the AFE Signal-to-Noise and Distortion Ratio (SNDR) as a function of the in-band input signal amplitude for both Mode-1 and Mode-2. In Mode-1, the dynamic range amounts 71 dB. In this design, the quantization noise of the ADC after decimation falls well below the noise floor of the AFE and, accordingly, the lower bound in Figure 6.6(a) is essentially due to the input-referred noise. The upper bound is at approximately -43 dBV, however, interferences as large as -17 dBV can be tolerated without saturation thanks to the auto-ranging block. In that sense, the input dynamic range extends in practice to 71 dB + 26 dB (with ARL). In Mode-2, the dynamic range amounts 83 dB based on the lossless reconstruction of input signals. However, in this case, the input referred noise raises to 4.8 μV_{rms}.

The experimental measurements in Figures 6.7-6.10 were carried out by reproducing with 2 function generators (Tek AFG3102) 4 pre-recorded 100 s long *in-vivo* LFP segments repeated 8 times in the same order along the 32 input channels. To this end, a small auxiliary board for connections was implemented. These signals were previously recorded from a Long-Evans rat model using 4 adjacent channels of a Utah array (Blackrock Microsystems, LLC) [10]. From top to bottom, Figure 6.7 shows (a) the input signals applied to channels #1 to #4, (b) the input-referred output signals obtained in Mode-1 using bipolar sensing, (c) the decoded signals calculated with (5.5) using the ASIC outputs, (d) the decoded signals when the residual offsets are filtered out by the high-pass filter in the micro-controller and (e) the differences between the signals

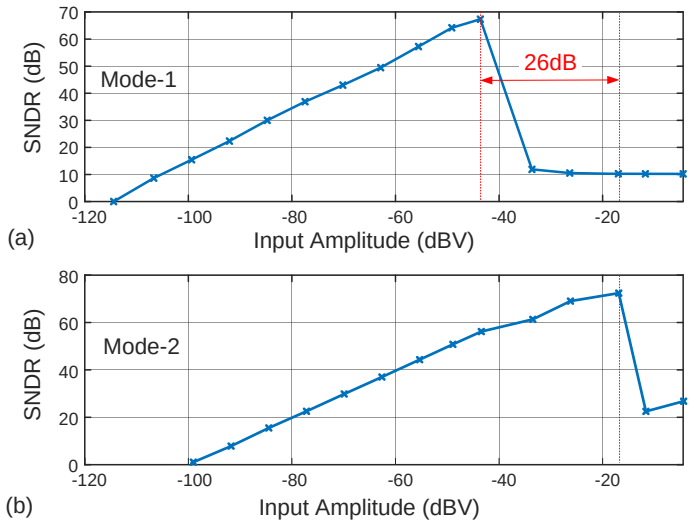


Figure 6.6: SNDR versus input amplitude for (a) Mode-1 and (b) Mode-2.

shown in (a) and (d), after removing the intentional offsets superposed in (a). Note that the input signals exhibit quite different DC offsets to illustrate the correct settling behavior of the AFE and the effectiveness of the DC servo loop. Comparing Figure 6.7(a) and (b), it can be also observed that the amplitude range of spatial delta encoded signals, inherently available in bipolar sensing mode, is smaller than the input channel voltages, excepting for channel #1 which is measured against the reference electrode according to (5.4). Indeed, it has been measured that the effective output code range is compressed by about 60% with spatial delta encoding. Similar results were also obtained with delta-encoded monopolar signals. This compression rate is also corroborated in Figure 6.8, whose histograms are presented in Figure 6.9.

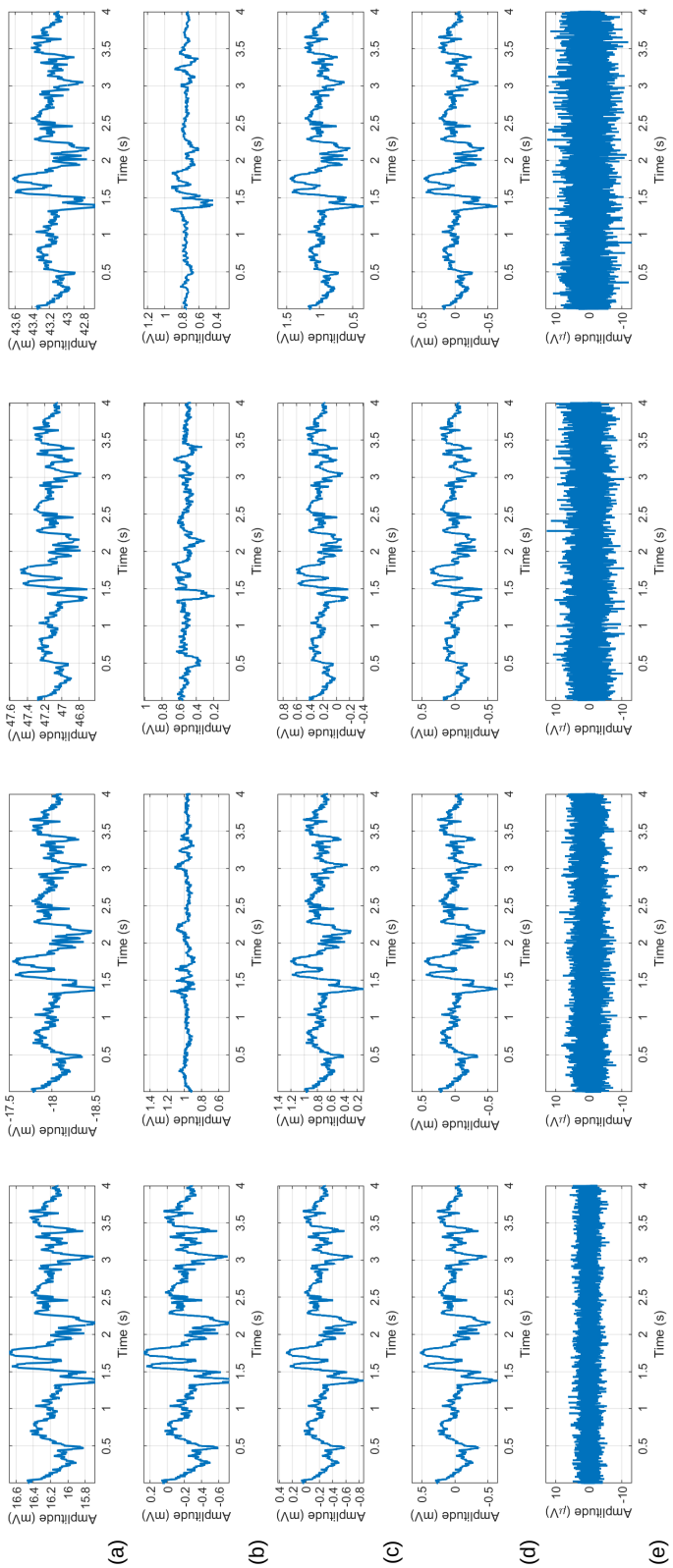


Figure 6.7: Signal set from channels #1-#4 to illustrate the spatial delta encoding techniques implemented in the ASIC: (a) Input signals, (b) input-referred signals using bipolar sensing mode, (c) input-referred signals after decoding, (d) same with residual offsets removed with the HPF in the micro-controller and (e) Input-referred decoding error.

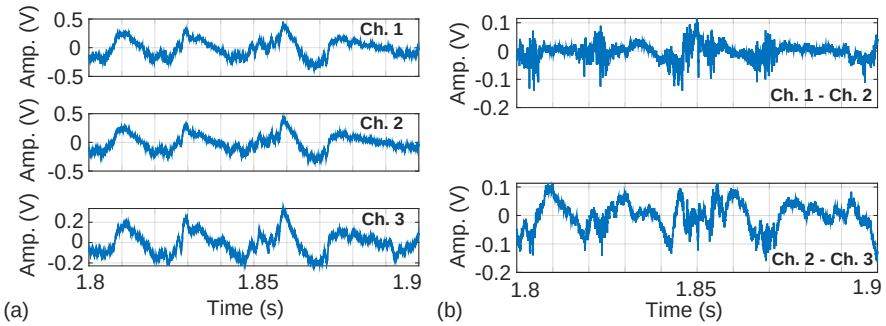


Figure 6.8: ADC output w/out (a) and with (b) bipolar sensing.

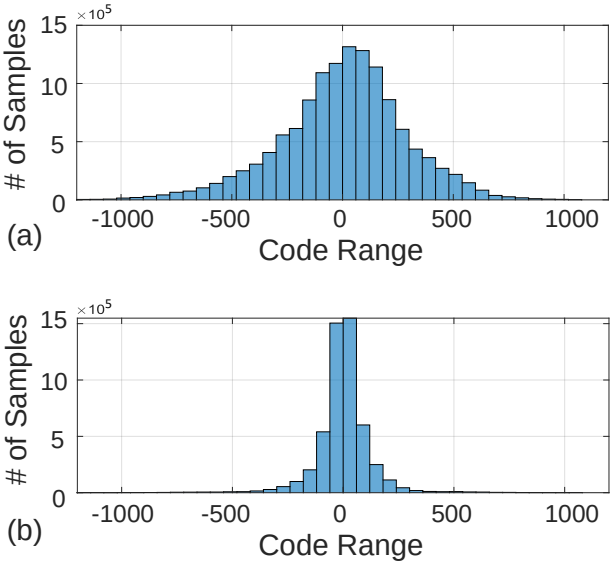


Figure 6.9: Output code range histograms for signals from Figure 6.8 w/out (a) and with (b) bipolar sensing.

It is worth observing from Figure 6.7(e) that decoding errors in bipolar sensing mode increase with the channel order. This is due to the cumulative nature of (5.5). In fact, it can be shown that the output-referred noise power, $\overline{v_{no,k}^2}$, of the k-th reconstructed signal can be approximated as,

$$\overline{v_{no,k}^2} \approx \frac{i}{OSR}\left[\frac{h^2}{12} + G_{AFE}^2 \cdot \overline{v_{n,\Delta}^2}\right] \tag{6.1}$$

where i is given by (5.2), h represents the ADC resolution after decimation and filtering and $\overline{v_{n,\Delta}^2}$ is the in-band input-referred noise variance of the Δ_k increments in (5.4) before conversion. Hence, the output rms noise increases with the square-root of index i. This problem observed with bipolar sensing is not present in delta-encoded monopolar signals because both coding and decoding are implemented in digital domain [see (5.3) and (5.5)] and errors cancel out

along signal decoding. This is illustrated in Figure 6.10 which compares the experimental output signals generated by the encoded monopolar and bipolar techniques after decoding. In both cases, the reconstructed signals are compared to the input signals and the mean absolute value deviations are quantified in effective LSBs. Measurements have been taken over the 32 available channels. Clearly, with monopolar signals, coding errors remain independent of the channel order. This suggests that bipolar recordings can relax specifications on AFE dynamic range, DC offset rejection or CMRR but they should be periodically refreshed to avoid that decoding errors increase indefinitely.

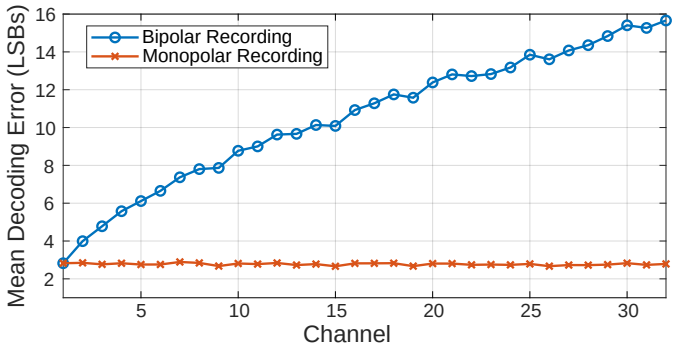


Figure 6.10: Average decoding output error obtained by the monopolar and bipolar spatial delta-encoding in terms of the channel index i.

The main objective in this design was the recording of LFP/ECoG signals; however, it is not completely true that spikes cannot be recorded. Certainly, it is not possible in Mode-1, but APs can be acquired in Mode-2 at a sampling rate of 6kS/s. This can be appreciated in Figure 6.11 using a pre-recorded in vivo signal (similar to that used in Figure 6.7). Figure 6.11, (a) shows the original signal sampled at 30kS/s and (b) shows the signal captured by our circuit in Mode-2. As can be observed, spikes can be identified although with lower number of samples compared to the input signal as well as some increase in the noise floor because the signal is not decimated and filtered. However, it is hardly feasible to identify the putative single-units responsible for the spikes with such a low number of samples.

6.2 In-vitro Measurements

The following experiments were made with recording electrodes immersed in a Phosphate Buffered Saline (PBS) solution. Electrical signals, either in current or voltage form, were applied to the solution through a platinum electrode and recordings were captured in monopolar, non-coded configuration. Figure 6.12 shows the experimental setup.

The crosstalk between channels was evaluated in saline by applying a set of 5 mV_{pp} tones to channel #1 (aggresor) and measuring the impact on the

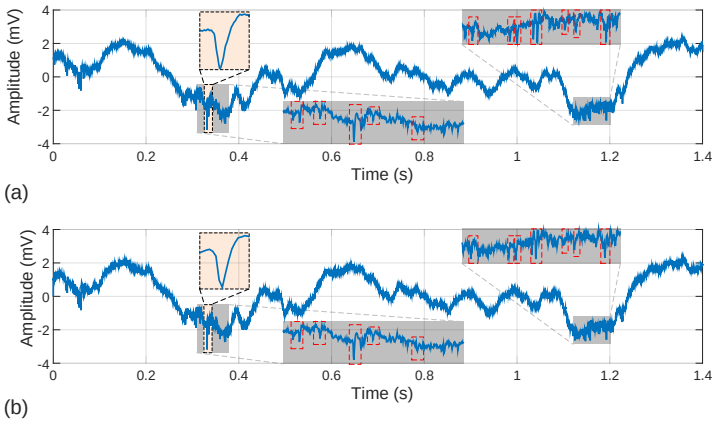


Figure 6.11: (a) Pre-recorded in vivo signals containing APs captured at 30kS/s. (b) Signal captured by the proposed circuit in Mode-2 at 6kS/s.

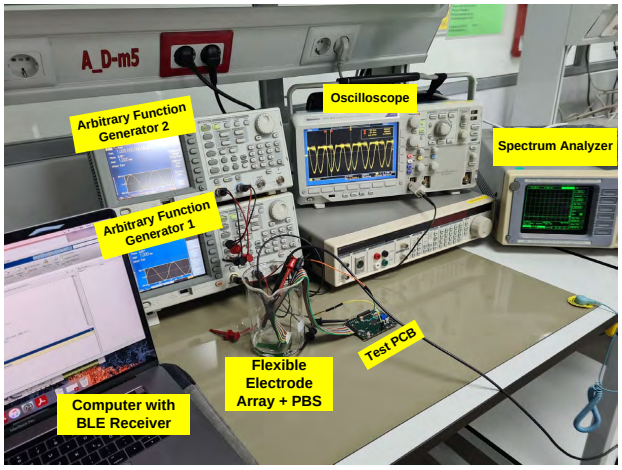


Figure 6.12: Experimental setup for *in-vitro* measurements.

other channel (victims) which were referenced to ground. These measurements showed that interferences remain below −62 dB for all channels across the signal band. However, this result cannot be attributed to the ASIC because same results were measured from the unmounted PCB alone. The capacitive couplings between the long interconnection lines running in parallel on the PCB are likely the cause of the observed crosstalk (similar to illustrated in Chapter 2). Hence, it can be estimated that the crosstalk induced by the ASIC is lower than the referred value (−85 dB according to simulations).

Figure 6.13 shows the results obtained when the solution was voltage driven by a long pre-recorded motion artifact superposed on a 1.5 mV_{pp}, 78 Hz tone as signal of interest. A polymide-based sub-dural microelectrode array with 32 nanoporous gold electrodes separated by 300 μm (diameter 30 μm) was used for signal recording. The input waveform is shown in Figure 6.13(a), while Figures 6.13(b-e) show the outputs obtained from channel #1 along three different

experiments with the same signal. Figure 6.13(b) shows the output when the ARL is disabled, resulting in the saturation of the AFE main signal path and, therefore, the lost of the signal of interest. In another experiment, Figure 6.13(c) shows the system output in Mode-1 with ARL enabled. Note that the signal of interest can be recovered although perturbed by the imperfect cancellation of the artifact, which is attenuated by 22dB (in agreement with Figure 5.16). In any case, the output safely remains within the linear range of the AFE. Finally, Figures 6.13(d) and (e) show, respectively, the compression code from the ARL loop and the reconstructed input signal in Mode-2. In this case, the combined waveform can be recovered with 99% correlation accuracy with respect to the original signal.

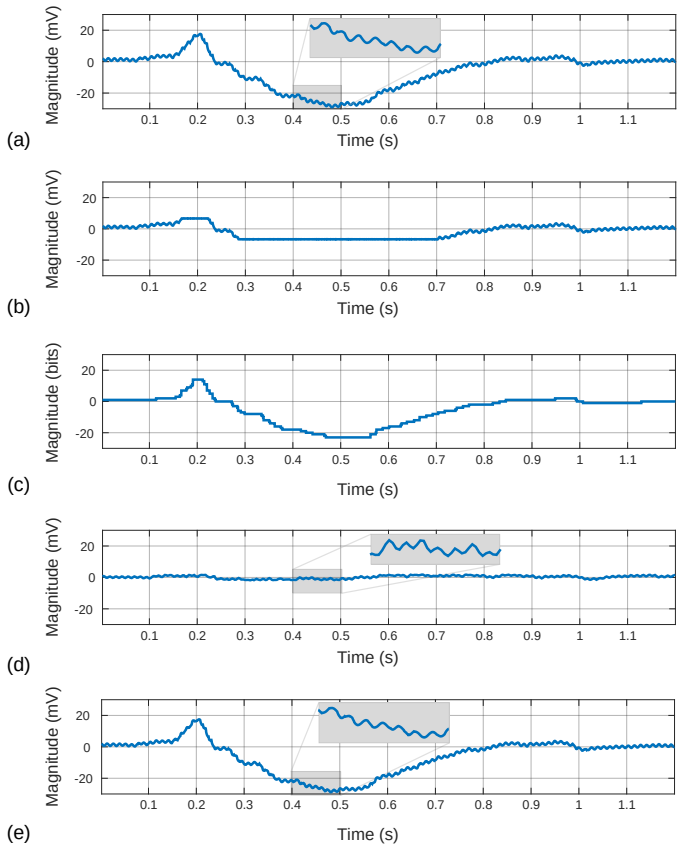


Figure 6.13: (a) Pre-recorded motion artifact plus in-band 1.5 mV_{pp} tone applied to the saline solution, (b) output with ARL disabled, (c) Mode-1 output signal, (d) artifact compression code and (e) reconstructed signal in Mode-2.

Using the same setup as in Figure 6.13, a symmetric biphasic stimulation current pulse was applied to the PBS solution through a voltage-controlled Howland current pump circuit. The duration of the cathodic/anodic phases is 2 ms, with an interphase delay of 400 μs, and a peak current amplitude of 100 μA. Figure 6.14(a) shows the voltage recorded at the electrode interface with a commercial acquisition system (USB-ME32-FAI, Multi Channel Systems

MCS, GmbH). The other plots in Figure 6.14 were obtained with the proposed neural recording system along three different experiments with the same current stimulation. As in the previous example, Figure 6.13(b) shows the output with no auto-ranging, resulting in saturation; Figure 6.13(c) shows the system output in Mode-1 with ARL enabled and Figures 6.14(d) and (e) were obtained in Mode-2, representing the correction code and the reconstructed output, respectively. In this case, the reconstructed signal, including the artifact, is also almost identical to the signal recorded with the commercial equipment (97% correlation) and the attenuation of the artifact in Mode-1 amounts 25dB.

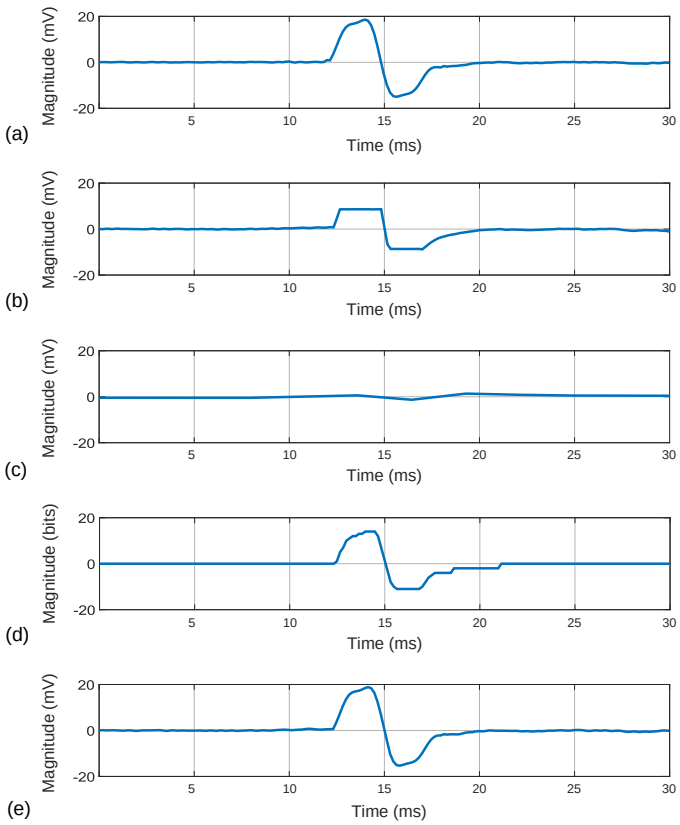


Figure 6.14: (a) Voltage in the saline solution after applying a biphasic stimulation current pulse, (b) output with ARL disabled, (c) Mode-1 output signal, (d) artifact compression code and (e) reconstructed signal in Mode-2.

Table 6.1 compares the presented proposal to other state-of-the-art high dynamic range neural recording systems. Although operation in Mode-2 is conceived as an auxiliary testing facility, it has also been included in the table for completeness. The table includes other artifact-aware [58, 9, 55, 41] and TDM [17, 12] proposals reported in the literature. As can be seen, this work performs comparably to other proposals along all metrics with noticeable improvements on input range, CMRR, linearity and dynamic range. Furthermore, all the functionalities discussed in this work have been implemented on-chip

with the exception of the large interference reconstruction operation in Mode-2, which is done in the μ-C.

Table 6.1: Comparison with State of the Art

	[9]	[41]	[17]	[55]	[58]	[12]	**This work**	
							Mode-1	**Mode-2**
Year	2014	2017	2018	2018	2019	2020	**2020**	
Technology (nm)	180	180 HV	180	65	130	65	**180**	
Supply voltage (V)	1	1	1	0.8	1.2	2.5	**1.2**	
Power per channel (μW)	4.53	8	7	0.8	0.99	2.98	**1.5**	**2.5**
Area per channel (mm^2)	0.129	-	0.0039	0.024	0.011	0.0023 ‡	**0.022**	
Artifact insentive	DM	DM	-	DM	CM/DM	CM/DM ‡	**CM/DM**	
# multiplexed channels	1	1	20	1	1	64	**32**	
Input differential range (V_{pp})	8	100	17 †	260	10	110	**300**	
IRN per channel (μV_{rms})	3.83	1,6	5.6	1	2.6	1.66 ⋆	**1.4**	**4.8**
Signal bandwidth	5.7 kHz	-	15 kHz	500 Hz	1-500 Hz	1-1000 Hz ⋆	**0.5-200 Hz**	**0.5-3000 Hz**
NEF/PEF per channel	3.09/9.72	7.8/60.8	4.7/22.4	1.8/2.6	3.5/15.2	2.21/12.2 ⋆	**4.5/24**	**5/20**
Crosstalk (dB)	-	-	-	-	-	-92	**-85**	
CMRR (dB)	-	-	50	81 (0-60Hz)	78	76	**87**	
THD	<1%@3mV$_{pp}$	0.7%@100mV$_{pp}$	2%@17mV$_{pp}$ †	71 (SFDR)	70.1 (SFDR)	<1%@5mV$_{pp}$	**0.1%@5mV$_{pp}$**	**<1%@80mV$_{pp}$**
Dynamic Range (dB)	66	90	66-68 †	92	60 †	91	**71+26 (w/ARL)**	**83**
Channel FoM (pJ/c-step) [a]	0.139	0.309	0.401	0.025	0.052	0.013 ⋆	**0.065**	**0.036**

† Estimated value not explicitly mentioned in the reference.
⋆ For nominal recording operation, w/out CM artifact suppression.
‡ Off-chip DM artifact suppression.
△ ADC not included.
a. Channel-FoM(DR) = $P_{ch}/(2\,BW \cdot 2^{ENOB(DR)})$, where $ENOB(DR)$ = (DR(dB)- 1.76)/6.02.

6.3 Discussion

Time-division multiplexing AFEs have been explored as a new promising paradigm for the design of multi-channel neural sensing devices because of their benefits regarding area and power consumption. Nevertheless, their inherent noise folding components significantly compromises the scalability of these systems. Techniques and architectures to overcome this issue have been explored.

Charge-sampling [126, 11] and windowed integration sampling [17] have been proposed to reduce this negative effect. The basic structure in both techniques consists in a G_m-cell driving a sample-and-hold capacitor. The hold operation attenuates high frequency noise components and effectively reduces the noise equivalent bandwidth to $NEB = f_s/2$. Whilst simple, this circuit is not without drawbacks: the DC-gain and time constant of the AFE suffers from deviations due to process variations which may demand for some tuning mechanism; flicker noise, falling in the LFP/ECoG frequency band, and dc offsets are not reduced; large common-mode signals can drastically change the operation point of the G_m-cell, giving rise to distortion or even saturation; and the common-mode rejection ratio can be significantly lower than in closed-loop architectures. The two latter points can be solved by means of a passive SC arrangement before the charge-sampling stage [11, 148], but this is at the expense of increasing the noise floor of the AFE.

Table 6.2: Time-multiplexed Amplification-Filtering Stages Comparison

	CDS	CS / WIS
Architecture	Closed-loop	Open-loop
Noise filtering	$S_{CDS} \cdot sync^2$	$sync^2$
Noise folding	Yes	No
Flicker reduction	Yes	No
CM tolerance	High	Low
Clock/Process variations	Robust	Weak
Power	Medium/High	Low

In this work, a different approach based on narrow-band Correlated Double Sampling instrumentation amplifiers is proposed. The DC gain of the structure is well-defined by ratioed capacitances and it inherently exhibits low-pass filtering characteristics which effectively reduces the bandwidth of the AFE transfer function. Additionally, the technique offers high linearity, large common-mode range and is tolerant against process variation. It also attenuates DC offsets and flicker noise [149] with no need for an additional dummy channel [148] which either reduces the equivalent sampling frequency per channel or demands for larger master clock frequencies. The cut-off frequency of the amplifier, f_{IA}, can be made much lower than the sampling frequency, f_s, so that folded noise

components falling in the bandwidth of interest are attenuated [149, 150]. To lower the folded noise even further and, hence, reduce the input-referred noise of the structure, techniques such as oversampling are needed at the expense of larger power consumption compared to the charge sampling approach. Other techniques, a priori more suitable for reducing noise folding, such as chopping modulation [47, 159, 127], are difficult to implement in rapid time-multiplexing systems due to the need to remove up-modulated noise and offset components per channel with large time-constant low-pass filters [17, 126]. Table 6.2 summarizes the main differences between the presented WIS and CS techniques and the employed narrow-band CDS architecture.

CHAPTER 7

CONCLUSIONS

This thesis was divided into two main parts. The first set of chapters (from Chapters 2 to 4) presented a review of multi-channel neural recording systems. In the second part, based on this study, this thesis proposed a prototype for implantable multi-channel neural recording applications (Chapters 5 and 6).

The main contributions of this work are detailed below:

- To offer a complete review of recording techniques and architectures for high-channel-count, densely-spaced microelectrode arrays. This provides high-performance strategies to optimize the area occupation and the power consumption of the silicon-based conditioning circuitry without penalizing other conventional neural sensing microsystems considerations.
- To propose a novel study of the electrode-AFE interface where the pros and cons of embedding the input amplifiers adjacent to the electrodes are disclosed. The impact of the different noise sources at this stage has been evaluated by presenting a non-previously reported noise-crosstalk trade-off analysis.
- To analyze different techniques and architectures to overcome the problems related to large artifacts in closed-loop interfaces. A classification in differential and common-mode artifacts-aware front-ends is proposed, including a sub-taxonomy related to the suppression or not of the interference.
- To include a novel taxonomy for time-division multiplexing neural front-ends regarding the number of multiplexed stages. This addresses the

advantages and disadvantages of each architecture not only in terms of the front-end but also related to the electrode-AFE interface. Hence, a review of architectures including time-division multiplexing at the electrode interface has been provided due to their promising results in terms of area and power saving.

- To design a neural front-end capable of multiplexing 32 inputs. A new approach based on narrowband correlated double sampling has been used to reduce the noise folding effect in time-division multiplexing AFEs. The system input incorporates the selection between monopolar and bipolar recording by applying the spatial delta encoding technique, which compresses the signal range. Moreover, an artifact-aware auto-ranging algorithm has been implemented by a mixed-signal loop, including the possibility of attenuating or reconstructing the signal after the interference.

- To experimentally verify the prototype fabricated in a standard 180 nm CMOS process via *in-vitro* measurements. The circuit has shown an integrated input-referred noise in the 0.5–200 Hz band of 1.4 μV_{rms} for a spot noise of about 85 nV$\sqrt{Hz}$. The system draws 1.5 μW per channel from 1.2 V supply and obtains 71 dB + 26 dB (with artifact compression) dynamic range, without penalizing other critical specifications such as crosstalk between channels or common-mode and power supply rejection ratios.

- To prove the performance of the proposed design by measuring different pre-recorded local field potentials. Action potentials contained in the neural signal have been also captured with the circuit operating in Mode-2. The large compression provided by the spatial delta encoding technique has been evaluated along with its inherent reconstruction error.

- To test the tolerance to large interference signals by observing the *in-vitro* response of the system to different artifacts. The operation of the auto-ranging algorithm compressed the artifacts avoiding the saturation of the signal path. Artifact reconstruction and suppression at the output of the system have been also demonstrated.

7.1 Future Works

In general, it is necessary to perform *in-vivo* validation of the system. However, due to causes outside our control (and, of course, our interest), including mobility and interpersonal relationship restrictions which have resulted in limitations to access labs (furthermore if they are allocated in different institutions), it has not been possible to perform *in-vivo* validations so far. This is actually our main

priority and, as the first step after this thesis, is to take *in-vivo* measurements and to perform an in-depth characterization of the *in-vivo* results.

Once the circuit was *in-vivo* characterized, the next aim relies on integrating it in a bidirectional interface with a neural stimulator. Although the design of the stimulator is carried out in parallel by another researcher at the Institute of Microelectronics of Sevilla, there are still some design constraints from the point of view of the recording front-end that have to be met: i) the input switches of the multiplexer have to be properly designed to tolerate the large stimulation voltages without breaking; ii) the number of recording channels has to be reconfigurable to employ the same electrodes for signal acquisition and stimulation; iii) the control unit has to perform a closed-loop operation by observing the neural activity and the response of the tissue to the stimulation pulses.

Furthermore, there is still room for incremental improvement of the front-end. Firstly, the applied impedance boosting loop presented large variations which are undesirable for future designs. Herein, other approaches, for instance, to employ an auxiliary path as proposed in [95], can be studied. On the other hand, the second IA_2 was thought to be replaced by a programmable gain amplifier to palliate the degradation of the interface and to increase the longevity of the implant. Both changes have to be carried out without penalizing the current specifications of the interface.

On the other hand, this 32-channel prototype has been built as a *proof-of-concept* for a future 4096-channel neural recording system for *in-vitro* measurements. The idea behind this new circuit is to integrate 128 instances of our current design in order to scale the number of recorded channels, and, therefore, the spatial resolution of the system.

Finally, future developments in our recording device should follow the trend of increasing the number of recording channels. Although not addressed in depth during this work, one of the main problems related to these devices is the amount of raw data. Herein, increasing the number of channels considerably increases the amount of data to be processed and transmitted. This leads to a considerable increment of the power consumption in the digital part of neural recording systems, making it comparable with that of the analog part. Moreover, as these systems are intended for long-duration implants, the amount of data to be stored could be too large. New techniques for data compression and feature extraction must therefore be studied and implemented to address these problems.

APPENDIX A

NOISE ANALYSIS OF THE CDS AMPLIFIER

The method explained in [154] has been used for the noise analysis of the instrumentation amplifier in Figure 5.4(a). The analysis has covered all major noise sources in the circuit, including the thermal noise from the switch-on resistances as well as the white and flicker noise contributions of the OTA. However, only the white noise component of the OTA is herein presented as it has the largest impact on the noise spectral density of the circuit. The method is based on the calculations of (i) the continuous-time transfer functions $F_{x,p}(s)$ between the noise source and the circuit capacitor C_x during the clock phase Φ_p, $(p = 1,2)$ and (ii) the transfer functions $H_{x,p}(z)$ between the noise voltage across capacitor C_x and the circuit output on phase Φ_p. Taking into account the parameter definitions in Table A.1, where A_0 is the OTA dc gain, C_p is the parasitic capacitance at the input of the OTA and C_L is the load capacitance – the other capacitances are identified in Figures 5.4-5.5 –, functions $F_{x,p}(s)$ from the input node of the OTA to the input (C_{in}), feedback (C_{fb}), and hold (C_{az}) capacitances are given by:

$$\mathbf{F}(s) = \begin{bmatrix} F_{in,1}(s) = \frac{1}{1+\epsilon_1+s/p^{(1)}} \\ F_{fb,1}(s) = \frac{1}{1+\epsilon_1+s/p^{(1)}} \\ F_{az,1}(s) = \frac{-1+\beta_1}{\beta_1(1+\epsilon_1+s/p^{(1)})} \\ F_{in,2}(s) = \frac{1}{1+\epsilon_2+s/p^{(2)}} \\ F_{fb,2}(s) = \frac{-1+\beta_2}{\beta_2(1+\epsilon_2+s/p^{(2)})} \\ F_{az,2}(s) = \frac{-1}{\beta_2(1+\epsilon_2+s/p^{(2)})} \end{bmatrix} \tag{A.1}$$

Table A.1: Instrumentation Amplifier Parameters

Parameter	Definition
$C_{az,m}$	$C_{az}+C_m$
$C_{fb,m}$	$C_{fb}+C_m$
β_1	$C_{az,m}/(C_{in}+C_{fb}+C_{az,m}+C_p)$
β_2	$C_{fb,m}/(C_{in}+C_{fb,m}+C_p)$
$C_{eq,1}$	$(C_{az,m}(1-\beta_1)+C_L)/\beta_1$
$C_{eq,2}$	$(C_{fb,m}(1-\beta_2)+C_L+C_{az})/\beta_2$
ϵ_1	$1/(\beta_1 A_0)$
ϵ_2	$1/(\beta_2 A_0)$

where it is assumed that the frequency response of the closed-loop circuit can be modelled on each clock phase by a single pole at $p^{(q)} = g_m/C_{eq,p}$.

Similarly, the discrete-time transfer functions on phases 1 and 2 between said capacitors and the output node are given by:

$$\mathbf{H}(z) = \begin{bmatrix} H_{in,1}(z) = \frac{C_{in}(C_3 - C_1 z)}{C_3 C_4 - C_1 C_2 z} \\ H_{fb,1}(z) = \frac{C_{fb}(C_3 - C_1 z)}{C_3 C_4 - C_1 C_2 z} \\ H_{az,1}(z) = \frac{-1}{(1+\beta_1\epsilon_1)} \\ H_{in,2}(z) = \frac{C_{in}(C_4 - C_2 z)}{C_3 C_4 - C_1 C_2 z} \\ H_{fb,2}(z) = \frac{-1}{(1+\beta_2\epsilon_2)} \\ H_{az,2}(z) = -1 \end{bmatrix} \tag{A.2}$$

where

$$\begin{array}{ll} C_1 = C_{fb,m}(1+\epsilon_2) & C_3 = C_1 + C_{az} \\ C_2 = C_{az,m}(1+\epsilon_1) & C_4 = C_1 - C_{fb} \end{array} \tag{A.3}$$

Let us build the square matrices $|\mathbf{F}(s)|^2 = \mathbf{F}(s)\mathbf{F}^{\mathrm{t}}(-s)$ and $|\mathbf{H}(z)|^2 = \mathbf{H}(z)\mathbf{H}^{\mathrm{t}}(z^{-1})$, as well as the cross-spectral density matrix $\mathbf{S}(j\omega) = S_a(\omega)|\mathbf{F}(j\omega)|^2$ where $S_a(\omega)$ is the input-referred thermal noise spectral density of the OTA in Figure 5.5, approximately given by:

$$S_a(\omega) \approx \frac{16\,\eta\, V_t\, k_B\, T}{3\, I_b} \tag{A.4}$$

where I_b is the biasing current of the OTA, V_t is the thermal voltage, η is the sub-threshold slope factor, k_B is the Boltzmann constant and T is the temperature.

According to [154], the k-th replica due to sampling of the output noise power spectral density of the circuit due to the input white noise component of the OTA is given in compact form as,

$$S_k(\omega) = \frac{1}{T_s^2} \sum_{p,q=1}^{2} \mathbf{u}_p \Big(|\mathbf{H}(z)|^2 \circ \mathbf{S}(j\Omega_k) \Big) \mathbf{u}_q^{\mathrm{t}} e^{-j\Omega_k \frac{T_s(p-q)}{2}} \tag{A.5}$$

where T_s is the sampling period, $z = e^{j\omega T_s}$, $\Omega_k = \omega - 2\pi k/T_s$ and '$\circ$' denotes the element-wise Hadamard product. Vectors $\mathbf{u}_1$ and $\mathbf{u}_2$ are respectively given by $\mathbf{u}_1$ = [111000] and $\mathbf{u}_2$ = [000111]. Summing over all the replicas, the output noise spectrum of the CDS amplifier in Figure 5.4(a) is given by

$$S_{CDS}(\omega) = \sum_{k=-\infty}^{\infty} S_k(\omega) \tag{A.6}$$

Although too complex to gain direct insight, this expression provides an accurate mechanism, as demonstrated in Figure 5.9, for exploring and optimising the design space of circuit components.

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Education

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2016–2017 **Master in Microelectronics: Design and applications of micro/nanometer systems**, *IMSE-US*, Seville, Spain.

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Theses

PhD's Thesis

Title Low-Power Artifact-Aware Implantable Neural Recording Microsystems for Brain-Machine Interfaces.

Advisor Dr. Manuel Delgado Resituto.

Advisor Dr. Ángel Rodríguez Vázquez.

Master's Thesis

Title Design of a Chopper-Stabilized amplifer for neural recording applications.

Advisor Dr. Manuel Delgado Resituto.

Advisor Dr. Ángel Rodríguez Vázquez.

Bachelor's Thesis

Title About the application of Chopper technique in order to reduce flicker noise in neural recording amplifiers.

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Professional Experience

2019 **Internship**, *Back telemetry circuit design for next generation of retinal implants*, Second Sight Medical Products Inc, California, US.

2018–2021 **Undergraduate Student Research**, *Doctoral scholarship of the Spanish Ministry of Economy and Enterprise (MINECO)*, Integrated Pattern-Adaptive optical NEurostimulator with Multi-site recording Array (IPANEMA), IMSE-CNM. Seville, Spain

2016–2018 **Predoctoral Researcher**, *Scholarship in the University of Seville Researcher Foundation (FIUS)*, Study of recording and conditioning analog and mixed-signal interfaces for neural signals recording, IMSE-CNM.
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Publications

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2019 **A High TCMRR, Charge Balanced Bidirectional Front-End for Multichannel Closed-Loop Neuromodulation**, *José Luis Valtierra, Rafaella Fiorelli, Norberto Pérez-Prieto, Manuel Delgado-Restituto, Ángel Rodríguez-Vázquez*, Biomedical Circuit and Systems Conference (BioCAS), Nara, Japan.

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Courses and Programs

2020 **Artificial Vision with MATLAB**, *MATLAB*, IMSE-US, Seville, Spain.

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2018 **Innovus implementation system: blocks**, *Cadence*, Online.

2018 **IMFAHE mentor program**, *University of Seville - Harvard University*.

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2016 **Machine Learning Course**, *University of Stanford, imparted by Coursera*, Online.

Languages

Spanish	Mother tongue	
English	**Reading** Fluent	*Cambridge First Certificate Exam (B2) (2016).*
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	Oral Fluent	
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	Oral Basic	

Other Skills

Microcontroller Programming	Intermediate	*nRF, TI...*
Android Programming	Basic	*Android Studio.*
Driving Licence	B	

References available upon request.