A Simple Modulation Approach for Interfacing Three-Level Neutral-Point-Clamped **Converters** to the Grid

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Abstract

Multilevel converters are nowadays an enabling key in the integration of electric power into the **grid as they introduce less distortion and, thus, they are more compliant with the grid standards, among other benefits.** A well-known topology is the three-level Neutral-Point-Clamped (NPC) whose control requires to deal with the capacitors voltage unbalance. This paper presents a modulation approach where the injection of a common component in the modulated voltage is studied in order to achieve such voltage balance. **An optimization problem that, apart from the voltage balance, aims the lowest number of commutations and can be solved very efficiently with up to five computations of the cost function is formulated. The main advantages of the proposed modulation strategy are its simplicity and its flexibility, since it is also valid for unbalanced grid conditions and, with little added complexity, for low (and even zero) power factor conditions.** Simulation results under unbalanced grid conditions are provided in order to show its validity under this scenario. The strategy is evaluated **and compared with a space-vector-based approach in an experimental setup, yielding similar total harmonic current distortion (4.4%), a 30% reduction in the number of commutations, and better voltage balance performance for lower power factor conditions.**

Keywords: Synchronous rectifier application, neutral-point-clamped (NPC) converter, multilevel converter, grid-connected rectifier, voltage balancing, optimum zero-sequence voltage injection.

1. Introduction

Electronic power converters are nowadays the most used devices for interfacing systems that absorb or generate energy with the grid. Thanks to their capability of transforming the characteristic of the electrical energy, whether if it is ac, dc or intermittent,

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they handle the power flow to fulfill the requirements of their applications. One of the typical uses comprehends dealing with the ac nature of the grid to either inject/absorb active power to/from a dc load/source or inject/absorb reactive power into the grid. No matter the aim, the quality of the handled power for grid-connected applications is crucial [1, 2]. In such applications, multilevel converters offer several advantages compared with the basic two-level configuration: lower current distortion and smaller voltage stress for the semiconductor devices among others [3]. These features make them very appealing for medium and high power applications where the voltage boundaries of the power devices are very limiting [4]. Among the broad choices of different multilevel converter topologies, three-level diode-clamped converter—also known as Neutral-Point-Clamped converter (NPC)—has been widely accepted in the industry and many applications have been developed for it [5–7]. However, the use of three-level NPC converters gives rise to a new control problem with respect to the two-level case: the dc-link capacitors voltage balance. This is an inherent feature in multilevel converters as more capacitors appear when the number of levels increases and their voltage might not remain the same under normal operating conditions. Therefore, it is crucial to consider how this unbalance can be compensated and to design a strategy to achieve the capacitors voltage equalisation.

Considering the three-level NPC topology, the unbalance issue appears due to uneven currents that go through each capacitor, i.e. current entering/exiting the neutral point (NP) [5]. Avoiding the current going through the NP will, however, neglect the benefits of the three-level converter. That is why plenty of research have been carried out as the solution for this problem is not unique. A common approach is to separate the control system into two stages: the power flow control and the modulation. The first one is similar in multilevel and two-level topologies and defines some reference signals for the second stage such that the power flow is handled as desired. The second stage is in charge of commanding the switching devices in order to implement the previous control signals into the system, thus determining which capacitors are used. In this stage, there are remaining degrees of freedom that can be used for the capacitors voltage balance objective.

In a grid-connected power converter, the modulation can be carrier-based pulse width modulation (CBPWM) [8] or space-vector pulse width modulation (SVPWM) [9], among others [10, 11]. Carrier-based approaches use one or several carrier signals to modulate the desired output signal of smaller frequency. The output signals to modulate are sampled at an specific rate—referred as switching frequency (f_{sw})—, and these samples are compared with the carrier signals—usually sawtooth or triangular shaped—whose value goes along its full range every period of f_{sw}. Thus, the switching signals change in the intersections of these samples and the carrier. In this kind of modulation for three-level, three-wire grid-connected converters, there exists a common component called zero-sequence that can be added/subtracted to the three output signal samples simultaneously without affecting the modulated phase-to-phase voltage but allowing to modify the dc-link points that are connected. This fact is specially interesting for controlling the capacitors that are charged/discharged [12]. Alternatively, SVPWM generally uses the nearest three-vector (NTV) strategy [7, 13] or the nearest three-virtual-vector (NTV^2) one [14] to achieve modulation. The main idea is to consider simultaneously the output signals of the three phases by using several concatenated switching vectors, although, there exist redundant switching vectors that provide the same output voltage

value but they use different levels. Therefore, the exploitation of this degree of freedom also makes possible to modify the connected points [6]. In summary, in order to deal with the modulation and the capacitors voltage balancing, CBPWM uses carriers and the zero-sequence component, while SVPWM uses concatenated switching vectors, including redundant ones [15]. In spite of being different techniques, several works in the literature have found equivalences between the zero-sequence injection and the redundant switching vectors use [16].

In early CBPWM approaches, the zero-sequence component was computed as a third harmonic signal that, in summary, entails the injection of a current into the NP that correct the unbalance [17]. This approach, however, requires to know the phase of the grid in addition to costly trigonometric computations. Nowadays, several approaches exist that considerably reduce the computational burden, solve the balancing issue and mitigate the low-frequency voltage oscillations of the NP [12, 16, 18–22]. Paper [20] summarizes the different kind of zero-sequence voltage injection control into: 1) Constant injection; 2) Constant charging injection; and 3) Maximum charging injection. Reference [19] presents two approaches based on the zero-sequence voltage injection, which exhibit their simplicity in terms of computational burden compared with other existing methods at the expense of increasing the number of commutations. From the NP current perspective, in [22], an analysis of the zero-sequence computation is made in order to obtain the relationship between it and the neutral current. In this way, a precise algorithm is proposed that computes the exact value of the zero-sequence to achieve the desired neutral current. However, such accuracy may not be necessary for a real application as the ripple at steady state that would result from not doing so could be negligible. Later, in [12], an analysis of the previous paper is developed resulting in a simpler flowchart with less computation burden. In [23], the equivalences among several neutral point current control approaches that achieve balancing with CBPWM and SVPWM are presented. However, none of the approaches presented in [12, 19, 22, 23] aims to reduce as much as possible the number of commutations at the same time that the voltage balance is achieved.

There exists a controllability issue in the capacitors voltage balancing with zero-sequence injection when the operating conditions have a power factor different from unity. Depending on this value and the modulation index, the zero-sequence degree of freedom may not be enough to achieve voltage balancing at all time [18]. In this regard, [18] analyses the zero-sequence injection with an additional carrier in CBPWM such that this issue is overcome. The additional carrier introduces the use of another level within the switching period, which increases the total number of commutations.

Regarding SVPWM, firstly, it is necessary to locate the voltage vector within the three-level Space Vector hexagon, i.e. the sector where it is located, in order to know which switching vectors, among the 27 available for NPC converters, should be used to modulate it. Then, these switching vectors are sequenced and theirs duty ratios are computed. The switching vector selection and sequencing, however, is not unique and plenty of criteria can be used [9, 14, 15, 24, 25]. Indeed, this is one of the advantages of SV-based approaches as many degrees of freedom are exhibited, although it is more complex to implement compared with CBPWM approaches [26] as several steps have to be taken into account: sector location, vectors selection, duty ratios computation,

vectors sequencing and hardware implementation. Paper [9] presents a straightforward application of SVPWM to three-level NPC voltage and current inverters where these tasks are achieved. This application does not consider capacitors voltage balancing, though. In NPC converters, the switching vectors are classified as large, medium or short. The first ones do not create unbalance; the second ones inject one phase current into the NP; while the third ones come in pairs that produce the same effect on the system power flow control but inject the opposite current into the NP. Therefore, to achieve capacitors voltage balancing and without changing the switching vector positions, the redundant switching vectors can be used. In this way, [15] proposes a SVPWM with balancing capabilities by combining the medium vectors—that creates unbalances—with the redundant vectors. Alternatively, [25] presents a similar approach but aiming a reduction in the number of commutation. There exists a modification of SVPWM known as virtual space vector (VSV) [14]. It basically creates inherent switching vectors in the hexagon by combining fixed duty ratios of surrounding switching vectors. Thus, paper [24] modifies the VSV in order to achieve balancing capabilities by considering the redundant switching vectors in the creation of switching vectors. This approach will be referred as mVSV in this paper.

As it was mentioned for CBPWM approaches, there exists an issue in the balancing when low power factor operating conditions are given. Using only the redundant switching vector degree of freedom to achieve balancing might be not enough depending on the modulation index and the power factor value [25]. Thus, none of the cited SVPWM approaches [9, 14, 15, 24, 25] presents an straight solution for this issue.

Comparing SVPWM with CBPWM, carrier-based approaches are usually much easier to implement than those based on Space-Vector-Modulation (SVM). That is why in [16] an analysis of the SVPWM approach is presented in order to obtain a method based on CBPWM that provides the same results. Thus, an algorithm based on several checks and the knowledge of the sector where the voltage vector is located within the space vector hexagon is proposed such that the zero-sequence component is determined.

In this paper, a CBPWM approach is considered where the zero-sequence determination is expressed as an optimization problem based on the minimization of a piecewise-linear function of one variable. In this way, the derivation of the zero-sequence computation algorithm is simpler and easier to follow than the previous approaches. In contrast to [12, 14, 15, 19, 22–24], the minimum amount of commutations is achieved by keeping one phase at one level while the other two commute between two adjacent levels each. For this, it suffices to evaluate the proposed cost function just in the cases when one phase stays at one level and choose the minimum of them. Therefore, a simple optimal CBPWM approach, which has led to an international patent [27], that reduces the commutations and actively solves the unbalance is presented along with its justification.

Regarding unbalanced grid conditions, the proposed strategy does not rely on any balanced-grid-voltage assumption. Therefore, the strategy may be suitable for this conditions keeping its simplicity compared with other CBPWM approaches [28].

This paper also considers an enhancement of the base algorithm to improve the balancing capabilities. This is considered for those operation points where using the zero-sequence injection with one phase fixed at one level during the sampling period and the other two phases at two adjacent levels each is not enough to achieve balancing at all time. Thus, one phase is allowed to use the three levels while the other two follow

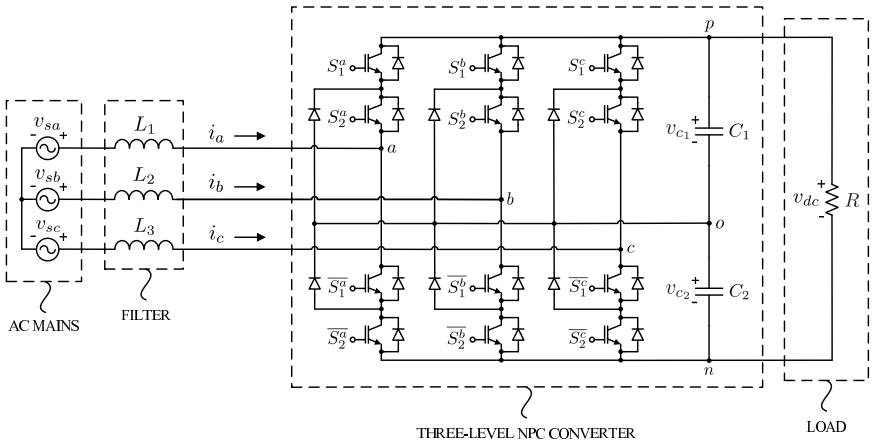

Figure 1. Schematic diagram of the three-phase three-level NPC rectifier.

the same principle than the base algorithm. This modification requires to compute a new expression for the cost function that still keeps the property of being piece-wise linear. In contrast to [18], no additional carrier is required, and the enhancement is only applied until the capacitors voltage difference is small enough, reducing the number of commutations at steady-state.

On the whole, the proposed method is easier to follow and simpler to implement than the SVM-based approaches [9, 14, 15, 24, 25] as no switching vector sequencing and large duty computations are required. The zero-sequence value and the duty ratios, for both the proposed algorithm and its enhancement, can be computed straightforwardly with no added difficulty in comparison with other CBPWM approaches [16, 18, 28], at the same time that both look for the lowest amount of commutations while achieving capacitors voltage balancing. Besides, simulation results show its capacitors voltage balancing validity under unbalanced grid voltages scenarios, due to its inherent lack of assumption of balanced grid voltages. Furthermore, the enhancement seeks covering those operation points with power factor lower than 1, where, at some instants, the base algorithm fails to achieve capacitors voltage balancing. The results are further validated by experiments under different operating conditions.

The outline of the paper is as follows: Section 2 presents the converter dynamical model along with its system variables and components, and the required controllers corresponding to the stage previous to the modulation; Section 3 introduces the modulation stage where this paper focuses on and where the main contribution is presented, in addition to the advantages with respect to other methods; besides, an enhancement is introduced in order to improve the voltage balancing capabilities under lower power factor operating conditions; Section 4 depicts the experimental results and comparisons with mVSV [24]; and Section 5 draws some final conclusions.

2. Model and Control of the System

As it has been said before, this paper focuses on grid-connected three-phase, three-level NPC converters working as rectifier with a resistive load in the dc side (Fig. 1). **The system should handle the active power to match the one absorbed by the load such that the dc-side voltage is equal to its reference, which is specified by the user. The system should also track the specified reactive power according to the power factor conditions required by the application. With reference to Fig. 1,** points $\{a, b, c\}$ are the outputs of the converter whose voltage levels are set by switching signals $\{S_1^i, S_2^i\}$ for $i = \{a, b, c\}$. The grid voltages are denoted by v_{si}, for $i = \{a, b, c\}$, while phase currents are i_i. Inductive filters are considered $\{L_1, L_2, L_3\}$ whose inductances are assumed to have the same value L. Two capacitors constitute the dc-link side $\{C_1, C_2\}$ with the same capacitance value C and whose voltages are expressed by variables $\{v_{c1}, v_{c2}\}$. To express the unbalance, variable v_d is defined as $v_{c1} - v_{c2}$. The three connection points of the dc-link are referred to as $\{p, o, n\}$ and the resistive load R is connected in parallel to it. In this way, dc-link voltage v_{dc} is equal to $v_{c1} + v_{c2}$.

Based on [29], a model for this converter in $\alpha\beta\gamma$ coordinates—**obtained by transforming the** *abc* **variables using the power-invariant Clarke transformation**—is obtained. An averaged model over a switching period is considered by using duty ratios d_{kj} for $k = \{\alpha, \beta, \gamma\}$ and level $j = \{p, o, n\}$—i.e. this duty ratios express the amount of time in a switching period that output of component k is connected to level j. In this way,

$$L\frac{di_\alpha}{dt} = v_{s\alpha} - (d_{\alpha p} - d_{\alpha n})\frac{v_{dc}}{2} - (d_{\alpha p} + d_{\alpha n})\frac{v_d}{2} \tag{1}$$

$$L\frac{di_\beta}{dt} = v_{s\beta} - (d_{\beta p} - d_{\beta n})\frac{v_{dc}}{2} - (d_{\beta p} + d_{\beta n})\frac{v_d}{2} \tag{2}$$

$$C\frac{dv_{dc}}{dt} = (d_{\alpha p} - d_{\alpha n})i_\alpha + (d_{\beta p} - d_{\beta n})i_\beta - 2\frac{v_{dc}}{R} \tag{3}$$

$$C\frac{dv_d}{dt} = (d_{\alpha p} + d_{\alpha n})i_\alpha + (d_{\beta p} + d_{\beta n})i_\beta. \tag{4}$$

The objective in the following sections will be to **present** a control algorithm which provides the values of d_{kj} for $k = \{\alpha, \beta, \gamma\}$ as a function of the measured variables v_{si}, i_i, v_{c1} and v_{c2}. Notice that d_{ij} in *abc* can be computed directly from d_{kj} by applying the inverse power-invariant Clarke transformation. Notice also that duty ratios of component γ do not appear in (1)–(4), and therefore their values can be considered as degrees of freedom that can be used for other control objectives. Similarly, duty ratios d_{ko} do not appear in the model but they can be computed from the rest of duty ratios in *abc* frame according to the constraints

$$\sum_{j=\{p,o,n\}} d_{ij} = 1, \quad d_{ij} \in [0, 1]; \quad i = \{a, b, c\}. \tag{5}$$

To introduce the controller design, and inspired by (1)–(2), three control variables

are defined

$$u_\alpha = d_{\alpha p} - d_{\alpha n} \tag{6}$$
$$u_\beta = d_{\beta p} - d_{\beta n} \tag{7}$$
$$u_\gamma = d_{\gamma p} - d_{\gamma n}, \tag{8}$$

where u_γ is directly related to the homopolar component of the d_{ij} variables for $i = \{a, b, c\}$. By introducing these variables into the current dynamics (1)–(2) and assuming that variable v_d is small enough to be neglected, a simplified model is obtained

$$L\frac{di_\alpha}{dt} = v_{s\alpha} - u_\alpha \frac{v_{dc}}{2} \tag{9}$$
$$L\frac{di_\beta}{dt} = v_{s\beta} - u_\beta \frac{v_{dc}}{2}. \tag{10}$$

Notice that these equations recall the current dynamics of a simple two-level converter with u_α and u_β as control inputs. Moreover, variable u_γ does not appear in the current dynamics and therefore, it is left as a degree of freedom.

At this point, the converter requires a control algorithm to handle the power taking into account the model dynamics. In this regard, two cascaded controllers are usually used [30]: an outer loop to compute the power required p^r to keep v_{dc} towards its reference v_{dc}^r; and an inner faster loop in charge to drive the active and reactive powers p, q close to the previous reference and the desired reactive power q^r, respectively. In spite of the fact that these stages are not the aim of this paper, the algorithms used in the simulation and experiments are presented here for the sake of completeness.

2.1. Dc-link Voltage Regulation Loop

The total capacitors voltage of the dc-link (v_{dc}) should reach its reference (v_{dc}^r) at steady state. To achieve so, a PI controller is used to compute the required amount of power (p^r) **[30],**

$$p^r = k_p^{dc}({v_{dc}^r}^2 - v_{dc}^2) + k_i^{dc}\int_0^t ({v_{dc}^r}^2 - v_{dc}^2)d\tau, \tag{11}$$

where $\{k_p^{dc}, k_i^{dc}\}$ are control parameters to be tuned, **which can be done using any approach existing on literature [30, 31].** After this, the references for the current control $\{i_\alpha^r, i_\beta^r\}$ are obtained by applying the instantaneous power theory to $\{p^r, q^r\}$, where q^r is the user-defined reactive power reference.

2.2. Current Controller

Once $\{i_\alpha^r, i_\beta^r\}$ are computed, a current controller stage is implemented such as to reduce the current tracking error $\{\widetilde{i_\alpha}, \widetilde{i_\beta}\} = \{i_\alpha^r - i_\alpha, i_\beta^r - i_\beta\}$ as much as possible. In

this way, **considering** (9)-(10)**,** a non-ideal proportional-resonant controller [32] tuned at the grid frequency is implemented.

$$G_{PR_\omega}(s) = k_p + \frac{2k_r\omega_c s}{s^2 + 2\omega_c s + \omega^2} \tag{12}$$

$$\begin{bmatrix} u_\alpha \\ u_\beta \end{bmatrix} = \frac{2}{v_{dc}} \left(-G_{PR_{\omega_g}} \begin{bmatrix} \widetilde{i_\alpha} \\ \widetilde{i_\beta} \end{bmatrix} + \begin{bmatrix} v_{s\alpha} \\ v_{s\beta} \end{bmatrix} \right), \tag{13}$$

where $\{k_p, k_r\}$ are, respectively, the proportional and resonant control gains; ω_c is the cut-off frequency of the low-pass filter implemented into the resonant part; ω is the resonant frequency—in this case, tuned at the grid one ($\omega_g = 2\pi f_{\text{grid}}$)—; and $\{v_{s\alpha}, v_{s\beta}\}$ are the grid voltages in the $\alpha\beta\gamma$ reference frame. **Bear in mind that this paper does not focus on this stage and that any other existing controller in the literature (e.g. [21, 33]) could be used instead as long as it provides the modulator with the values of u_α and u_β.**

3. Modulation Stage with Voltage Balance Capabilities

This section **presents the main contributions of this paper by providing** an algorithm that computes the duty ratios d_{ij} such that the results of the current controller, namely $\{u_\alpha, u_\beta\}$, are implemented **optimizing the number of commutations at the same time that the capacitors voltage are balanced. In the following subsections the base algorithm, its evaluation under unbalanced grid conditions and an enhancement to improve its balancing capabilites are shown.**

3.1. Zero-sequence Component Computation

As it has been said in the previous section, the output of the current controller is the value of u_α and u_β. In order to convert them to *abc* coordinates there is a remaining degree of freedom, namely the homopolar component u_γ. For simplicity, in the following, variable x is introduced as $x \doteq u_\gamma/\sqrt{3}$. In this way,

$$\begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & 0 & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & \frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \\ -\frac{1}{2} & -\frac{\sqrt{3}}{2} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} u_\alpha \\ u_\beta \\ u_\gamma \end{bmatrix} = \begin{bmatrix} \sqrt{\frac{2}{3}}u_\alpha + x \\ -\sqrt{\frac{1}{6}}u_\alpha + \frac{1}{\sqrt{2}}u_\beta + x \\ -\sqrt{\frac{1}{6}}u_\alpha - \frac{1}{\sqrt{2}}u_\beta + x \end{bmatrix} \doteq \begin{bmatrix} \eta_a + x \\ \eta_b + x \\ \eta_c + x \end{bmatrix}, \tag{14}$$

where variables η_a, η_b, η_c have been defined. These variables are known once u_α and u_β are computed by the current controller. Notice that the maximum and minimum values for x are imposed by the constraint $u_i \in [-1, 1]$ for $i = \{a, b, c\}$—**obtained from** (5) **and** $u_i = d_{ip} - d_{in}$—in conjunction with (14) resulting in $x \in [-1 - \min(\eta_a, \eta_b, \eta_c), 1 - \max(\eta_a, \eta_b, \eta_c)] \doteq [x_{\min}, x_{\max}]$. Moreover, it can be seen that the feasibility condition $x_{\min} \leq x_{\max}$ is equivalent to the requirement that vector (u_α, u_β) is inside the SVM hexagon.

Equation (14) can be interpreted with the help of Fig. 2 [34]. To put things in context, in the left graph of this figure a reference vector is shown in the usual space

vector hexagon. This reference vector corresponds to particular values of u_α, u_β that, with the approach used in this paper, are given by (13). This reference vector moves as time moves on. In the same way, variables η_a, η_b, η_c implicitly defined in (14) depend on time. In steady state, they describe a sinusoidal wave as shown in the central graph of Fig. 2 where $t = t_1$ corresponds to the same instant than the reference vector shown in the left graph. The right graph corresponds to this time instant. In it, the actual discrete levels for the three-level converter are represented by the values $\{-1, 0, 1\}$ and the leaning lines depict the values of $u_a(x), u_b(x), u_c(x)$ as a function of the value of x to be chosen. The dashed vertical lines represent the boundaries $x_{\min} \leq x \leq x_{\max}$. Notice also that for $x = 0$, $u_i = \eta_i$. As time advances, these three lines move according to the movement of η_i in the central graph. One advantage of the approach can be spotted on the right graph where the degree of freedom associated with the homopolar component u_γ (or, analogously x) is explicit, while it is not so evident in the space vector representation of the left graph. The black dots in the right graph will have an important relevance below. An animation of the time evolution of the three lines of the right graph of Fig. 2 and its relationship with η_a, η_b and η_c and the space vector hexagon can be observed in the following link: `http://grupo.us.es/tep102/lines_animation.mp4`.

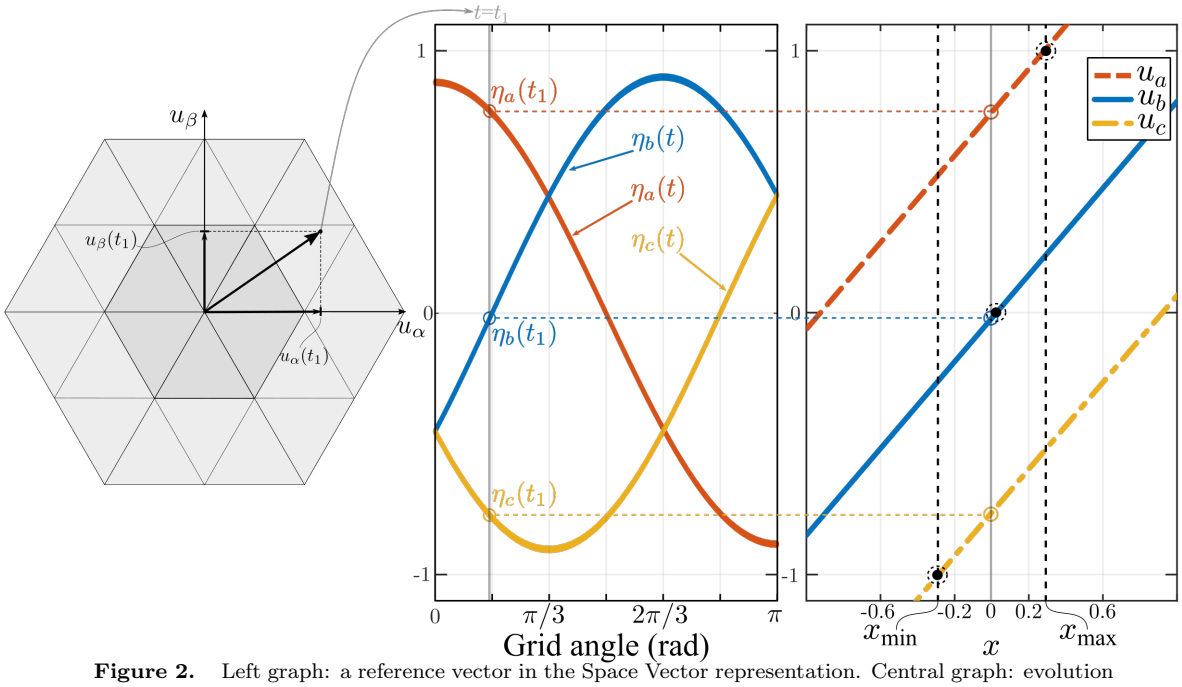

Figure 2. Left graph: a reference vector in the Space Vector representation. Central graph: evolution of $\eta_i(t), i = a, b, c$; the vertical line corresponds to the same time instant $t = t_1$ than the left graph. Right graph: Representation of equation (14) at $t = t_1$.

Back to the capacitors voltage unbalance dynamic formulation (4), it can also be transformed to *abc*, resulting in

$$C\frac{dv_d}{dt} = i_a(d_{ap} + d_{an}) + i_b(d_{bp} + d_{bn}) + i_c(d_{cp} + d_{cn})\,. \tag{15}$$

Therefore, the capacitors voltage balance can be addressed as an optimisation problem. For this, based on (15) the following cost function is defined

$$f_{\text{cost}} \doteq \text{sign}(v_d) C \frac{dv_d}{dt} = \text{sign}(v_d) \left(i_a(d_{ap} + d_{an}) + i_b(d_{bp} + d_{bn}) + i_c(d_{cp} + d_{cn}) \right), \quad (16)$$

which **reflects straightforwardly the capacitors voltage balance objective—making sign**$(v_d)\frac{dv_d}{dt} < 0$ **will make** v_d **go towards 0. The lower its value, the faster the capacitors voltage equalization.**

Initially, in order to reduce the number of commutations, it can be imposed the use of the nearest two levels modulation (NLM) to modulate the output. This is equivalent to make one of the duty ratios $\{d_{ip}, d_{in}\}$ of each phase equal to zero which results in the following constraint for the duty ratios

$$\text{NLM:} \begin{cases} d_{in} = 0 & \text{if} \quad u_i \geq 0 \\ d_{ip} = 0 & \text{if} \quad u_i < 0 \end{cases} \qquad i = \{a, b, c\}. \quad (17)$$

Also notice that $u_i = d_{ip} - d_{in}$ for $i = \{a, b, c\}$ is obtained from (6)–(8) in abc frame. Therefore, under (17), f_{cost} can be expressed as

$$f_{\text{cost}} = \text{sign}(v_d) \left(i_a |u_a| + i_b |u_b| + i_c |u_c| \right). \quad (18)$$

Considering that, according to (14), u_a, u_b and u_c depend on x, the following optimization problem is defined:

$$\min_{x \in [x_{\min}, x_{\max}]} f_{\text{cost}}(x) = \text{sign}(v_d)(i_a |u_a(x)| + i_b |u_b(x)| + i_c |u_c(x)|). \quad (19)$$

Under this formulation, $\{i_a, i_b, i_c\}$ and v_d are the state variables measured in the system every sampling time, $x_{\min}$ and $x_{\max}$ can be computed as functions of $\{\eta_a, \eta_b, \eta_c\}$—obtained from the current control—and $u_i(x)$ are determined by (14) for each value of x. Therefore, function f_{cost} depends only on variable x, resulting in a piecewise-linear function of one variable. Thus, the minimum must lie in the boundaries of the linear intervals additionally to the boundaries $\{x_{\min}, x_{\max}\}$. It can be easily seen that the boundaries of the linear intervals are for $x = \{-\eta_a, -\eta_b, -\eta_c\}$. Therefore, the set of potential optimal values for x is $\mathcal{X} = \{-\eta_a, -\eta_b, -\eta_c, x_{\max}, x_{\min}\}$, which are the represented black dots in Fig. 2. Notice that points $\{-\eta_a, -\eta_b, -\eta_c\}$ should be considered only if, at the considered time instant, they lie inside interval $[x_{\min}, x_{\max}]$ otherwise they are not feasible and should be avoided. In this regard, notice that the larger the modulation index—**which would yield larger amplitudes of** $\{\eta_a, \eta_b, \eta_c\}$— , the shorter the interval $[x_{min}, x_{max}]$ and the fewer points that lie inside the boundaries as it can be seen in Fig. 3, depicted as an example. In summary, the optimisation problem can be solved by evaluating the cost function f_{cost} at the points given in Table 1.

Consequently, the selection of the smallest value of f_{cost} leads to the optimum value of x. **Thus, the only information required for computing the zero-sequence component are the variables** η_a, η_b, η_c**, the sign of** v_d **and the phase currents, in**

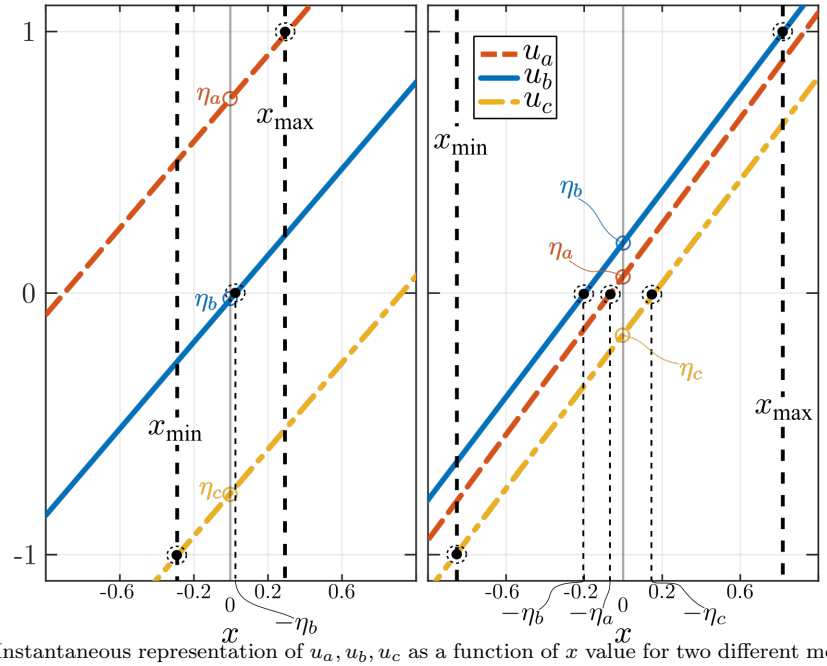

Figure 3. Instantaneous representation of u_a, u_b, u_c as a function of x value for two different modulation indexes $m = \{1.1, 0.25\}$ with $\{u_\alpha, u_\beta\}$ being $\{0.93, 0.59\}$ (left) and $\{0.19, 0.16\}$ (right) respectively.

Table 1. Optimal point candidates

x **value**	$f_{\mathbf{cost}}(x)\mathbf{sign}(v_d)$	**Condition**
$-\eta_a$	$i_b \lvert\eta_b - \eta_a\rvert + i_c \lvert\eta_c - \eta_a\rvert$	$x_{\min} \leq -\eta_a \leq x_{\max}$
$-\eta_b$	$i_a \lvert\eta_a - \eta_b\rvert + i_c \lvert\eta_c - \eta_b\rvert$	$x_{\min} \leq -\eta_b \leq x_{\max}$
$-\eta_c$	$i_a \lvert\eta_a - \eta_c\rvert + i_b \lvert\eta_b - \eta_c\rvert$	$x_{\min} \leq -\eta_c \leq x_{\max}$
$x_{\min}$	$i_a \lvert\eta_a + x_{\min}\rvert + i_b \lvert\eta_b + x_{\min}\rvert + i_c \lvert\eta_c + x_{\min}\rvert$	$--$
$x_{\max}$	$i_a \lvert\eta_a + x_{\max}\rvert + i_b \lvert\eta_b + x_{\max}\rvert + i_c \lvert\eta_c + x_{\max}\rvert$	$--$

contrast to other CBPWM approaches like [16], where it is also required to know the sector within the voltage vector is located. Denoting this optimum as x^* and introducing it into (14), the values of u_i, and therefore $\{d_{ip}, d_{in}\}$, for $i = \{a, b, c\}$ are obtained. Afterwards, the computation of d_{io} for $i = \{a, b, c\}$ is straightforward from (5).

The overall scheme of the proposed controllers is depicted in Fig. 4. **Notice that variables $\{i_a, i_b, i_c, v_{c1}, v_{c2}, v_{sa}, v_{sb}, v_{sc}\}$ are measured with sensors and, therefore, the overall system is in closed loop**. The main result of this paper is represented as the optimization problem block that has been formulated by (19). Notice that the computational burden is quite small, since it suffices to compute **up to five expressions shown in Table 1 depending on the fulfillment of the stated conditions,** and to select the smallest value of them.

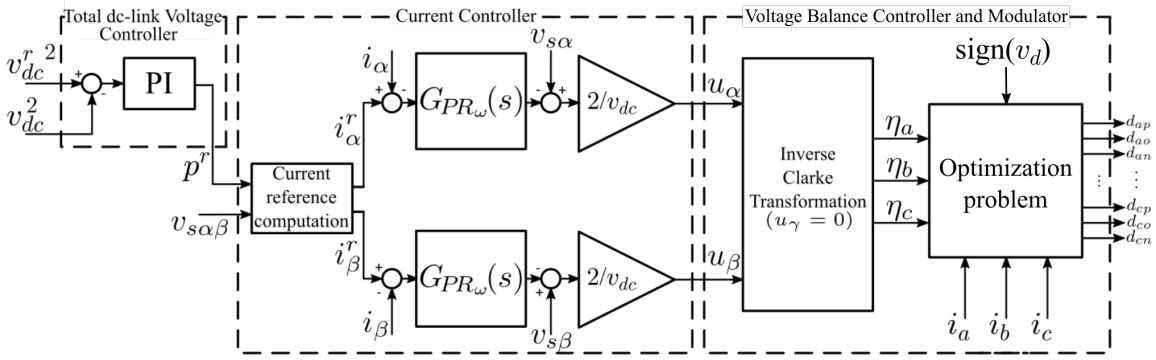

Figure 4. Complete schematic block diagram of the controllers.

3.2. Behaviour under Unbalanced Grid Conditions

Considering a distribution network, unbalanced grid condition may be caused, among others, by the presence of nonlinear loads, grid faults or unequal power phase demand at some point of the grid network. As a result, a variation in the amplitude of the positive sequence and the presence of negative sequence might be present in the three-phase grid voltages. This condition alters the values of $\{\eta_a, \eta_b, \eta_c\}$ and $\{i_a, i_b, i_c\}$ as it is deeply explained in [28], where both set of variables are modelled in terms of positive, negative and zero sequence grid components. The optimisation problem formulated in (19) is still valid with these modified values, as it does not rely on any balanced grid condition assumption, except for $i_a + i_b + i_c = 0$ which is inherent in a three-phase system by the Kirchhoff laws. This approach, in comparison with [28], does not require complex computations for any condition of the grid. **In the worst-case scenario of extreme unbalances, such as grid-fault in one phase, the whole system would not work as it is an issue that has to be tackled from the power flow control perspective, which is not the aim of this paper. Nevertheless, the unbalances in a distribution network are not usually of such magnitude as the EN 50160 standard [35] does not allow a positive magnitude deviation greater than a 10%, nor a negative sequence presence greater than 2% of the positive one [1, 36].**

Simulations have been carried out to prove the effectiveness of this approach under highly unbalanced conditions. In this way, Fig. 5 depicts the evolution of the capacitors voltage both when the grid voltages are unbalanced and when they are not. This distortion is simulated with variables $v_{sa} = 160\sqrt{2}\sin(\omega_g t) + 30\sin(-\omega_g t)$, $v_{sb} = 230\sqrt{2}\sin(\omega_g t - 2\pi/3) + 30\sin(-\omega_g t)$ and $v_{sc} = 272\sqrt{2}\sin(\omega_g t + 2\pi/3) + 30\sin(-\omega_g t)$. Consequently, positive, negative and zero sequence are present in the grid components. **Notice that these conditions are much more unbalanced of that the standard admits [35].**

It can be seen in Fig. 5 how the balancing capabilities of the system are not altered when unbalanced grid conditions are considered. This is due to the active balancing property of the proposed approach, where the phase currents and capacitors voltage are taken into account when computing the duty ratios in order to obtain the optimal

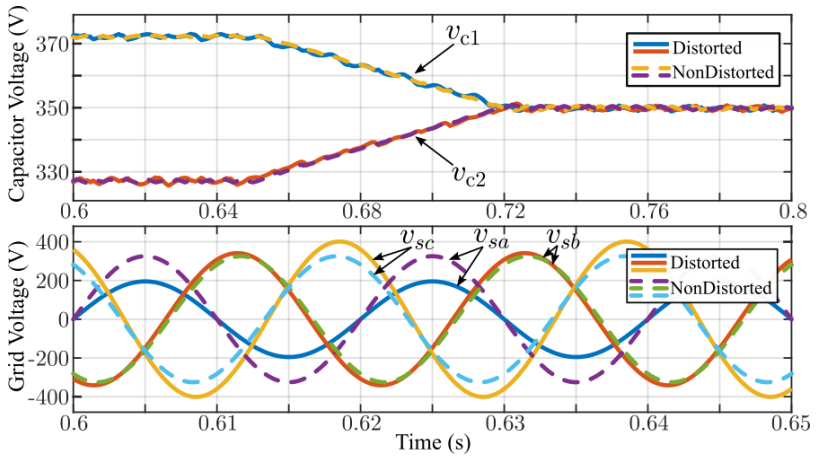

Figure 5. Capacitors voltage evolution (top) when considering highly unbalanced grid conditions (bottom). **The time axis are different due to the different time scales of these variables.**

balancing condition. **In this way, the algorithm does not require the grid voltages to be perfectly balanced, and its voltage balance capabilities are not altered by the potential unbalance.**

3.3. Enhancement to Cover Different Operating Conditions

As it is stated in [18], the degree of freedom associated with the injection of zero-sequence component for CBPWM approaches with one carrier may not be enough to achieve voltage balance at all time. Indeed, the larger the modulation index and the lower the power factor, the more difficult this target. This means that, at some instants, the balance objective $v_d \cdot \frac{dv_d}{dt} < 0$—which is equivalent to $f_{\mathbf{cost}} < 0$ in (19)—is not fulfilled and, therefore, the error signal increases. Numerical examples can be given with power factor different from unity for which there are time instants where none of the five considered points result in a negative value of $f_{\text{cost}}(x^*)$. Although, it does not entail that v_d is unbounded. In fact, whenever the integral value of $f_{\text{cost}}(x^*)$ over a grid period results in a negative number, the variable v_d will get closer to zero at the end of the period but not necessarily in a monotone way. This yields an oscillation and a reduction in the decreasing speed of v_d. **In order to avoid this kind of behaviour, [18] proposes the use of an additional carrier such than an additional level is used. Alternatively, this paper introduces an enhancement of the base algorithm, which does not require additional carrier, for the cases when the condition $f_{\mathbf{cost}}(x^*) < 0$ is not achievable.**

To achieve this, the constraints (17) are suppressed for one of the phases. Consequently, one phase will have both d_{ip} and d_{in} different from zero. This implies an increment in the number of commutations (and, therefore, more losses) but, with this new possibility, it will be easier to achieve a negative value of f_{cost}. The determination of the duty ratios from u_i, $i = \{a, b, c\}$ is now not unique given that $u_i = d_{ip} - d_{in}$. For

this, the value of the intermediate duty ratio d_{io} is fixed to a positive value and denoted as ϵ in the following. The advantage of this approach can be seen from (15): the phase whose constraints are suppressed would contribute to (15) with $(d_{jp}+d_{jn})i_j = (1-\epsilon)i_j$. Consequently, a small value of ϵ should be selected at the same time that the phase with the more appropriate current is chosen. In summary, the new constraints for the considered phase are

$$\begin{array}{c} 1 = d_{ip} + \epsilon + d_{in} \\ u_i = d_{ip} - d_{in} \end{array} \rightarrow \begin{cases} d_{ip} = (u_i + 1 - \epsilon)/2 \\ d_{in} = (-u_i + 1 - \epsilon)/2 \end{cases} . \tag{20}$$

In this way, one of the phases implements the three levels while the other ones apply the previous algorithm.

Therefore, the same optimization problem is reformulated as

$$\min_{x \in [x_{\min}, x_{\max}]} f_{\text{cost}}(x) = \text{sign}(v_d) \left(i_j(1-\epsilon) + i_{i_1} |u_{i_1}(x)| + i_{i_2} |u_{i_2}(x)| \right), \tag{21}$$

where j is the phase that switches among the three levels while i_1 and i_2 are the other two. Notice at this point that, such as to achieve the smallest possible value of the cost function, it has to be evaluated again with this addition at the feasible values of x in Table 1, therefore a different x^* could be obtained. As a consequence, up to 15 new points have to be evaluated: three phases with the inclusion of the third level, five times each for $x = \{x_{\min}, x_{\max}, -\eta_a, -\eta_b, -\eta_c\}$ as it is shown in Table 2. In this way, the number of evaluations of f_{cost} would change to **a maximum of** 15 in the case that none of the points in Table 1 achieve $f_{\text{cost}}(x^*) < 0$.

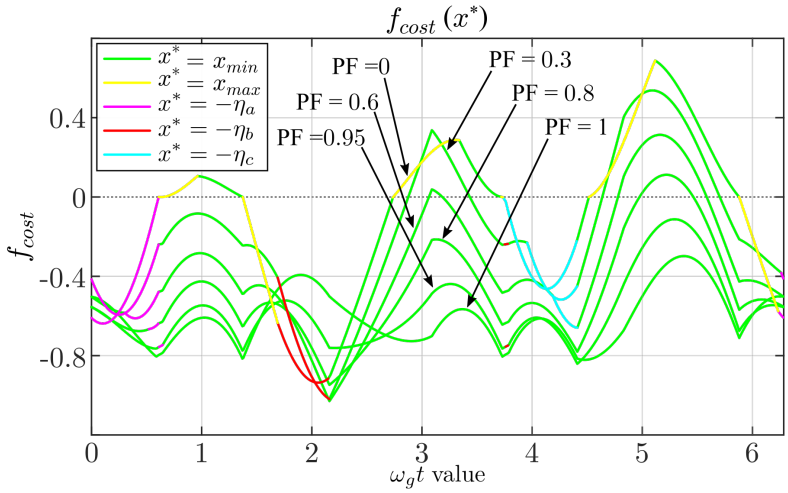

Figure 6. Value of $f_{\text{cost}}(x^*)$ assuming constant sign of v_d without the enhancement for different power factors.

The minimum value of f_{cost} with no enhancement is depicted in Fig. 6 for different power factor values along one grid fundamental period and the value of x^* it entails.

Table 2. Extended optimal points candidates

Phase j	x value	$f_{\mathbf{cost}}(x)\mathbf{sign}(v_d)$	Condition
a	$x_{\min}$	$i_a(1-\epsilon)+i_b\lvert\eta_b+x_{\min}\rvert+i_c\lvert\eta_c+x_{\min}\rvert$	$\lvert\eta_a+x_{\min}\rvert\leq 1-\epsilon$
	$x_{\max}$	$i_a(1-\epsilon)+i_b\lvert\eta_b+x_{\max}\rvert+i_c\lvert\eta_c+x_{\max}\rvert$	$\lvert\eta_a+x_{\max}\rvert\leq 1-\epsilon$
	$-\eta_a$	$i_a(1-\epsilon)+i_b\lvert\eta_b-\eta_a\rvert+i_c\lvert\eta_c-\eta_a\rvert$	$x_{\min}\leq-\eta_a\leq x_{\max}$ & $\cancel{\lvert\eta_a-\eta_a\rvert}\leq 1-\epsilon$
	$-\eta_b$	$i_a(1-\epsilon)+i_b\cancel{\lvert\eta_b-\eta_b\rvert}+i_c\lvert\eta_c-\eta_b\rvert$	$x_{\min}\leq-\eta_b\leq x_{\max}$ & $\lvert\eta_a-\eta_b\rvert\leq 1-\epsilon$
	$-\eta_c$	$i_a(1-\epsilon)+i_b\lvert\eta_b-\eta_c\rvert+i_c\cancel{\lvert\eta_c-\eta_c\rvert}$	$x_{\min}\leq-\eta_c\leq x_{\max}$ & $\lvert\eta_a-\eta_c\rvert\leq 1-\epsilon$
b	$x_{\min}$	$i_b(1-\epsilon)+i_a\lvert\eta_a+x_{\min}\rvert+i_c\lvert\eta_c+x_{\min}\rvert$	$\lvert\eta_b+x_{\min}\rvert\leq 1-\epsilon$
	$x_{\max}$	$i_b(1-\epsilon)+i_a\lvert\eta_a+x_{\max}\rvert+i_c\lvert\eta_c+x_{\max}\rvert$	$\lvert\eta_b+x_{\max}\rvert\leq 1-\epsilon$
	$-\eta_a$	$i_b(1-\epsilon)+i_a\cancel{\lvert\eta_a-\eta_a\rvert}+i_c\lvert\eta_c-\eta_a\rvert$	$x_{\min}\leq-\eta_a\leq x_{\max}$ & $\lvert\eta_b-\eta_a\rvert\leq 1-\epsilon$
	$-\eta_b$	$i_b(1-\epsilon)+i_a\lvert\eta_a-\eta_b\rvert+i_c\lvert\eta_c-\eta_b\rvert$	$x_{\min}\leq-\eta_b\leq x_{\max}$ & $\cancel{\lvert\eta_b-\eta_b\rvert}\leq 1-\epsilon$
	$-\eta_c$	$i_b(1-\epsilon)+i_a\lvert\eta_a-\eta_c\rvert+i_c\cancel{\lvert\eta_c-\eta_c\rvert}$	$x_{\min}\leq-\eta_c\leq x_{\max}$ & $\lvert\eta_b-\eta_c\rvert\leq 1-\epsilon$
c	$x_{\min}$	$i_c(1-\epsilon)+i_a\lvert\eta_a+x_{\min}\rvert+i_b\lvert\eta_b+x_{\min}\rvert$	$\lvert\eta_c+x_{\min}\rvert\leq 1-\epsilon$
	$x_{\max}$	$i_c(1-\epsilon)+i_a\lvert\eta_a+x_{\max}\rvert+i_b\lvert\eta_b+x_{\max}\rvert$	$\lvert\eta_c+x_{\max}\rvert\leq 1-\epsilon$
	$-\eta_a$	$i_c(1-\epsilon)+i_a\cancel{\lvert\eta_a-\eta_a\rvert}+i_b\lvert\eta_b-\eta_a\rvert$	$x_{\min}\leq-\eta_a\leq x_{\max}$ & $\lvert\eta_c-\eta_a\rvert\leq 1-\epsilon$
	$-\eta_b$	$i_c(1-\epsilon)+i_a\lvert\eta_a-\eta_b\rvert+i_b\cancel{\lvert\eta_b-\eta_b\rvert}$	$x_{\min}\leq-\eta_b\leq x_{\max}$ & $\lvert\eta_c-\eta_b\rvert\leq 1-\epsilon$
	$-\eta_c$	$i_c(1-\epsilon)+i_a\lvert\eta_a-\eta_c\rvert+i_b\lvert\eta_b-\eta_c\rvert$	$x_{\min}\leq-\eta_c\leq x_{\max}$ & $\cancel{\lvert\eta_c-\eta_c\rvert}\leq 1-\epsilon$

As expected, the curve moves towards positive values as the power factor decreases, increasing the ripple of v_d at steady state and making the balancing slower.

In order to corroborate that $f_{\text{cost}}(x^*)$ is reduced with the addition of this enhancement, its time integral over a grid period is drawn (Fig. 7). In this way, the larger this integral is, the slower the balancing results. To picture this figure, it has been assumed that the sign of v_d does not change over a grid period and that the phase currents (i_i) and output waveforms (η_i) are normalised as $i_i=\sin(\omega_g t+\sigma_i+\phi)$ and $\eta_i=m\sin(\omega_g t+\sigma_i)$ with $\{\sigma_a,\sigma_b,\sigma_c\}=\{0,-2\pi/3,2\pi/3\}$, where $\cos\phi$ is used as an indicator of the power factor—the voltage drop of the grid filter is neglected for this comparison— and m is the modulation index. Consequently, the integral may be calculated based on the power factor indicator and the modulation index. It can be seen that the incorporation of this enhancement makes the integral to yield lower values of $f_{\text{cost}}(x^*)$.

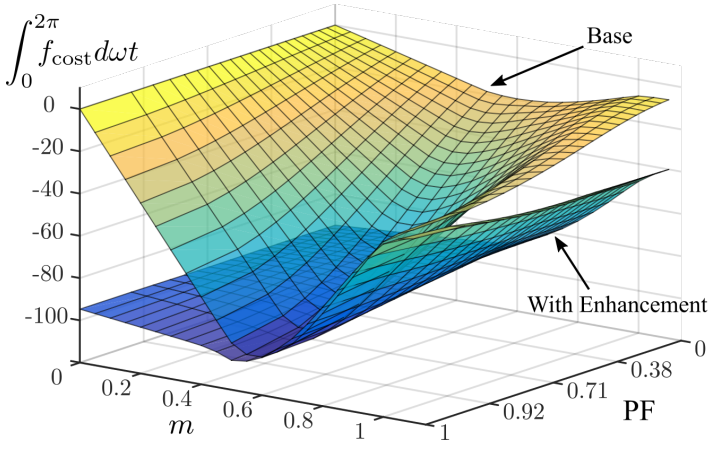

Figure 7. Integral of $f_{\text{cost}}(x^*)$ over a grid period for different values of power factor and the modulation index with and without the enhancement.

The proposed enhanced algorithm coincides with the base one when at least one value of f_{cost} for the cases of Table 1 is negative. In the case when no points gets negative values, the enhancement is implemented to decrease it. **The voltage balance capabilities are improved but at the cost of increasing the number of levels used and, therefore, the number of commutations and the switching losses. To avoid this, in contrast to [18], and** considering that it is not necessary that v_d goes to zero but it suffices that it is small enough, a band of value ζ is defined such that only when the value of $|v_d|$ is outside of it, the enhancement is applied. **Consequently, the increased number of commutations occurs only during the transient period when v_d is large and, thus, the base algorithm is used at steady state.** A brief flow chart with the enhancement implementation is plotted in Fig. 8.

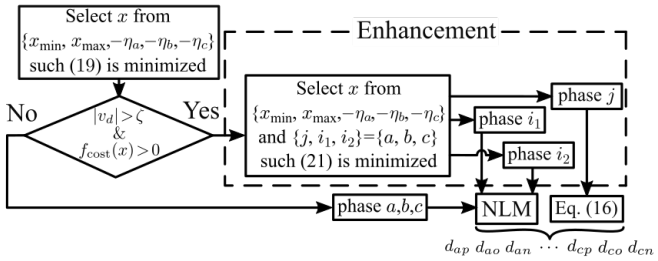

Figure 8. Flow chart of the implementation of the algorithm enhancement

4. Experimental Verification

This section aims to show the behaviour of the proposed algorithms in an experimental prototype of 12 kVA (Fig. 9). The circuit and control parameters of the converter are shown in Table 4, whereas the parameters that change along the experiment are given in Table 3 together with the time interval where they take place. **The system consists of a grid-connected three-level converter controlled by a real-time target machine. The system power rate and all components have been designed according to the limits of the available infrastructure. The system acts as a rectifier capable of injecting or subtracting reactive power from the grid. Besides, the resistor connected to the dc-link uses a chopper circuit to demand different power rates which allows to emulate different resistance values. Considering this, the system is suitable for evaluating the algorithm proposed in this paper.**

Several operating points are emulated by modifying user-input variables: v_{dc}^r, q^r; and circuit parameter: R. Unless otherwise stated, q^r is assumed to be zero to achieve unity power factor. Furthermore, to provide a comparison with other published approaches, the results of the experiments using a modified version of SVPWM approach with balancing capabilities [24] are also included in the figures— referred as modified virtual-space-vector (mVSV) from now on. In the experiments, **both dc-link and current controllers are kept the same for the mVSV approach and the proposed ones.**

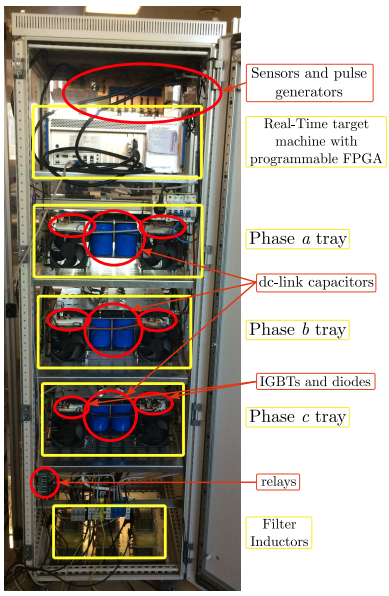

Figure 9. Experimental prototype of the three-level NPC rectifier.

Table 3. Experiment Parameters Variation

Time Interval	R	v_{dc}^r
$0 \rightarrow 0.8\,s$	$120\,\Omega$	$700\,V$
$0.8 \rightarrow 1.5\,s$	$60\,\Omega$	$700\,V$
$1.5 \rightarrow 2.2\,s$	$60\,\Omega$	$700 \rightarrow 800\,V$
$2.2 \rightarrow 3.8\,s$	$60\,\Omega$	$800\,V$
$3.8 \rightarrow 4.5\,s$	$120\,\Omega$	$800\,V$

The phase currents, instantaneous active power and switching states of phase a are plotted in Fig. 10 for both the base algorithm and the mVSV approach. It can be seen that the base algorithm shows a very similar behaviour compared with mVSV except for the number of commutations. Considering the results presented in Fig. 10, the base algorithm yields 265 commutations—number of 1-level transitions— per grid period, while the mVSV algorithm yields 375.

Regarding the current distortion, Fig. 11 depicts the harmonic spectrum and the total harmonic distortion (THD) value for the currents of Fig. 10 for the base algorithm and the mVSV one. It can be seen that the proposed algorithms and the mVSV have very similar current distortion, therefore this proposal does not worsen the current quality

Table 4. Experiment Parameters

Parameter	**Value**	**Parameter**	**Value**
Grid frequency f_{grid}	50 Hz	Sampling frequency (f_s)	10 kHz
Grid Voltage v_{sa}, v_{sb}, v_{sc}	230 V_{RMS}	Switching frequency (f_{sw})	10 kHz
Filter Inductance L	2 mH	Current control P gain k_p	5
Capacitance C	3300 μF	Current control R gain k_r	100
dc voltage control P gain k_p^{dc}	0.05	dc voltage control I gain k_i^{dc}	1
Enhancement parameter ϵ	0.1	Current control resonant cut-off frequency ω_c	1 rad/s
Enhancement band ζ	10 V		

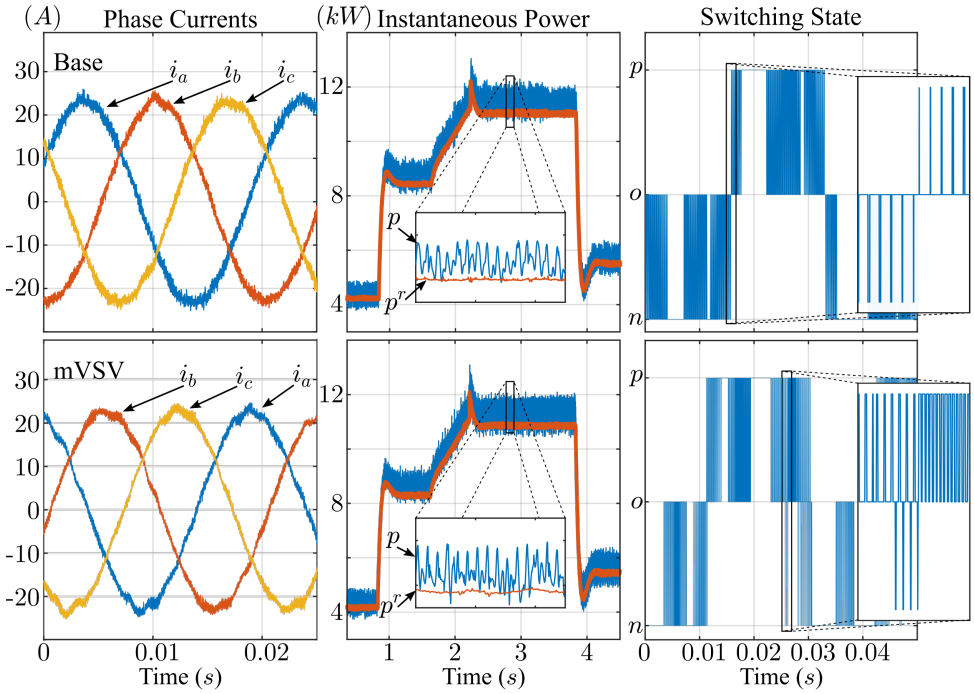

Figure 10. Experimental results at steady state with $v_{dc} = 800\,V$ and $R = 60\,\Omega$: (top) base algorithm, (bottom) mVSV algorithm: (left) three phase currents at steady state with $v_{dc} = 800\,V$ and $R = 60\,\Omega$; (center) evolution of system power (p) and power reference (p^r) along different operating points; (right) switching state of phase a output

when compared with other space-vector-based algorithm. In summary, at steady state the base algorithm presents less number of commutations, and thus it generates less losses, with similar current distortion when compared with the mVSV approach [24].

In terms of balancing capabilities, two experimental tests starting from an unbalanced situation with different operation points are considered as depicted in Fig. 12: a) unity power factor, and b) zero power factor. Figure 12a) shows a comparison of the balancing performance between the proposed algorithm and the mVSV, once the current controller is at steady state, with $v_{dc} = 700\,V$, $R = 120\,\Omega$ and unity power factor. It can be seen that the balanced situation is achieved almost at the same time for both approaches, making the proposed algorithm suitable for balancing purposes when compared with other existing solution. On the other hand, in order to exhibit the relevance of the enhanced algorithm, Fig. 12b) is depicted for power factor equal to zero. It shows how, under this condition, the balancing capability of the base algorithm is slowered, increasing the time it takes to reach the balanced condition. Similarly, **the mVSV algorithm presents much slower behaviour in terms of balancing capabilities**. On the contrary, by implementing the enhanced algorithm, the balancing capability is considerably improved whenever $|v_d| > \zeta$. In this way, a suitable approach for balancing purposes under different operating points is proposed. Notice that at steady state, the base and the enhanced algorithm show similar behaviour as the differences between them

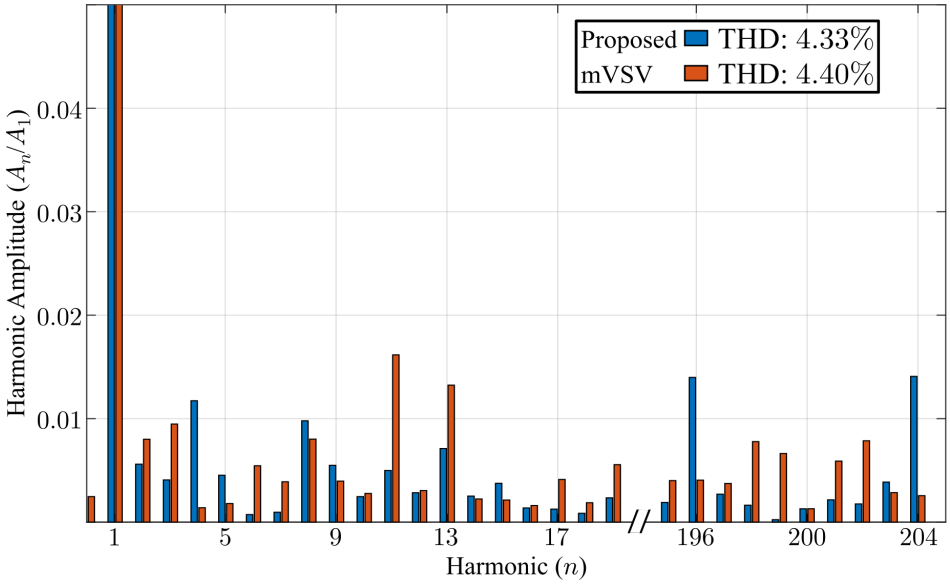

Figure 11. Experimental results: Harmonic spectrum of currents of phase a shown in Fig. 10 and corresponding THD value for the proposed algorithms and the mVSV one

only appear when $|v_d| > \zeta$. Nevertheless, this modification entails an increment in the amount of commutations as depicted in Fig. 13. This increase is due to the occasional use of a third level during a transient period where $|v_d| > \zeta$ and the operating conditions yield $f_{\text{cost}} > 0$ for the base algorithm. In this regard, during this transient stage, the enhanced algorithm yields 627 commutations per grid period according to Fig. 13. Nevertheless, this increased number only occurs during a short transient (less than 0.1 seconds in Fig. 12b) **until variable v_d is within the band $|\zeta|$.**

5. Concluding Remarks

In this paper, the capacitors voltage balance **for grid-connected three-level NPC converters has been addressed as an optimisation problem based on a cost function directly related to the balance dynamic equation. The proposed strategy minimizes the number of commutations at the same time that the voltage balance is tackled.** Furthermore, given that the proposal only depends on the normalised output voltage, it can be implemented with any kind of current/power control.

Besides, an enhancement in the algorithm assists in the capacitors voltage balancing when the previous approach could yield large balancing times. In this way, the capacitors voltage balance is improved for different operation points.

The validity of the proposal has been tested in an experimental setup and compared with a modified version of virtual space vector modulation with voltage balance capabilities (mVSV). **This comparison shows that the proposed approach and**

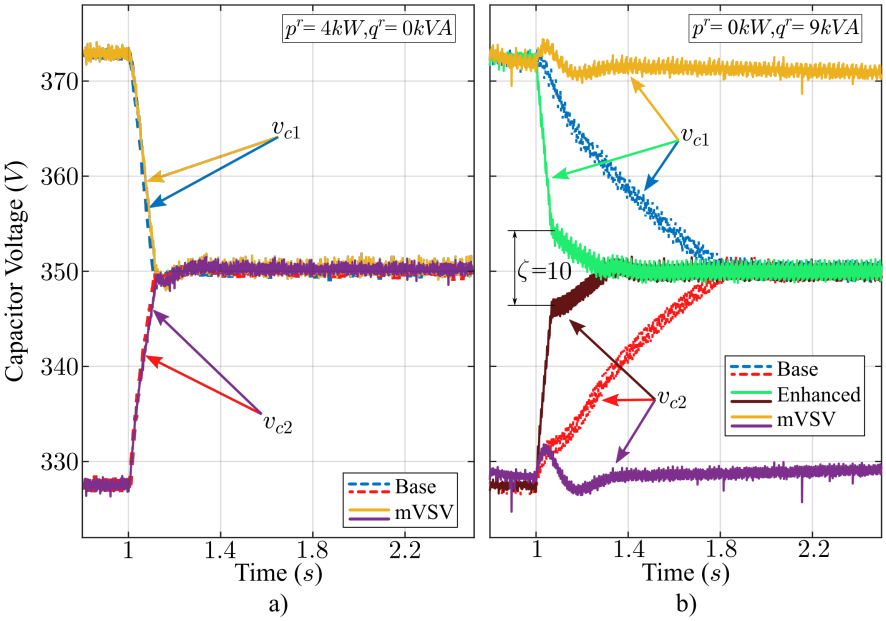

Figure 12. Experimental results: Evolution of the capacitors voltage starting from an unbalanced situation: a) Base algorithm compared with mVSV with $v_{dc} = 700\,V$ and $R = 120\,\Omega$; b) Base algorithm compared with the enhanced one **and mVSV** with $v_{dc} = 700\,V$, $R = \text{inf}\ \Omega$ and $\zeta = 10\,V$.

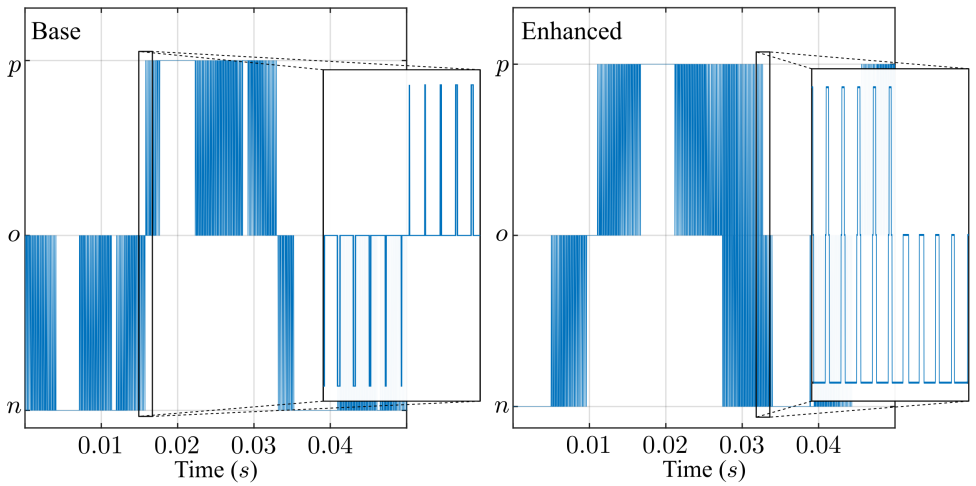

Figure 13. Experimental results: Switching state of phase a at steady state for the base algorithm with $v_{dc} = 800\,V$ and $R = 120\,\Omega$ (left) and the enhanced one during a transient state where $v_d > \zeta$ with $v_{dc} = 800\,V$ and $R = \text{inf}\ \Omega$ (right).

its enhancement achieve similar balancing capabilities for a wider range of power factor values, with no deterioration of the current distortion (4.4% THD for mVSV and the proposed algorithm) but without the added diffi-

culty of implementing space vector modulation. Indeed, the implementation complexity is as simple as those of carrier-based. Besides, the number of commutations is reduced by 30% at steady-state in comparison with mVSV. Therefore, a valid approach for interfacing NPC rectifiers with the grid is presented. In addition, the extension of this approach to three-level NPC inverters is straightforward considering just the corresponding change of the current control and the direction of the currents.

Acknowledgements

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