A novel Controller for Grid-interfacing Solar Arrays through Five-level Diode-clamped Converters

Topic category: **Power Electronic Converter Topologies, Design and Control**

***Abstract*—This paper presents an approach to control a grid-connected, five-level, diode-clamped inverter with solar arrays directly connected to each capacitor of the dc-link. On one hand, the control of such converters is challenging as the voltage imbalance among the capacitor mights affect the power controller. On the other hand, when dealing with solar arrays, the dc voltage is a key point considering that the efficiency of the array highly depends on it. This article presents a solution where both aims are fulfilled: the desired capacitor voltages, set by the maximum power point tracking (MPPT) algorithm, are reached at the same time that these values are taken into account in the power controller. This is an unusual approach for five-level NPC converters that avoids the use of DC-DC stages, therefore it makes the system more affordable and avoids extra losses. Thanks to the closed-loop capacitor voltage controller, proper power extraction from each solar array is achieved. The theoretical presentation of this approach is shown along with simulation results that validates its effectiveness.**

I. Introduction

Nowadays, multilevel converters are a desirable application for renewable and high-power applications [1]–[3]. This is due to the output property of the multilevel converter that sets several line-to-line voltage steps according to the number of levels. This property reduces the voltage limits of each switching device and, at the same time, it improves the current distortion.

Regarding renewable applications, photovoltaic energy is being considered one of the most profitable and affordable source of renewable energy due to its constant improvement and cheapening [4]. There had been many researches focused on developing better topologies, controls or maximum power point tracking (MPPT) algorithms for integrating the photovoltaic energy into the grid [5], [6]. Any set of solar arrays has an output current that depends on the dc voltage across them, the irradiation and the solar array disposition. As a result, there is, at least, one point which corresponds to the maximum output power point. The aim of the MPPT is, then, to set the voltage that maximizes its total output power [7]. The usual strategy to achieve this is by inserting a DC-DC Stage between the converter dc-link and the solar array, in this way the converter dc-link voltage stays constant while the solar array dc voltage is set according to the MPPT.

Nowadays, there are many works that considered the idea of using multilevel converters with dc-link-connected solar arrays [8]–[10]. However, these previous works generally considered only one dc-link-connected solar array either directly or through a DC-DC Stage. This configuration requires the solar array to be of similar dc voltage magnitude than the dc-link point of operation which means a long array of serial-connected solar cells. Therefore, all issues related to loss of efficiency of one or more solar cells might compromise the whole system power output. This issue can be solved by using cascaded converters [11], [12], where each module has its own capacitor and solar array. This topology separates the total dc-link voltage into two or more modules per phase, thus avoiding that a loss of efficiency of one solar cell affects the whole system. However, three-phase cascaded converters, such as cascaded H-bridge converters (CHB), would require at least two modules per phase resulting in 6 modules in a five-level configuration, which increases the volume and price along with the complexity of balancing such an amount of capacitors. As an alternative, in [12] a three cascaded three-phase two level voltage source inverter (VSI) is mentioned. Every VSI in this topology can attach a solar cell to its dc-link; however the necessity of including 3 extra coils in the interconnection makes it bigger and less efficient than other solutions as coils are well-known for being bulky and a source of losses.

This paper is focused on the diode-clamped converters (DCC) topology due to its acceptance in the power electronic industry. Three-level DCC are widely used and it is still being commercialized by several companies. Nevertheless, five-level DCC finds some reluctance to be implemented in the industry due to its higher complexity both in hardware and software [13]. Whereas three-level DCC needs to assure the same voltage for two capacitors, five-level DCC needs to accomplish this objective for four capacitors. This means that in three-level DCC only one error signal has to be regulated –apart from the usual control objectives– while in five-level DCC three error signals have to be monitored and controlled. In the literature, there are several approaches for this objective. These approaches include, among others, the use of additional circuitry [14], [15] or exploiting the degree of freedom associated to redundant switching vectors while using SVM techniques [16], [17]. In this paper, the voltage balance closed loop control along with the modulation proposed in [18] is considered and analyzed.

The contribution of this work comes from avoiding the DC-DC stage insertion while fulfilling the MPPT outputs. In this way, the system is simplified at the same time it is made cheaper, less bulky and more efficient. In [19] a 3-level NPC converter is presented with capacitor-attached solar

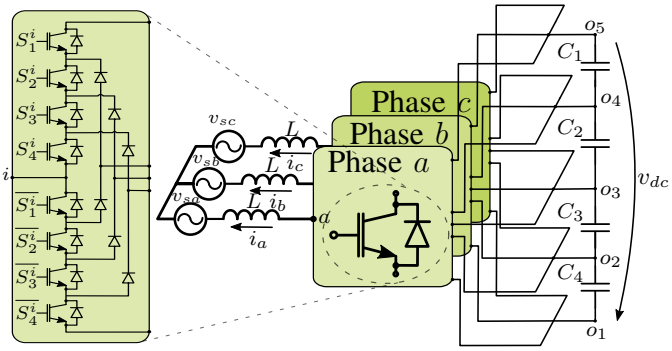

Fig. 1. Schematic diagram of the five-level diode-clamped converter operating as an inverter connected to the grid.

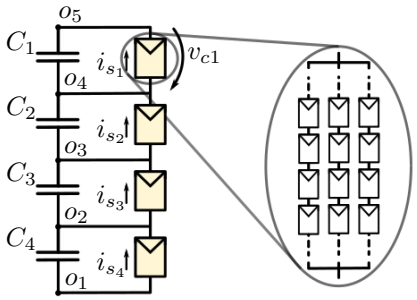

Fig. 2. Schematic diagram of the solar arrays connected to the dc-link side

arrays, although it does not consider an MPPT algorithm but a simple capacitor voltage equalization. As the MPPT algorithm may provide different capacitor voltage references, they will be taken into account in the design of the modulation stage.

A five-level DCC model as an inverter is introduced first. Secondly, the current control, dc-link voltage regulation, individual capacitor voltage control and the modulation stage are presented. Afterwards, some simulations are depicted and discussed in order to prove the fulfillment of the control objectives. Finally, some conclusions are drawn.

II. Five-level DCC Model

A. Five-level DCC converter description

A five-level DCC converter is depicted in Fig. 1. The dc-link is composed of four capacitors (C_1, C_2, C_3 and C_4) with the same capacitance (C) and each phase has a branch of eight semiconductor devices and six diodes that allow the phase current to flow from or into the points o_j for $j = 1, 2, 3, 4, 5$ depending on the state of the semiconductors. The lower semiconductor gating signals are the opposite of the upper ones and, thus, four signals are required to control a phase branch: $S_1^i, S_2^i, S_3^i, S_4^i$ for $i = a, b, c$. Each phase branch output –point i for $i = a, b, c$– is connected to its correspondent grid phase (v_{sa}, v_{sb} and v_{sc}) through an inductor whose inductance is equal to L.

Therefore, the total dc-link voltage (v_{dc}) is composed of the addition of the four capacitor voltages $v_{c_1}, v_{c_2}, v_{c_3}$ and v_{c_4}. The phase currents i_a, i_b and i_c are defined positive in the way depicted in Fig. 1, that is, positive when going from the converter to the grid. From now on, the grid is considered balanced so the equations $v_{sa}+v_{sb}+v_{sc} = 0$ and $i_a+i_b+i_c = 0$ are always fulfilled.

B. Solar arrays

The solar arrays are attached individually to each dc-link capacitor, resulting in four power sources. Figure 2 shows how the solar arrays are attached to the converter. As it has been said, MPPT algorithms will provide the capacitor voltage controller with the voltage value each capacitor should have: $v_{c1_{\text{ref}}}, v_{c2_{\text{ref}}}, v_{c3_{\text{ref}}}, v_{c4_{\text{ref}}}$. The literature is plenty of MPPT algorithm implementations and, consequently this work will not consider its implementation but its output as a control objective. Also notice that the output currents of the solar arrays, $i_{s_1}, i_{s_2}, i_{s_3}, i_{s_4}$, may not be equal and their values will depend on the conditions under which they are.

C. Switching states

Considering the previous definitions, the output voltage of the converter for each phase i (v_i) measured with respect to o_3 can be obtained according to the value of its gating signals. In order to express this, variable f_{i_j} for $i = a, b, c$ and $j = 1, 2, 3, 4, 5$ is used as a switching function to indicate the switching state. If $f_{i_j} = 1$, it means that point i is connected to level o_j through the converter. As a result, $f_{i_j} = \{0, 1\}$ and only one f_{i_j} for every $i = a, b, c$ can be equal to one – $f_{i_1} + f_{i_2} + f_{i_3} + f_{i_4} + f_{i_5} = 1$. Accordingly, table I depicts this value along with the values of the gating signals, 1: ON; 0: OFF, and output voltage (v_i) for phase i.

TABLE I
Output voltage according to the gating signals

S_1^i	S_2^i	S_3^i	S_4^i	v_i	Switching State
0	0	0	0	$-v_{c_3} - v_{c_4}$	$f_{i_1} = 1$
0	0	0	1	$-v_{c_3}$	$f_{i_2} = 1$
0	0	1	1	0	$f_{i_3} = 1$
0	1	1	1	v_{c_2}	$f_{i_4} = 1$
1	1	1	1	$v_{c_2} + v_{c_1}$	$f_{i_5} = 1$

D. Averaged Model

In order to deal with a continuous model from a system with discrete variables, an averaged model is contemplated [18]. Consequently, the model is averaged within a switching period and the switching function $f_{i_j} = \{0, 1\}$ is replaced by its averaged value $d_{i_j} = [0, 1]$. In this manner, d_{i_j} means the fraction of the switching period that $f_{i_j} = 1$, i.e., the amount of time within a switching period that point i is connected to level o_j. These variables (d_{i_j}) will be referred as duty ratios of phase i and level j from now on. Accordingly:

$$d_{i_1} + d_{i_2} + d_{i_3} + d_{i_4} + d_{i_5} = 1, \quad i = a, b, c. \tag{1}$$

In order to express the relations among the capacitor voltages, the next balancing signals are defined

$$v_{d1} = v_{c4} - v_{c1} \tag{2}$$

$$v_{d2} = v_{c3} - v_{c2} \tag{3}$$

$$v_{d3} = v_{c2} - v_{c1}. \tag{4}$$

The dynamic of these signals can be obtained by substituting each capacitor voltage dynamic – retrieved from applying the

capacitor equation ($Cdv_C/dt = i_c$) to the previous definition of duty ratios – into (2–4).

$$C\frac{dv_{d1}}{dt} = \sum_{i=a,b,c} (d_{i_5} + d_{i_1})i_i + h_1 \tag{5}$$

$$C\frac{dv_{d2}}{dt} = \sum_{i=a,b,c} -d_{i_3}i_i + h_2 \tag{6}$$

$$C\frac{dv_{d3}}{dt} = \sum_{i=a,b,c} -d_{i_4}i_i + h_3. \tag{7}$$

$$\begin{pmatrix} h_1 \\ h_2 \\ h_3 \end{pmatrix} = \begin{pmatrix} -1 & 0 & 0 & 1 \\ 0 & -1 & 1 & 0 \\ -1 & 1 & 0 & 0 \end{pmatrix} \begin{pmatrix} i_{s_1} \\ i_{s_2} \\ i_{s_3} \\ i_{s_4} \end{pmatrix}$$

Considering the previous definition and the Kirchhoff's laws, the averaged model can be described as

$$\begin{aligned} L\frac{di_i}{dt} &= -v_{si} + (2u_i - u_{j_1} - u_{j_2})\frac{v_{dc}}{12} \\ &+ \frac{v_{d1}}{12}(2h_{d1_i} - h_{d1_{j_1}} - h_{d1_{j_2}}) \\ &+ \frac{v_{d2}}{12}(2h_{d2_i} - h_{d2_{j_1}} - h_{d2_{j_2}}) \\ &+ \frac{v_{d3}}{12}(2h_{d3_i} - h_{d3_{j_1}} - h_{d3_{j_2}}), \end{aligned} \tag{8}$$

$$\begin{aligned} u_i &= -2d_{i_1} - d_{i_2} + d_{i_4} + 2d_{i_5} \\ h_{d1_i} &= -2d_{i_1} + d_{i_2} - d_{i_4} - 2d_{i_5} \\ h_{d2_i} &= -2d_{i_1} - 3d_{i_2} - d_{i_4} - 2d_{i_5} \\ h_{d3_i} &= -2d_{i_2} + 2d_{i_4} \end{aligned}$$

where $i = a, b, c$ and j_1 and j_2 are the other two phases for each value of i. Variable u_i represents the output voltage (v_i) per unit of capacitor voltage set by the converter at point i when the capacitor voltages are equal, i.e., $u_i = 4v_i/v_{dc}$. Whereas variables h_{d1_i}, h_{d2_i} and h_{d3_i} represents the effect on the same output voltage when the capacitor voltages are not equal. It can be noted that the duty ratio d_{io_3} does not appear in the averaged model due to the fact that its output voltage is equal to zero.

E. Averaged model in $\alpha\beta\gamma$ coordinates

In order to simplify the model in abc frame (8), the $\alpha\beta\gamma$ frame is considered. Accordingly, the $\alpha\beta$ coordinates express the state of the balanced abc coordinates, whereas γ coordinate indicates the zero component of these coordinates. Obviously, in a balanced system, such as the one under consideration, the γ coordinate for current and voltage is equal to zero, i.e., $v_{s\gamma} = 0$, $i_\gamma = 0$.

Consequently, by applying the power-invariant form of the Clarke transformation to (8) yields

$$\begin{aligned} L\frac{di_k}{dt} &= -v_{sk} + \frac{v_{dc}}{4}u_k \\ &\quad + \frac{1}{4}\left(v_{d1}h_{d1_k} + v_{d2}h_{d2_k} + v_{d3}h_{d3_k}\right), \\ u_k &= -2d_{k_1} - d_{k_2} + d_{k_4} + 2d_{k_5} \\ h_{d1_k} &= -2d_{k_1} + d_{k_2} - d_{k_4} - 2d_{k_5} \\ h_{d2_k} &= -2d_{k_1} - 3d_{k_2} - d_{k_4} - 2d_{k_5} \\ h_{d3_k} &= -2d_{k_2} + 2d_{k_4} \end{aligned} \tag{9}$$

where $k = \alpha, \beta$. It can be seen in (9) that the γ component is not present in the dynamic equation. Similarly, the dynamic of the balancing signals (5)-(7) can be expressed in the $\alpha\beta\gamma$ frame:

$$C\frac{dv_{d1}}{dt} = \sum_{k=\alpha,\beta} \left(d_{k_5} + d_{k_1}\right) i_k + h_1 \tag{10}$$

$$C\frac{dv_{d2}}{dt} = \sum_{k=\alpha,\beta} \left(d_{k_1} + d_{k_2} + d_{k_4} + d_{k_5}\right) i_k + h_2 \tag{11}$$

$$C\frac{dv_{d3}}{dt} = \sum_{k=\alpha,\beta} -d_{k_4}i_k + h_3. \tag{12}$$

Notice that (1) is used when transforming from (6) to (11), as a result, d_{i_3} for $i = a, b, c$ is suppressed as control input and it is determined by (1).

III. Controller Design

This section presents how the control of five-level NPC converter is achieved. In order to fulfill the control objectives, a change of variables is firstly considered. There are eight d_{k_j}, therefore let us consider eight control variables, u_l $l = 1, \ldots, 8$ inspired by (9)-(12):

$$u_1 = u_\alpha + 1/v_{dc}(v_{d1}h_{d1_\alpha} + v_{d2}h_{d2_\alpha} + v_{d3}h_{d3_\alpha}) \tag{13}$$

$$u_2 = u_\beta + 1/v_{dc}(v_{d1}h_{d1_\beta} + v_{d2}h_{d2_\beta} + v_{d3}h_{d3_\beta}) \tag{14}$$

$$u_3 = d_{\alpha_5} + d_{\alpha_1} \tag{15}$$

$$u_4 = d_{\beta_5} + d_{\beta_1} \tag{16}$$

$$u_5 = d_{\alpha_1} + d_{\alpha_2} + d_{\alpha_4} + d_{\alpha_5} \tag{17}$$

$$u_6 = d_{\beta_1} + d_{\beta_2} + d_{\beta_4} + d_{\beta_5} \tag{18}$$

$$u_7 = -d_{\alpha_4} \tag{19}$$

$$u_8 = -d_{\beta_4}. \tag{20}$$

In this way, (13)–(20) express the relation between these control variables (u_l) and the duty ratios in $\alpha\beta$ frame. As this change of variables is invertible, once the control variables are known and assuming the balancing signals are slow enough to be considered constant over a switching period, the value of the duty ratios can be retrieved directly by inverting (13)–(20).

A. Total dc-link voltage controller

Given the fact that the dc-link capacitors are attached to solar arrays whose optimum voltage do not remain constant, it is necessary to include a total dc-link voltage regulation into the controller system. This controller will set the amount of output active power (p_{ref}) according to the actual value of the total dc-link voltage (v_{dc}) and the desired one ($v_{dc_{\text{ref}}}$). Considering $v_{dc_{\text{ref}}} = v_{c1_{\text{ref}}} + v_{c2_{\text{ref}}} + v_{c3_{\text{ref}}} + v_{c4_{\text{ref}}}$, once the MPPT algorithm of each capacitor provides the desired capacitor voltages, the aimed dc-link voltage is known. Therefore, by applying a PI controller

$$p_{\text{ref}} = k_p^{v_{dc}}(v_{dc_{\text{ref}}}^2 - v_{dc}^2) + k_i^{v_{dc}} \int_0^T (v_{dc_{\text{ref}}}^2 - v_{dc}^2)dt, \tag{21}$$

the value of p_{ref} is obtained. On the other hand, the amount of output reactive power (q_{ref}) is set externally to this controller, usually equal to zero in order to achieve unity power factor.

B. Current Controller

By applying (13)–(20) into (9), the current dynamics are expressed as:

$$L\frac{di_\alpha}{dt} = -v_{s\alpha} + \frac{v_{dc}}{4}u_1$$

$$L\frac{di_\beta}{dt} = -v_{s\beta} + \frac{v_{dc}}{4}u_2.$$

Control variables u_1 and u_2 represent the voltage output of the converter in α and β frame normalized by the fourth part of the total dc-link. These dynamics are similar to those of a two-level converter, therefore any control strategy of this converter [20], [21] can be extended to this case. For the sake of simplicity, a current control in $\alpha\beta$ frame is considered here.

$$u_1 = \frac{4}{v_{dc}}(k_p e_\alpha + k_i \int_0^T e_\alpha dt + v_{s\alpha}) \tag{22}$$

$$u_2 = \frac{4}{v_{dc}}(k_p e_\beta + k_i \int_0^T e_\beta dt + v_{s\beta}), \tag{23}$$

where $e_\alpha = i_{\alpha_{\text{ref}}} - i_\alpha$, $e_\beta = i_{\beta_{\text{ref}}} - i_\beta$. Variables $i_{\alpha_{\text{ref}}}$ and $i_{\beta_{\text{ref}}}$ are obtained from applying the definition of instantaneous power [22] to the values p_{ref} and q_{ref}.

C. Capacitor Voltage Controller

By applying (13)–(20) into (10)-(12), the dynamics of the balancing signals are simplified to

$$\begin{pmatrix} \frac{dv_{d1}}{dt} \\ \frac{dv_{d2}}{dt} \\ \frac{dv_{d3}}{dt} \end{pmatrix} = \begin{pmatrix} i_\alpha & i_\beta & 0 & 0 & 0 & 0 \\ 0 & 0 & i_\alpha & i_\beta & 0 & 0 \\ 0 & 0 & 0 & 0 & i_\alpha & i_\beta \end{pmatrix} \begin{pmatrix} u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \\ u_8 \end{pmatrix} + \begin{pmatrix} h_1 \\ h_2 \\ h_3 \end{pmatrix}. \tag{24}$$

Consequently, the control of the balancing signals v_{d1}, v_{d2} and v_{d3} is decoupled from the current control. Control variables u_1 and u_2 are determined by the current controller, whereas u_3–u_8 can be used to regulate the balancing signals. Thus, defining $\widehat{v_{dp}} = v_{dp_{\text{ref}}} - v_{dp}$ for $p = 1, 2, 3$, where $v_{d1_{\text{ref}}}, v_{d2_{\text{ref}}}, v_{d3_{\text{ref}}}$ are the desired value of the balancing signals obtained by inserting $v_{c1_{\text{ref}}}, v_{c2_{\text{ref}}}, v_{c3_{\text{ref}}}, v_{c4_{\text{ref}}}$ into (2)-(4); control variables u_3–u_8 are defined as follows

$$\begin{pmatrix} u_3 \\ u_4 \\ u_5 \\ u_6 \\ u_7 \\ u_8 \end{pmatrix} = \begin{pmatrix} i_\alpha & 0 & 0 \\ i_\beta & 0 & 0 \\ 0 & i_\alpha & 0 \\ 0 & i_\beta & 0 \\ 0 & 0 & i_\alpha \\ 0 & 0 & i_\beta \end{pmatrix} \begin{pmatrix} k^p_{\text{bal}}\widehat{v_{d1}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d1}} \\ k^p_{\text{bal}}\widehat{v_{d2}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d2}} \\ k^p_{\text{bal}}\widehat{v_{d3}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d3}} \end{pmatrix}, \tag{25}$$

where $k^p_{\text{bal}} > 0$ and $k^i_{\text{bal}} > 0$ are the control parameters of the capacitor voltage controller. As a result, by applying (25) into (24), the closed-loop dynamics are described by

$$\begin{pmatrix} \frac{dv_{d1}}{dt} \\ \frac{dv_{d2}}{dt} \\ \frac{dv_{d3}}{dt} \end{pmatrix} = (i_\alpha^2 + i_\beta^2) \begin{pmatrix} k^p_{\text{bal}}\widehat{v_{d1}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d1}} \\ k^p_{\text{bal}}\widehat{v_{d2}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d2}} \\ k^p_{\text{bal}}\widehat{v_{d3}} + k^i_{\text{bal}} \int_0^t \widehat{v_{d3}} \end{pmatrix} + \begin{pmatrix} h_1 \\ h_2 \\ h_3 \end{pmatrix}.$$

Considering the fact that $(i_\alpha^2 + i_\beta^2) = I_{\alpha\beta} > 0$, it can be seen that v_{dp} is exponentially stable around $v_{dp_{\text{ref}}}$ as the integral term $k^i_{\text{bal}} \int_0^t \widehat{v_{dp}}$ will compensate h_p at steady state.

D. Modulation stage

Once u_1-u_8 have been determined by (22),(23) and (25), it is time to revert the change of variables carried out in (13)–(20). By inverting theirs relations, the definitions of the duty ratios in $\alpha\beta$ frame according to the values of u_l are obtained.

$$\begin{bmatrix} d_{\alpha_1} \\ d_{\alpha_2} \\ d_{\alpha_4} \\ d_{\alpha_5} \end{bmatrix} = \begin{bmatrix} -\frac{1}{4} & d_{\alpha_{1_{u_3}}} & d_{\alpha_{1_{u_5}}} & d_{\alpha_{1_{u_7}}} \\ 0 & -1 & 1 & 1 \\ 0 & 0 & 0 & -1 \\ \frac{1}{4} & d_{\alpha_{5_{u_3}}} & d_{\alpha_{5_{u_5}}} & d_{\alpha_{5_{u_7}}} \end{bmatrix} \begin{bmatrix} u_1 \\ u_3 \\ u_5 \\ u_7 \end{bmatrix} \tag{26}$$

$$\begin{bmatrix} d_{\alpha_{1_{u_3}}} \\ d_{\alpha_{1_{u_5}}} \\ d_{\alpha_{1_{u_7}}} \\ d_{\alpha_{5_{u_3}}} \\ d_{\alpha_{5_{u_5}}} \\ d_{\alpha_{5_{u_7}}} \end{bmatrix} = \frac{1}{4v_{dc}} \begin{bmatrix} -3 & 1 & 2 & 3 \\ 1 & -3 & -2 & -1 \\ 2 & -2 & -4 & -2 \\ 3 & -1 & -2 & 1 \\ -1 & 3 & 2 & 1 \\ -2 & 2 & 4 & 2 \end{bmatrix} \begin{bmatrix} v_{d1} \\ v_{d2} \\ v_{d3} \\ v_{dc} \end{bmatrix}$$

Similar relations would be obtained when considering duty ratios in the β frame - $d_{\beta_1}, d_{\beta_2}, d_{\beta_4}, d_{\beta_5}$ - and u_l for $l = \{2, 4, 6, 8\}$. Consequently, the duty ratios in abc frame can be obtained, firstly by applying (26) in both α and β and, secondly by transforming from $\alpha\beta\gamma$ frame to abc frame through the reverted power-invariant Clarke transformation. It has been already stated that the value of d_{γ_j} has no effect on the fulfillment of the current controller, i.e., assuring that (22) and (23) are achieved. Despite this, the values of d_{γ_j} have a direct effect on the values of $d_{a_j}, d_{b_j}, d_{c_j}$ as d_{i_j} increases monotonically with d_{γ_j}, therefore it can not be ignored. In [18], some guidelines are given to select the values of d_{γ_j} for $j = 1, 2, 4, 5$ in order to avoid saturation of the d_{a_j}, d_{b_j} and d_{c_j} variables. Nevertheless, the steady state analysis performed in [18] is of no use in this system given the current injection from the solar arrays to each capacitor.

With the aim of avoiding saturation of d_{i_j} after applying the reverse power-invariant Clarke transformation, a criterion for selection of d_{γ_j} is provided. For this, the limits for d_{γ_j} can be retrieved by replacing the power-invariant Clarke transformation into the boundary values of d_{i_j}. Firstly,

$$d_{i_1} + d_{i_2} + d_{i_4} + d_{i_5} \leq 1 \quad i = \{a, b, c\}; \quad d^{\text{Sum}}_\gamma = \sum_{j=1,2,4,5} d_{\gamma_j}$$

$$\begin{cases} a :\rightarrow d^{\text{Sum}}_\gamma \leq \sqrt{3} - \sum_{j=1,2,4,5} \sqrt{2} d_{\alpha_j} & \text{(27a)} \\ b :\rightarrow d^{\text{Sum}}_\gamma \leq \sqrt{3} + \sum_{j=1,2,4,5} \left(\frac{d_{\alpha_j}}{\sqrt{2}} - \sqrt{\frac{3}{2}} d_{\beta_j} \right) & \text{(27b)} \\ c :\rightarrow d^{\text{Sum}}_\gamma \leq \sqrt{3} + \sum_{j=1,2,4,5} \left(\frac{d_{\alpha_j}}{\sqrt{2}} + \sqrt{\frac{3}{2}} d_{\beta_j} \right). & \text{(27c)} \end{cases}$$

Secondly,

$$d_{i_j} \geq 0 \quad j = \{1, 2, 4, 5\}$$

$$\begin{cases} a :\rightarrow d_{\gamma_j} \geq -\sqrt{2} d_{\alpha_j} & \text{(28a)} \\ b :\rightarrow d_{\gamma_j} \geq \frac{d_{\alpha_j}}{\sqrt{2}} - \sqrt{\frac{3}{2}} d_{\beta_j} & \text{(28b)} \\ c :\rightarrow d_{\gamma_j} \geq \frac{d_{\alpha_j}}{\sqrt{2}} + \sqrt{\frac{3}{2}} d_{\beta_j}. & \text{(28c)} \end{cases}$$

As a result, three constraints are imposed on d^{Sum}_γ that can be combined in the most restrictive one, and similarly for d_{γ_j}.

The solution adopted in this paper goes through selecting the values of d_{γ_j} for $j = 1, 5$ that fulfill (28) – otherwise it would make one $d_{i_j} < 0$ – and dividing among the three remaining levels – levels $2, 3, 4$ – the spare value of d_γ^{sum} in order to satisfy (27). The first choice pursues two objectives: granting there is enough d_γ^{sum} remaining for the rest of the levels; and reducing the commutations as the selected $d_{\gamma_{1\text{ or }5}}$ will make one $d_{i_{1\text{ or }5}}$ equal to zero. The second choice is made in order to assure that level $2, 3, 4$ always appear, avoiding forbidden commutations, e.g. $d_{i_2} \neq 0, d_{i_3} = 0, d_{i_4} \neq 0$.

In the case all d_{γ_j} are selected fulfilling (28) and despite this, constraint (27) is not met, then saturation is unavoidable. Accordingly, the selection criteria of d_{γ_j} is expressed in two cases as

$$d^{\text{Sum}}_{\gamma_{\min}} = \min(27) \quad ; \quad d_{\gamma_j^{\min}} = \max(28) \qquad j = 1, 2, 4, 5$$
$$d_{\gamma_j} = d_{\gamma_j^{\min}} \quad ; \quad d_{\gamma_{1,5}} = d_{\gamma_1} + d_{\gamma_5} \qquad j = 1, 5$$

$$1^{st}case: \quad (d^{\text{Sum}}_{\gamma_{\min}} - d_{\gamma_{1,5}}) \geq (d_{\gamma_2^{\min}} + d_{\gamma_4^{\min}})$$
$$\text{Gap} = (d^{\text{Sum}}_{\gamma_{\min}} - d_{\gamma_{1,5}}) - (d_{\gamma_2^{\min}} + d_{\gamma_4^{\min}})$$
$$d_{\gamma_2} = \text{Gap}/3 + d_{\gamma_2^{\min}}$$
$$d_{\gamma_4} = \text{Gap}/3 + d_{\gamma_4^{\min}}$$

$$2^{nd}case: \quad (d^{\text{Sum}}_{\gamma_{\min}} - d_{\gamma_{1,5}}) < (d_{\gamma_2^{\min}} + d_{\gamma_4^{\min}})$$
$$d_{\gamma_j} = d_{\gamma_j^{\min}} \qquad j = 2, 4$$

Notice that when 2^{nd} case is given, saturation is unavoidable and total dc-link voltage should be increased. This selection criteria is depicted in Fig. 3.

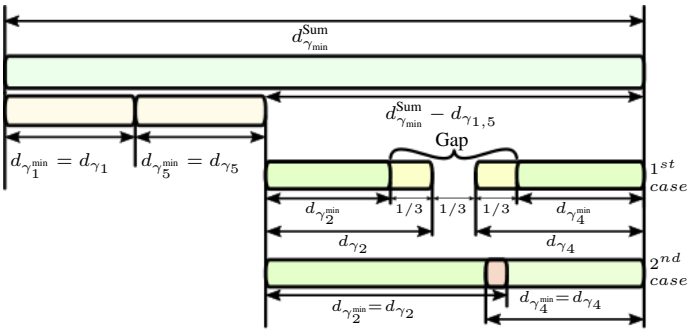

Fig. 3. Sample of distribution of gamma according to the stated cases

To finish this section, the duty ratios of level 3, $d_{a_3}, d_{b_3}, d_{c_3}$, are obtained from (1) given the fact that the rest of levels are already known. Then, all duties are inserted into the Modulator which sets the switching states f_{i_j} for $i = \{a, b, c\}$ and $j = [1, 5]$ at the switching frequency. Fig. 4 depicts the control strategy followed in this work.

IV. Simulation Results

This section is devoted to present the simulation results of applying such algorithm in the system described in the previous sections. The system parameters together with the control ones are depicted in table II. Note that $V_{C_m}^{P_{\max}}$ for $m = 1, 2, 3, 4$ is given emulating the MPPT output. These values refers to the voltage value of capacitor C_m which

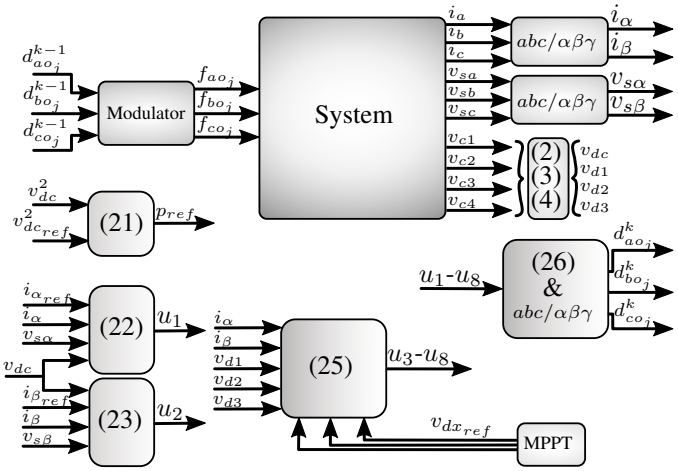

Fig. 4. Schematic diagram of the implemented controller

makes the solar array attached to it to provide the maximum power achievable, which is defined by $P_{C_m}^{\max}$. The solar output power curves (Curve $P-V$) are emulated by parabolas whose maximum point are $(V_{C_m}^{P_{\max}}, P_{C_m}^{\max})$ and the point whose power output is zero differs from one solar array to other in order to simulate different behaviors.

TABLE II
Simulation Parameters

Parameter	Value	Parameter	Value
Sampling	10 KHz	Switching	10 KHz
Grid	50 Hz	v_{si}	230 V_{rms}
L	2 mH	C_1, C_2, C_3, C_4	3300 μF
k_p	15	K_i	15
$k_p^{v_{dc}}$	0.05	$k_i^{v_{dc}}$	3
k_{bal}^p	0.002	k_{bal}^i	0.015
$P_{C_1}^{\max}$	2500 W	$P_{C_2}^{\max}$	2000 W
$V_{C_1}^{P_{\max}}$	260 V	$V_{C_2}^{P_{\max}}$	210 V
$P_{C_3}^{\max}$	1800 W	$P_{C_4}^{\max}$	2350 W
$V_{C_3}^{P_{\max}}$	180 V	$V_{C_4}^{P_{\max}}$	250 V

In order to show the satisfactory behavior of the algorithm, the simulations were carried out initially with $v_{dp_{\text{ref}}} = 0$ and at $t = 0.75\,s$ the values of $v_{dp_{\text{ref}}}$ are updated according to the values of $V_{C_m}^{P_{\max}}$ provided. Figure 5 shows the evolution of the error signals v_{dp} along with their references, where the favorable reference-tracking of the algorithm can be seen. It is also depicted in Fig. 6 how the output power of each solar array improves when the $v_{dp_{\text{ref}}}$-tracking is activated, reaching the established $P_{C_m}^{\max}$ value. To clarify this feature, Fig. 7 depicts the evolution of the capacitor voltages along with $V_{C_m}^{P_{\max}}$.

Regarding the current control and how this algorithm affects it, Fig. 9 shows the three-phase currents at steady state when $v_{dp_{\text{ref}}}$ have been reached, showing it positive performance. The THD value of these currents is $5\,\%$ at steady state and it reaches its worst value equal to $6.5\,\%$ for a brief time immediately after the algorithm is activated. Consider, though, that a dead-time band of $1.1\ \mu s$ is implemented and a simple $\alpha\beta$ current control is used, leaving some room for improvements if a more sophisticated control were used

instead. Finally, Fig. 8 depicts the switching states of phase a in steady state. It can be appreciated that all levels are present except for levels 1 and 5, which, thanks to the selection of d_{γ_j}, each one is omitted the third time of a fundamental period. This graph validates the selection of d_{γ_j} for all levels as saturation and forbidden commutations are avoided.

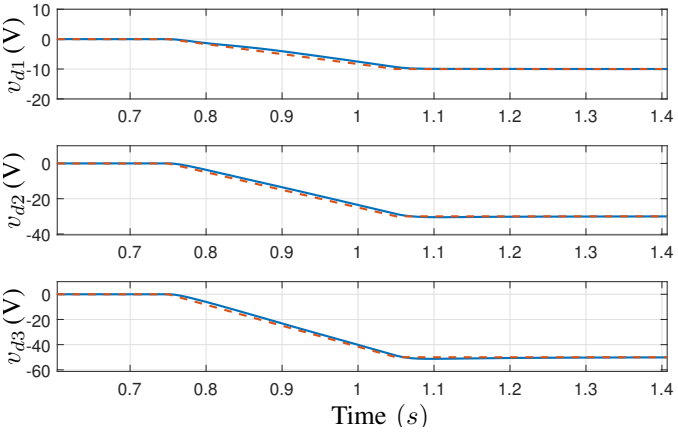

Fig. 5. Evolution of the error signals v_{dx} (solid) and their references $v_{dx_{\text{ref}}}$ (dashed)

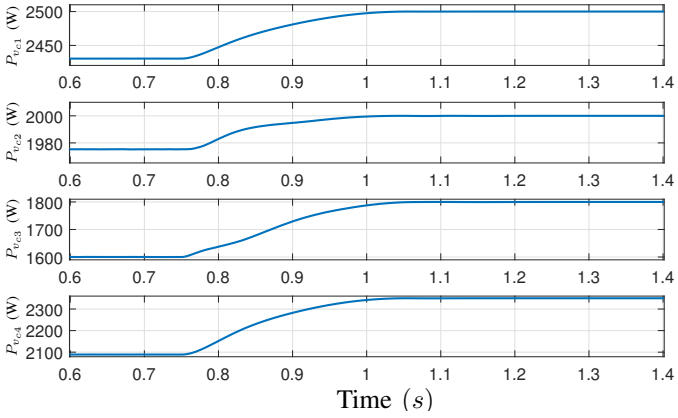

Fig. 6. Output power of each solar array when $v_{d_{\text{ref}}}$ tracking is activated at $t = 0.75\,s$

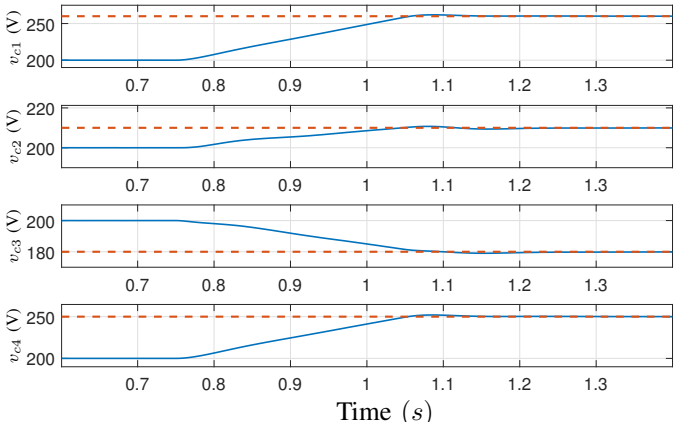

Fig. 7. Capacitor voltage values (solid) and their corresponding maximum output power voltage value (dashed)

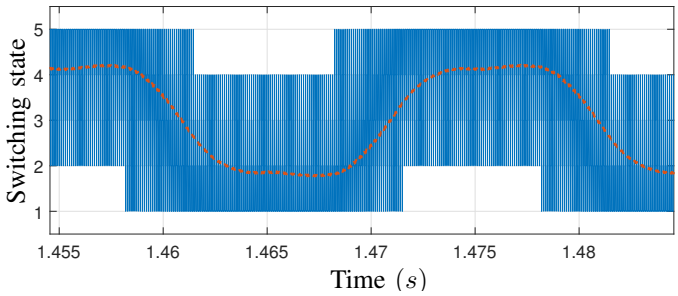

Fig. 8. Switching state of phase a and its filtered signal (dashed)

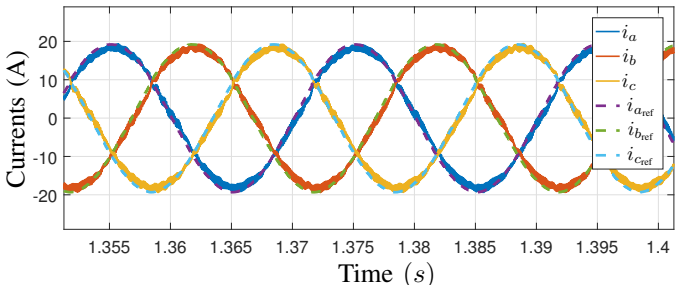

Fig. 9. Three-phase currents (solid) and their references (dashed) at steady state

V. Conclusions

On the whole, this work presents a workaround to interface several solar arrays with the grid using only a five-level NPC Converter. The main advantage of such approach is the reduction of the size and complexity of the system as no dc-dc stage is required between the capacitor side and the solar array. In addition, maximum power point tracking is guaranteed provided an MPPT algorithm set the maximum output power voltage of each solar array, which is a trivial task. Simulations results showed the good behavior of the algorithm and validated its implementation in a real environment.

Acknowledgments

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