Experimental Body-input Three-stage DC offset Calibration Scheme for Memristive Crossbar

Charanraj Mohan*, L.A. Camuñas-Mesa*, Elisa Vianello†, Carlo Reita†, José M. de la Rosa*,
Teresa Serrano-Gotarredona* and Bernabé Linares-Barranco*
*Instituto de Microelectrónica de Sevilla, IMSE-CNM (CSIC, Universidad de Sevilla), Sevilla, Spain
†CEA-LETI, Grenoble, France

***Abstract*—Reading several ReRAMs simultaneously in a neuromorphic circuit increases power consumption and limits scalability. Applying small inference read pulses is a vain attempt when offset voltages of the read-out circuit are decisively more. This paper presents an experimental validation of a three-stage calibration scheme to calibrate the DC offset voltage across the rows of the memristive crossbar. The proposed method is based on biasing the body terminal of one of the differential pair MOSFETs of the buffer through a series of cascaded resistor banks arranged in three stages- coarse, fine and finer stages. The circuit is designed in a 130 nm CMOS technology, where the OxRAM-based binary memristors are built on top of it. A dedicated PCB and other auxiliary boards have been designed for testing the chip. Experimental results validate the presented approach, which is only limited by mismatch and electrical noise.**

I. Introduction

Memristors evolved as a good choice of candidature for artificial synapses in neuromorphic circuits after HP labs proved the physical existence of Chua's finding [1]–[4]. Oxide-based Random-Access Memory (OxRAM) slowly rose to one of the promising synapses in neuromorphic computing systems due to their low-switching energy and high endurance [5]–[8]. The binary OxRAM synapses in a crossbar architecture used in this work are first formed and then switched between Low Resistance State (LRS) and High Resistance State (HRS) by applying a controlled voltage via a series connected MOSFET [9]. To prevent sneak-path currents, a selector MOSFET is connected in series to the OxRAM, leading to the so called–'1T1R' structure as shown in Fig. 1(a) [10].

The filament of the OxRAM is formed by applying a bias V_{TS}= 4 V, 10 μs pulse and gate bias V_{GS}= 1 V, with a recommended compliance forming current of about 1 μA. For a RESET operation, a bias of V_{ST}= 3 V, 100 ns pulse is applied by keeping the gate fully ON (V_{GT}= VDD). For a SET operation, a bias V_{TS}= 2.4 V, 100 ns pulse is applied along with the gate bias, V_{GS}= 1.5 V. For a read operation, a read voltage of V_{TS} or V_{Read}= 0.3 V is applied with a gate bias, V_{GS}= 3.8 V. During inference operation, when read pulses are applied across several memristors, power dissipation becomes critical, which limits the scalability of the crossbar [11]. To overcome this, we need to apply small inference read pulses. Fig. 1(b) shows OxRAM currents for read voltage pulses less than 1 V when LRS= 13.7 kΩ and HRS= 845.9 kΩ. However, applying such small read pulses becomes non-trivial,

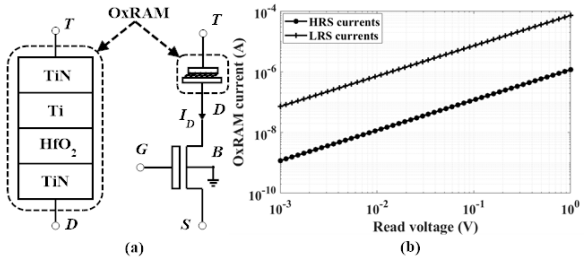

Fig. 1. (a) 1T1R memristive synapse structure (b) OxRAM currents for low read voltage pulses.

when the offset voltage of the system ruins the measurement. Therefore, the opamps used in the read circuit or the opamps used to buffer crossbar lines should be finely calibrated to keep their DC offset voltages as low as possbile. Conventional calibration schemes exist that compensate offset ranges in the order of few mV [12], [13]. However, this is not enough to increase the required scalability in neuromorphic processors. For this purpose, a three-stage DC offset calibration scheme is proposed by varying the bulk voltage of one of the differential pair MOSFETs of the buffer using a cascaded resistor ladder such that, a calibration step less than 0.1 mV is obtained [14]. This paper experimentally validates the proposed calibration approach. The circuits are designed in a 130 nm CMOS technology on which the OxRAMs are built. The calibration scheme can be applied to crossbars of any size irrespective of the type of synapse. Extensive simulations were carried out during design considering several variations such as technology process corner, monte carlo, temperature, noise and parasitic effects of the layout. A PCB is designed for having full control of the calibration scheme and the experimental results validate the proposed calibration approach. The results are only limited by mismatch, electrical noise and other fabrication defects such as nanobattery effect in OxRAM [15].

The rest of the paper is organized as follows: In Section II, the $N \times n$ 1T1R crossbar with calibration of DC offset voltage in each row is described. The three-stage substrate-based calibration scheme is also explained in this section. Section III presents the experimental setup of DC offset calibration scheme. Section IV depicts the experimental results of calibration scheme. Finally, conclusions are drawn in Section V.

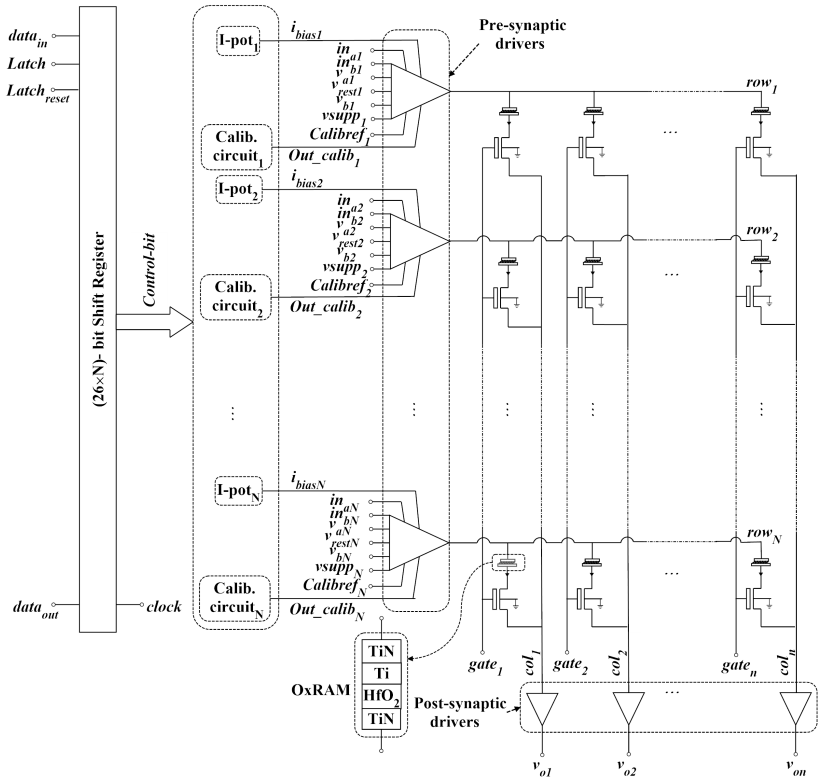

Fig. 2. Conceptual schematic of a $N \times n$ 1T1R crossbar with calibration scheme in each row.

II. $N \times n$ 1T1R CROSSBAR WITH CALIBRATION OF DC OFFSET VOLTAGE IN EACH ROW

Fig. 2 shows an $N \times n$ 1T1R memristive crossbar architecture with calibration of DC offset voltage in each row. Each row has its own pre-synaptic driver. Each pre-synaptic driver comprises an opamp, calibration circuit, pulse-shaping digital block and an I-pot. I-pots are digitally programmable current sources which, from a reference current can provide desired current with high precision, down to pA [16]. I-pots serve as current source biases for the opamps and are controlled by 14-bit control word. Opamps are P-MOSFET based differential two-stage opamps. Each column has its own post-synaptic driver. Each post-synaptic driver comprises an integrator and a comparator.

Fig. 3 shows the three-stage calibration scheme, pulse-shaping digital block and opamp across row_1. A similar schematic exists in each row. The pulse-shaping digital block is used to set three possible biases through digital control. The three-stage (coarse, fine and finer) calibration scheme is a cascade of resistor ladders whose resistor combinations are chosen by selectively turning ON the P-MOSFET switches via decoders. One of the differential pair MOSFET's body-voltage of the opamp is biased with the calibration range between V_{ref} - V_d and V_{ref} + V_d in order to compensate the offset across the rows, while the other MOSFET's body-voltage is biased with $Calibref_{1,2,..N}$. V_{ref} is the calibration reference voltage and V_d is the calibration differential voltage. The calibration scheme is digitally controlled by a 12-bit control word. To serve this purpose, a 26×N-bit edge-triggered D-flip flop based shift register is designed for having full-digital control of the I-pots and calibration schemes of the $N \times n$ crossbar.

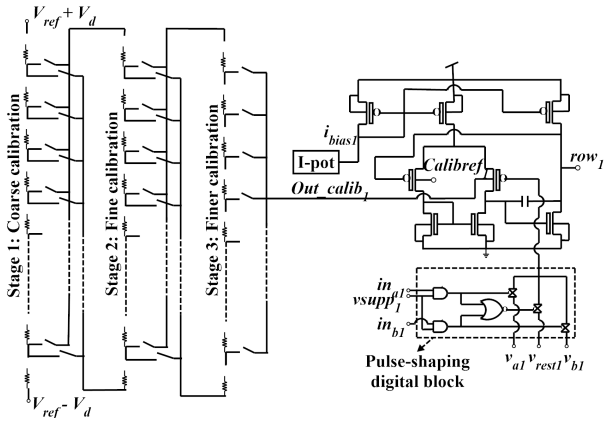

Fig. 3. Three-stage calibration scheme of the opamp across row_1.

III. EXPERIMENTAL SETUP OF DC OFFSET CALIBRATION SCHEME

Fig. 4 shows the experimental setup of the DC offset calibration scheme. It mainly comprises the test PCB which includes the chip under test, a SPARTAN 6 driver board, a button board, a resistor plug-and-play board, a logic analyser and its digital pod. Calibration circuit or scheme is part of the circuits in 'outer-ring' of the chip designed using 130

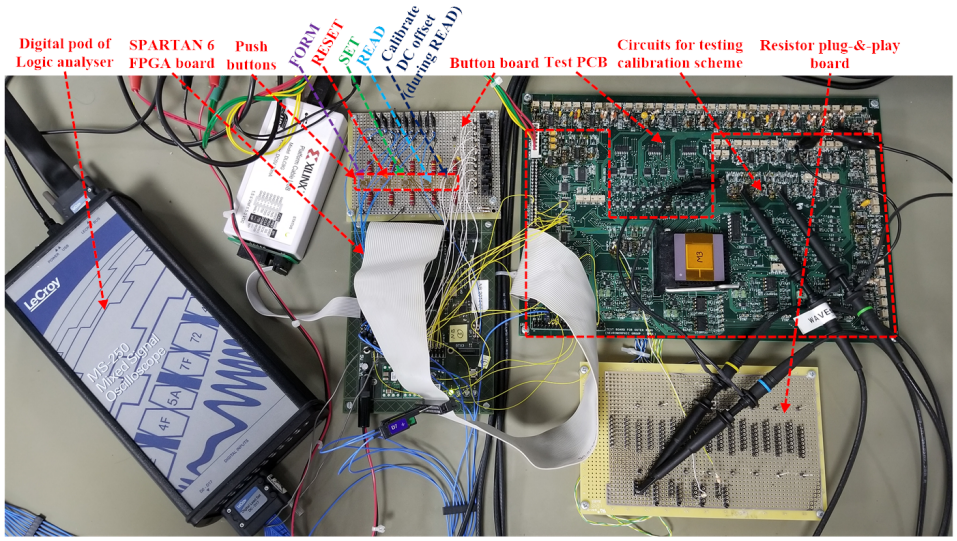

Fig. 4. Experimental setup of the DC offset calibration scheme.

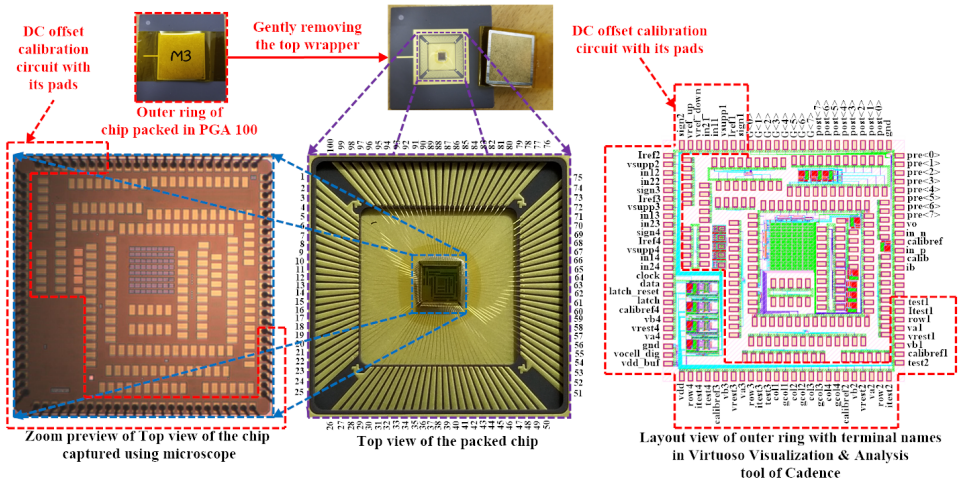

Fig. 5. Different previews of the packed chip with its labelled layout.

nm CMOS technology, which has the OxRAMs integrated above it. The 'outer-ring' of the chip is packed in a 100-pin PGA package, which is connected through a PGA 196-ZIF socket mounted on the test PCB. Fig. 5 shows different previews of the chip packed in PGA100 package with its labelled layout. For testing calibration scheme, a dedicated PCB is made, which mainly comprises components like opamps, level-shifters (3.3 V to 4.8 V), ADC, linear voltage regulator, switches and digital components like decoders, inverters, etc. Opamps on PCB are either used as power supplies opamps or integrating opamps or as comparators. The main purpose of the PCB is to assure desired analog biases at specific terminals of the chip, which are controlled by switches and digital circuits. These switches and digital circuits are further controlled by the SPARTAN 6 driver board. The button board has dedicated buttons to perform OxRAM operations- like FORM, SET, RESET, READ and to calibrate DC offset during READ. It also has jumper arrangements where one can choose the target synapse in a crossbar and also pick the input bit sequence for the calibration scheme. The button board and the SPARTAN 6 driver board are used together for two main purposes: (i) Target a synaptic 1T1R device in the crossbar and perform operations like FORM, SET, RESET and READ through a 3-bit control signal, (A,B,C) and (ii) Set the 12-bit control word for calibration scheme and perform calibration of DC offset during a READ operation.

IV. Experimental Results of Calibration Scheme

This section shows various results of the three-stage calibration scheme implemented in a 4×4 memristive crossbar. Fig. 6 shows a preview of the output screen when row_1 is calibrated when V_{read}= 0.33 V. After forming the targeted OxRAM, a READ operation is performed when A= OFF, B= OFF and C= OFF. Here (A,B,C) is the control signal that is

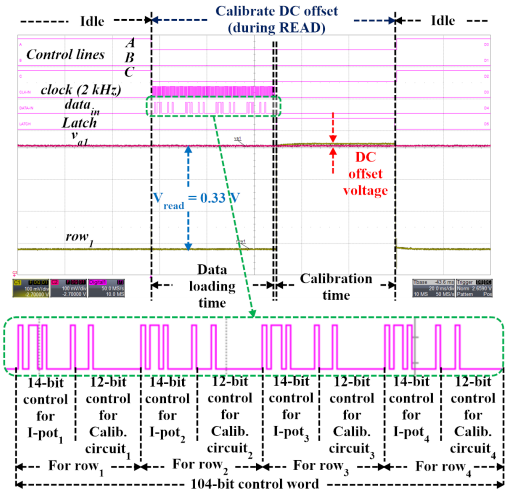

Fig. 6. Preview of output screen when calibrating DC offset across row_1.

used to set specific OxRAM operation. $data_{in}$ is the 26×4= 104-bit control word, which are the control-bits for I-pots and calibration circuits of the opamps in the experimented 4×4 crossbar. Frequency of $clock$ input to shift-register is kept at 2 kHz. Once, the calibration scheme is biased with V_{ref}= 4.5 V, V_d= 15 mV and $Calibref_{1,2,3,4}$= 4.5 V, $data_{in}$ is loaded into the shift-register. Following this, $Latch$ is turned ON and the targeted row is calibrated by varying the 12-bit input calibration sequence using button-board.

Fig. 7 shows the comparison of experimental and simulation results when row_1 of the crossbar is calibrated for DC offset voltage during stage 1 calibration for V_{Read}= 0.33 V. These results are taken by averaging 100 million samples in order to filter out noise, whose standard-deviation is about 200 μV. The power dissipation during inference READ operation is about 0.8 μW for a 4×4 crossbar when using a 50 mV read pulse whose DC offset voltage is finely calibrated. The zero-crossing region in Fig. 7 is targeted and DC offset voltages are calibrated during stage 2 and stage 3 calibration, whose results are shown in Fig. 8 and Fig. 9. Experimental results of the three-stage calibration scheme match simulation results.

V. Conclusions

The experimental results presented in this paper show that it is possible to reduce the DC offset of memristive-array read-out systems below 0.1mV. The proposed approach – based on the use of a bulk-input differential pair – is demonstrated by presented measurements, thus opening doors to increasing the scalability of memristive-based neuromorphic systems thanks to the use of lower pulse amplitudes with the subsequent benefits in terms of power dissipation.

VI. Acknowledgements

This work has been supported in part by the EU H2020 grants 687299 NeuRAM^3, 824164 HERMES, 871501 NeuRONN, 871371 MeM-Scales, by the Spanish Ministry of Economy and Competitiveness (with support from the European RDF) under contracts TEC2015-63884-C2-1-P (COGNET) and by G0086 ICON. Luis A. Camuñas-Mesa was funded by the VI PPIT through the Universidad de Sevilla.

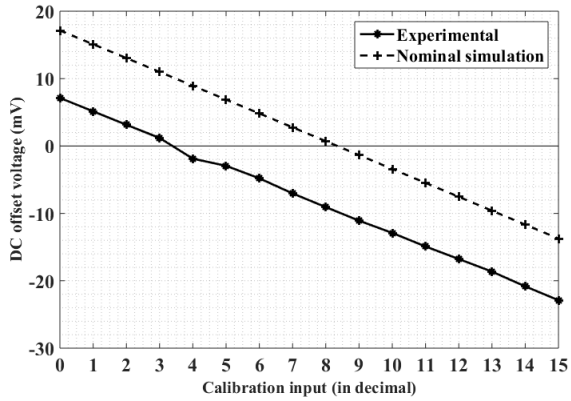

Fig. 7. Comparison of experimental and simulation results during stage 1 calibration of DC offset voltage across row_1.

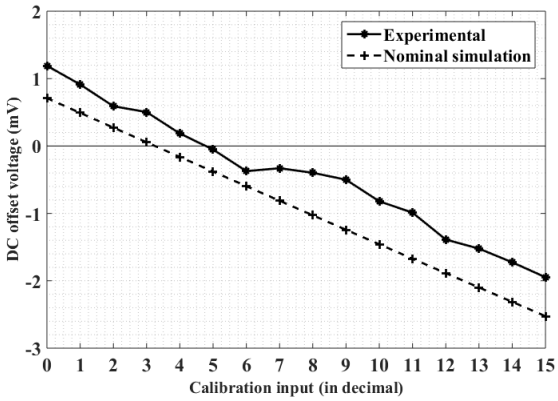

Fig. 8. Comparison of experimental and simulation results during stage 2 calibration of DC offset voltage across row_1 targeting the zero-crossing region.

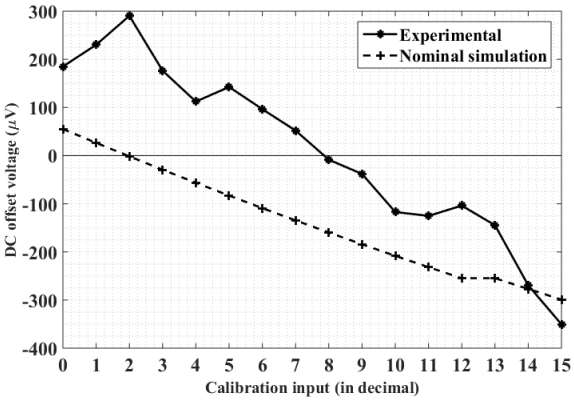

Fig. 9. Comparison of experimental and simulation results during stage 3 calibration of DC offset voltage across row_1 targeting the zero-crossing region.

REFERENCES

[1] L.O. Chua, "Memristor- The missing circuit element", *Transactions on Circuits theory IEEE*, vol. CT-18, no. 5, pp. 507-509, Sept. 1971.

[2] L. O. Chua and S. Kang, "Memristive devices and systems", *Proceedings of the IEEE*, vol. 64, no. 2, pp. 209-223, 1976.

[3] D. B. Strukov, Gregory S. Snider, Duncan R. Stewart and R. Stanley William, "The missing memristor found", *Nature*, 453 (7191), pp. 80-83, 2008.

[4] J. J. Yang, M. D. Pickett, X. Li, D. A. A. Ohlberg, D. R. Stewart and R. S. Williams,"Memristive switching mechanism for metal/oxide/metal nanodevices", *Nat. Nanotechnology*.,3, 429, 2008.

[5] R. Waser, R. Dittmann, G. Staikov and K. Szot,"Redox-based resistive switching memories-nanoionic mechanism, prospects, and challenges", *Adv. Mater*., 21 (25-26), pp. 2632-2663, July 2009.

[6] S. Yu, X. Guan and H. P. Wong,"Conduction mechanism of TiN/HfOx/Pt resistive switching memory: a trap-assisted-tunneling model", *Appl. Phys. Lett.*.,99, 063507-063507, 2011.

[7] Y. M. Kim and J. S. Lee,"Reproductive resistance switching characteristics of hafnium oxide-based nonvolatile memory devices", *J.Appl.Phys.104*, 114115, 2008.

[8] S. D. Ha and S. Ramanathan,"Adaptive oxide electronics: a review", *J.Appl.Physics*., 110, 071101, 2011.

[9] D. Garbin, E. Vianello, O. Bicher , Q. Rafhay, C. Gamrat, G. Ghibaudo, B. DeSalvo and L. Perniola,"HfO_2- Based OxRAM Devices as Synapses for Convolutional Neural Networks", *IEEE Transactions on Electron Devices*.,vol. 62, no.8, pp. 2494-2501, August 2015.

[10] Y. Cassuto, S. Kvatinsky and E. Yaakobi,"Sneak-path constraints in memristor crossbar arrays", *Information Theory Proceedings (ISIT), 2013 IEEE International Symposium on*.,10.1109/ISIT.2013.6620207, October 2013.

[11] E. Chicca,"Neuromorphic Electronic Circuits for Building Autonomous Cognitive Systems", *Proceedings of the IEEE*.,vol. 102, no. 8, pp. 1367-1388, September 2014.

[12] G. Nagy, D. Arbet and V. Stopjakova,"Digital methods of offset compensation in 90 nm CMOS operational amplifiers", in *Design and Diagnostics of Electronic Circuits Systems (DDECS), 2013 IEEE 16th International Symposium on*., pp. 124-127, 2013.

[13] A. J. Gins, E. Peralas and A. Rueda,"Background Digital Calibration of Comparator Offsets in Pipeline ADCs", in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems* ., vol. 23, no. 7, pp. 1345-1349, July 2015.

[14] C. Mohan, L. Camuñas-Mesa, E. Vianello, L. Periniolla, C. Reita, J. M. de la Rosa, T. Serrano-Gotarredona and B. Linares-Barranco,"Calibration of offset via bulk for low-power HfO_2 based 1T1R memristive crossbar read-out system", *Microelectronic Engineering, Elsevier*, vol 198, pp 35-47, 15 October 2018.

[15] Stefan Tappertzhofen, Eike Linn, Ulrich Böttger, Rainer Waser and Ilia Valov "Nanobattery Effect in RRAMs?Implications on Device Stability and Endurance", in *IEEE Electron Device Letters*., vol.35, no. 2, pp. 208-210, 2014.

[16] R. Serrano-Gotarredona, L. Camuñas-Mesa, T. Serrano-Gotarredona, Juan.A. Leñero-Bardallo and B. Linares-Barranco,"The Stochastic I-Pot: A Circuit Block for Programming Bias Currents", *IEEE Transactions on Circuits and Systems-II: Express Briefs*., vol. 54, no. 9, pp. 760-764, September 2007.