A 32 Input Multiplexed Channel Analog Front-End with Spatial Delta Encoding Technique and Differential Artifacts Compression

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***Abstract*—This paper describes a low-noise, low-power and high dynamic range analog front-end intended for sensing neural signals. In order to reduce interface area, a 32-channel multiplexer is implemented on circuit input. Furthermore, a spatial delta encoding is proposed to compress the signal range. A differential artifact compression algorithm is implemented to avoid saturation in the signal path, thus enabling reconstruct or suppressing artifacts in digital domain. The proposed design has been implemented using 0.18 μm TSMC technology. Experimental results shows a power consumption per channel of 1.0 μW, an input referred noise of 1.1 μVrms regarding the bandwidth of interest and a dynamic range of 91 dB.**

***Index Terms*—Brain Machine Interfaces; Analog Front-End; Neural Recording; Artifact Compression; Channel Multiplexing; Spatial Delta Encoding; Artifacts.**

I. Introduction

Neural recording has been one of the most studied fields of neuroengineering in recent years due to its effectiveness in treating neuronal diseases such as epilepsy, Parkinson's or Alzheimer's disease [1]. In addition, the birth and development of interfaces capable of controlling robotic manipulators through the information collected and processed from the brain, known as BMIs (Brain-Machine Interfaces) [2], have also been an incentive for the develop of techniques in neural recording.

BMIs require closed-loop systems that simultaneously stimulate and record information using the same integrated circuit (IC). Therefore, in addition to the characteristics required in any neural recording device [1], [3], such as low noise, low power consumption and small area; it is necessary to tolerate large artifact signals generated by the stimulation pulses. Therefore, we will need systems with larger dynamic ranges. Some techniques to improve the dynamic range of the system are presented in [4], [5], [6].

The evolution of BMIs creates the need for a considerable increase in electrode density, which translates into a significant increase in the number of electrodes used [7]. Traditionally, each of these electrodes is associated with an analog front-end (AFE) for conditioning the neuronal signal. However, the use of a single AFE for all electrodes is an important improvement to continue the evolution of BMIs, specially in terms of area [4].

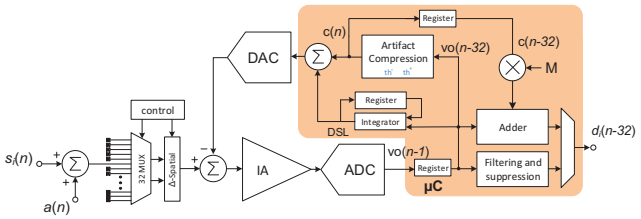

Fig. 1. Block diagram of the proposed circuit.

In this paper, a single AFE that allows the multiplexing of 32 input channels is proposed. In addition, to improve the signal compression range, a spatial delta encoding technique is employed. This technique takes advantage of the spatial correlation between the neural signals [8]. Moreover, a digital-feedback, implemented in a micro-controller, with the differential artifact compression algorithm (presented in [9]), is employed. This digital-feedback also allows us to reduce DC offset from electrodes. Finally, all these features are implemented regarding low noise and low power consumption.

The paper is organized as follows: Section II describes in detail the proposed AFE and the digital blocks. Finally, post-layout results are collected in Section III where a comparison with the current state of the art is also made.

II. Multiplexed Spatial Delta Encoding AFE Architecture

A. System Overview

Fig.1 shows the block diagram of the proposed time-multiplexed 32-channel neural recording analog front-end (AFE). The unshaded blocks have been integrated in an Application Specific Integrated Circuit (ASIC), while the rest of components have been implemented in a Nordic® Semiconductor micro-controller (nRF-52832) which also features a Bluetooth Low Energy communication link. The recording bandwidth is nominally defined in the range between 0.5 and 200Hz, associated to the neural Local Field Potential (LFP) band.

Taking advantage of the low frequency content of LFPs and the large correlation between signals recorded from adjacent

channels [8], the proposed AFE implements input signal time multiplexing and spatial delta encoding. Both operations are digitally controlled on-chip and measurements show -85dB crosstalk between channels. These techniques favor the reduction of area and power consumptions and endow the system with the capability to compress the information processed by the AFE, including artifacts. Moreover, as all the recorded signals pass through the same AFE, structural mismatch problems are avoided [10].

A programmable-gain two-stages low-noise instrumentation amplifier (IA) amplifies the incremental signals from the delta encoder. The IA is able to reject common-mode (CM) artifacts of up to 600 mVpp amplitude. Then, the amplified signals are converted by a fully-differential 10-b Successive Approximation Register (SAR) Analog-to-Digital Converter (ADC) which is oversampled to reduce its quantization-related contribution to the input-referred noise of the AFE.

The system uses two digital feedback loops; one DC Servo-Loop (DSL) for input offset rejection [11] and one differential-mode (DM) artifact compression loop [9] for effectively expanding the dynamic range of the AFE. Both loops use a common 9-bit switched-capacitor based digital-to-analog converter (DAC) for feeding back a combined error signal to the AFE input. A look-up table, represented in Fig.1 by a multiplier with scaling factor M, is used for compensating the transfer function nonidealities of the DAC [4]. The artifact compression loop allows either to reconstruct the input signal including artifacts by means of a weighted adder, or to attenuate DM artifacts by means of a FIR filtering stage [9].

The ASIC of the AFE operates at 1.2V supply voltage and it is driven by a 2.5MHz clock. This clock is internally divided for driving the different blocks. A complete integration of the AFE, including the digital sections of Fig.1, is currently ongoing.

B. Analog Front-End

The 32-channel multiplexer is implemented at the input of a modified parasitic-insensitive Correlated-Double Sampling (CDS) amplifier [12], as shown in Fig. 2 (a). Each channel is subtracted to its adjacent one to perform the spatial delta encoding operation. The first input pair difference ($V_{ref} - V_{in_1}$) is taken as reference for reconstructing the signals, V_{in_i}, $i = 1, \ldots, 32$. The amplifier architecture, besides reducing flicker noise, also improves the common-mode rejection ratio (CMRR), rejecting up to 600 mVpp amplitude. This increase is due to the employment of a feedback topology and the charge redistribution in the input capacitors during ϕ_2 phase. The operational transconductance amplifier (OTA) is implemented by a current reuse topology to achieve a lower noise efficiency factor (NEF) [1]. In addition, a second CDS amplifier is used to increase the overall gain of the system and to feed the ADC input capacitors.

The timing diagram of the AFE is illustrated in Fig. 2 (b). The 10-b SAR requires 13 clock cycles for each conversion: 2 sampling cycles, 10 bit conversion cycles and a final reset cycle [13] [14]. While the ADC is converting, two adjacent

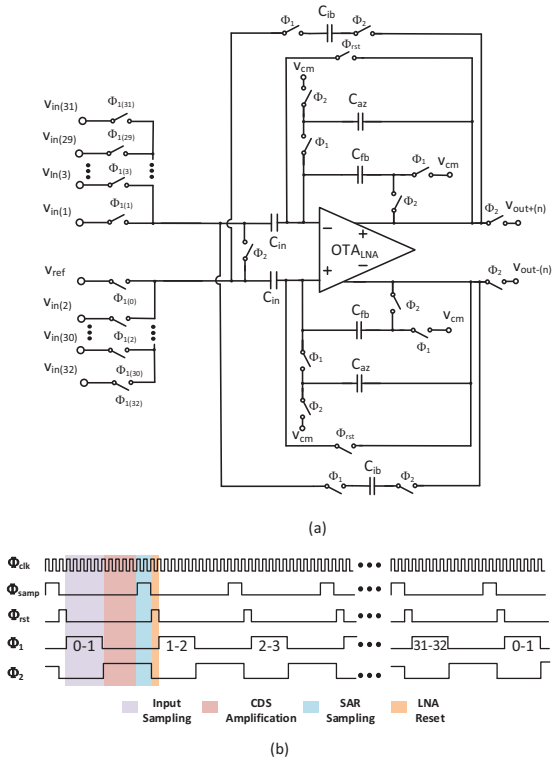

Fig. 2. (a) LNA with input multiplexing and spatial delta encoding. (b) Timing diagram of the circuit.

channels are sampled at the input capacitors of the LNA (Φ_1) and amplified (Φ_2). Once the SAR converter samples the amplified signal (Φ_{samp}), the LNA is reset (Φ_{rst}) for reducing crosstalk between successive channels. Herein, the main clock is divided by the 13 SAR cycles. This sets an operating frequency (192kHz) considerably higher than the LFPs bandwidth (200 Hz), reducing noise folding and allowing time multiplexing. Each channel is sampled every 32 samples, so that the effective operating frequency for each channel is 6 kHz. This frequency is about 16 times higher than the Nyquist frequency for LFPs. Thus, the signal is oversampled with an oversampling ratio (OSR) of 16.

A sampled impedance boosting technique (capacitors C_{ib} in Fig. 2) provides larger input impedance. In this technique, signal current through the loop is injected into the input capacitor at the same phase that the input switch is closed (Φ_1). This way, values of up to $30M\Omega$ on the input impedance of the system are achieved (more than 100 times higher than without impedance boosting). The DC input impedance is also boosted due to the digital feedback [15]. However, we are working to increase this result in an on-going integration.

C. Digital Feedback

Referring to the current input channel pairs ($s_i(n)$ in Fig. 1), the signal after the digital conversion corresponds to the output value of the previous channel pairs ($vo(n-1)$). This value is

stored in a register of 32 positions whose output is the previous output value of the current input channel pairs ($vo(n-32)$). Herein, digital blocks (DSL and artifact compression block) are always working with the output value of the current input signal with a delay of 32 samples (corresponding to the rest of channels). This signal remains compressed (due to spatial delta encoding) for employing smaller digital registers and allowing a faster output transmission.

Differential artifacts demand a digital feedback to avoid saturation states. This digital block performs an artifact compression algorithm [9]. Basically, each time the output voltage exceeds certain threshold values discrete voltage values are subtracted from the input of the IA. This control voltage values proportionally increase/decrease with the amplitude of the signal. Herein, saturation of the signal path is avoided. Finally, artifacts can be reconstructed, by weighted-adding these control values to the output signal or suppressed by low-pass filtering.

Time multiplexing precludes the use of analog large time constant blocks. For this reason, a digital DSL provides the high-pass filter to the circuit. This filter is mainly implemented by an integrator, $a/(z-1)$, where a can be modified to tune the pole of the filter. A 32-position register must be implemented to keep previous values of each channel. This is necessary for the artifact compression and the DSL.

Finally, the output signal is transmitted to a computer through the micro-controller BLE protocol. Here, band-pass filters reduce residual offset and all undesirable high-frequency components, by decimating and filtering. Besides, a sum register completes the reconstruction of each channel signal. The circuit is intended to sense LFPs, however, due to this post-processing filtering, APs (action potentials) can also be recorded.

III. Experimental Results

A prototype including the integrated circuit and the micro controller has been embedded on a printed circuit board (PCB). Experimental measurements have been performed to prove the performance of the proposed topology. These measurements have been carried out introducing the microelectrodes into a phosphate buffered saline (PBS) solution and employing as input a low distortion function generator.

Fig. 3 demonstrates the correct performance of the multiplexing system. Input signals from two adjacent channels are injected into the circuit (Fig. 3 (a)). After spatial delta encoding, amplification and digital conversion, the output signal from the second channel is shown in Fig. 3 (b). Then, this signal is reconstructed and filtered (Fig. 3 (c)). There is a notable difference in the amplitude of both signals (expressed in bits), which also proves the efficiency of the compression due to the spatial delta encoding.

Measured transfer function of the proposed AFE for each channel is shown in 4. The effective low-pass pole is set around 3.1 kHz. Digital DSL provides a high-pass corner at 0.5 Hz. Finally, the system is post-filtered (employing Chebyshev

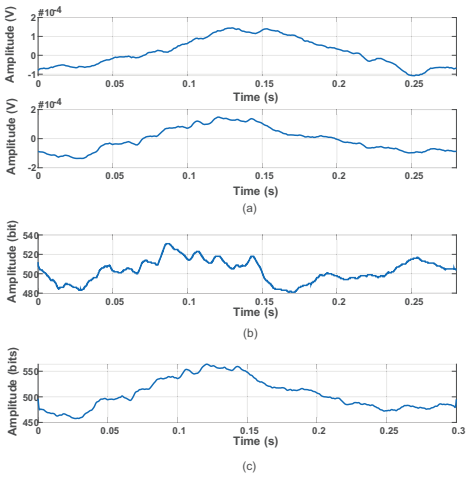

Fig. 3. (a) Output voltages from adjacent channels. (b) Signal from the second channel without reconstruction. (c) Reconstructed signal from the second channel.

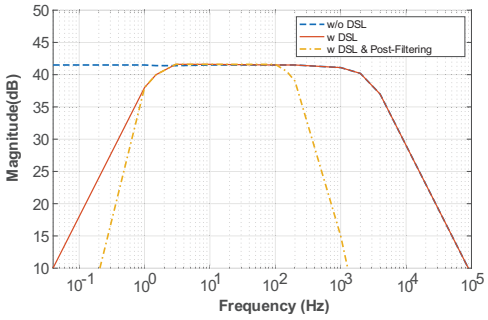

Fig. 4. Different transfer functions of the AFE.

IIR filters) showing an effective transfer function with poles at 0.5 Hz and 200 Hz.

The input referred noise of the IA is illustrated in Fig. 5, with a noise floor around 55 $nV/\sqrt{Hz}$. In terms of noise and distortion, Fig. 6 shows the AFE signal-to-noise distortion ratio (SNDR) as function of the of the input amplitude, with and without artifact reconstruction. DM suppression and reconstruction results have been previously reported in [9], showing the correct performance of this technique. Therefore, for large signal amplitudes, the artifact compression tech-

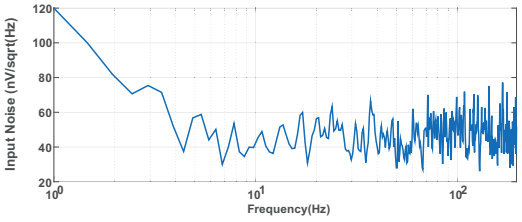

Fig. 5. Input referred noise of the AFE.

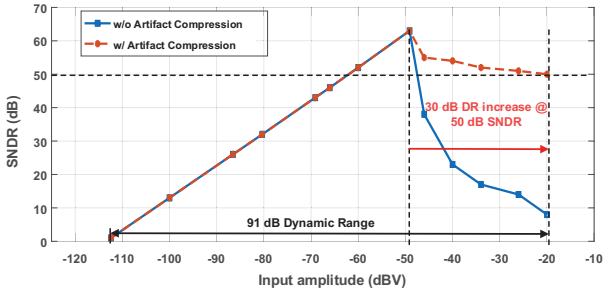

Fig. 6. SNDR as a function of the input amplitude.

TABLE I
STATE OF ART COMPARISON

	Johnson 2017 [15]	Kim 2018 [16]	Smith 2017 [4]	**This Work**
Technology (μm)	180 HV	40	65	**180**
Ch. Power (μW)	8	0.8	2.98	**1.0**
Supply (V)	1	1	2.5	**1.2**
Artifact aware	DM	DM	CM DM	**CM DM***
Multiplexed Channels	-	-	64	**32**
Peak Input (mVpp)	100	200	110	**200**
Ch. IRN (μVrms)	1.6	1	2.98	**1.1**
Ch. NEF/PEF	7.8/60.8	1.81/2.6	3.7/34	**3/10**
Crosstalk (dB)	-	-	-75	**-85**
Ch. Area (mm^2)	-	0.135	0.0023	**0.026****
Bandwidth (Hz)	500	500	1-1k	**0.5-200*****
Dynamic Range (dB)	96	92	91	**91**

* DM compression, no cancellation.
** Only the integrated area.
*** Digital pre and post filtered. Possibility to tune.

nique allows the SNDR to be maintained above 50 dB by reconstructing the signal. Thus, the overall dynamic range is extended up to 91 dB (Fig. 6).

Table I shows the main characteristics of the AFE and a comparison with the current state of the art. Finally, Fig. 7 shows a microphotography of the proposed AFE.

IV. Conclusions

In this paper, an analog front-end capable of multiplexing 32 inputs has been proposed. In addition, the system incorporates a spatial delta encoding technique that increases the data compression rate and the dynamic range of the system. A digital feedback is implemented for further reduction of artifacts and DC offset. All this is done while maintaining state-of-the-art specifications, which is particularly interesting in terms of noise and power consumption.

Acknowledgment

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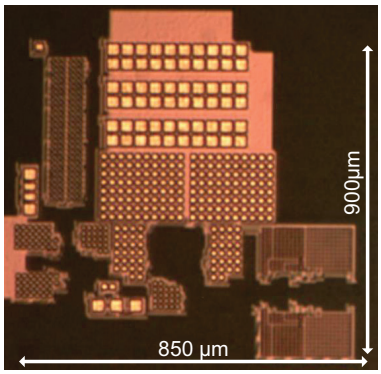

Fig. 7. Microphotography of the proposed AFE.

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