LDO compensation with variable Miller series resistance

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A new compensation method for low dropout (LDO) voltage regulators is proposed, where the series resistor of the conventional Miller compensation changes with the load current to track the variations in the first non-dominant pole.

Introduction: In the context of low dropout (LDO) voltage regulation, a significant number of topologies have been proposed that provide accurate output voltage and fast regulation with low quiescent current and area consumption; most of them are internally compensated. These features make the LDOs appropriate for system on chip devices where integration is a key issue.

In the classical approach (Fig. 1), by assuming a single-stage error amplifier (A_{EA}), the LDO can be considered to be a two-pole system, and the dominant pole compensation can be used. To make an internally compensated LDO, the dominant pole must be fixed by the large pass transistor gate capacitance (C_{GATE}) and the output resistance of the error amplifier. In that case, the non-dominant pole is determined by the output resistance of the LDO (R_{OUT}) and the load capacitor C_{LOAD}. As the load current (I_{LOAD}) becomes smaller, the non-dominant pole of the system moves its position closer to the unity gain frequency (UGF). Therefore, the internally compensated LDO structures suffer from a stability problem due to variations of the non-dominant pole.

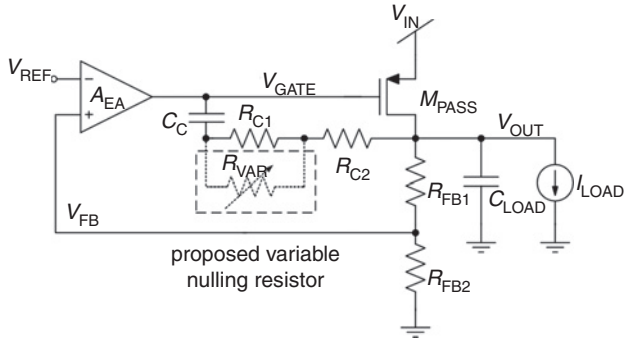

Fig. 1 *Classical topology with Miller compensation and proposed compensation scheme (dotted line)*

In the past few years, different techniques to internally compensate for the LDOs have been proposed. In [1–3], current amplifier Miller compensation was used to reduce the size of the on-chip capacitor. However, the major drawback of this technique is the presence of complex-conjugate poles which may cause instability. Another proposed technique is the so-called damping-factor-control, which was presented in [4]. To deal with stability issues, some authors have used techniques which are traditionally applied to multi-stage amplifiers. For instance, a reverse nested Miller compensation (RNMC) that uses current buffers (RNMCCBs) was presented in [5]. This technique provides two left half plane (LHP) zeros, which are conveniently placed to cancel one of the non-dominant poles and to increase the stability of the system. Nevertheless, the complexity and the power consumption are increased.

Another solution found in the literature is the split-length compensation [6] that is accomplished by splitting the length, L, of a single transistor into two shorter transistors with $L1$ and $L2$ lengths. This configuration allows the use of one of those transistors as a CB, thereby reducing the size of the compensation capacitance. However, the major drawback of this technique is an increment of the dropout voltage. Furthermore, the compensation capacitor must be larger than that of a Miller capacitance.

Another approach [7] uses a pole-zero tracking technique to cancel the first non-dominant pole. A load-dependent zero is added to maintain the UGF constant. However, in order to obtain a robust solution, an exhaustive design is required to cancel out the output pole.

From the techniques explained above, those which are able to manage a zero-load current [2–4] without disturbing the stability require a high quiescent consumption, thus decreasing the efficiency of the regulator. In addition, they suffer from a lack of robustness.

Proposed compensation: In this Letter, a novel compensation scheme based on a variable Miller series resistance to stabilise an LDO is proposed. This scheme is proven to be a robust technique that maintains the voltage regulator stable even for a zero-load current, at constant quiescent power consumption for the whole I_{LOAD} range.

As is well-known, the Miller compensation introduces a right half plane (RHP) zero due to the feed-forward path formed by the compensation capacitance C_C. This zero can be moved to the LHP by choosing an appropriate value for the nulling resistor R_C. To achieve a good compensation in the full load range, the Miller compensation is first optimised for a zero-load current:

$$H(s) \simeq \frac{-A_0\left(1+\left(s/z_1\right)\right)}{\left(1+\left(s/p_1\right)\right)(1+as)} \tag{1}$$

$$a \simeq R_C C_{gd} + \frac{C_L}{gm_{pass}}\left[1+\frac{R_C}{R_2}\right] \tag{2}$$

$$z_1 \simeq \frac{1}{R_C C_C} \tag{3}$$

$$p_1 \simeq \frac{1}{gm_{pass} R_{OUT} R_{OUT,EA} C_C} \tag{4}$$

A high value for R_C will be required to move the RHP zero position closer to the UGF, which provides a good phase margin. Nevertheless, when the I_{LOAD} increases, the non-dominant pole will move to a high frequency whereas the zero (3) remains unchanged. This will lead to a shift of the UGF to a high frequency, thereby drastically reducing the phase margin. This problem can be solved, by decreasing the R_C value that pushes the zero to a high frequency. Since a critical pole-zero tracking is not required, the proposed technique proves to be robust against the process and the mismatch variations.

In a practical implementation (dotted line in Fig. 1), the R_C resistor is split into three resistors. R_{C1} is optimised to guarantee the stability of the LDO for the zero-load current. A second resistor, R_{VAR}, is placed in parallel with R_{C1}, which is a variable resistor implemented by a transistor (M_{P2}) in the ohmic region whose value is controlled by the gate voltage (V_{GATE}) of M_{PASS} (and, in turn, by the output current). Finally, R_{C2} is a small resistor that ensures a LHP zero for any value of R_{VAR}.

The M_{P2} resistance is controlled by the circuit in Fig. 2, where M_{P1} and I_{BIAS} represent a replica of the output branch, A_1 is a large gain differential amplifier which fixes the V_{REF_GATE} to the gate voltage of the M_{PASS} transistor for the $I_{LOAD} = 0$ (i.e. V_{COMP} in Fig. 2 is given by the value of V_{FB} in Fig. 1 for $I_{LOAD} = 0$); A_2 is a low gain differential amplifier which drives the gate voltage of the variable resistor M_{P2}. Note that the M_{P2} resistance does not follow a precise variation, as the proposed technique does not require an accurate pole-zero tracking.

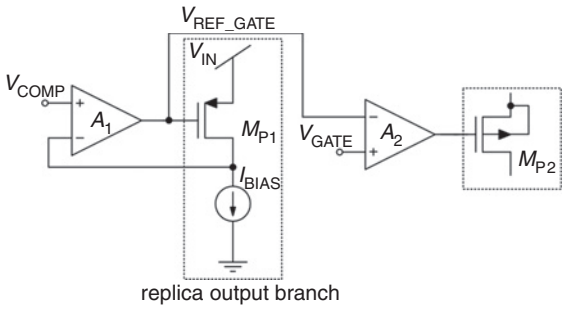

Fig. 2 *Control loop of variable resistor*

Simulations results: The proposed compensation scheme has been implemented in a standard 65 nm CMOS technology with $V_{THP} = -0.4$ V and $V_{THN} = 0.575$ V for the PMOS and the NMOS transistors, respectively. V_{IN} is set to 1 V and the maximum load current value is 100 mA.

Table 1 shows the variation of the phase margin with respect to the load current. In the first column, the phase margin with a classical Miller compensation using a zero nulling resistor (ZNR) optimised for the maximum output current is represented whereas the second column shows the phase margin of the proposed compensation scheme.

Table 1: LDO phase margin simulations, nominal corner

Phase margin LDO compensation scheme (°)					
I_{LOAD} (mA)	Classical ZNR (°)	Proposed scheme (°)	I_{LOAD} (mA)	Classical ZNR (°)	Proposed scheme (°)
100	95.33	106	0.1	18.4	113.6
10	63.3	122.7	0.01	28.77	65.76
1	30.53	124.7	0	57.44	56.5

As can be inferred from Table 1, when a static value of the nulling resistor R_C is used, the zero is located in a fixed frequency. This value is acceptable when the load current is low. However, when the I_{LOAD} increases, this zero will move the UGF to higher frequencies, providing a drastic reduction of the phase margin. The proposed scheme solves this problem, allowing a full working range, as shown in Fig. 3.

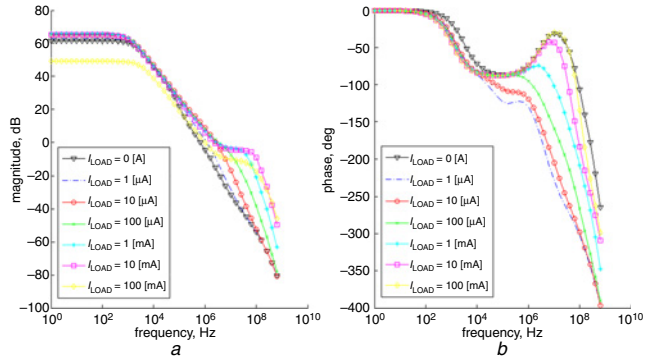

Fig. 3 *Frequency response with V_{IN} = 1 V and different I_{LOAD} values*

In Fig. 4, Monte Carlo simulations are shown where both the process variations and the mismatch are taken into account. These simulations have been performed for $I_{LOAD} = 0$ and $I_{LOAD} = 1$ mA at $V_{IN} = 1$ V.

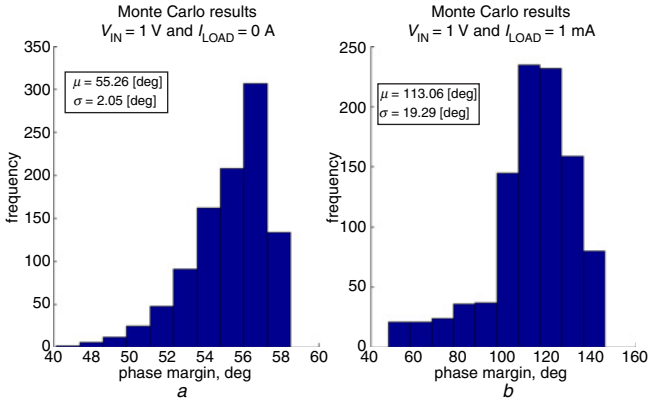

Fig. 4 *Monte Carlo simulations for V_{IN} = 1 V and I_{LOAD} = 0 A and I_{LOAD} = 1 mA*
a $I_{LOAD} = 0$ A
b $I_{LOAD} = 1$ mA

Conclusion: A new compensation scheme for the internally compensated LDOs has been proposed which uses a classical Miller compensation with a variable nulling resistor. Decreasing the nulling resistor when the output current increases provides a large enough phase margin in a wide load current range, maintaining the stability of the LDO even for the zero output current. Resistor tuning based on a replica circuitry is used to provide robustness against the mismatch and the process variation.

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One or more of the Figures in this Letter are available in colour online.

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