An Academic Approach to FPGA Design Based on a Distance Meter Circuit

Carlos Jesús Jiménez-Fernández, Carmen Baena Oliva, Pilar Parra Fernández, F. Eugenio Potestad-Ordóñez, and Manuel Valencia-Barrero

***Abstract*— Digital design learning at Register Transfer (RT) level requires practical and complex examples as learning progresses. FPGAs and development boards offer a suitable platform for the implementation of these designs. However, classroom practice sessions usually last two hours, which does not allow the complexity of the designs be high enough. For this reason, interesting designs that can be made in several sessions are required. In this paper, the construction of a distance measuring system is presented. For this purpose, a distance measurement module based on ultrasound is available, the results are displayed in 7-segment displays on a Nexys4 board. This approach has been applied to three Electronic subjects at the University of Seville. The degree of satisfaction on the part of the students as well as the result of the evaluation of the experience by the teachers involved are shown.**

***Index Terms*— Active learning methodologies, project based learning (PBL), VHDL, digital systems design, distance meter, field programmable gate arrays (FPGA).**

I. Introduction

THIS contribution is an extension of the article presented at the congress TAEE2018 [1] having been chosen by the organizing committee as one of the three best papers of the conference. The article deals with the design of a digital system in the laboratory sessions of the subject Advanced Digital Design [2] of the Degree in Industrial Electronics. In this extension the methodology used is justified in a more detailed way, more information is included on how the design of the system is carried out, a new figure has been incorporated to clarify some aspects of the design. A new section (IV) has also been included with the data relating to the evaluation of the results obtained in the actual implementation of the proposal. This refers to the reception by the students, the difficulties encountered in the development of the activity and the assessment made of the experience as a whole.

In addition to the theoretical contents, which are essential to acquire basic knowledge in any subject, in electronic subjects, and even more in engineering degrees, it is essential to complement them with the development of practical skills. Training at a practical level allows the achievement of multiple objectives. On the one hand, the development of transversal skills such as group work or communication and presentation of results is achieved. On the other hand, the motivation of students when doing practical work is higher, which facilitates the learning process and the strengthening of concepts acquired at a theoretical level. Also, the use in the laboratory of commercial design tools at both software and hardware level allows students to connect with their professional future. Practical training also allows students to acquire the ability to solve problems autonomously.

The application of a methodology based on active learning which in some cases takes the form of project-based learning (PBL) facilitates this task [3]–[6]. There are many examples in the literature of the application of this methodology that is carried out at several university grades [7]–[11].

The proposal is to apply these methodologies in digital design subjects that are taught in advanced courses of electronic qualifications. In them you can use hardware description languages for the description of circuits. Besides, FPGA devices are used as a platform to experimentally test the behaviour of designed circuits. This methodology has many advantages. One of them is the use of a single CAD environment for the design, verification and programming of devices. In addition, this software is offered free of charge for educational use by FPGA manufacturers. Another advantage is the availability of development boards, which include the FPGA, displays and interface elements that allow to enter values to the inputs and see results on the outputs. For all these reasons, teaching digital design with the VHDL-FPGA tandem is an alternative at an acceptable cost and, above all, very practical and highly attractive for students.

This alternative is being applied in the course Advanced Digital Design, an elective in the fourth year of the Degree in Industrial Electronics at the Polytechnic School of the University of Seville. The aim of this course for students is to learn the most important concepts of digital design. The only prerequisites for this subject are the subjects Industrial Electronics and Digital Electronics, both in the second year.

This work was supported in part by the CESAR Project under Grant TEC2013-45523-R, in part by the INTERVALO Project under Grant TEC2016-80549-R, and in part by the LACRE Project under Grant CSIC 201550E039. *(Corresponding author: Carlos Jesús Jiménez-Fernández.)*

Carlos Jesús Jiménez-Fernández, Carmen Baena Oliva, Pilar Parra Fernández, and Manuel Valencia-Barrero are with the Departamento de Tecnología Electrónica, Universidad de Sevilla, 41011 Sevilla, Spain, and also with the Instituto de Microelectrónica de Sevilla, 41092 Sevilla, Spain (e-mail: cjesus@imse-cnm.csic.es; baena@imse-cnm.csic.es; parra@imse-cnm.csic.es; manolov@imse-cnm.csic.es).

F. Eugenio Potestad-Ordóñez is with the Instituto de Microelectrónica de Sevilla, 41092 Sevilla, Spain (e-mail: potestad@imse-cnm.csic.es).

The subject Industrial Electronics is a subject of the common training block of the industrial branch, taught in the first term of the second year. It is the first subject that students have in this degree related to electronics. The contents of this subject [12] basically consist of an analogue and a digital block. In the digital block, the basic concepts of digital electronics are introduced, from switching algebra to the design of state machines, through the concepts of logic gates and flip-flops.

The subject Digital Electronics is a compulsory subject in the degree curriculum. It is taught in the second term of the second year. Its contents [13] develop those initiated in Industrial Electronics. They include the real features of logic gates and flip-flops, analysis and design of digital circuits (both combinational and sequential) and combinational and sequential subsystems. The latest topics in the course introduce concepts related to design at RT level (circuit structure based on control unit and data unit), Algorithm State Machine charts and basic microprocessor principles.

With this previous knowledge on the part of the students, in the course Advanced Digital Design they are taught the description of digital circuits using the VHDL hardware description language and the way to implement them on FPGA devices (in this case Xilinx). The subject is approached in a very practical way, so that the students design small circuits in the laboratory sessions. As the subject progresses, these laboratories increase in complexity, but in the time allotted to the laboratories (a maximum of two hours) there is no time to carry out designs that have a minimum complexity.

One solution to this problem is the realization of a design in several sessions. But for this solution to be interesting it must have several characteristics: on the one hand, each part must be self-contained (it must have a design objective that can be achieved in a laboratory session) and, on the other hand, it must involve a gradual construction of the functionality to be achieved.

In this paper a set of four laboratory sessions to build a distance meter is presented. To this purpose, an ultrasonic distance measuring device, a set of 7-segment displays to show the result, as well as a sound element that beeps more frequently as the obstacle is closer are used. This proposal is highly motivating for students because of its relation to a real application: the obstacle detector in the reverse of vehicles.

The structure of this communication is as follows: the second section briefly explains the design to be carried out. Section III details the contents and objectives of each of the sessions into which the design has been divided, as well as the results to be obtained. In Section IV the results obtained after the application on different groups of students are presented. Finally, some conclusions are drawn.

II. Design to Be Developed

The aim of the proposed set of laboratory sessions is to design a distance meter based on a commercial device. It is the HC-SR04 [14] (Fig. 1) which, by means of ultrasound, is capable of measuring distances within a given range. The measures must be presented in 7-segment displays. In addition,

Fig. 1. Distance Meter HC-SR04.

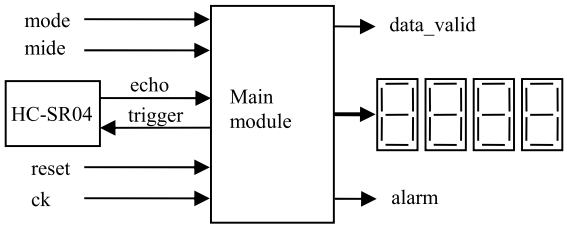

Fig. 2. Block diagram of the measuring system.

when the distance is less than a limit, sounds are emitted as a proximity warning.

The system must incorporate two operating modes: continuous mode and unitary mode. In continuous mode, the system will permanently activate the distance meter and display the measurements continuously. However, in unitary mode, the system will perform a single task each time the corresponding command is given.

The realization of the complete system involves the development of several additional elements such as code converters and a control unit that will be part of what will be the main module of the system.

In the block diagram of the measuring system (Fig. 2), the connection between the HC-SR04 module, the main module and the 7-segment displays is shown. With respect to the external inputs of the system, in addition to the reset and *ck* signals, the mode signal is displayed, which allows the user to choose between the two operating modes (unitary and continuous) and the *mide* signal which activates the measurement operation in the unitary mode. As for the outputs, *data_valid* informs that the data shown on the displays already contains the measured distance and alarm is a signal that is activated when the distance to the obstacle is within a predefined range. This signal may control a module to obtain an acoustic signal of variable frequency.

The main module interacts with the HC-SR04 module through two signals, one input to the distance meter (*trigger*) and one output (*echo*). After receiving a pulse at the trigger input, the meter emits an ultrasonic signal and waits to receive the returned signal after hitting the obstacle. During this waiting time the meter generates a positive pulse for the *echo* output that will be proportional to the distance to be measured (Fig. 3). This distance is within a range between 2 cm and 4 m.

The main module is composed of a control unit, maxsonar_control, and a binary to 7-segments code converter. The control unit is in charge of supplying the trigger signal to the

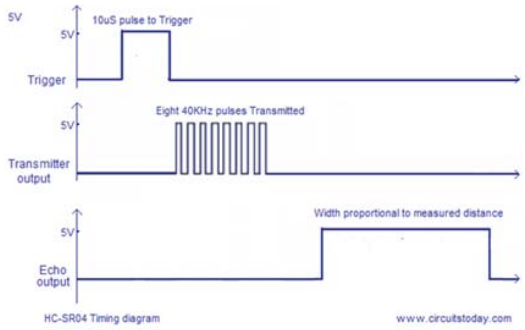

Fig. 3. Distance meter HC-SR04 operation.

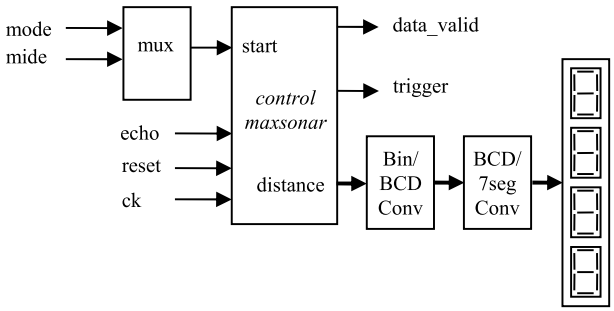

Fig. 4. Block diagram of *max_sonar* system.

distance meter and evaluating the output echo to obtain the distance to the binary object as well as activating the alarm signal. The code converter receives the result of the distance and supplies it to the displays. This distance must have an accuracy of 0.25 cm.

The complete system is designed by the students in four sessions. First, the unit control_maxsonar is designed and simulated (Lab1). Subsequently, in Lab2, the HC_SR04 meter is emulated by VHDL code. This makes it possible to have randomly timed echo signals and to simulate distance measurements. In Lab3, the entire system is brought to the board. To do this, the main module is finished by adding the converter and removing the emulator of the distance meter, since the main module can now interact with the real meter. Finally, in Lab4 the main module is completed with the alarm output that will be connected to a buzzer.

III. Development of Laboratory Sessions

In this section, each of the sessions into which the design has been partitioned are detailed.

A. Session 1 (Lab1)

In Lab1 the control unit, *control_maxsonar*, is created. It has the following inputs and outputs.

Regarding the inputs: a clock signal *ck* of 100 MHz coming from the development board, an asynchronous reset signal (*reset*), a distance measurement start signal (*start*) and the *echo* signal coming from the measuring module. As for the outputs: a *trigger* signal that activates each measurement and will be connected to the measuring module, an output bus that shows the value of the measured distance (*distance*) and a signal that indicates the validity of this measurement (*data_valid*) (see the *control_maxsonar* block in Fig. 4).

The tasks to be performed by this module are as follows:

- Generate a pulse at the *trigger* output each time the *start* signal is activated. Since *trigger* will be connected to the measuring module, it must be ensured that it complies with the specifications of this module (it must be greater than 10 μs) (Fig. 3). *Data_valid* signal must also be activated when the distance measurement process is completed.
- Measure the time while the signal *echo* is 1. For this purpose, a frequency signal suitable for the accuracy of the measurement will be used, which in this case is 0.25 cm. To this end, a Xilinx IP block is incorporated into the design to divide the input frequency that is excessive (100 MHz). With the divided clock the number of cycles that the signal *echo* is 1 will be counted being this the measure of the distance in quarters of a centimeter.

The design must be done using a state machine complying with the synthesis restrictions. A testbench must also be created to simulate the functionality of the designed module.

The student must determine the period of the divided clock signal. This period must be 58/4 us (f = 68.96 kHz) since, according to the specifications of the distance meter, pulses of 58 us correspond to distances of 1 cm. They must also calculate the number of bits needed for the output distance as a function of its upper limit (400 cm) and the required accuracy. In this case, 11 bits will be needed, 9 for the integer part and two for the fractional part.

To satisfy these requirements, the IP block to be incorporated is a configurable module. This is a challenge for students, as this is the first time they use this type of module. It is a counter that operates at 100 MHz, and the student must give the module of the counter as a parameter. Specifically, for the clock frequency needed (68.96 kHz), the module of the counter must be 1450. The most significant bit of this counter will oscillate at the required frequency. This signal will not have a duty cycle of 50% since it is not a complete counter (module $\neq 2^k$). This fact is a novelty for students who are used to balanced clock signals.

In order to count the number of cycles that the *echo* signal is at 1 (distance in quarters of a centimeter) a module 2^{11} counter is incorporated into the design with a count enable signal that will be controlled by the *echo* signal (Fig.5).

B. Session 2 (Lab2)

In Lab2 a functional model of the distance meter is designed. This will allow us to test the proper operation of the meter-*control_maxsonar* set by simulation before moving on to the test with the real meter and the board.

Once the simulation is successfully completed, the students can use the Nexys4 [15] development board along with the real distance meter to perform the experimental tests. For the connection between both of them it is established that the *trigger* output and the *echo* input of the control are connected

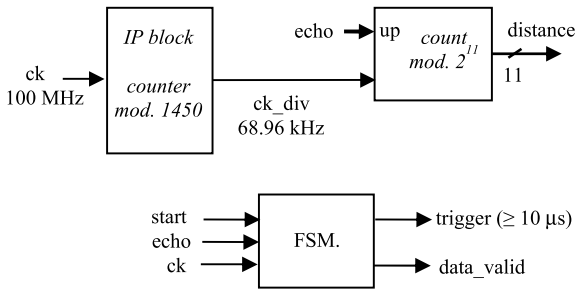

Fig. 5. Block diagram of *control_maxsonar*.

to specific pins of the board. The *ck* signal must be connected to the 100 MHz clock of the board, the *reset* signal and the *start* signal to pushbuttons, the distance output to a set of leds and, finally, the *data_valid* signal also to another led.

To test the set, the student must activate the *reset* and then activate the *start* using the pushbuttons, wait for the led associated with *data_valid* to switch on and interpret in binary the value of the distance shown on the leds.

C. Session 3 (Lab3)

In Lab3 a block called *maxsonar_system* is designed. This contains the previously developed *maxsonar_control*, a binary to 7-segments converter for the output distance and an additional circuit that is simply a multiplexer (mux) to control the *start* signal depending on the *mode* and *mide* inputs.

For the conversion system, instead of designing a binary/7-segment converter, the aim is to reuse two designs that the student developed in previous practices. These are a binary/BCD converter with 13 input bits and 16 output bits and a 4-digit BCD/7-segment converter. With this, the student incorporates previous modules and practices common techniques in the bottom-up design methodology.

Since in the *control_maxsonar* design only 11 bits are used to encode the distance output, the two most significant bits of the converter input will be set to 0. Since the converter works with integers it is necessary to represent the distance with 9 bits after a rounding process of the fractional part.

The fact of having a converter that admits 13 bits in its input allows, with small modifications in the *control_maxsonar* module, to change the number of bits destined to measure the distance if you want to work with a meter that has a greater range in the measure. This modification is limited to the cycle counter of the clock *ck_div*, which instead of module 2^{11} would become module 2^{13}.

The block diagram of the *maxsonar_system* is shown in *Fig. 4.*

To test the operation of the system on the development board, the same pins used in Lab2 will be used for *echo* and trigger while the input *mide* and *mode* will be connected to a pushbutton and a switch respectively.

D. Session 4 (Lab4)

In Lab 4 the design is completed by adding the *alarm* output. The purpose of this output is to generate a sound signal

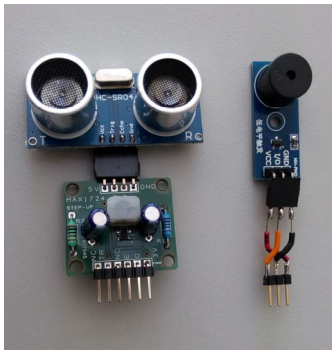

Fig. 6. Distance meter (left) and buzzer (right).

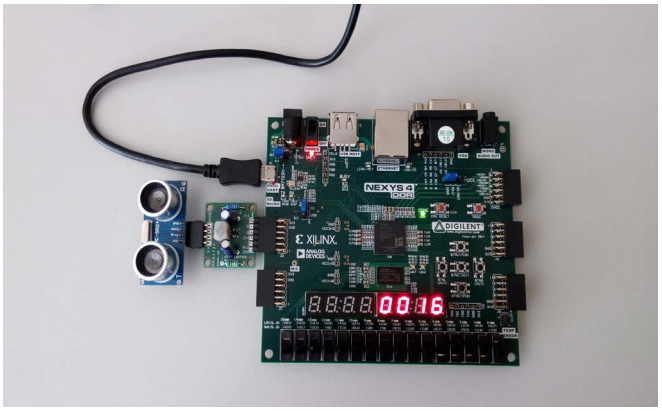

Fig. 7. Development board and meter. Results after Lab3.

that indicates the proximity to an object. To do this, there is a buzzer to which the *alarm* output is connected. The operating mode is as follows: for the buzzer to be off, the *alarm* output must be set to 1 and to be on, it must be set to 0.

Four cases will be considered depending on the distance to the object:

- If the distance to the object is between 100 cm and 75 cm, short but distant beeps will occur.
- If the distance value is between 75 cm and 50 cm the beeps will be slightly longer and less distant.
- If the distance to the object is between 50 cm and 25 cm, the beeps will be even less distant.
- Finally, if the distance is less than 10 cm, the beep must be continuous.

To achieve these objectives, the student must modify the previous code, program the board and then check the operation of the entire system.

IV. Evaluation of the Experience

This section presents some images taken after the project was carried out in the laboratory and analyses the degree of satisfaction with the experience from both the point of view of the student and the teacher.

The Fig. 6, 7 and 8 show images obtained in the laboratory. Fig. 6 shows the modules that are connected to the development board: the HC_SR04 distance meter and the buzzer used to generate the sound signal. The other two images

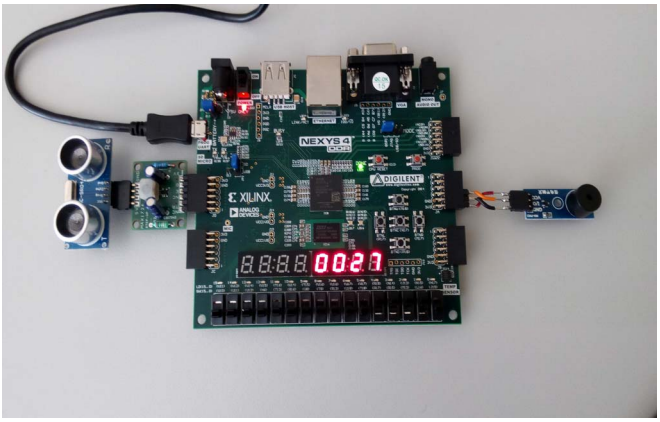

Fig. 8. Development board, meter and buzzer. Results after Lab4.

(Fig. 7 and Fig. 8) correspond to photographs taken in the laboratory to illustrate the result achieved by the students after finishing the last sessions. Specifically, Fig. 7 is the result of Lab3, where the distance to the object is shown in the four 7-segment displays and Fig. 8 corresponds to the result obtained after the completion of Lab4 since the buzzer module is incorporated.

With regard to the degree of satisfaction after the accomplishment of these practices, this is very high. From the student's point of view, this is true although it is an optional subject and the level of demand is quite high in comparison with other subjects of this type. At the end of the course, the students must complete a test in which, among others, two questions appear: "what would you not remove from the course?" and "would you recommend the course to another student?" In the answer to the first of the questions, there is an almost unanimous opinion that the practical work carried out in the laboratory should not be eliminated. Some students also show their predilection for those sessions in which designs are implemented on boards instead of sessions that are limited to simulation. And when it comes to the question of whether you would recommend the subject to other students, there is also an almost unanimous answer that they would. Some students add a comment that the subject requires a much greater effort than other optional subjects, so they would not recommend it if you are looking for a subject that requires little effort, but they would if you want a motivating subject that raises an objective connected with reality and that represents the achievement of an interesting challenge.

From the teacher's point of view, the difficulties encountered during the development of the experience have been analyzed. Firstly, it is necessary to comment the difficulty that appears in the second Session. In this Session, a design that emulates the behavior of the distance measuring module that provides a random value as measured distance is asked. This block is useful to verify the developed system. As this module will not be synthesized, because the real meter is available, all constructions of the VHDL standard can be used, even those that are not synthesizable. It is the only time that they make a design of this type and it is difficult for them to understand it. In many cases they try to make the module following the recommendations of the synthesizable designs and, although it can also be done in this way, the design is greatly simplified using non-synthesizable constructions and functions.

Secondly, the realization of a design in several sessions has the disadvantage that not all students advance at the same pace. There are students who do not reach the goal set in the time stipulated for a session. In these cases it is necessary to allow these students to finish the design in the next laboratory session.

For this reason, it has been proposed to introduce an additional session that will allow all students to complete the work. Those students who have done the work in the four sessions will use this additional session to make modifications to the design that may be interesting, for example, eliminating the bounces on the button.

Teacher satisfaction is also very high. On the one hand, the motivation and interest shown by the students contribute to this, as well as being able to achieve objectives of greater complexity than those allowed by the practice sessions when they are not connected to each other. On the other hand, it is interesting to be able to reuse modules designed in sessions prior to the project presented, such as, in Session 3 with the BCD/7-segment code converter.

V. Conclusion

With this set of laboratory sessions, the students face a design of medium-high complexity splitting it into simpler designs. Furthermore, each of the parts into which the design has been partitioned corresponds to a single laboratory session. In addition, in each session the complete design process is incorporated, i.e. the writing of the VHDL code, debugging of errors, writing of the stimulus file (*testbench*) that allows functional simulation and, where appropriate, implementation on the board and experimental testing. Finally, the evaluation of the experience carried out has shown a high degree of acceptance by both students and instructors.

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