# OPTIMIZATION TECHNIQUES FOR DYNAMIC BEHAVIOR MODELING OF DIGITAL CMOS VLSI CIRCUITS IN NANOMETRIC TECHNOLOGIES*

*Alejandro Millan, Manuel J. Bellido, Jorge Juan*

Instituto de Microelectronica de Sevilla (CNM-CSIC)
Av. Reina Mercedes s/n (Edificio CICA), 41012 Sevilla (Spain)

Departamento de Tecnologia Electronica (Universidad de Sevilla)
Av. Reina Mercedes s/n (ETS Ing. Informatica), 41012 Sevilla (Spain)

Tel.: +34 954556161 - Fax: +34 954552764
E-mail: {amillan, bellido, jjchico}@dte.us.es

**ABSTRACT**

In the field of logic simulation, the constant advance of technology influences remarkably in the circuits dynamic behavior. Our main aim is to increase precision of logic simulators by taking into account this influence. This task has two main objectives: (a) developing a model for logic gates that unifies the functional behavior and the dynamic one and (b) developing techniques that improve the characterization processes by using accurate and feasible characterization methods to reduce the error introduced during parameters extraction. The first task has yielded to develop the Internode model, what is based on a finite state machine that represents the internal state of the gate depending on the electrical local of its internal nodes. Such model allows simulators to take into account all the power consumption cases (not only the usually considered ones). On the second task, we have developed a characterization technique based on the use of sampled signals. This technique has improved measurement precision by 5%-8% in the SCMOS inverter case (350 nm technology).

## 1. INTRODUCTION

In the field of verification of digital VLSI systems, it is necessary not only to verify the functional behavior but also the dynamic one, in order to guarantee that the design fulfills frequency and power consumption specifications. The logic level is the best one to carry out this process since, on the one hand, verification at the lower level (transistor level) has a very high computational cost what limits its application to very small systems and, on the other hand, verification at the higher level (RTL, register transfer level) does not obtain the sufficient precision for checking the system dynamic behavior.

However, in the field of logic simulation, the technology is advancing constantly. This advance influences remarkably in the circuits dynamic behavior causing that: (a) new effects appear that have been obviated due to their low importance in previous technologies, (b) changes appear in the behavior of the effects already considered, and (c) simulation precision get worse because the same absolute errors involve bigger relative errors due to the frequency increase. Thus, in order to maintain/increase the precision of logic simulators, it is necessary to adapt the modeling techniques to this advance taking into account each new aspect (e.g. low voltage [1], very large scale integration [2], transition waveforms [3], power consumption [4]). Also, we must denote that these changes in the models behavior imply significant modifications on the simulation algorithms in most cases.

Our work is focused on this field by trying to deal with two essential problems that prevent logic simulation from reaching optimal results. On the one

*This work has been partially supported by the MEC META project TEC 2004-00840/MIC of the Spanish Government.

hand, the processing that current simulators perform on a gate separates the functional behavior from the dynamic one. This is not a suitable point of view since each behavior type influences in the other one being essential to unify both behaviors in a single model. This can be achieved by considering that a gate can be in different states and that its dynamic behavior depends not only on the input transitions (as usual) but also on the gate state. On the other hand, most of the models used in logic simulation use a parameter set that has to be characterized [5]. Parameter characterization methods need to be supplied with new behavioral models. The lack of suitable characterization methods or non-efficient approaches may render the behavioral model useless. Additionally, the usual characterization techniques introduce important errors in these parameters that influence remarkably on the precision of corresponding model.

Thus, following the essential aim of increasing precision of logic simulators, our work is focused on two main aspects: (a) developing a model for logic gates that unifies the functional behavior and the dynamic one and (b) developing techniques that improve the characterization processes by using accurate and feasible characterization methods to reduce the error introduced during parameters extraction. In next sections, we analyze these two aspects in more detail by emphasizing some of the results already obtained as well as our current work lines.

## 2. FUNCTIONAL AND DYNAMIC BEHAVIORS UNIFICATION

The unification of the gate functional behavior and the dynamic one in a single model makes an important headway in logic simulation. In an intuitive way, this approach already starts to be applied when, for example, a different temporal behavior is considered based on what input causes the gate output to change. Nevertheless, it is necessary to develop a methodology that allows to reflect this aspect in a comprehensive and methodical way. The proposed model (called Internode, Internal node logic computational model [6]) is based on a finite state machine that represents the internal state of the gate depending on the electrical load of its internal nodes (Fig. 1). Such model allows to consider aspects unachievable from traditional models like input collisions and internal power consumption, among others.

On the one hand, input collisions, caused by multiple input transitions happening close in time, may lead to different dynamic behaviors (propagation delays) depending on the input timing and the internal state of the gate. On the other hand, internal power consumption refers to the consumption caused by any input transition. In traditional models only power consumption when an output change exist is considered. Nevertheless, an input transition causes power consumption always and, although this consumption has been traditionally neglected, this effect becomes more important as the integration scale increases. Thus, Internode is a meta-model that allows modeling in a comprehensive and detailed way the gate behavior but, at the same time, to maintain the simulation at the logic level.

In ours first tests, we have analyzed the internal power consumption in a NOR2 gate in 130, 350 and 600 nm technologies. In these preliminary tests we have found power peaks of the same order of magnitude than the ones caused when an output change exists (Fig. 2).

## 3. CHARACTERIZATION PROCESS OPTIMIZATION

Every behavioral model defines a parameter set that needs to be calculated in order to apply the model, but parameter characterization is not a trivial task except for simplistic models. The lack of a feasible and computationally efficient characterization method may render a behavioral model useless for practical applications, but this side is often unconsidered by model developers. Besides, CMOS foundries invest months in inefficiently characterizing their cell libraries for models based on look-up tables. Thus, accurate and predictable characterization methodologies become essential to apply models to practical problems.

Additionally, during any characterization process measurement errors take place. These errors suppose a very important error source since they distort the parameter set and are accumulated to the model error itself. The first aspect that the current methodology must improve is the generation of input signals. Common techniques are based on the use of variable slope input ramps which allow an accurate control of the transition time but causing a considerable error in the measurement since the gate is stimulated with signals very different from the real ones.

In order to optimize this aspect we have developed a characterization technique based on the use of sampled signals. The proposed method consists of sampling a gate output and using these data to construct the input signals necessary for the characterization process. This point of view allows, on the one hand, to accurately control the input slope (by scaling the

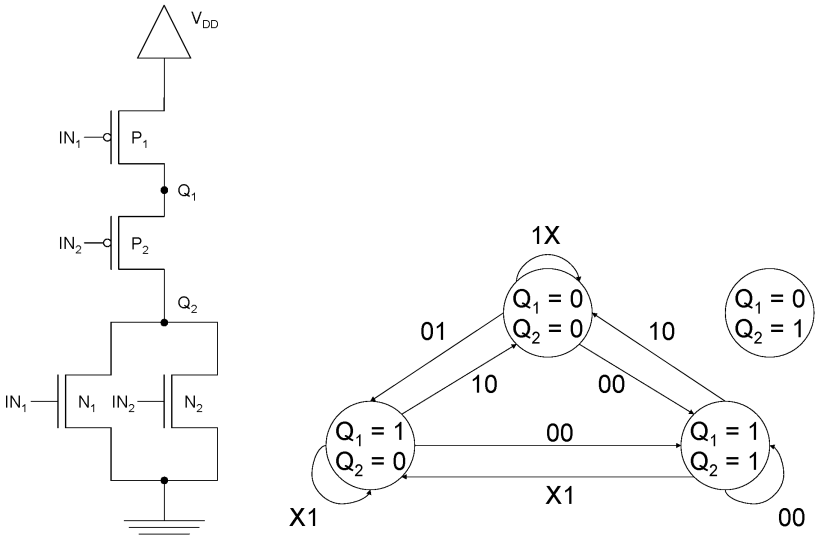


Figure 1: Internode models all the possible transitions in the input for each internal state what allows to form different behavior models for each case (figure shows the NOR2 model).

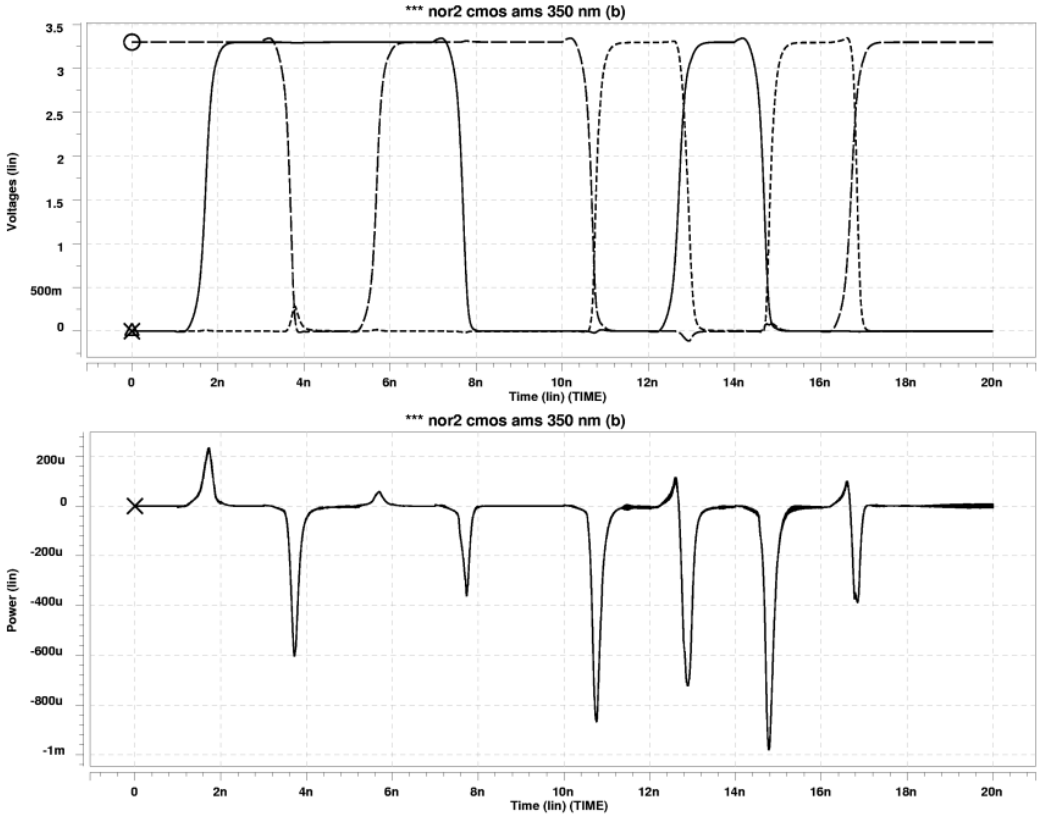


Figure 2: Power consumed in a NOR2 gate for different input transitions. Consumption caused by input transitions without output change (2 through 8 ns) is of the same order that the corresponding one when output change exists (11 through 17 ns).

| | Case | Input ramp | Sampled input |
|---|---|---|---|
| $t_{p0}$ | 1-R | 7.91% | 1.08% |
| | 1-F | 4.53% | 1.23% |
| | 2-R | 6.10% | 0.61% |
| | 2-F | 5.64% | 2.70% |
| $\tau_{out}$ | 1-R | 8.35% | 0.42% |
| | 1-F | 4.91% | 1.00% |
| | 2-R | 7.28% | 0.20% |
| | 2-F | 7.25% | 2.38% |

Table 1: Mean error made in the measurement of the normal propagation time ($t_{p0}$) and the output transition time ($\tau_{out}$) for the CMOS inverter in 350 nm technology under two driving conditions: inverter chain, case 1, and NAND gates chain, case 2; both of them for rising (R) and falling (F) output.

data) and, on the other hand, to drive the gate with signals very similar to the real ones considerably reducing the measurement error.

In ours first tests, we have applied this technique to the characterization of the CMOS inverter in 350 nm technology [7]. After subject it to a comprehensive analysis under different slope and load conditions, we have obtained very good results: the measurement precision improves by 5%-8% with respect to the one obtained by the usual input ramp method (Table 1).

## 4. DISCUSSION AND CURRENT WORK LINES

The presented motivation as well as the results currently obtained encourage us to continue in this work lines making a special effort on the following tasks: (a) applying Internode to gates with more inputs and in greater integration scale technologies and analyzing its usefulness in the study of the effects mentioned (input collisions and internal power consumption) as well as to new effects that becomes more important with the technology advance and (b) applying the presented characterization technique to other gate types and technologies as well as developing new techniques in order to continue improving the characterization process.

## 5. REFERENCES


[1] T. Kuroda, "Low-voltage technologies and circuits," in *Low-power CMOS design* (A. Chandrakasan and B. R., eds.), pp. 61–65, New York, NY, USA: Wiley-IEEE Press, 1998.

[2] J. M. Daga and D. Auvergne, "A comprehensive delay macromodeling for submicrometer CMOS logics," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 1, pp. 42–55, 1999.

[3] A. I. Kayssi, K. A. Sakallah, and T. N. Mudge, "The impact of signal transition time on path delay computation," *IEEE Transactions on Circuits and Systems-II: Analog and Digital Signal Processing*, vol. 40, no. 5, pp. 302–309, 1993.

[4] A. Chandrakasan, S. Sheng, and B. R., "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 4, pp. 473–484, 1992.

[5] A. Millan, J. Juan, M. J. Bellido, P. Ruiz-de Clavijo, and D. Guerrero, "Characterization of normal propagation delay for delay degradation model (DDM)," in *Proc. 12th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, (Seville, Spain), pp. 477–486, Springer, September 2002.

[6] A. Millan, M. J. Bellido, J. Juan, D. Guerrero, P. Ruiz-de Clavijo, and E. Ostua, "Internode: Internal node logic computational model," in *Proc. 36th Annual Simulation Symposium (part of the Advanced Simulation Technologies Conference, ASTC)*, (Orlando, Florida, USA), pp. 241–248, IEEE Computer Society, March 2003.

[7] A. Millan, J. Juan, M. J. Bellido, P. Ruiz-de Clavijo, D. Guerrero, and E. Ostua, "Signal sampling based transition modeling for digital gates characterization," in *Proc. 14th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)*, (Santorini, Greece), pp. 829–837, Springer, September 2004.