energies

Article

A Survey on Bidirectional DC–DC Power Converter Topologies for the Future Hybrid and All Electric Aircrafts

Álvaro Ojeda- Rodríguez [1], Pablo González-Vizuete [1], Joaquín Bernal-Méndez [2,*] and María A. Martín-Prats [1]

[1] Dpto.Ingeniería Electrónica, Escuela Técnica Superior de Ingeniería, Universidad de Sevilla, 41092 Seville, Spain; aorodriguez@us.es (Á.O.R.); pgonzalez17@us.es (P.G.-V.); mmprats@us.es (M.A.M.-P.)
[2] Dpto.Física Aplicada III, Escuela Técnica Superior de Ingeniería, Universidad de Sevilla, 41092 Seville, Spain
* Correspondence: jbmendez@us.es; Tel.:+34-954-486191

Received: 24 July 2020; Accepted: 7 September 2020; Published: 17 September 2020

Abstract: DC–DC isolated converters allowing a bidirectional flow of energy between High-Voltage DC and Low-Voltage DC networks have been proposed to be integrated in future on board power distribution systems. These converters must meet the specially stringent efficiency and power density requirements that are typical of the aeronautic industry. This makes it specially challenging to determine which converter topology is best suited for each particular application. This work presents a thorough review of several topologies of bidirectional DC–DC power converters that are considered good candidates to meet certain important aeronautic requirements, as those related with high efficiency and high power density. We perform simulations on virtual prototypes, constructed by using detailed component models, and optimized following design criteria that are in accordance with those typically imposed by aeronautic requirements. This comparative analysis is aimed to clearly identify the advantages and drawbacks of each topology, and to relate them with the required voltage and power levels. As an outcome, we point out the topologies that, for the required power level at the chosen switching frequencies, yield higher efficiency in the whole range of required operation points and that are expected to allow more important weight reductions.

Keywords: dual active bridge (DAB); active bridge active clamp (ABAC); current doubler (CD); DC–DC converter; power electronics; more electric aircraft (MEA)

1. Introduction

In order to respond to the growing needs of energy distribution on board and, at the same time, safeguard the ambitious objectives proposed in the aeronautical sector in terms of cost reduction and reliability of future aircrafts [1], new electric power systems have been proposed. In More Electric Aircraft (MEA) and All Electric Aircraft (AEA) pneumatic, hydraulic or mechanical systems are replaced by electrical systems [2–5]. As an example, electric generation in Boeing 787 is more than 1 MW, which is a significant increase compared to Boeing 737 (100 kW of electrical power) [6]. Airbus A380 electrical generation is 600 kVA, twice the electrical generation in A330 [7]. As a consequence of the increase in electric power, the trends in modern power distribution systems are toward an increase in voltage, with the aim to increase efficiency and decrease the weight of the energy distribution system. In particular, one of the preferred proposed solutions consists on replacing the current electric power system, based on a three-phase 115 VAC or 230 VAC at 400 Hz (or variable frequency on more modern aircrafts such as the Boeing 787 or Airbus 380), for a high-voltage DC distribution system (HVDC). Proposed HVDC nominal voltages are 270 VDC or 540 VDC, ie ± 270 VDC [3,8]. The development of

a new electric power system based on HVDC creates the need to design a new generation of power converters to supply electrical power to the avionic loads of the aircraft, which typically require a low voltage 28 VDC bus. In this context, power electronics converters are key elements to efficiently adapt aircraft loads to novel distribution architectures.

Converters with bidirectional capability for MEA and AEA applications is a current research topic. Bidirectional power converters are strongly linked to power management in aircraft applications with Electrical Storage Systems (ESS) [9]. Such ESS can be present in buses with regenerative loads, or in microgrid electrical distribution architectures, in which generators operate in parallel and sources and loads are balanced by means of ESS [10]. Microgrid architectures are considered a promising alternative to one-generator-per-bus conventional electrical architectures, as it is expected to lead to generators size reduction [10]. A recent application example is found in [11], where a bidirectional power converter for 270 VDC/28 VDC is investigated, with a focus on control capability of different energy storage sources (multiport converter). In this context, high-voltage DC (HVDC) to low-voltage DC (LVDC) bidirectional converters have been proposed as interface element between HVDC and LVDC buses in pure HVDC architectures [8]. Bidirectional capability might be used to increase system redundancy. For example, in aircraft emergency operation in which HVDC source is not available, they may operate in boost mode to feed critical loads from LVDC bus.

In the above mentioned context, this paper focuses on the key aspects of the design of power converters enabling bidirectional power transfer between a HVDC network and avionics 28 VDC buses. Converter versatility is targeted, in the sense that power converter should be able to generate either LVDC or HVDC voltages (operation in buck or boost modes, respectively), and to transfer power under the presence of an externally generated HVDC or LVDC bus. Internal current control capability is expected to facilitate control under this scenario. In particular, we will focus on suitable topologies for ∼3 kW bidirectional isolated power transfer between 270 VDC/28 VDC. This comparative study is the first design step of a modular converter design, in which power capability can be extended to up to 20 kW by means of parallelization, and compatibility with ±270 VDC voltages by mean of series/parallel modules connection. It is interesting to note that in such modular solution, the performance of the modular connection is very close to the performance of the single modules that we have considered in this study, at least in terms of efficiency and power density. While modules nominal rating in the HVDC side is 270 VDC, results of achievable performances in a ±270 VDC distribution network can also be extrapolated from the results of this study, which make this comparative study valid for any voltage level of the HVDC distribution network. As a final remark, an optimized design of a 270 VDC module will outperform a wide range module in the complete range of 270 VDC to 540 VDC HVDC voltage range, since wider operation ranges always involve poorer performances. Since aeronautic stringent requirements requires a high degree of optimization, we have decided to limit voltage range as much as possible, respecting voltage ranges defined in MIL-STD-704 standards.

Several topologies have been proposed as suitable solutions for this mission in literature. Typically, one of the preferred topologies for isolated bidirectional power transfer is Dual Active Bridge (DAB) [12]. For this topology, the simplest modulation scheme is the so called phase shift modulation [13], in which the phase shift between the two full bridges (operating at maximum duty cycle) is controlled. Several alternative modulation schemes have been proposed for DAB to improve its performance. In [14,15], the so called dual-phase-shift is presented as an alternative to phase shift modulation. In [12,16], a general study of all modulation possibilities of DAB is presented, and their potential in terms of efficiency and power density is assessed in a 2 kW isolated automotive application, under a wide operation range. The design, which implements the so called Extended Triangular Trapezoidal (TT) modulation, is stated as a promising solution, in terms of efficiency, power density and modulator simplicity. In [12], DAB optimized converter is compared with other suitable topologies such as the bidirectional current doubler (CD) topology [17], three phase dual active bridge [18] and bidirectional LLC (operating at fixed switching frequency, as in [19]). All topologies

are optimized for wide range operation as well, and they are included in the topology comparison in terms of efficiency and power density. However, the comparison in [12] does not consider the impact of including recent WBG semiconductors in the design optimization.

In contrast to voltage sourced DAB based topologies, current sourced topologies represent a set of suitable solutions for isolated bidirectional applications. An extensive review of the state of the art of isolated bidirectional current fed topologies and modulation schemes is carried out in [20], for renewable energy applications (20 VDC–40 VDC to 400 VDC, 2 kW). A topology comparison based on optimized modelled designs performance is carried out. As in [12], a large set of topologies are compared under the similar operating conditions, and a weight comparison is carried out. Still, efficiency performance is only reported for boost operating mode, and no information is provided about efficiency variation with load or voltage.

As far as the authors know, no extensive topology and modulation comparison have been carried out for HVDC/LVDC bidirectional MEA applications. However, several topologies have been proposed for this particular application, and non exhaustive topologies comparisons have been carried out in the literature. As an example of MEA application, in [21], several topologies for bidirectional 270 VDC/28 VDC power conversion have been investigated. DAB (with phase shift modulation) shows the most promising results based in the simulations. A 1.2 kW DAB SiC(HV)/Si(LV) demonstrator based on this topology is developed, with a maximum measured efficiency of ∼93% at half load, and efficiency ∼90% at full load. Switching frequency is 100 kHz.

Several bidirectional HVDC/28 VDC converter prototypes for MEA application are presented in [22]. A 1 kW DAB prototype, switching at 24 kHz was built, with achieved efficiencies of 95.8% at half load, and 94.4% at full load. Moreover, a 10 kW Series Resonant converter was built, with high efficiencies of 98% at nominal load. However, these high efficiencies come at the expense of a low switching frequency (20 kHz), which might lead to low power densities (not available data regarding weight). Finally a 20 kW Quadruple Active Bridge (as in [11]) prototype is also presented in [22], with nominal efficiencies of 98%, although no information is provided about switching frequency or power density.

In this brief state-of-the-art review, we must also cite the designs that implement what they call multicell architectures. In [23], they optimize a bidirectional 10 kW 540 VDC/28 VDC bidirectional multicell converter, which can be seen as an extension to 'n' phases of bidirectional current doubler topology [12]. They successfully implement GaN Mosfets in LV switches, taking advantage of low currents per phase due to the large number of phases. In [24], two possible solutions are proposed for the same application as [23]. First, a parallelization of interleaved 3 kW modules (phase shift full bridge, with push pull in LV side) is developed. Then, a multi-cell architecture is proposed to achieve better performance than in the modular solution. Summing up, although the achieved performance in [23,24] prove suitability of multi-cell topologies for a MEA application, their scope differs from the targeted modular approach of this study, in which lower power and voltage rated converters can be configured in series/parallel configurations.

Finally, a novel topology for the particular application studied here is presented in [25]. This topology, referred to as Active Bridge Active Clamp (ABAC), is an alterative to DAB phase shift topology. ABAC is a DAB variant with floating DC links on the LV side, and interleaved LV DC inductors. The ABAC architecture features inherent current control capability, very low LV output ripple, and short circuit current control capability. While DAB and DAB-3p inherently lack these desirable capabilities, a filter and control structure such as the proposed in [12] would enable them. The comparison in [25] neglects the consideration of a more favourable filter structure for DAB.

In this work we select a set of five promising topologies which, according to the literature review presented above, seem specially suitable for the concrete application that we are focused on. We compare these topologies from the efficiency and power density points of view, taking also into account control and filtering aspects. We describe the topologies and we establish design criteria which are in accordance with typical specifications imposed in the aeronautic industry. We make use

of detailed models of switches and passive components to justify the selection of components and their configuration. This allows us to analyze the chosen topologies with an emphasis in comparing power densities and efficiencies. To facilitate an effective comparison between topologies, we will calculate efficiency maps from half power to full power, in the whole input and output DC ranges where the converters are expected to operate [26], and for both buck and boost operation modes. The main contribution of this study is to merge the aspects listed below:

- Study of a wide set of relevant topologies for HVDC/LVDC application.
- Efficiency optimization in a wide voltage input and output operation range defined by specific aeronautic standards, as well a as wide load range.
- Losses break down analysis.
- Estimation of passives weight.
- Filters are included in all topologies to achieve similar versatile control features, and comparable filtering features.
- Switching frequencies considered in this study are oriented to high power density designs.

As final remark, it is convenient to indicate that the focus of this work is on topology and power electronics considerations. Due to that, the control techniques proposed in this work are based on frequency response of the discretized and linearized converter model. However, it must be pointed out that enhanced control laws that inherently deal with converter discrete and non-linear nature, such as Sliding Mode Control, have proven in the last few years to be an interesting solution for aeronautic applications [27–30].

2. Analisys

2.1. Methodology

The main goal of the present study is to compare topologies, for a particular application, under similar conditions, and assess the impact of recent technologies on their performance. A schematic representation of the methodology followed in this work is shown in Figure 1.

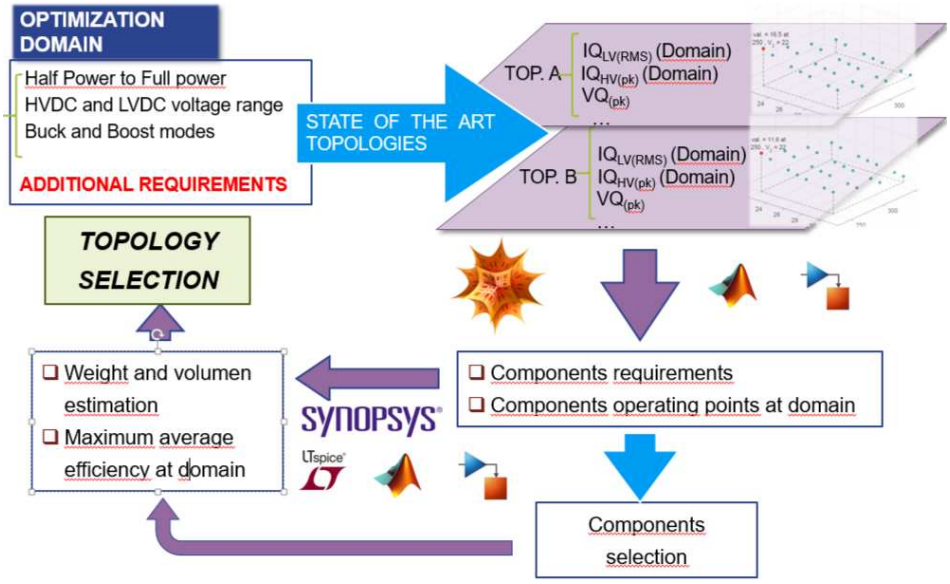


Figure 1. Followed methodology for topology comparison and architecture definition.

The first step of the study is the selection of a set of suitable topologies and modulation techniques based on literature review. Lossless models of each topology are then developed either by means of simulation models, and/or analytical expressions. Lossless models allow to estimate components

stress, and select a set of suitable components. Two potential switching frequencies are considered in this study: 100 kHz and 200 kHz. Topologies, with their associated design aspects are described in Section 2.2.

Detailed components losses models are then developed in order to evaluate efficiency at all the operating points of the optimization domain. In particular, the switching losses of a switching cell (typically a voltage sourced half bridge) is modelled as a function of switched current and voltage, and conduction losses are modelled based on components datasheets. Custom magnetics models losses as a function of switching frequency, voltage and current waveforms are also used in this study. Magnetics and capacitors weight is estimated from manufacturers data. Components selection and loss models are described in Section 2.3.

An optimization of topologies design values that have the greatest impact in efficiency and power density is carried out by means of parametric simulations: Lossless model waveforms for each design parameter considered value are calculated in the whole efficiency optimization domain (operating points). For each converter operating point, each component loss is evaluated through the detailed loss model, taking lossless model waveforms as inputs. Apart from essential components required for basic converter operation, additional components that enable the required current and voltage control capabilities in both buck and boost modes, and certain comparable filtering capabilities, are also included in the comparison. Comparisons of efficiencies and weights of the optimized designs of the selected topologies are reported in Section 3.

2.2. Topologies Design Considerations

Based on the literature review of potential topologies that might better suit our application, we have chosen five topology/modulation solutions: Dual Active Bridge (DAB) with Phase Shift modulation (PS) and modified Triangular Trapezoidal modulation scheme (TT) [12]. Moreover, three phase version of DAB (3P-DAB), Active Bridge Active Clamp (ABAC) and Full Bridge Current Doubler topology (CD) have been analyzed. These topologies are represented in Figure 2.

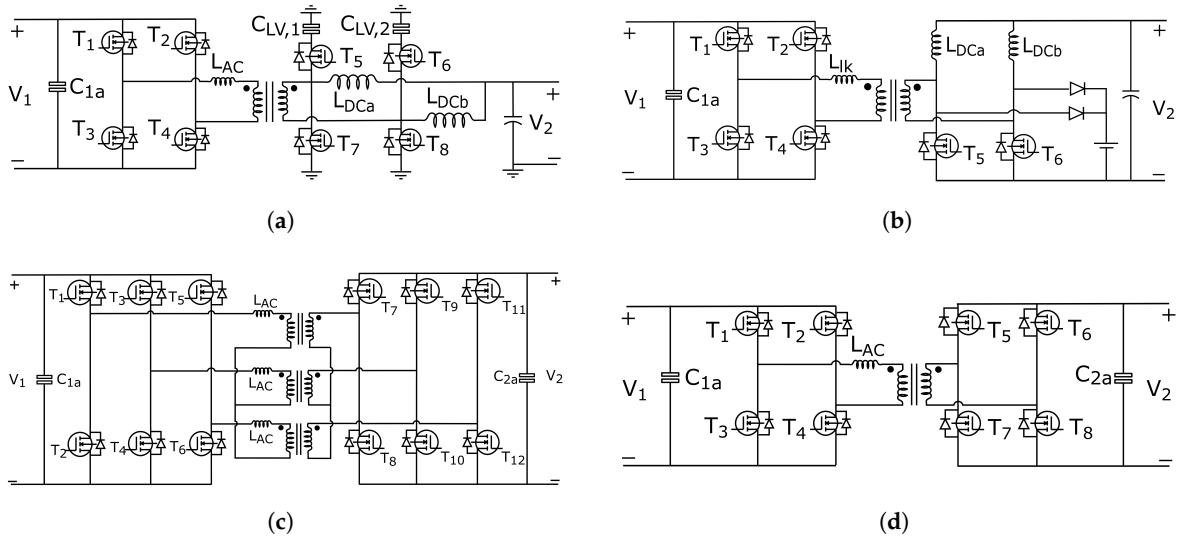


Figure 2. Schematics of considered topologies in this study. (**a**) Active Bride Active Clamp; (**b**) Current Doubler; (**c**) Three Phase Dual Active Bridge; (**d**) Dual Active Bridge: Phase Shift and extended Triangular-Trapezoidal [12] modulations.

Single phase DAB (Figure 2d), either with PS or TT modulation schemes, as well as DAB-3P (Figure 2c) feature voltage sourced ports interfacing both HV and LV bridges. Power transfer is based on setting a controlled AC voltage to AC inductors in series with the transformer.

Single phase DAB PS modulation does not guarantee ZVS switching in the HV bridge switches for certain converter operating points [12], which might produce important switching losses in the HV side, specially if Si MOSFETs are used. Several alternative modulation techniques extend the ZVS range, and might reduce currents, leading potentially to higher efficiencies. In [12], extended triangular-trapezoidal modulation scheme (TT) is presented as an alternative modulation scheme aimed to improve performance without excessively complicating the implementation of the modulator. In the TT scheme, not only the phase shift between bridges is controlled, but also each bridge duty cycle. As a consequence, the TT scheme achieves full range ZVS capability in the HV MOSFETs. Moreover, lower AC currents than in the PS design are expected. As a remark, the AC inductor requires a different design in DAB PS and DAB TT for optimal performance.

Large rms currents in capacitors is one of the main disadvantages of DAB PS and DAB TT [12]. By contrast, in DAB-3P topology, these AC currents are much lower than in single phase DAB topologies, and the ripple frequency is six times the switching frequency (fs), instead of twice fs, thus leading to lower filtering requirements for DAB-3P. Moreover, although DAB-3P only allows Phase Shift modulation, its components stress is lower than in single phase DAB topologies, partly due to the higher components count.

The design components that have greatest impact in DAB-based topologies are transformers turns ratio, n and transformer series AC inductance, L_{AC}. In all DAB based topologies, maximum power transfer depends on switching frequency, n and L_{AC}, for given bus voltages, $V1$ and $V2$, according to the following equation: [12]

$$P_{max}(V1, V2, n, L_{AC}, f_s) = \frac{knV_1V_2}{f_s L_{AC}} \tag{1a}$$

$$P_{max}(V1_{min}, V2_{min}, n_0, L_{AC,max}, f_s) \simeq 1.4P_{nom} \tag{1b}$$

where 'k' is a dimensionless factor that depends on each particular DAB topology. It is usually required by specifications that the converter should be able to transfer nominal power for the worst combination of input and output voltages. For this reason we have imposed a design constraint that ensure 1.4 times nominal power transfer capability for HVDC voltage of $V1_{min} = 250$ V and LVDC bus voltage of $V2_{min} = 22$ V. We have checked several combinations of n and L_{AC} and estimated losses in switches in the whole optimization domain. We have found that a suboptimal solution is found for $n_0 = 10$ (and $n_0 = 5$ for ABAC) and $L_{AC} = L_{AC,max}$, where $L_{AC,max}$ is the maximum AC inductance value that ensures required power transfer under worse operating conditions, as shown in Equation (1b). We must point out that, for optimization of n and L_{AC} we have only taken into account the solutions with less average losses in switches (suboptimal solution).

ABAC (Figure 2a) can be considered a variant of DAB PS, in the sense that its operation principle is based in power transfer through the transformer series AC inductor, and it implements PS modulation. Typically, HV side waveforms are indentical to those in a DAB-PS, and power transfer inductor design is identical in both topologies [25]. On the other hand, there are some differences with DAB in the LV side:

- Transformer turns ratio is typically a half of that for DAB.
- LV components currents change between buck and boost modes.
- Voltage sourced half bridges are floating, instead of a full bridge connected to the LV bus.
- LV floating buses voltage is twice the LV bus voltage.
- A DC inductor is connected to the output of each LV half bridge.

One of the main advantages of ABAC compared to DAB PS is the ripple cancellation of the two DC inductors at the LV ports [25], which would lead to lower filtering requirements if LV voltage regulation was not required.

Current doubler topology (Figure 2b) is current sourced in the LV side, whereas the HV side sets a controlled voltage at the output of LV switching block through the transformer [12]. The transformer leakeage inductance value is not essential for the converter operation principle, unlike in DAB or

ABAC topologies . Still, having a certain inductance in this kind of LV current sourced topologies extends ZVS range in the HV side in buck mode [31]. On the other hand, if transformer leakage inductance is too large, it leads to an increase of rms currents in the converter, so a trade-off has been reached in this study. An important feature of CD topology is that it only presents one switch in the LV side, instead of a full bridge. This is expected to give rise to less losses than other half-brigde variants such as full bridge current fed [32] or full bridge with push-pull circuit [12,33].

An important characteristic of the CD topology is that its voltage capability is limited by its turn ratio. If the impact of leakage inductance, switching times and other non-ideal effects are neglected, the modulation parameter D sets steady state output voltage according to the following expression:

$$D = n\frac{2V_2}{V_1}. \tag{2}$$

where D takes values between 0 and 1. If we impose that minimum steady state V1 ($V1_{min}$) must be compatible with maximum V2 ($V2_{max}$) steady state values, we get an upper limit for transformer turns ratio:

$$n < \frac{D_{max}V_{1min}}{2V_{2max}} \tag{3}$$

In this work, the steady state maximum value of D has been set to D_{max} = 0.8, to leave a certain margin for transients, and to compensate for the effects of switching times and leakage inductance in Equation (2).

Taking this constraint into account, we have chosen the transformer turns ratio as n = 3 (close to its upper limit). Transformer turns ratio and HV bus voltage determine the maximum blocking voltage of LV switches, to $V1_{max}/n$. Thus, lower n, would lead to higher required voltage ratings in the LV side.

Another important feature of CD topology is the comparatively high LV MOSFETs turn-off in boost mode. In boost mode operation, LV switches voltage must be clamped after turn-off, during the transient in which leakage inductor current equals the difference of DC inductor currents. The use of snubbers and clamping methods has been proposed in the literature to avoid destructive overvoltages during such turn-off transients in similar current sourced topologies [20,23]. In [12], a modulation scheme that theoretically avoids voltage spikes by means of modulation (at the expense of increased converter rms currents) is presented. This solution seems promising, because it achieves ZCS turn-off in boost mode, and it would reduce LV MOSFETs required voltage rating. Still, modulator signals must be accurately calculated to successfully implement this technique, which might be unfeasible in converter transients. While we have checked the performance of the proposed modulation in [12], we did not consider it as the preferred option, for the aforementioned reasons. Instead, we have considered a clamping scheme based in a regenerative snubber, as it has been implemented in [23] for a topology with the same operation principle in this aspect. From the LV switching operation point of view, the clamping circuit can be seen as a diode in series with a DC source, as it has been illustrated in Figure 2b.

There are certain differences in the filter structure of the different topologies. Figure 2 shows the essential components for topology operation. Since all the analyzed topologies are voltage sourced in the HV side, all of them include a thin film capacitor bank (C_{1a}). In the LV side, though, there are differences between topologies. In DAB-based topologies, a ceramic capacitor bank (C_{2a}) directly interfaces LV bridge. In ABAC, each floating DC link of LV half bridges is also made of ceramic capacitors ($C_{LV,1}$, $C_{LV,2}$). In CD, since LV bridge is current sourced, no HF capacitors have been considered in the LV side. Capacitors represented in the LV buses of Figure 2a,b are electrolytic capacitors included mainly for voltage regulation purposes (in real design there would also be additional HF capacitors in parallel).

In our analysis, both filtering and control capability requirements are taken into account. Or this purpose, we have implemented additional passives to the essential components, as shown in Figure 3.

In all the topologies and at both HV and LV sides, at least a DC inductor is required for current control, for short circuit current regulation capability, and also to set a minimum filter order providing at least a 40 dB per decade roll-off. Note that, unlike for the other topologies, LV inductors are essential for topology operation for CD and ABAC. The HF capacitors in bridge DC links are designed to ensure a minimum voltage ripple. Still, a minimum value for the bridge capacitance has been considered for control reasons and also because a certain filtering capability for frequencies below switching frequency is required. DC inductor current control has been designed to achieve desired cutoff frequencies of 1.5 kHz. We have imposed that resonance of DC inductors whith C_{1a} and C_{2a} (when existing) is in the order of ten times the desired current control cutoff frequency. Design criteria for all passives are summarized below:

- $\boldsymbol{C_{1a}}$: RMS current ripple in HV bridges bus due to converter switching operation must be lower than 1% nominal HVDC voltage. Capacitance must be greater than 10 uF (6.6 uF in case of 3p-DAB) due to control aspects.
- $\boldsymbol{C_{2a}}$: RMS current ripple in LV bridges of DAB topologies bus due to converter switching operation must be lower than 1% of nominal LVDC voltage. Capacitance must be greater than 1 mF (6.6 mF in case of 3p-DAB) due to control aspects.
- $\boldsymbol{C_{LV,1}}$, $\boldsymbol{C_{LV,2}}$ in ABAC: Ripple in the worse case must be lower than 5% of RMS LVDC bus nominal voltage.
- $\boldsymbol{L_{DCa}}$, $\boldsymbol{L_{DCb}}$ in CD. See Figure 2b). Minimum inductance value to ensure that peak to peak current ripple of the sum of inductors currents is less than 40% of LV output current in all considered operating voltages, at nominal power.
- $\boldsymbol{L_{DCa}}$, $\boldsymbol{L_{DCb}}$ in ABAC: See Figure 2a). Minimum inductance value to ensure that peak to peak current ripple of each inductor current is less than 80% of a half of LV output current, in all considered operating voltages, at nominal power.
- $\boldsymbol{L_{1a}}$,$\boldsymbol{L_{1b}}$, $\boldsymbol{R_1}$: Damped inductor network present in all topologies. Included for current control and short circuit control capabilities (Figure 3). Resonance with C_{1a} is set to 15 kHz (23 kHz for 3p-DAB). $L_{1a} = 2\ L_{1b}$. $R1 = 3\ Z_0$, where Z_0 is the undamped resonator characteristic impedance.
- $\boldsymbol{L_{2a}}$,$\boldsymbol{L_{2b}}$, $\boldsymbol{R_2}$: Damped inductor network present in all DAB topologies. Included for current control and short circuit control capabilities (Figure 3). Resonance with C_{2a} is set to 15 kHz (23 kHz for 3p-DAB). $L_{2a} = 2\ L_{2b}$. $R2 = 3\ Z_0$, where Z_0 is the undamped resonator characteristic impedance.

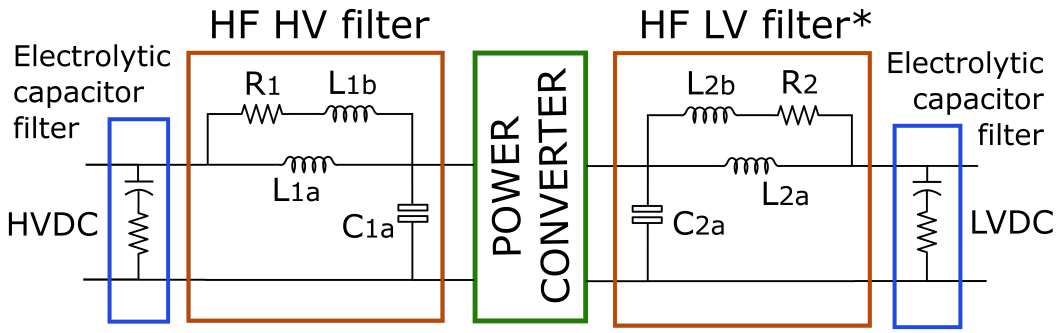


Figure 3. Complete converters filter structure. * HF LV filter block is not required in ABAC and CD topologies.

Regarding the filter design criteria for the ABAC topology, some aspects must be clarified. In ABAC, the maximum HF capacitors voltage ripple and DC inductors current ripple allowed by design can be reduced and increased, respectively, compared to other topologies, because interleaving LV inductors completely cancels out LV bus ripple. This is stated in [25] as an important advantage of ABAC compared to other DAB-based topologies. However, we must point out certain aspects that counteract this potential advantage of ABAC:

- Limiting ripple of half bridges floating capacitors is desirable for modulation purposes. Therefore, capacitor banks are required.
- Ripple fundamental component of each half bridge occurs at the switching frequency, whereas for other topologies it is twice the switching frequency (6 times for DAB-3p DC links).
- AC excitation of DC inductors is very large. This, along with the fact that fundamental frequency is the swiching frequency, make significant the required size of the inductors.

2.3. Components Models

In this analysis, we have optimized the performance of each topology by comparing performances obtained by using different components with different technologies. Topologies performance greatly depend on their components technology. In order to get the maximum achievable performance of each topology for the most recent technologies, loss models of several state-of-the-art component technologies have been developed.

In the case of HV switches, three single MOSFET configurations have been compared. Namely, a SiC MOSFET, a low $R_{DS,on}$ Si MOSFET, and a low reverse recovery Si MOSFET. In the LV side, several combinations of paralelled MOSFETs have been tested, and the possibility of implementing LV GaN MOSFETs has been studied. The impact of gate drive circuit, and layout inductance has been modelled and optimized by means of SPICE simulations.

In this section, the switching losses of a switching cell (a voltage sourced half bridge) are modelled as a function of switched current and voltage. The impact on converter efficiency at different converter operating points is analyzed in Section 3.1.

2.3.1. HV MOSFETs

HV MOSFETs data are listed in Table 1. Since HV DC link has the same voltage for all the considered topologies, those MOSFETs are suitable for all topologies. A voltage rating of ≃2 has been considered for the switches to withstand dynamics voltage overshoots, and ringings due to switching operation.

Table 1. HV MOSFETs data.

	Mosfet Ratings			**Bus Voltage**	**Parallel Operation**	
Part Number	**Voltage Rating (V)**	**Continuous Drain Current (A)**	**Technology**	**Bus Nominal Voltage (V)**	**n Parallel**	**Rds_{on} @ 100 °C**
IPW60R031CFD7	600	40	Si	HVDC, 270	1	50 mΩ
IPW60R070CFD7	600	20	Si	HVDC, 270	1	105 mΩ
C3M0030090K	900	40	SiC	HVDC, 270	1	37 mΩ

Figure 4 compares curves of switching losses as a function of load current for a half bridge for the three switches in Table 1. Those curves have been calculated for nominal voltage and at a constant current load. Positive currents indicate positive Drain to Source current in the turn-off. The considered constant current load is a reasonable approximation of the practical scenario provided by the AC inductor of the converter. This approximation is specially accurate for DAB topologies, which usually have large AC inductances.

It can be observed in Figure 4 that switching losses in the HV side reach a minimum value when there is ZVS, which occurs for positive currents larger than 3A to 8A (depending of each particular MOSFET model). Zero Current Switching (ZCS) occurs for negative currents, which is the most unfavourable case, due to hard turn off. For low currents, high switching losses still occur, due to the fact that switches undergo both hard turn-off and hard turn-on. In Figure 4 it can also be appreciated that SiC MOSFET not only present lower losses for all the range of currents, but it also presents the widest ZVS range, starting at 3A.

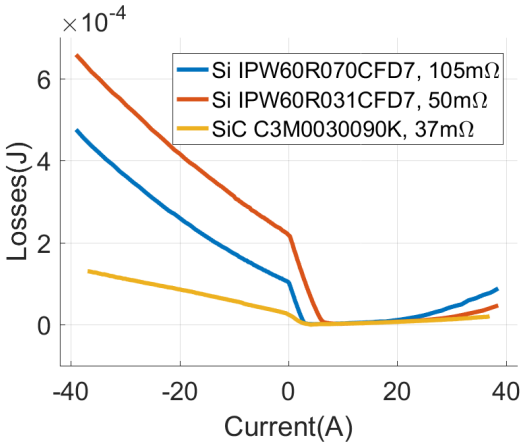


Figure 4. Switching losses in HV switches for the three MOSFET alternatives listed in Table 1 at 270 V switching voltage and Tj = 100 °C

Results in Figure 4 allow us to conclude that ZVS is a very desirable condition for achieving low switching losses, especially in the case of Si MOSFETs. We can also observe that Si MOSFET models with fast intrinsic diodes can lead to much lower switching losses than their low $R_{DS,on}$ counterparts. On the other hand, $R_{DS,on}$ of SiC MOSFETs is lower than those of Si ones. Moreover, SiC MOSFETs feature ZVS for drain to source turn-off currents greater than only 3A. They also have lower switching losses than Si MOSFETs when ZVS does not occur. As a consequence, the impact of having negative drain to source HV turn-off currents at certain operating points might be admissible in terms of converter efficiency if SiC MOSFETs are used.

In conclusion, this study on HV switches performance reveals that the use of SiC MOSFETs will lead to optimal performance in all the topologies. In later section we will specially focus on topology performance with the SiC model, though we will also overview the impact of using the Si models.

2.3.2. LV MOSFETs

Unlike at the HV side, the voltage rating of the LV switches depends on the topology. Switched voltage and chosen voltage ratings are shown in Table 2. A voltage overrating of $\simeq$3 has also been considered to take into account both bus voltage variations and spikes due to switching operation. Voltage spikes (relative to bus DC voltage) are expected to be higher in LV switches than in HV switches [12].

Table 2. LV MOSFETs data.

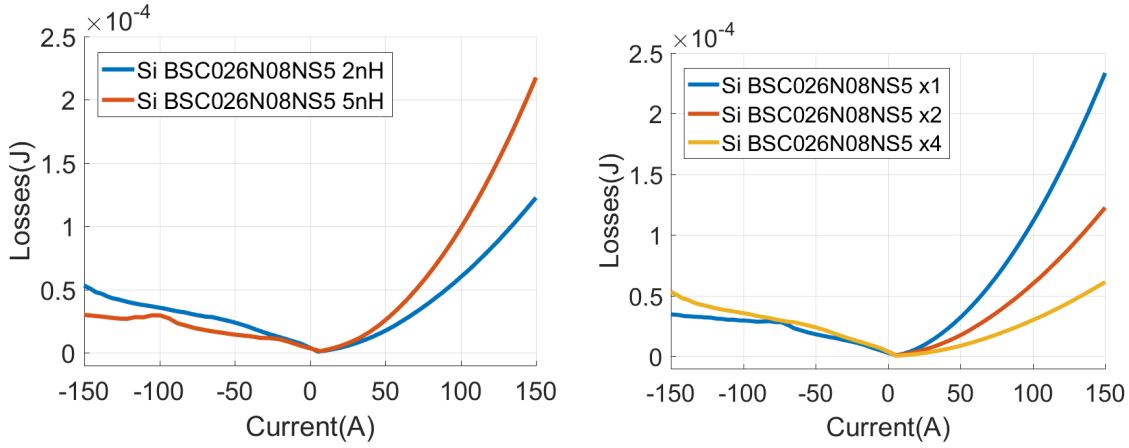
	Mosfet Ratings			Bus Voltage	Parallel Operation	
Part Number	**Voltage Rating (V)**	**Continuous Drain Current (A)**	**Technology**	**Max. Switching Voltage (V)**	**n Parallel**	**Rds$_{on}$ @ 100 °C**
BSC026N08NS5	80	100	Si	LVDC, 28	4	1 mΩ
IPB200N25N3	250	46	Si	Clamp, 150	8	5 mΩ
IPB044N15N5	150	123	Si	2xLVDC, 56	4	1.75 mΩ
EPC2206	80	90	GaN	LVDC, 28	4	1 mΩ

Stray inductances of LV switches layout has an important impact in LV switching losses [34–36]. In this study we have considered the impact of source inductance and drain inductance. Each inductance accounts for both the package inductance, and the impact of layout. In the case of the source inductance, we must differentiate common source inductance (source parasitic inductance that is part of gate drive loop [34]) from total source inductance. In Figure 5a we show the impact of varying source and drain parasitic inductances in a half bridge made of two paralelled MOSFETs. These results have been obtained by simulation with PSPICE. Drain and source inductances refer to

layout inductances (external to package) per paralelled MOSFET. An external constant common source inductance of 0.3 nH per MOSFET is included in both simulations. It can be observed that layout inductances have a significant impact in switching losses. In particular, low layout inductances of 2 nH lead to a significant reduction in switching losses for positive drain to source turn-off currents, compared to 5 nH layout inductances. While the 5 nH layout yields slightly lower losses for negative drain to source turn-off currents, we can conclude that the 2 nH layout outperforms the 5 nH layout. Therefore, external drain and source parasitic inductances of 2 nH have been considered for the efficiency evaluation carried out in Section 3. Regarding this aspect, it is worth mentioning that we have also checked that low common source inductance leads in most cases to low switching losses (results not shown).

On the other hand, since LV side handles high currents, MOSFETs paralellization is required to reduce both conduction and switching losses. Several combinations of paralelled MOSFETs have been evaluated. As an example, Figure 5b shows switching losses in a half bridge for DAB topologies for a single MOSFET (×1), two paralelled MOSFETs (×2) and four paralleled MOSFETs (×4). The impact of MOSFET parallelization is very beneficial for the case of positive turn-off currents, and has a very slight negative impact in the ZCS operation region, thus parallelization is positive to reduce switching losses. Layout parasitic inductances of 2 nH per MOSFET (as described in the previous paragraph) have been considered in simulations of Figure 5b.

As a result of the previous study, four Si MOSFETs per switch have been chosen as the best feasible solution for all the topologies, except for CD that requires eight MOSFETs per switch to keep low the losses in LV switches, caused by the high clamping voltage in the LV side. Note that, even if CD topology has only two switches in the LV side, the required amount of discrete MOSFETs is very similar to half bridge switching cells. The MOSFET configurations used for efficiency calculation in Section 3.1 are summarized in Table 2. For efficiency estimation, we have assumed that the resistance of paralleled MOSFETs is the equivalent resistance corresponding to the parallel combination of the resistances of each single MOSFET.



(**a**) Stray inductance variation effect on switching losses at 28 V switching voltage

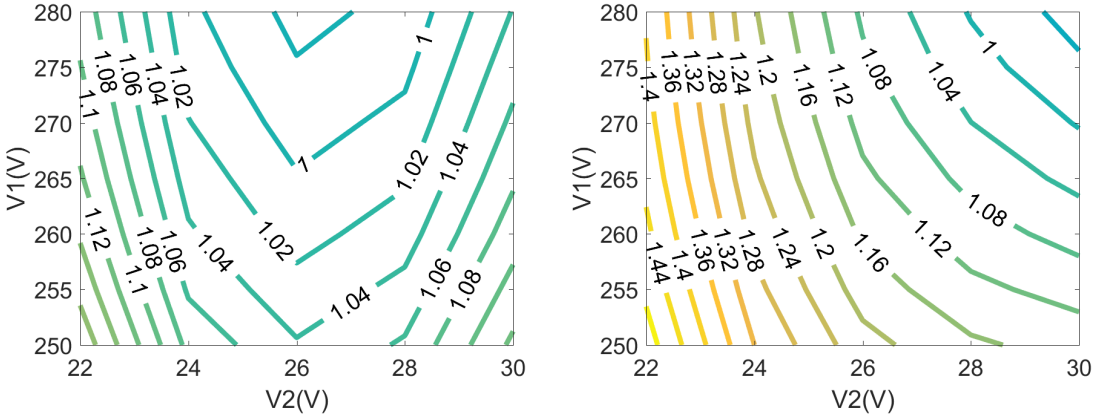
(**b**) Doubling MOSFET in parallel effect - BSC026N08NS5 at 28 V switching voltage

Figure 5. Effect on switching losses where doubling MOSFET in parallel.

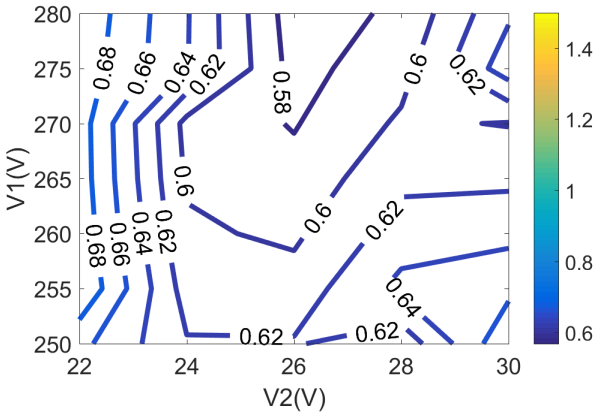
2.3.3. Passives

For the third party design of custom magnetics, we imposed that total magnetics losses in the worse scenario should not exceed 60 W, at 60° ambient temp, and then design should be optimized to achieve lowest weights. A loss model of custom magnetics for each topology and each considered switching frequency was provided by magnetics manufacturer ('Frenetic') as a function of voltage and current rms excitation. For the generation of loss model, the manufacturer excited the

designed magnetics with scaled waveforms with the shape of converter nominal operating point. This approximate method models the impact of magnetics non linear losses with frequency (waveform harmonics), but it does not account for differences in harmonic content between different operating points. In Figure 6 we show an example of custom magnetics losses for different topologies, at full power. It is worth mentioning that, for the calculation of converter losses in Section 3, excitations from lossless topology models are the input to magnetics manufaturers provided loss models.



(**a**) ABAC (**b**) 3P-DAB



(**c**) DAB-TT

Figure 6. Magnetic losses in % (magnetics losses divided by converter transferred power) for all the operating points at nominal power and 100 kHz.

Finally, apart from the loses in essential magnetic, we have also estimated losses in HF capacitors and damped DC inductor networks. For this purpose, we have extracted inductors and capacitors equivalent series resistance from manufacturers datasheets. By multiplying these resistances with inductors DC currents, or capacitors AC currents, we have obtained losses of such passives. As a result, we have observed that these losses are much lower than those of switwes and essential magnetics discussed previously. In a view to facilitate comprehension of this article, we did not include these negligible losses in efficiency calculations of later sections.

In order to optimize the power density of the different topologies we have taken into account the weight of essential passives, and HF filter passives. The contribution to the total weight of electrolytic capacitors has not been included in the comparison study because their main design constraint is voltage regulation, which is expected to have similar impact in all topologies, independently of switching frequency.

3. Results

In this section we compare efficiencies and weights for the different converter topologies, focusing specially on the design at a switching frequency of 100kHz. Results at 200kHz will also be commented in Section 3.3. Unless otherwise specified, results in this section correspond to optimized topologies, components selections and optimized switches layout described in Section 2.

The HVDC and LVDC voltage ranges are indicated in Table 3. We assume as a requirement that the converters under design should be able to operate at full power, in steady state, for any input and output voltage combination. Efficiency at full power has a special interest because it will determine heat sinking steady state requirements. This aspect will be analyzed in Section 3.1.1. Efficiencies from half power to full power for nominal output voltage are analyzed in Section 3.1.2. In Section 3.2 topologies are compared in terms of weight, taking into account the weight of passive components.

Table 3. Operating domain, based on MIL-704F standard [26] . Nominal conditions definition.

$V1_{nom}$ (V)	$V2_{nom}$ (V)	P_{nom} (W)	$V1_{min}$ (V)	$V1_{max}$ (V)	$V2_{min}$ (V)	$V2_{max}$ (V)
270	28	3000	250	280	22	30

3.1. Efficiency Comparison

3.1.1. Full Power Efficiency Maps

Figures 7 and 8 show contour plots of efficiency, in buck and boost modes, respectively, as a function of input and output voltages calculated at the nominal power of 3 kW.

From Figure 7, we can see that DAB topologies yield higher efficiency than ABAC and CD in buck mode. Particularly, three-phase DAB and single phase DAB with TT modulation exhibit the highest efficiencies, whereas CD yields the poorest result. Table 4 highlights maximum and minimum efficiency values in buck mode for each topology.

Table 4. Maximum and minimum full power efficiency map values in buck mode.

Topology	Maximum Efficiency			Minimum Efficiency			Variation [%]
	V_1 [V]	V_2 [V]	Eff [%]	V_1 [V]	V_2 [V]	Eff [%]	
ABAC	280	30	96.8	250	22	95.5	1.3
CD	250	30	96.3	275	22	93.8	2.5
3P-DAB	280	30	97.5	250	22	96.4	1.1
DAB-TT	280	26	97.5	250	30	96.6	0.9
DAB-PS	280	26	97.0	250	22	95.7	1.3

From Figure 7 it can also be observed that the dependencies of efficiency with input and output voltages are different for each topology. It can be seen that efficiency of the CD topology in buck mode depends almost exclusively on LVDC voltage. In particular, low V2 values greatly penalize efficiency. The same behaviour can be observed in ABAC, with the difference that low HVDC voltages (V1) lead to a decrease in efficiency at LVDC voltages greater than 25 V. On the other hand, all DAB topologies present a similar efficiency behaviour: Efficiency increases with V1, whereas extreme values of LVDC bus voltage penalize efficiency. Maximum and minimum efficiencies at full power in buck mode are summarized in Table 4. Note that CD shows the largest dependency with input and output voltage (2.1% of difference between maximum and minimum efficiencies), which is undesirable in wide operation applications. Moreover, note that efficiency at nominal HVDC and LVDC voltages ($V1_{nom}$, $V2_{nom}$) at full power are close to maximum efficiency in all topologies.

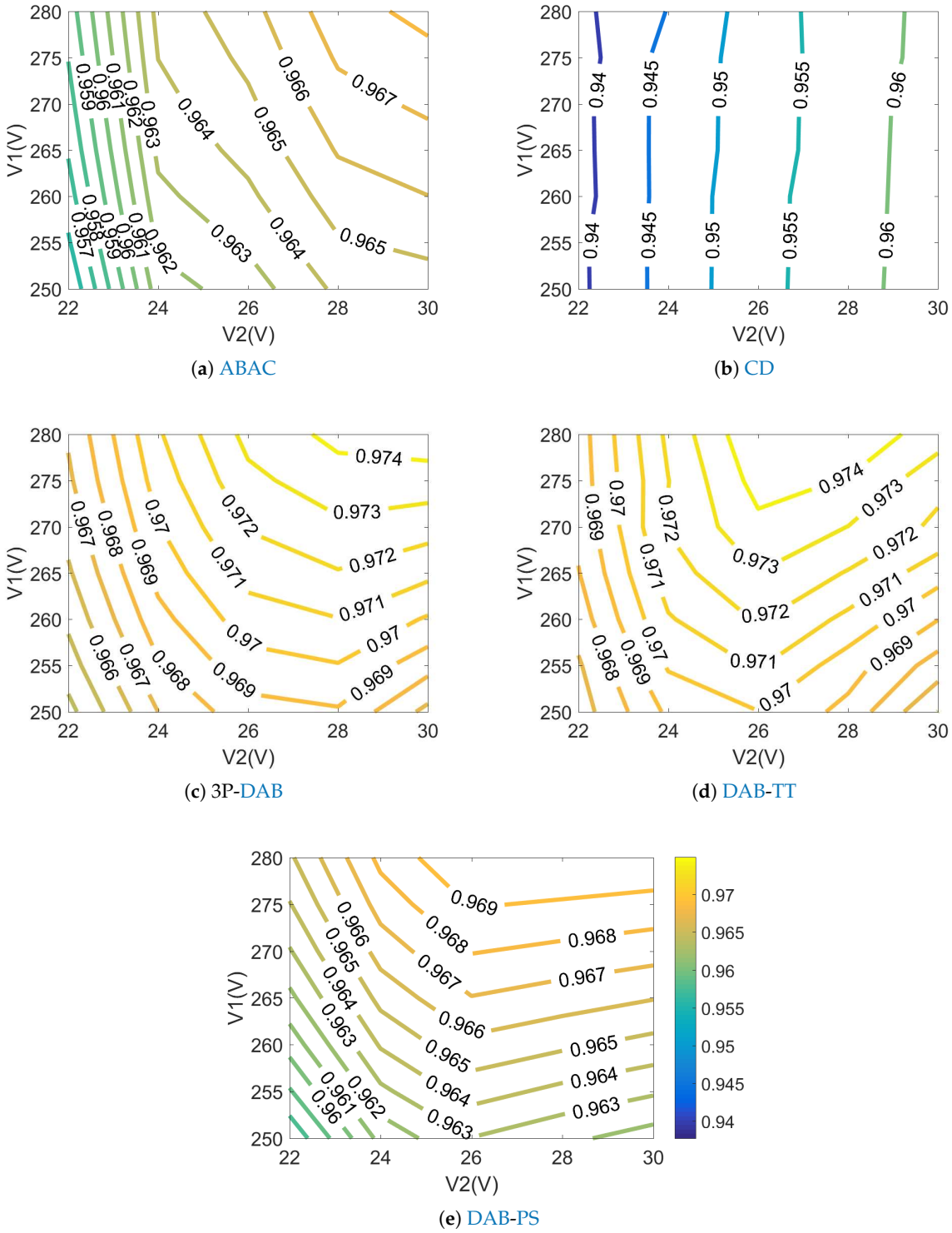
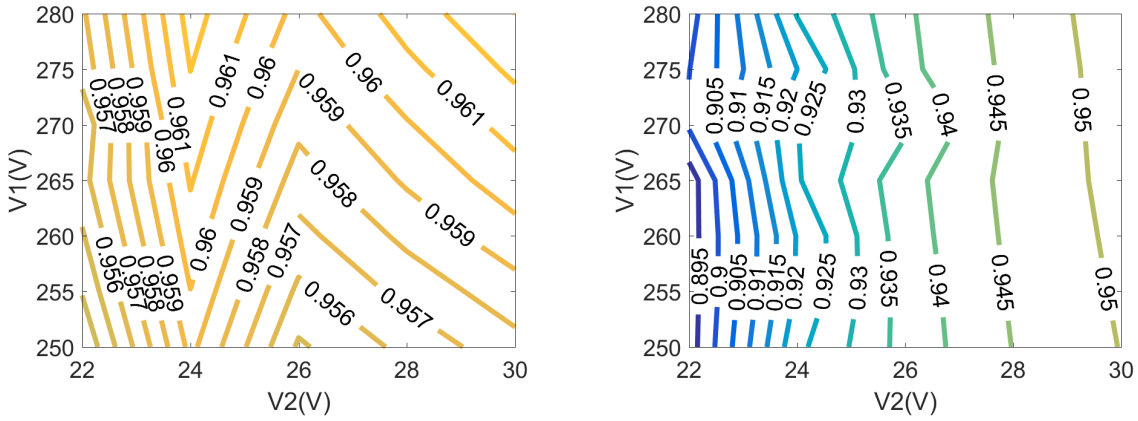


Figure 7. Full power efficiency maps in buck mode.

In boost mode, DAB topologies have the same behaviour as in buck mode. Therefore efficiency contour plots for these toplogies have been omitted in Figure 8. Figure 8a,b reveal that ABAC and CD topologies yield lower efficiency values in boost mode compared with buck mode. Table 5 provides maximum and minimum efficiency values for ABAC and CD in boost mode, as well as efficiency variations. Note that difference between maximum and minimum efficiencies is specially large for CD within the considered voltage ranges.



(**a**) ABAC (**b**) CD

Figure 8. Efficiency map at full power, in boost mode. DAB topologies performance in boost mode is the same as in buck mode, as shown in Figure 7.

Table 5. Maximum and minimum full power efficiency map values in boost mode.

Topology	Maximum Efficiency			Minimum Efficiency			Variation [%]
	V_1 [V]	V_2 [V]	Eff [%]	V_1 [V]	V_2 [V]	Eff [%]	
ABAC	280	30	96.3	250	22	95.3	1
CD	280	30	95.3	265	22	89.2	6.1

For the CD topology, the efficiency behaviour in boost mode is very similar to the efficiency in buck mode, i.e., it depends only on V2. ABAC presents a more complicated pattern in boost mode, as shown in Figure 8a. Efficiencies are also close to maximum values at nominal voltages in boost mode as well as in buck mode.

Due to the important impact that maximum (worst case) losses have on heat sinking requirements it is interesting to calculate maximum converter losses yielded by each topology. Table 6 provides these figures and it also specifies the operating point within the voltages domain given in Table 3 at which these worst case losses are achieved for each topology. In that table, negative power values mean boost mode operation. Those results show that CD power losses are significantly higher than those of the other topologies. Moreover, ABAC has slightly higher losses than DAB topologies, with DAB presenting the lowest worst case losses. As a final remark, we have checked that maximum losses in all topologies occur at full power, so minimum efficiencies in Table 6 are coincident with minimum efficiency values in Table 4 or 5.

Table 6. Maximum losses for each topology at a specified operating point within the range defined in Table 3.

Topology	V1(V)	V2(V)	P(kW)	eff	Loss (W)
ABAC	250	22	–3	95.31	140.7
CD	265	22	–3	89.22	323.4
3p-DAB	250	22	±3	96.36	109.1
DAB-TT	250	30	±3	96.60	102.1
DAB-PS	250	22	±3	95.72	128.5

3.1.2. Nominal Output Voltage Efficiency Maps

Since in most converter operating scenarios converter control will regulate output voltage to its nominal value, it is interesting to analyze, for each topology and for the output voltage fixed to its nominal value, how efficiency varies with output power and with input voltage. Figures 9 and 10

represent contour plots of efficiency when output power goes from half power to its nominal value for input voltages within the (Vin_{min},Vin_{max}) range specified in Table 3.

From the buck mode efficiency maps shown in Figure 9 it can be observed that the highest efficiency values are achieved by three phase DAB and DAB with TT modulation. Then, DAB with PS modulation and ABAC follow them, whereas CD yields the worst peak efficiency. Moreover, it is interesting to note that ABAC and CD have similar efficiency patterns in the sense that for a given input voltage V1, efficiency decreases at higher powers. On the contrary, for the CD topology, efficiency dependency with power is negligible. For DAB topologies, efficiency increases as the input voltage increases, with a maximum at a power value between the nominal power and half power. Maximum and minimum efficiencies extracted from these graphs are summarized in Table 7. This table also displays efficiency variation in buck mode. Results in Table 7 show that DAB-TT has the best performance, whereas the CD topology has the lowest efficiencies. However, there are no significant differences in efficiency variations between topologies.

Table 7. Maximum and minimum nominal output voltage efficiency map values in buck mode.

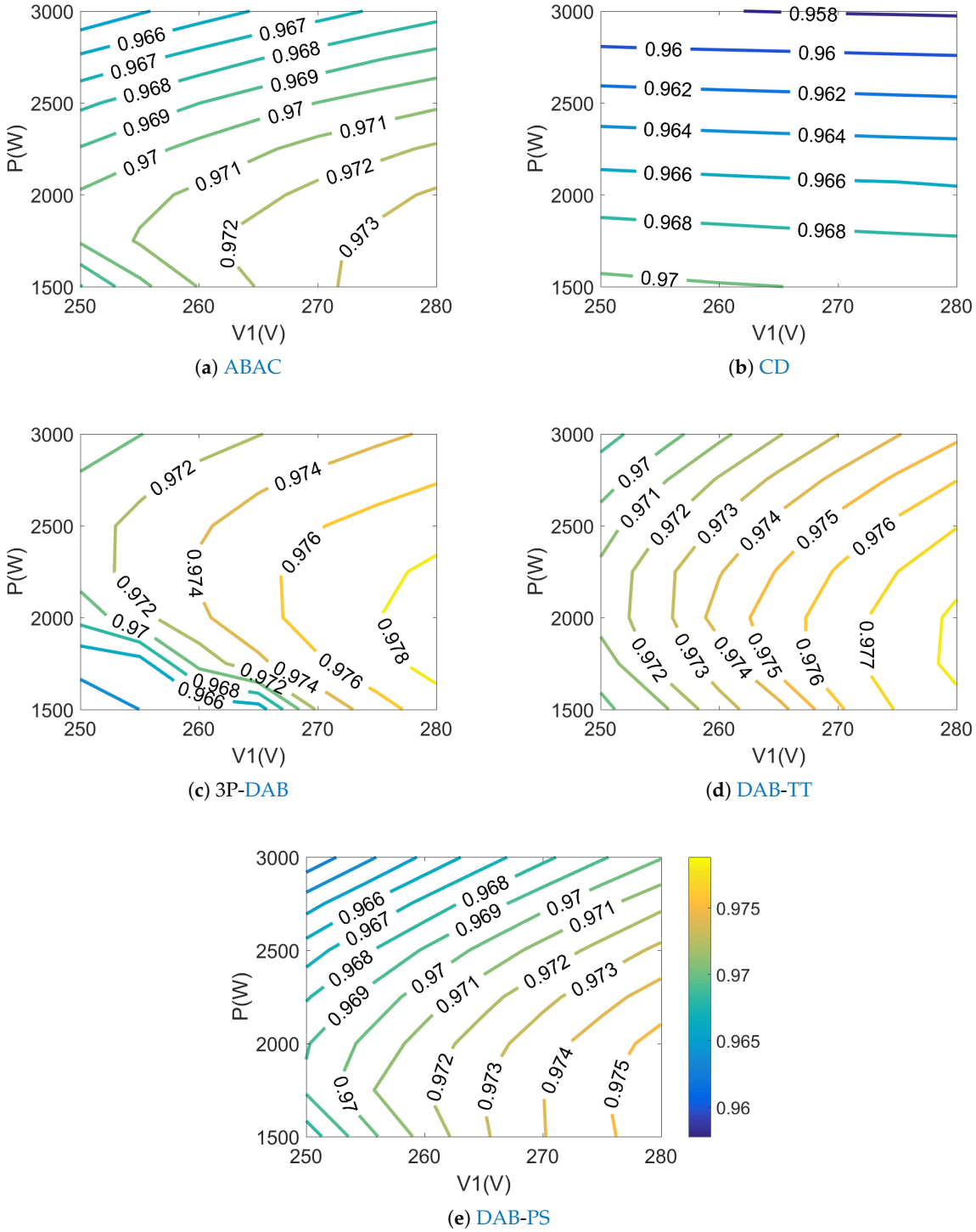
Topology	Maximum Efficiency			Minimum Efficiency			Variation [%]
	V_1 [V]	P [W]	Eff [%]	V_1 [V]	P [W]	Eff [%]	
ABAC	280	1500	97.4	250	3000	96.4	1.0
CD	250	1500	97	280	3000	95.8	1.2
3P-DAB	280	2000	97.9	250	1500	96.3	1.6
DAB-TT	280	1750	97.8	250	3000	96.9	0.9
DAB-PS	280	1750	97.6	250	3000	96.2	1.4

Performance in boost mode is different than in buck mode, as it can be observed in Figure 10. Such difference can be explained by the fact that, in the case of ABAC and CD, the performance of these topologies strongly depends on power transfer sign. Moreover, HVDC and LVDC voltage ranges of the optimization domain differ in buck and boost modes. Figure 10 shows that in all topologies efficiency tends to decrease at higher powers, as in buck mode. If we attend to efficiency variation with LVDC input voltage, we can observe different behaviours depending on the topology. In DAB based topologies, highest efficiencies occur at central voltages. In CD efficiency increases with input voltage. Finally, in the case of ABAC, a clear dependency between input voltage and efficiency cannot be established.

Maximum and minimum efficiencies in boost mode for nominal output voltage are provided in Table 8. The highest efficiency values in boost mode are reached by 3P-DAB and DAB-TT topologies, both of them with low efficiency variation too. All DAB based topologies have almost the same maximum efficiencies (0.1% difference) and minimum efficiencies (0.3% difference) CD exhibits the worst performance again. In the case of ABAC, highest efficiencies are close to those of DAB topologies, but there is a significant difference between maximum and minimum values.

Table 8. Maximum and minimum nominal output voltage efficiency map values in boost mode.

Topology	Maximum Efficiency			Minimum Efficiency			Variation [%]
	V_2 [V]	P [W]	Eff [%]	V_2 [V]	P [W]	Eff [%]	
ABAC	24	1500	97.8	22	3000	95.5	2.3
CD	30	2000	95.8	22	3000	90.1	5.7
3P-DAB	26	1750	97.9	30	1500	96.5	1.4
DAB-TT	26	2000	97.9	30	1500	96.6	1.3
DAB-PS	24	1500	97.8	22	3000	96.3	1.5



(**a**) ABAC

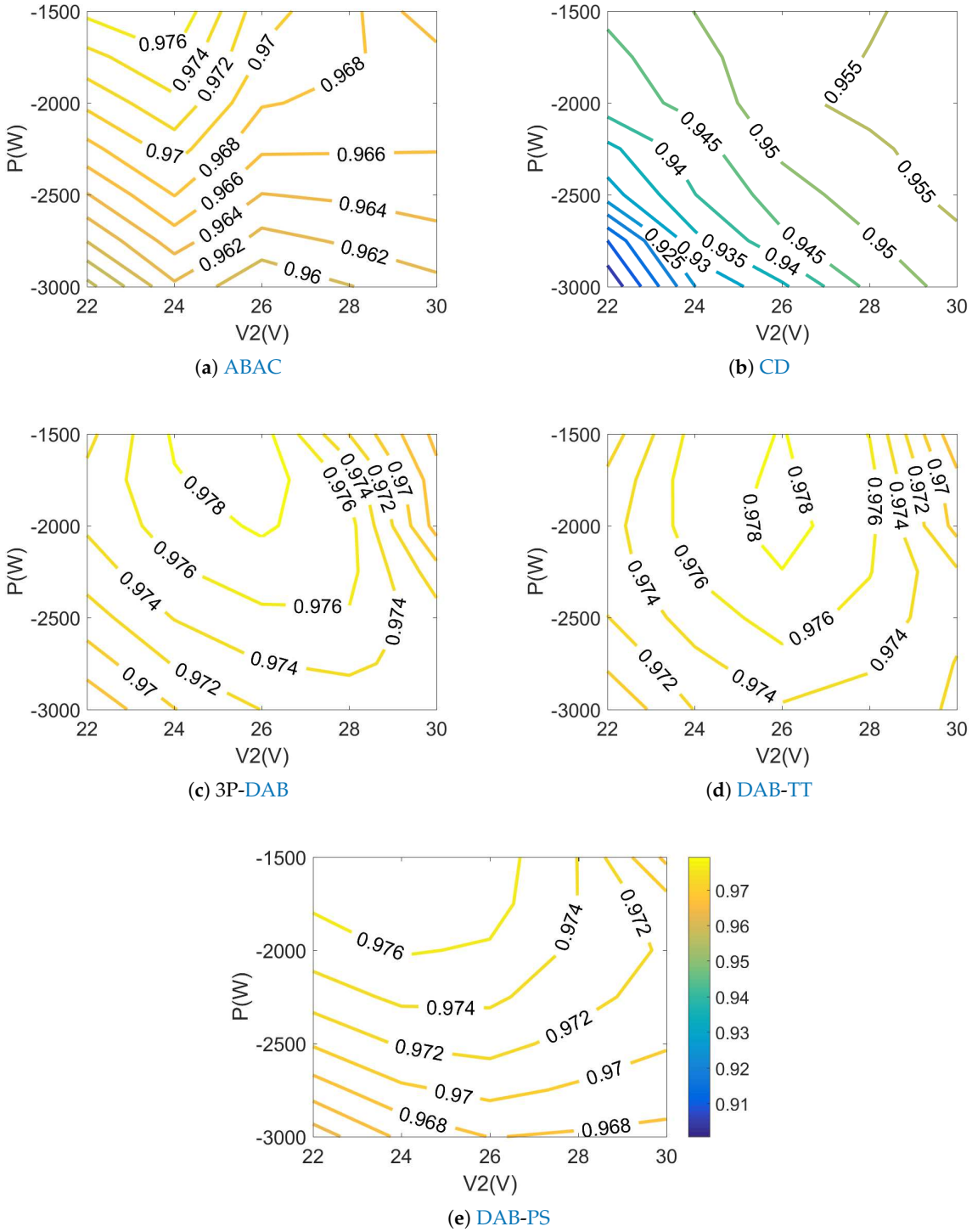
(**b**) CD

(**c**) 3P-DAB

(**d**) DAB-TT

(**e**) DAB-PS

Figure 9. Efficiency map in buck mode, from half power to full power, wide V1 input range, and nominal V2.



(**a**) ABAC (**b**) CD

(**c**) 3P-DAB (**d**) DAB-TT

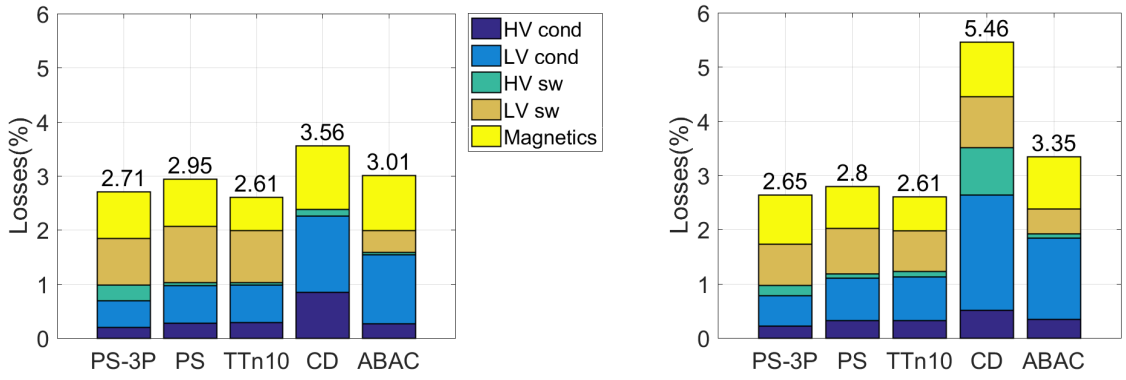
(**e**) DAB-PS

Figure 10. Efficiency map in boost mode, from half power to full power, wide V2 input range, and nominal V1.

3.1.3. Average Efficiency Comparison

As a way to complement efficiency results, in this section we compare average losses, calculated in the entire optimization domains, of the five topologies studied here. Results for both buck and boost modes are displayed in the two graphs in Figure 11. In those bar graphs, we represent total average losses and also the contribution of each type of loss: Losses at essential magnetics, conduction losses at

both voltage sides (HV cond. and LV cond.) and switching losses at both voltage sides (HV sw. and LV sw.).



(**a**) Buck mode (**b**) Boost mode

Figure 11. Average losses in % (converter losses divided by transferred power), including losses breakdown.

As expected from contour plots presented above, the CD topology exhibits the worst performance, specially in boost mode. Then, it is followed by ABAC topology, which is outperformed by all the DAB topologies in both modes of operation. The DAB topologies present average losses below 3% in both modes. The DAB topology with TT modulation has the lowest average losses in both modes.

Focusing on losses breakdown in Figure 11, we realize that conduction and switching losses at the LV side dominate total losses. In particular, in DAB topologies LV switching losses dominate (1% losses), whereas in ABAC and CD, conduction losses are the dominant term (1.3% losses). Regarding this, it must be pointed out that required voltage rating of CD and ABAC LV MOSFET is 5 times and 2 times, respectively, the required voltage rating for DAB topologies. The remarkable fact that losses in LV switches are 3 to 5 times the losses in HV switches is partly accounted for by the fact that SiC switches are used in HV side while the switches in the LV side are Si switches.

In HV switches, conduction losses are 4 to 5 times larger than switching losses in most cases. An exception is DAB-3p in both modes, in which conduction and switching losses are similar. This fact can be explained by the fact that for this topology ZVS in HV switches is not ensured in the full range of operation points. Furthermore, even if in 3p-DAB, MOSFETs losses per switch are multiplied by six to obtain overall conduction losses, such overall HV conduction losses are lower than in single phase DAB topologies, partly because switches rms currents are much lower than in single phase topologies, and conduction losses increase with the square of the current.

A comparison of Figure 11a,b reveals that for most topologies there exist no significant difference between average efficiencies when comparing buck and boost modes of operation. An interesting exception is the CD topology. This topology shows a significant asymmetry in performance with power direction that can be explained by the important difference in waveforms when only power sign is changed. For example, the factor of two in HV conduction losses in CD is explained because HV rms currents are much larger in buck mode than in boost mode. On the other hand, ZVS in HV MOSFETs is achieved only in buck mode, which explains the significant difference of 1% in HV switching losses between buck and boost modes. We can also observe that in buck mode, LV switching losses are negligible, while in boost mode they contribute in 1% to average losses. This is accounted for by the fact that there is soft switching in LV switches both at turn-on and turn-off in buck mode. By contrast, in boost mode hard turn off occurs.

We have also analysed the impact of using different suboptimal HV switches technologies on average efficiency, from half power to full power, constant nominal output voltage and wide input range. Results are shown in Table 9. Results of optimized selection that has been widely discussed

in this section are highlighted in orange background. Si_1 accounts for HV Si MOSFET with part number IPW60R031CFD7, and Si_2 accounts for HV Si MOSFET with part number IPW60R070CFD7. Si_1 has lower $R_{DS,on}$ than Si_2, and Si_2 has faster intrinsic diode than Si_1. SiC MOSFET outperforms Si MOSFETs in both conduction losses and switching performance. In general we observe that the fastest Si MOSFET Si_2 leads to higher efficiencies than Si_1: The use of SiC MOSFET involves an average efficiency increase of 1.5% compared to Si_1, and 0.8% compared to Si_2. We can observe that for this wide operating range application, the use of fast HV MOSFETs that do not penalize excessively non ZVS operation and extend its range in (as it is the case of Si_2 and SiC) is in general more beneficial than MOSFETs with reduced conduction losses. Even if Si_1 and Si_2 feature the same recent technology, there is a difference of 0.7% in average efficiencies. The only exception in which Si_1 outperforms Si_2 occurs in CD, in buck mode, where there is ZVS in HV MOSFETs in the whole range,and large rms currents in HV switches.

Table 9. Average efficiency comparison between different switches technologies. Optimized proposed solution is highlighted in orange.

Topology	Average Efficiency—Buck Mode				Average Efficiency—Boost Mode			
	HV/LV *SiC/Si*	HV/LV *Si_1/Si*	HV/LV *Si_2/Si*	HV/LV *SiC/GaN*	HV/LV *SiC/Si*	HV/LV *Si_1/Si*	HV/LV *Si_2/Si*	HV/LV *SiC/GaN*
ABAC	96.7	96.4	96.5	-	96.7	96.2	96.0	-
CD	96.4	96.1	94.8	-	94.5	90.0	91.6	-
3P-DAB	97.3	93.8	96.5	97.7	97.4	95.2	96.6	97.7
DAB-TT	97.4	96.1	96.9	97.8	97.4	96.0	96.7	97.7
DAB-PS	97.1	96.5	96.5	97.6	97.2	96.7	96.6	97.6

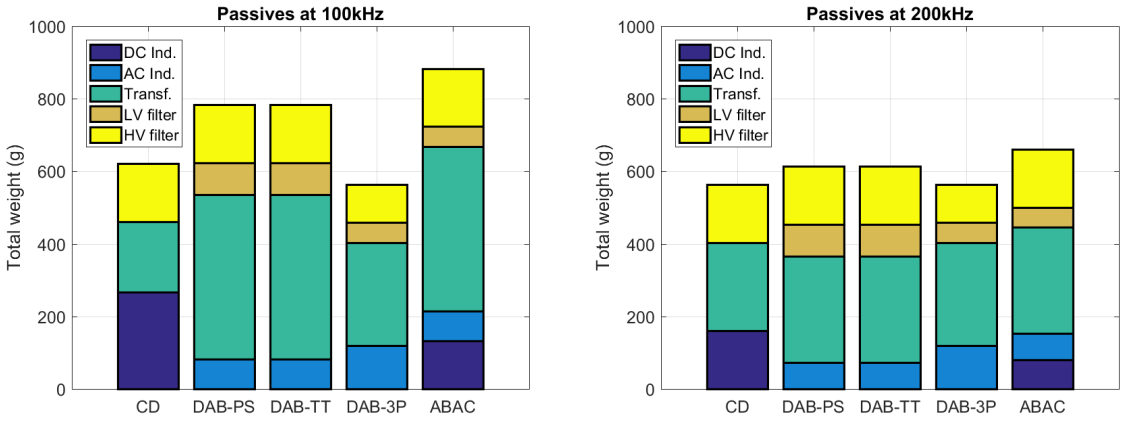
We have also assessed the impact of implementing GaN switches in DAB topologies, as defined in Table 2. The propoposed GaN switches configuration has very similar conduction losses and lower switching losses than the porposed Si LV MOSFETs solution. However, the use of GaN MOSFETs only increases average efficiency in 0.35% for 3p-DAB and DAB-TT, and 0.45% for DAB-PS. Pros and cons of implementing GaN switches will be discussed in Section 3.3.

3.2. Weight Estimation

Since power density is one of the main constraints in the design of power converters for aeronautical applications, it is convenient to compare expected weights of the five topologies analyzed in this work. Figure 12 shows such a weight comparison for the 100 kHz design (Figure 12a) and the 200 kHz design (Figure 12b). In those bar graphs the total weights are broken down into the contributions of the different passive elements that we have considered in this study. Regarding this, the "DC ind." label stands for the contribution of the DC inductors that are required for topology operation in CD and ABAC topologies. "LV filter" and "HV filter" labels refer to high frequency capacitors required for the DC links that interface bridges, and OTS DC inductors added for extended control and filtering purposes. Finally, labels "Transf." and "AC ind." make reference to the contribution of the transformer and the AC inductors. Those components, together with DC inductors in CD and ABAC, are custom magnetics. Design criteria of these components have been expounded in Section 2.3.

Figure 12 shows that in all the cases, weight of magnetics that are essential for topology operation have the most important impact in total weight. We will focus here first on results for a switching frequency of 100 kHz. Figure 12a shows that at this switching frequency custom magnetics weights go from 400 g in 3p-DAB to 650 g in the case of ABAC. Transformer and AC inductor weights in ABAC are very similar to those for DAB-PS and DAB-TT topologies, but the additional DC inductors make ABAC a less preferable solution in terms of weight. An advantage of the CD topology is that, since low

AC inductance value is required (compared to DAB topologies), the transformer leakage inductance can be used for this purpose, so there is not contribution of AC inductance to total weight. However, LV inductors currents in CD are not interleaved at 180°, as in ABAC, which makes it necessary to employ larger inductances that penalize total weight for this topology.



(**a**) fs 100kHz (**b**) fs 200kHz

Figure 12. Topologies passives weight estimation.

As explained in Section 2.3, all the topologies require a DC filter stage at the HV side with the same structure and very similar values of components. As a consequence, it can be seen in Figure 12a that HV filters weights are similar for all topologies, with the exception of 3P-DAB. In 3P-DAB weight has been reduced to 2/3 thanks to the much lower filtering requirements of this topology. Further reductions are precluded by dynamics and control aspects. As a final remark, we must point out different set of design criteria to those presented in Section 2 might modify these results.

In the LV side, filter structure depends on topology. For example, no additional LV filter components are required in CD. In ABAC, only LV HF capacitors are included in the "LV filter" weight in Figure 12a. On the other hand, the weight of the filter at the LV for the 3P-DAB topology is 2/3 times that for single phase DAB topologies.

Considering the weight of HV and LV filters together, this weight goes from ∼150 g in 3p-DAB and CD to ∼250 g in single phase DAB topologies and ABAC.

It must be noted that, in the ABAC topology, the added weight of LV DC inductors and LV filter (includes only LV capacitor bank) is ∼180 g, which is approximately twice the weight required for the LV filter in DAB topologies. This fact might be surprising if we take into account that one of the advantages of ABAC compared with DAB topologies is the expected reduction in ABAC LV filter size due to its inherent output ripple total cancellation [25]. The large weight of LV filter components in ABAC can be explained by the design criteria chosen here. Namely, we require less than 5% of peak to peak ripple in each half bridge bus, and less than 80% peak to peak current ripple in each DC inductor, at nominal power (see Section 2). The fact that ABAC LV passives excitation ripple frequency is equal to the switching frequency (instead of twice or six times the switching frequencies, as in other topologies), along with the doubled DC link voltage, increases the required weight of its LV filter components.

Summing up, for a switching frequency of 100kHz the total passives weight is estimated to go from ∼560 g for 3p-DAB to ∼880 g in the case of ABAC. If we compare the weight estimations of the two topologies that, according with results in Section 3.1, present the higher average efficiencies it can be seen that the passives weight of DAB-TT is estimated to be 220 g more (i.e., ∼40% more) than that for 3p-DAB.

Figure 12b shows a passive weight estimation for 200 kHz switching frequency. In the case of LV filter and HV filter components, no weight differences are expected with respect to the 100 kHz case presented in Figure 12a. This can be easily understood if we note that in the 100 kHz design, filter passives where determined by control aspects rather than filtering aspects. Increasing switching frequency might further reduce passives size due to filtering requirements, but, as far as the authors know, it does not allow to reduce passive size from the control point of view. It must be mentioned that a less conservative approach in control design considerations might take some advantage of doubling switching frequency to reduce filters passives weight. However that detailed study is beyond the scope of this work.

In any case, the most interesting result found when comparing Figure 12b with Figure 12a is that in some cases significant weight savings can be obtained in magnetics by this increase of the excitation frequency. For example, in the case of DAB-PS and DAB-TT, the 200 kHz magnetics weight is ∼170 g less than those required at 100 kHz. However, no significant weight savings are achieved by this increase of frequency for the 3p-DAB topology. In the case of CD, a significant weight reduction is only achieved for DC inductors. For the ABAC topology, both transformer and DC inductors reduce its weight when increasing switching frequency. In principle, the increase in switching frequency could be expected to yield more generalized and significant weight savings in AC magnetics. However, the moderate weight savings actually achieved could be explained by the fact that the decrease in required inductances associated with the increase of frequency is partially counteracted by an increase in AC resistances and core losses, which grow with frequency as well.

Summing up, we can conclude that the weight savings associated to increasing switching frequencies has important dependencies with the chosen topology. If we focus on most promising topologies, we can observe that doubling switching frequency up to 200 kHz yields no weight reduction in 3p-DAB, and a weight reduction of roughly 20% in the case of DAB-TT. In any case, the achieved weight reductions seem not large enough to compensate for the negative impact in losses increase associated to the use of higher frequencies.

3.3. Efficiencies at 200 kHz *and Use of GaN Switches*

GaN MOSFETs outperform Si MOSFETs, in terms of figures of merit that relate devices on resistance with parasitic capacitances [37]. In other words, they feature less conduction and/or switching losses than their Si counterparts, so it is expected that their use might yield a certain efficiency improvement in the LV MOSFETs. For this reason, we have assessed their impact in DAB topologies, which have proven to be the most promising ones for our particular application. In this section we have also analysed the impact of using a 200 kHz switching frequency. Note that the potential advantage of GaN switches is expected to be more significant at higher switching frequencies, as switching losses increase proportionally to switching frequencies.

In order to estimate the impact of GaN technology in our particular DAB designs, we have considered a half bridge of four paralleled GaN switches. Layout parasitics were modelled following manufacturer design guidelines [37], and a loss model based on SPCICE simulations was obtained, as a function of bus voltage and inductive load current. Obtained results for nominal LVDC voltage are depicted in Figure 13. Both GaN and Si MOSFETs half bridges feature very similar conduction losses, but GaN MOSFETs swtiching losses are roughly 1/3 those of the Si ones.

In Figure 14a we can see graphically that implementing GaN switches in the LV side leads to only 0.4% efficiency increase compared to the Si solution, due to lower switching losses of the GaN proposed switches. In Figure 14b we can see that doubling switching frequency has an important impact in converter average losses: 1.5% more losses in 3p-DAB and 1.1% more losses in single phase DAB designs. When switching frequency is doubled, both LV and HV switching losses are doubled, and magnetics losses change as well, according to manufacturer loss models. In particular, LV switching losses are the loss component that penalizes doubling switching frequency. Doubling switching frequency involves an efficiency decrease of roughly 1%, only due to the increase of LV

switching losses, for the chosen Si MOSFETs. Under this scenario, the use of GaN switches becomes an interesting technology from the efficiency point of view.

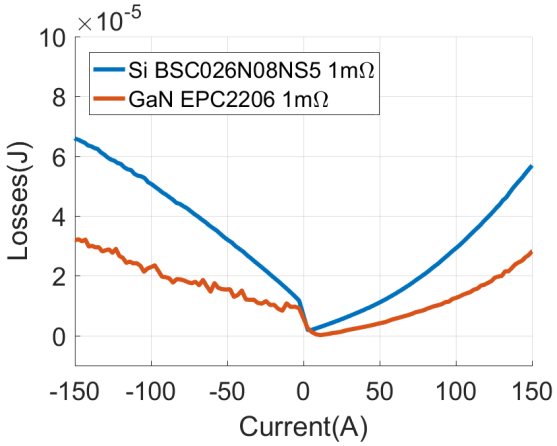
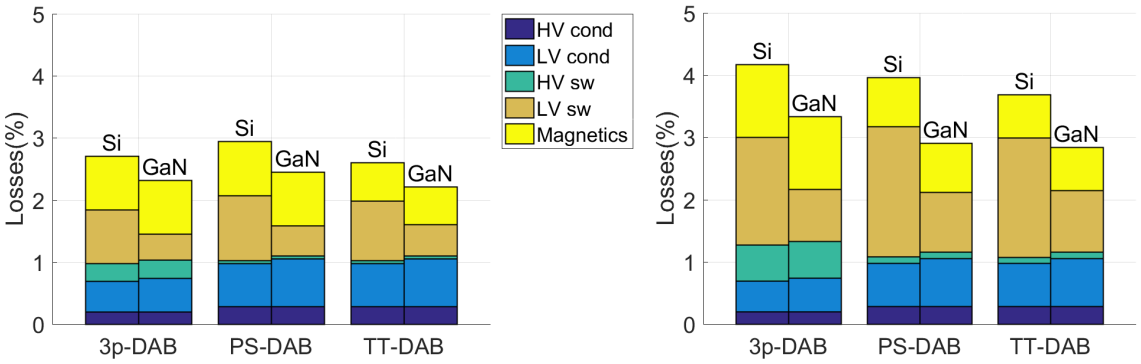


Figure 13. Simulated switching losses of four paralleled GaN (EPC2206) and Si (BSC026N08NS5) MOSFET, at 28 VDC.

As a particular result of this work, the use of 200 kHz switching frequency does not involve a very significant weight reduction compared to 100 kHz (see Section 3.2), and since GaN impact in average efficiency becomes relevant only at 200 kHz, the use of GaN is not justified in principle for this particular application. As far as the authors know, the field of application of these GaN swiches is typically limited to lower power applications, or multicell applications in which converters currents are distributed between many branches [23]. Implementation of GaN switches is specially challenging as power rating increases, mainly due to the complexity to effectively paralelize GaN MOSTETs by keeping low inductance and very symmetrical layout. In general, the robustness of GaN technology for these required power ratings has not been demonstrated. The required effort to implement GaN switches would be justified in a design that exploits better the increase in switching frequency to achieve a more significant weight reduction in passives.



(**a**) Switching frequency 100kHz (**b**) Switching frequency 200kHz

Figure 14. Average losses in % (converter losses divided by transferred power), including losses breakdown. DAB based topologies.GaN (EPC2206) vs Si (BSC026N08NS5) MOSFET comparison.

4. Conclusions

In this work we have carried out an thorough comparison of converter topologies that are good candidates for a bidirectional power converter linking a HV 270 VDC bus and a LV 28 VDC bus, which are of interest for developing advanced HVDC power distribution systems in more electrical and all electrical aircrafts.

In this analysis, an optimization in terms of efficiency in a wide operating range, and passives weight has been carried out. State-of-the-art semiconductors, and custom magnetics have been considered for this study. As far as the authors know, no recent comparative studies with these features exist. As an outcome, this work provides insight on several promising topologies for bidirectional isolated HVDC-LVDC power converters. In this work we have payed special attention to design trade-offs and comparison of wide bandgap devices with their Si counterparts.

In this work, we have started by imposing exigent requirements in terms of range of operation filtering and control requirements to justify the main design criteria that have been adopted. The analysis carried out has allowed us to conclude that, for these design considerations, using switching frequencies of 100 kHz seems to be preferable than 200 kHz, because doubling switching frequency leads to insufficient passives weight reduction. For example, 20% of estimated weight reduction in single phase DAB topologies, 27% in the case of ABAC, and insignificant changes in CD and 3p-DAB.

From the efficiency point of view 3p-DAB and DAB-TT show the best performance among the optimized designs at 100 kHz. Minimum efficiencies at full power (which determine maximum converter losses) in the whole HVDC-LVDC voltage range are 96.4% and 96.6%, respectively. By comparison, DAB-PS, ABAC, and CD yield minimum full power efficiencies of 95.7%, 95.3% and 89.2%, respectively. DAB-3p and DAB-TT also show highest average efficiencies (97.3%) for fixed nominal output voltage, full input voltage range, and half power to full power. ABAC and CD show the lowest average efficiencies: 96.8% and 95.5%, respectively. Moreover, CD performance presents a relatively high dependence with power transfer mode and power, having specially poor performance at high powers, and in boost mode.

Moreover, efficiency variation in the operating domain have been studied. With regard to this aspect, DAB topologies have the most uniform efficiencies in the optimization domain, especially DAB-TT (1.3% maximum difference). Regarding losses breakdown, it is interesting to note that LV losses are the dominant component in most topologies, mainly because of high LV currents. By contrast, HV switches losses are much smaller due to the low losses that are inherent to SiC technology and also because ZVS is achieved in most of the operating range in most topologies. The use of SiC involves an average efficiency increase of 0.8% compared to the best alternative option: Si MOSFET with fast recovery diode. In the case of the GaN solution, LV switching losses can be reduced to 1/3 approximately, which leads to average efficiency increase of 0.4% in DAB topologies.

Summing up, we have concluded that the best choice in terms of efficiency is DAB-TT, followed by 3p-DAB with little difference. Nevertheless, differences between topologies at 100 kHz are small, being the CD an exception. In terms of weight, at 100 kHz switching frequency, 3p-DAB is the best option. An additional advantage of 3p-DAB compared to DAB-TT is its modulator simplicity and its much lower filtering requirements. While filters size in 3p-DAB are only 2/3 the size of DAB-TT filters due to control conservative design considerations, filtering requirements are much lower in 3p-DAB, because of the phases inherent interleaving. This means that less additional passives for EMI filtering are expected to be required in 3p-DAB compared with other topologies. Taking all this into account, we conclude that 3p-DAB is the most suitable topology for our particular application and design constrains.

It must be pointed out that for this comparative work, we focused on a very specific voltage range, and a particular power range (half power to full power) which is of interest for the aeronautical industry. In that sense, results can be generalized only within this framework. We have also taken design decisions that are based on reasoned criteria, but that could be modified in a different context with a different set of specifications. In particular, a redefinition of custom magnetics design, a redefinition of filter design considerations to take more advantage of higher switching frequencies, or redefining filtering requirements according to standards might lead to different conclusions in some of the aspects treated in this work. Furthermore, more advanced control techniques that inherently deal with converter discrete and non linear nature, as Sliding Mode Control, might also be investigated, as it

might result in an increase in control robustness, and may relax certain constraints in filter dynamics. A detailed study of the impact of design criteria on topologies performance is considered by the authors as an interesting future work. Moreover, as a future work, we are contemplating extending this study to other promising topologies, such as resonant topologies.

Author Contributions: Conceptualization, J.B.-M. and M.A.M.-P.; methodology, J.B.-M.; software, Á.O.R.; validation, P.G.-V. and Á.O.R.; formal analysis, P.G.-V. and Á.O.R.; investigation, P.G.-V. and Á.O.R.; resources, M.A.M.-P.; data curation, Á.O.R.; writing—original draft preparation, J.B.-M. and Á.O.R.; writing—review and editing, J.B.-M. and M.A.M.-P.; visualization, Á.O.R. and P.G.-V.; supervision, M.A.M.-P. and J.B.-M.; project administration, M.A.M.-P.; funding acquisition, J.B.-M. and M.A.M.-P. All authors have read and agreed to the published version of the manuscript.

Funding: This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No.831942.

Conflicts of Interest: The authors declare no conflict of interest. The content of this article reflects the author's view and the European Comission is not responsible for any use that may be made of the information it contains.

References

1. ACARE. *Aeronautics and Air Transport: Beyond Vision 2020 (Towards 2050)*; Technical Report Towards 2050; ACARE: Taipei, Taiwan; 2010.
2. Rosero, J.; Ortega, J.; Aldabas, E.; Romeral, L. Moving towards a more electric aircraft. *IEEE A&E Syst. Mag.* **2007**, *22*, 3–9.
3. Roboam, X.; Sareni, B.; De Andrade, A. More Electricity in the air. *IEEE Ind. Electron. Mag.* **2012**, 233–259, doi:10.1016/b978-0-240-52023-0.50009-1.
4. Sarlioglu, B.; Morris, C.T. More Electric Aircraft: Review, Challenges, and Opportunities for Commercial Transport Aircraft. *IEEE Trans. Transp. Electrif.* **2015**, *1*, 54–64, doi:10.1109/TTE.2015.2426499.
5. Tariq, M.; Maswood, A.I.; Gajanayake, C.J.; Gupta, A.K. Aircraft batteries: Current trend towards more electric aircraft. *IET Electr. Syst. Transp.* **2017**, *7*, 93–103, doi:10.1049/iet-est.2016.0019.
6. Wheeler, P.; Bozhko, S. The more electric aircraft: Technology and challenges. *IEEE Electrif. Mag.* **2014**, *2*, 6–12, doi:10.1109/MELE.2014.2360720.
7. Hartmann, M. Ultra-compact and ultra-efficient Three-phase PWM Rectifier Systems for More Electric Aircraft. Ph.D. Thesis, ETH Zurich, Zurich, Switzerland, 2011.
8. Chen, J.; Wang, C.; Chen, J. Investigation on the selection of electric power system architecture for future more electric aircraft. *IEEE Trans. Transp. Electrif.* **2018**, *4*, 563–576, doi:10.1109/TTE.2018.2792332.
9. Emadi, A.; Ehsani, M. Aircraft power systems: Technology, state of the art, and future trends. *IEEE Aerosp. Electron. Syst. Mag.* **2000**, *15*, 28–32, doi:10.1109/62.821660.
10. Gao, F.; Bozhko, S.; Costabeber, A.; Asher, G.; Wheeler, P. Control Design and Voltage Stability Analysis of a Droop-Controlled Electrical Power System for More Electric Aircraft. *IEEE Trans. Ind. Electron.* **2017**, *64*, 9271–9281, doi:10.1109/TIE.2017.2711552.
11. Buticchi, G.; Costa, L.F.; Barater, D.; Liserre, M.; Amarillo, E.D. A Quadruple Active Bridge Converter for the Storage Integration on the More Electric Aircraft. *IEEE Trans. Power Electron.* **2018**, *33*, 8174–8186, doi:10.1109/TPEL.2017.2781258.
12. Krismer, F. Modeling and Optimization of Bidirectional Dual Active Bridge DC DC Converter Topologies. Ph.D. Thesis, ETH Zurich, Zurich, Switzerland, 2010. doi:10.3929/ethz-a-006395373.
13. Kheraluwala, M.N.; Gascoigne, R.W.; Divan, D.M.; Baumann, E.D. Performance Characterization of a High-Power Dual Active Bridge dc-to-dc Converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1294–1301, doi:10.1002/9780470179765.ch6.
14. Bai, H.; Mi, C. Eliminate reactive power and increase system efficiency of isolated bidirectional dual-active-bridge dc-dc converters using novel dual-phase-shift control. *IEEE Trans. Power Electron.* **2008**, *23*, 2905–2914, doi:10.1109/TPEL.2008.2005103.
15. Zhao, B.; Song, Q.; Liu, W. Power characterization of isolated bidirectional dual-active-bridge dc-dc converter with dual-phase-shift control. *IEEE Trans. Power Electron.* **2012**, *27*, 4172–4176, doi:10.1109/TPEL.2012.2189586.

16. Krismer, F.; Kolar, J.W. Efficiency-optimized high-current dual active bridge converter for automotive applications. *IEEE Trans. Ind. Electron.* **2012**, *59*, 2745–2760, doi:10.1109/TIE.2011.2112312.
17. Flores, L.A.; García, O.; Oliver, J.A.; Cobos, J.A. High-frequency Bi-directional DC–DC converter using two inductor rectifier. *IECON Proc. (Ind. Electron. Conf.)* **2006**, 2793–2798, doi:10.1109/IECON.2006.347424.
18. De Doncker, R.W.; Divan, D.M.; Kheraluwala, M. A three-phase soft-switched high power density dc/dc converter for high power applications. *IEEE Trans. Ind. Appl.* **1991**, *27*, 63 – 73.
19. Bhat, A.K.S.; Member, S. Fixed-Frequency PWM Series-Parallel Resonant Converter. *IEEE Trans. Ind. Appl.* **1992**, *28*, 1002–1009.
20. Pan, X.; Li, H.; Liu, Y.; Tianyang, Z.; Ju, C.; Rathore GAE, A.K. An Overview and Comprehensive Comparative Evaluation of Current-Fed Isolated Bidirectional DC–DC Converter. *IEEE Trans. Power Electron.* **2019**, *35*, 2737–2763, doi:10.1109/tpel.2019.2931739.
21. De, D.; Castellazzi, A.; Lamantia, A. 1.2 kW dual-active bridge converter using SiC power MOSFETs and planar magnetics. In Proceedings of the 2014 International Power Electronics Conference, IPEC-Hiroshima—ECCE Asia 2014, Hiroshima, Japan, 18–21 May 2014; pp. 2503–2510, doi:10.1109/IPEC.2014.6869941.
22. Buticchi, G.; Costa, L.; Liserre, M. Improving System Efficiency for the More Electric Aircraft: A Look at dc\/dc Converters for the Avionic Onboard dc Microgrid. *IEEE Ind. Electron. Mag.* **2017**, *11*, 26–36, doi:10.1109/MIE.2017.2723911.
23. Brandelero, J.C. Conception et réalisation d ' un convertisseur multicellulaire DC–DC isolé pour application aéronautique. Ph.D. Thesis, INP de Toulouse, Toulouse, France, 2015.
24. Asfaux, P.; Bourdon, J. Development of a 12 kW isolated and bidirectional DC–DC Converter dedicated to the More Electrical Aircraft: The Buck Boost Converter Unit (BBCU). In Proceedings of the PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management, Nuremberg, Germany, 10–12 May 2016; pp. 1814–1821.
25. Tarisciotti, L.; Costabeber, A.; Chen, L.; Walker, A.; Galea, M. Current-Fed Isolated DC–DC Converter for Future Aerospace Microgrids. In *IEEE Transactions on Industry Applications*; Institute of Electrical and Electronics Engineers Inc.: Piscataway, NJ, USA, 2019; Volume 55, pp. 2823–2832, doi:10.1109/TIA.2018.2889845.
26. Department of Defense USA. *MIL-STD-704F Aircraft Electric Power Characteristics*; 2004.
27. Canciello, G.; Cavallo, A.; Lo Schiavo, A.; Russo, A. Multi-objective adaptive sliding manifold control for More Electric Aircraft. *ISA Trans.* **2020**, doi:10.1016/j.isatra.2020.07.032.
28. Cavallo, A.; Canciello, G.; Guida, B. Supervisory control of DC–DC bidirectional converter for advanced aeronautic applications. *Int. J. Robust Nonlinear Control* **2018**, *28*, 1–15, doi:10.1002/rnc.3851.
29. Cavallo, A.; Canciello, G.; Russo, A. Integrated supervised adaptive control for the more Electric Aircraft. *Automatica* **2020**, *117*, doi:10.1016/j.automatica.2020.108956.
30. Cavallo, A.; Canciello, G.; Guida, B.; Kulsangcharoen, P.; Yeoh, S.S.; Rashed, M.; Bozhko, S. Multi-objective supervisory control for DC–DC converters in advanced aeronautic applications. *Energies* **2018**, *11*, 3216, doi:10.3390/en11113216.
31. Sabate, J.a.; Vlatkovic, V.; Ridley, R.B.; Lee, F.; Cho, B.H. Design considerations for high voltage high power full bridge zero voltage switched pwm converter. In Proceedings of the Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition, Los Angeles, CA, USA, 11–16 March 1990; pp. 275–284.
32. Xuewei, P.; Rathore, A.K. Novel bidirectional snubberless naturally commutated soft-switching current-fed full-bridge isolated DC–DC converter for fuel cell vehicles. *IEEE Trans. Ind. Electron.* **2014**, *61*, 2307–2315, doi:10.1109/TIE.2013.2271599.
33. Yamamoto, K.; Hiraki, E.; Tanaka, T.; Nakaoka, M.; Mishima, T. Bidirectional DC–DC converter with full-bridge/push-pull circuit for automobile electric power systems. In Proceedings of the PESC Record—IEEE Annual Power Electronics Specialists Conference, Montreal, QC, Canada, 3–10 January 2006; doi:10.1109/PESC.2006.1711776.
34. Zhang, B.; Yang, J. Effect and utilization of common source inductance in synchronous rectification. In Proceedings of the Twentieth Annual IEEE Applied Power Electronics Conference and Exposition (APEC 2005), Austin, TX, USA, 6–10 March 2005; Volume 3, pp. 1407–1411.

35. Wang, J.; Chung, H.S.H.; Li, R.T.H. Characterization and experimental assessment of the effects of parasitic elements on the MOSFET switching performance. *IEEE Trans. Power Electron.* **2013**, *28*, 573–590, doi:10.1109/TPEL.2012.2195332.
36. Chen, Z.; Boroyevich, D.; Burgos, R. Experimental parametric study of the parasitic inductance influence on MOSFET switching characteristics. In Proceedings of the 2010 International Power Electronics Conference—ECCE Asia (IPEC 2010), Sapporo, Japan, 21–24 June 2010; pp. 164–169, doi:10.1109/IPEC.2010.5543851.
37. Reusch, D.; Strydom, J. Effectively paralleling gallium nitride transistors for high current and high frequency applications. In Proceedings of the Conference Proceedings—IEEE Applied Power Electronics Conference and Exposition—APEC 2015, Charlotte, NC, USA, 15–19 March 2015; pp. 745–751, doi:10.1109/APEC.2015.7104433.