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A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

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Abstract: This paper presents a methodology to design a wideband radio frequency variable gain amplifier (RF-VGA) in a low-cost SiGe BiCMOS 0.35 µm process. The circuit uses two Class A amplifiers based on second-generation controlled current conveyors (CCCII). The main feature of this circuit is the wideband input match along with a reduced NF (5.5–9.6 dB) and, to the authors' knowledge, the lowest die footprint reported (62 × 44 µm^2 area). The implementation of the RF-VGA based on CCCII allows a wideband input match without the need of passive elements. Due to the nature of the circuit, when the gain is increased, the power consumption is reduced. The architecture is suitable for designing wideband, low-power, and low-noise amplifiers. The proposed design achieves a tunable gain of 6.7–18 dB and a power consumption of 1.7 mA with a ±1.5 V DC supply. At maximum gain, the proposed RF-VGA covers from DC up to 1 GHz and can find application in software design radios (SDRs), the low frequency medical implant communication system (MICS) or industrial, scientific, and medical (ISM) bands.

Keywords: radio frequency variable gain amplifier (RF-VGA); wideband amplifier; broadband amplifier; second-generation controlled current conveyor (CCCII); BiCMOS; ISM; MICS; SDR

1. Introduction

In radio frequency integrated circuits, the design of wideband amplifiers has been intensively discussed over the past few decades [1]. The most widely used wideband amplifier architecture is the distributed amplifier, which requires high power consumption and a large area due to the considerable number of stages and the extensive use of inductors [2–4].

Another commonly used technique is the use of feedback amplifiers [5–10]. This solution offers a good return loss, but, due to the feedback, it is difficult to achieve a low noise figure with a reasonable power consumption.

As an alternative to these two previous topologies, some authors have proposed the design of wideband circuits by converting narrowband circuits into broadband [11–13]. This is usually achieved by modifying the input matching network to act as a broadband filter and replacing the narrowband load (typically a tank circuit) with any of the wideband RC load implementations: series-peaking, shunt-peaking, shunt-series-peaking, etc. [14–16]. Again, as in the case of the distribute amplifier technique, the main limitation of this solution is the area as they use a large number of inductors. Note that the issues of large area and high power consumption are aggravated when variable gain is desired.

To reduce the area constraints, some authors have proposed the use of common-base or common-gate wideband amplifiers [14–16]. These topologies take advantage of the fact that, in such configurations, it is possible to obtain a broadband input impedance equal to 50 Ω by properly biasing the transistor. However, the gain and noise figure are determined by this biasing and consequently fixed to a certain value.

At system level, when implementing a wideband analog RF front-end, the most popular scheme includes a wideband low noise amplifier (LNA) followed by a variable gain amplifier (VGA). This maximizes the dynamic range of the upcoming stages and prevents the saturation of the receiver if a high-powered signal is received [17]. In these cases, the implementation of a wideband RF-VGA is of upmost interest.

This work addresses the design of a very compact, low power, low voltage, and high bandwidth RF-VGA using second generation controlled current conveyors. A CCCII is a four terminal device that can perform many useful analog signal processing functions when arranged with other electronic elements in specific circuit configurations [18]. CCCIIs have been successfully used in high frequency current mode applications such as filters [19] and LNAs [20]. The proposed radio frequency variable gain amplifier (RF-VGA) is based in the CCCII proposed in [21] and has been designed and fabricated in a low cost 0.35 µm SiGe BiCMOS technology. The rest of the paper goes as follows: Section 2 reviews the CCCII and describes the proposed RF-VGA topology and the design methodology, Section 3 focuses on the circuit performance and the analysis of the obtained results; finally, some conclusions are drawn in Section 4.

2. RF-VGA Based on the Current Conveyor

CCCIIs can be used to implement numerous functions, such as filtering, amplification, or impedance transformation. They also provide better performance than traditional OTAs, namely, improved power consumption and larger cut-off frequency [19].

A CCCII is a device with three ports (X, Y and Z) and a DC bias current (I_0). Each port is characterized by an impedance (Z_X, Z_Y and Z_Z) resulting from the implementation of the conveyor with non-ideal components. These impedances are defined by parasitic elements, which are highly dependent on the selected technology of fabrication and the bias current I_0. Thus, the concept of controlled current conveyor appears due to this dependence on I_0. The relationship that governs the interactions between the ports of the conveyor is defined as follows:

- between ports X and Z the device acts as a current follower,
- between ports Y and X it operates as a voltage follower,
- between ports Z and Y it behaves as a transconductor.

The matrix that defines these relationships is given by

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} Y_Y(I_0) & 0 & 0 \\ \beta(s) & Z_X(I_0) & 0 \\ 0 & \alpha(s) & Y_Z(I_0) \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

where Y_Y is the conductance of port Y, and Y_Z, the conductance of port Z. In addition, the terms $\alpha(s)$ and $\beta(s)$ represent the unity current and voltage transfer functions. The resistive component of Z_X (defined as R_X) is particularly relevant since it can be used to define the interaction between ports.

Variable gain amplifiers can be implemented using CCCIIs [19–21], where the gain tuning is performed by means of adjusting the bias current of the conveyor. The dependence of R_X on the bias current I_0 can be exploited to provide wideband input matching without including a single passive component, resulting in a circuit with a very low input return loss. This situation is desirable in scenarios where the amplifier is the first integrated circuit in the reception path. For example, if a preceding LNA is added externally, the proposed RF-VGA facilitates impedance matching with

this element, and the signal coming from the LNA is received with a very low loss. In addition, the proposed design can potentially obtain a high cut-off frequency and low die footprint due to the reduced number of active devices needed to implement the conveyor.

To implement an RF-VGA, two CCCII blocks are connected as shown in Figure 1 [20]. Provided that the impedances Z_{X1} and Z_{X2} are entirely resistive, $V_{IN}(t)$ is transformed into a current $I_{IN}(t)$. This current is then converted into a voltage signal again thanks to Z_{X2}. Due to the relationship between R_X and the bias current I_0, it can be proved that the gain G of the amplifier reduces to:

$$G = \frac{V_{OUT}(t)}{V_{IN}(t)} = \frac{I_{01}}{I_{02}} \tag{2}$$

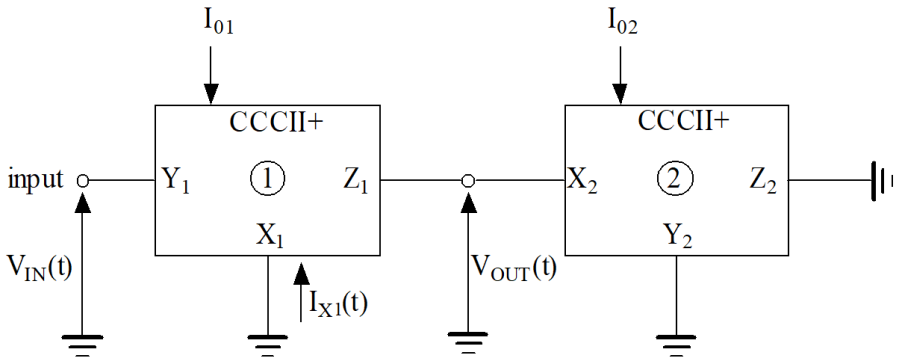

Figure 1. Connection of two CCCII blocks to provide voltage amplification.

Since the node Y_1 presents a high input impedance [19], the input signal is applied at node X_1. By doing so, the input impedance is reduced and can be controlled by the bias current I_{01}. Thus, the input impedance Z_{IN} of the RF-VGA can be adjusted by means of adjusting the value of the bias current I_{01}, which is fixed to obtain $|Z_{IN}| = 50\ \Omega$.

The value of the bias current I_{01} can be fixed to perform wideband input matching, and so the gain can be adjusted by setting the value of I_{02}. Due to the inversely proportional relationship given by (2), it is possible to increase the gain by reducing the bias current I_{02}. Therefore, higher gain settings lead to lower power consumption. A simple Class-A implementation scheme with CCCIIs is shown in Figure 2a. To obtain the structure depicted in Figure 1, nodes Z_1 and X_2 must be connected together, yielding the circuit depicted in Figure 2b. As mentioned above, the input signal is applied at node X_1 to facilitate input matching, allowing the elimination of transistor Q_{11}. The resulting scheme after simplification is presented in Figure 3. With this result, the number of BJTs is reduced as much as possible, yielding a higher cut-off frequency and a better noise performance [22]. The required values of the bias current I_{01} obtained in simulation to achieve a 50 Ω input impedance are plotted in Figure 4 for various transistor areas from the 0.35 µm SiGe design kit used.

The voltage gain and the bandwidth of the RF-VGA are plotted in Figure 5. The values between 100 µA and 250 µA present a trade-off between gain and bandwidth and can be used to determine the optimal combination of device area and bias current I_{02}. When I_{02} augments, the gain of the circuit drops while the bandwidth raises. The gain is not significantly affected by the variation in the transistor area, but, as expected, the bandwidth is increased if the area is reduced. Although the RF-VGA may be preceded by an LNA, its noise figure (NF) is one of the most relevant parameters in the design. If the LNA gain is low, the RF-VGA must provide a reduced NF and high gain to avoid degradation of the receiver performance.

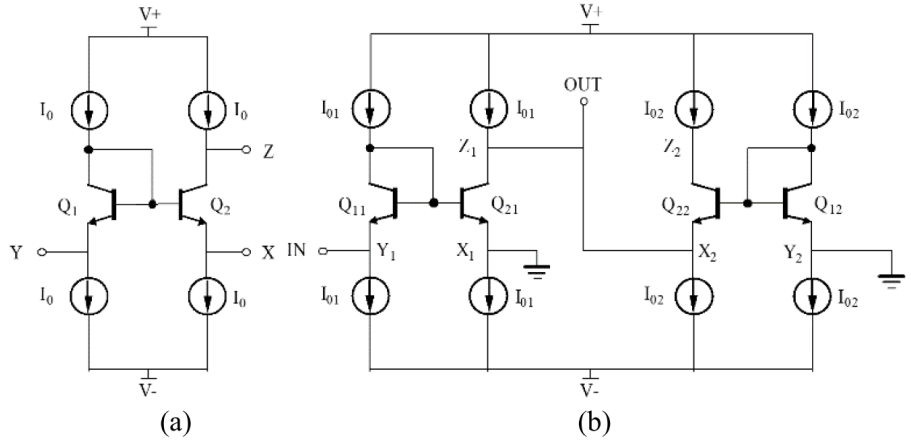

Figure 2. Class-A CCCII basic schematic (**a**) and topology of a voltage-mode amplifier using two basic class-A blocks (**b**).

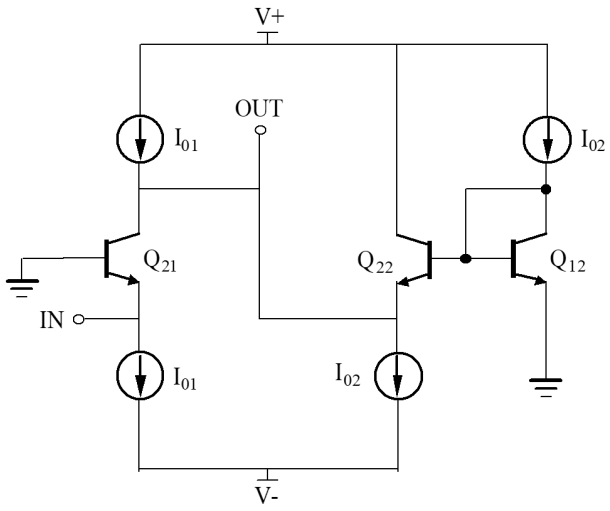

Figure 3. Schematic of the RF-VGA after simplification.

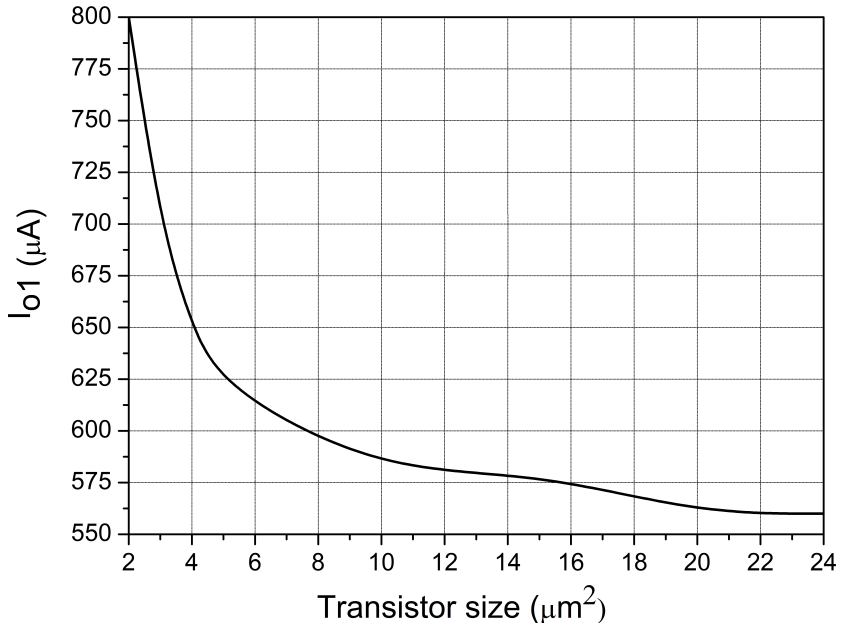

Figure 4. Bias current I_{01} vs. transistor size to obtain an input impedance of 50 Ω.

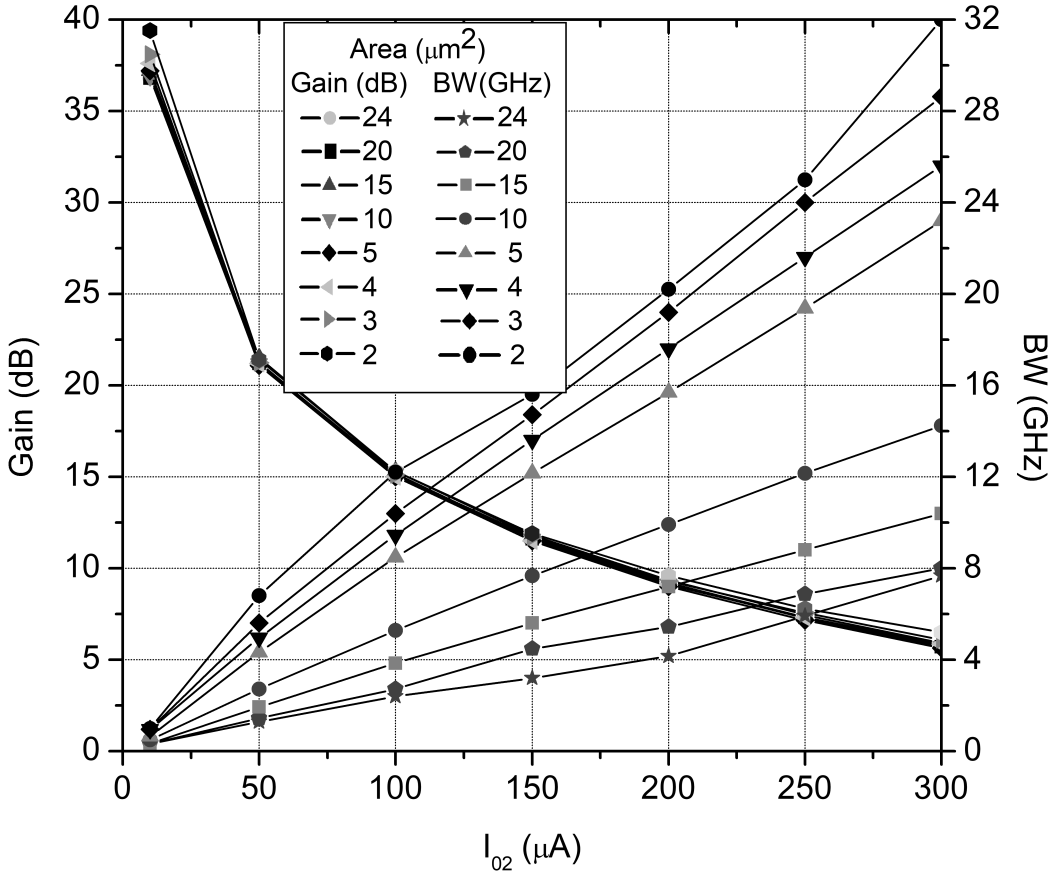

Figure 5. Simulated gain and bandwidth results of the RF-VGA at $V_{DC} = \pm 1.5$ V.

Depending on the application of interest, a trade-off between gain, noise, and bandwidth must be considered by the designer. In this implementation, the number of elements in the signal path is kept as low as possible (only tree BJTs), and there is a total absence of passive elements. Consequently, the noise introduced by spurious elements is minimized and the main noise contribution is due to the input transistor Q_{21}. Figure 6 depicts the simulated NF of the circuit for different transistor areas, where it is shown that the NF decreases when the device area is increased. The noise figure of the RF-VGA is also plotted against I_{02} in Figure 7 for a transistor area of 20 μm^2. Note that the noise figure is strongly dependent on the bias current, so that, when I_{02} increases, the gain is reduced and the NF augments. If a high gain and a low NF is desired, a lower I_{02} and a higher transistor area are required. However, this situation limits the achievable bandwidth since a low bias current combined with a high aspect ratio yields a reduced frequency performance (see Figure 5). As a result, a trade-off between noise figure, gain, and bandwidth is present and should be considered depending on the design specifications.

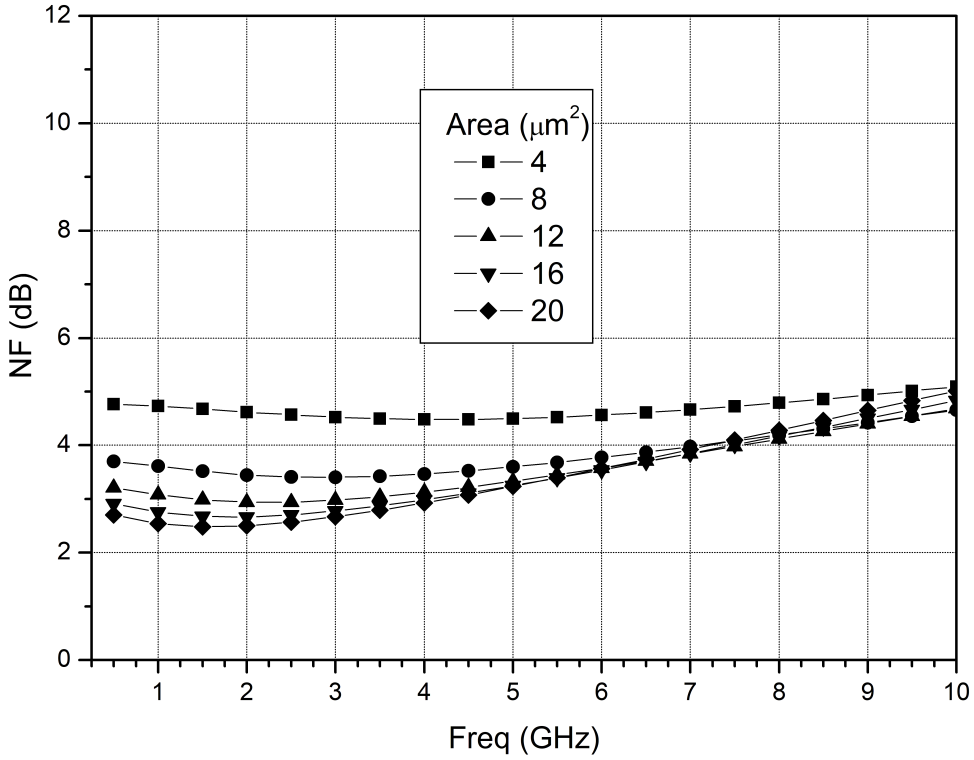

Figure 6. Noise figure vs. transistor area.

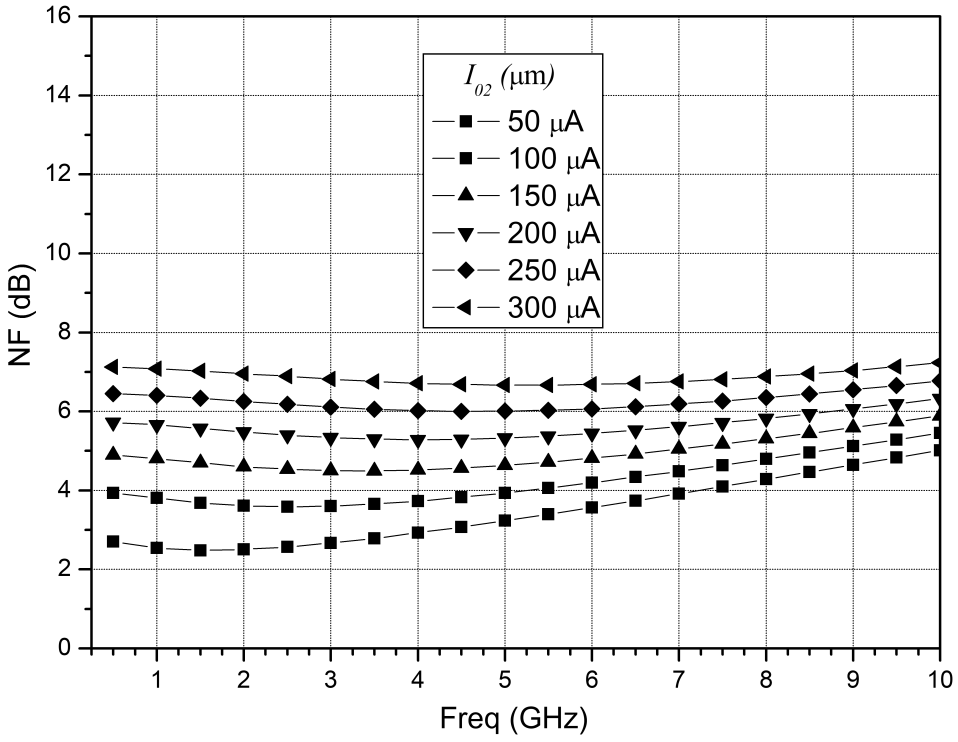

Figure 7. Noise figure vs. I_{02} for a transistor with 20 μm^2.

The final RF-VGA schematic is shown in Figure 8, where the current sources have been replaced with MOS transistors. The RF-VGA was designed and laid out in a BiCMOS SiGe 0.35 μm process with a DC supply of ±1.5 V. The layout of the circuit is presented in Figure 9. The layout was realized taking into account critical aspects of analog RFICs, such as circuit symmetry and transistor matching techniques to reduce PVT variations. The selected areas for each transistor were chosen to achieve a

maximum gain of 18 dB and a 900 MHz bandwidth with a total current consumption below 2 mA. The size of Q_{21} is 20 μm^2, which is twice the size of Q_{12} and Q_{22}, with 10 μm^2 each. The aspect ratio of the NMOS and PMOS transistors is 20/1 (μm/μm).

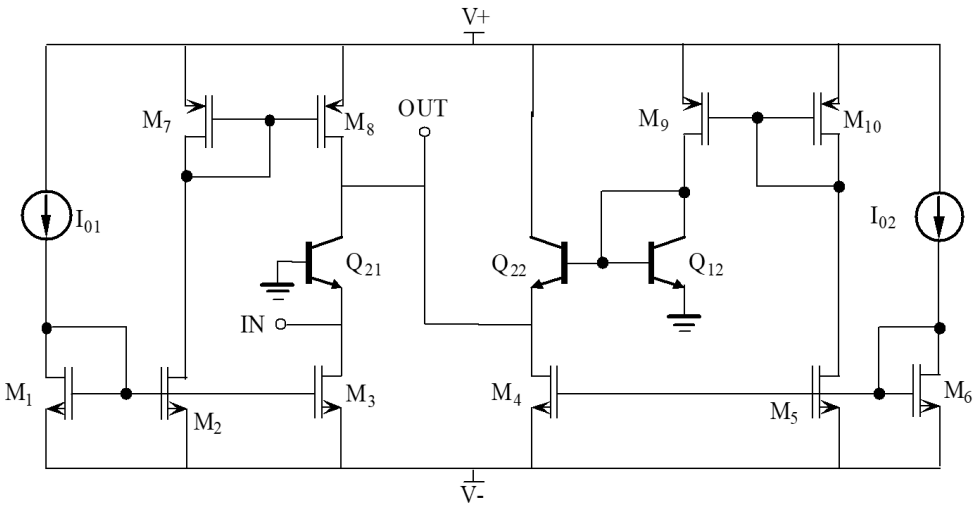

Figure 8. Schematic of the proposed RF-VGA.

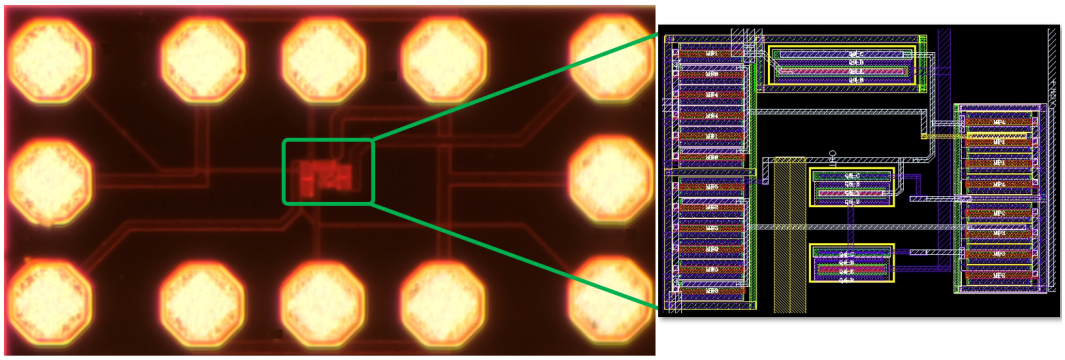

Figure 9. Die micro-photograph of the RF-VGA.

3. Measurements

Probe pads were added for on–wafer measurements. Two ground-signal-ground (GSG) and two signal-ground-signal (SGS) pads structures with 150 μm pitch were used. The DC supply is ±1.5 V and the amplifier draws a current of 1.7 mA. The total chip size of the RF-VGA including pads is 800 × 430 μm^2, but the core of the circuit occupies an area as low as 62 × 44 μm^2. The voltage gain of the RF-VGA is plotted in Figure 10 for a frequency range of DC–3 GHz vs. bias current I_{02}. A good agreement between measurement and simulation can be found with an error below ±1.1 dB in the entire band. As expected, when I_{02} is increased, the gain of the circuit decreases while the bandwidth raises. The simulation and measurement results of the NF of the proposed design are depicted in Figure 11. As can be seen, the NF increases with the bias current I_{02}. A reduced bias current (i.e., higher gain) is needed if a low noise figure is required. As mentioned above, the drawback is a reduction in the bandwidth of the amplifier. In many applications, it is desirable to extend the bandwidth thus a multistage approach or a bandwidth enhancement technique would be needed to obtain a high-gain and wide-band. For NF, the error between simulation and measurement is below 1.4 dB.

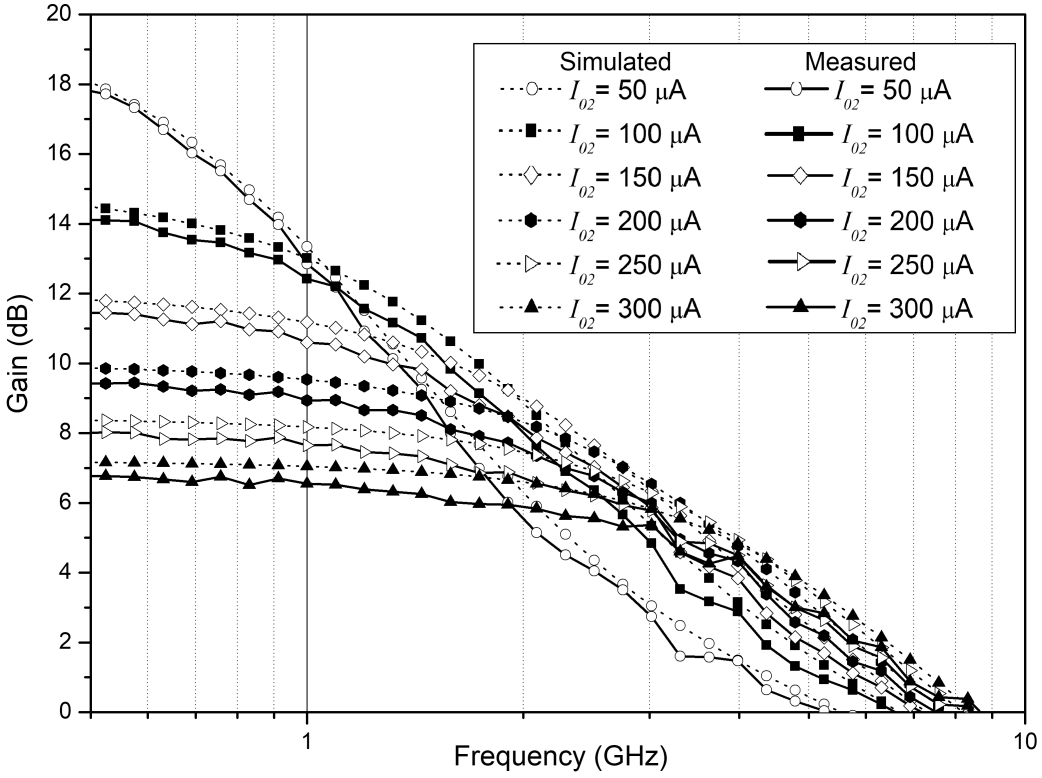

Figure 10. Measured and simulated gain of the RF-VGA for different bias currents I_{02}.

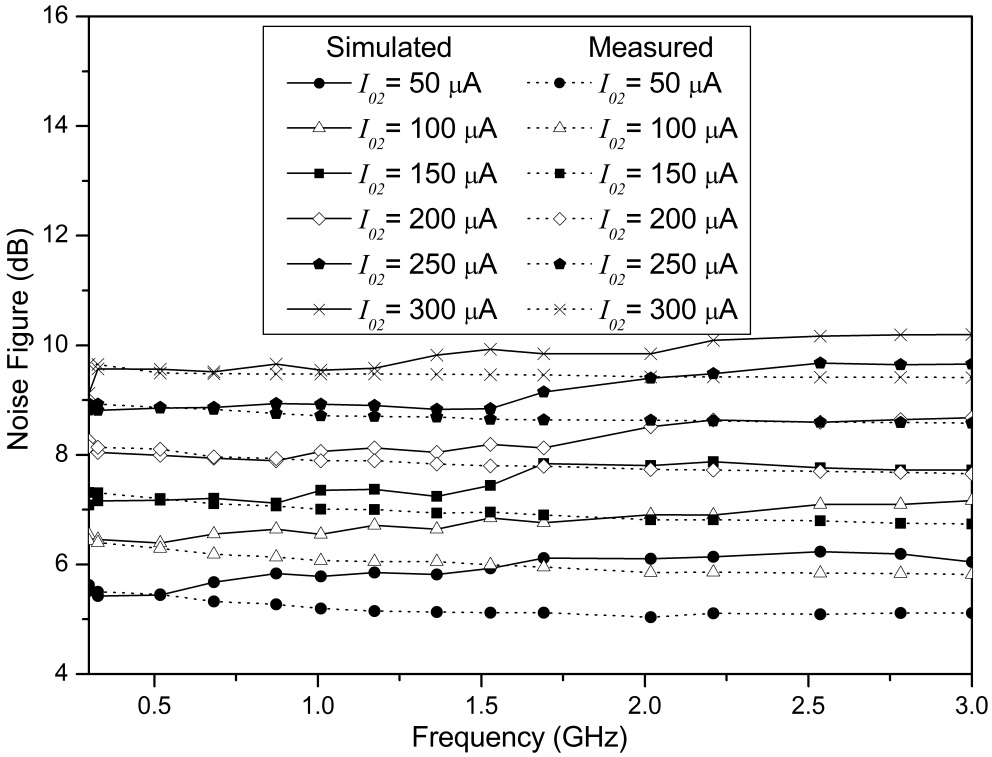

Figure 11. Measured and simulated NF of the RF-VGA for different bias currents I_{02}.

Another key parameter for the performance of the RF-VGA is the input return loss. When the LNA is implemented externally, the RF-VGA is the first integrated device in the receiver; thus, a broadband 50 Ω input match is required. The simulated and measured S_{11} are shown in Figure 12, where the measured magnitude for the S_{11} is better than 20 dB for frequencies up to 10 GHz.

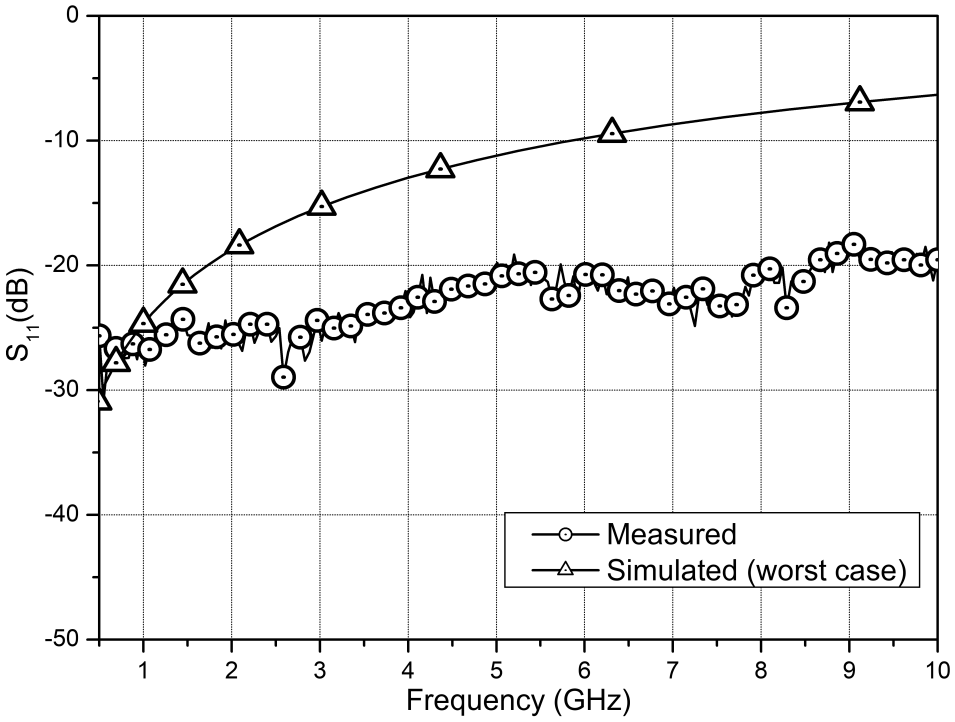

Figure 12. Measurement and simulation of the input return loss S_{11} for for $I_{01} = 600$ μA and $I_{02} = 50$ μA.

The linearity of the proposed RF-VGA was evaluated by measuring the input 1-dB compression point (P_{1dB}) using a test tone of 666 MHz. The measurement results for maximum gain settings (I_{01} = 600 μA and I_{02} = 50 μA) are plotted in Figure 13, obtaining a value of –20.18 dBm for the input P_{1dB}.

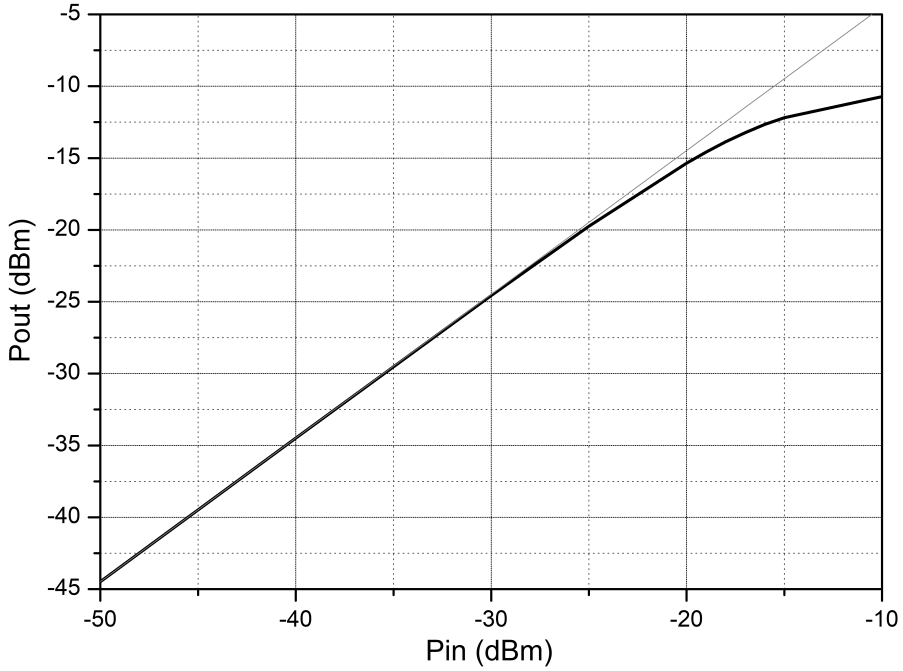

Figure 13. Measurement of the input 1-dB compression point for $I_{01} = 600$ μA and $I_{02} = 50$ μA.

A summary of the performance of the proposed RF-VGA versus I_{02} is presented in Table 1 for $I_{01} = 550$ µA and $V_{DC} = \pm 1.5$ V. A brief overview of similar works available in the literature is given in Table 2 [23–30]. With the exception of [26], which uses 40 nm technology, our work has better bandwidth. Compared with other authors, a good trade-off between gain and bandwidth is obtained. We have achieved a competitive noise figure, not exceeding 9.6 dB for the worst case. The power consumption is small, but not the lowest one, this is because the others authors have used more advanced technologies. To the best of the authors' knowledge, the present work achieves the lowest area occupation reported in the literature while showing competitive performances in terms of gain, NF and BW with a power consumption similar to that of other proposed solutions.

Table 1. Summary of measured results with $I_{01} = 550$ µA and $V_{DC} = \pm 1.5$ V.

I_{02} [µA]	50	100	150	200	250	300
Gain [dB]	18	14	11.4	9.4	8	6.7
BW [GHz]	0.85	1.3	1.9	2.7	3.26	4.3
NF [dB]	5.5	6.5	7.2	8	8.9	9.6
$\lvert Z_{out}\rvert$[Ω]	500	256	175	133	105	90

Table 2. Performance comparison.

Reference	Gain [dB]	BW [GHz]	NF [dB]	Vdd [V]	Power [mW]	Area [mm^2]	Technology
[23]	−10–50	2	17–30	1.0	2.5	0.013	90 nm CMOS
[24]	−28–23	1	3.9–5.2	1.5	8.2	0.051	0.18 µm CMOS
[25]	2–24	2–2.2	24–29	1.2	3.5	0.010	65 nm CMOS
[26]	18.4–27.1	9.3	3.3–4.4	1.1	21.5–31.4	0.26	40 nm CMOS
[27]	−25–20	0.2–3.3	3.4–20	1.2	19	0.15	130 nm CMOS
[28]	−54–46	0.98–2.15	8–15	–	–	0.539	0.18 µm CMOS
[29]	4.6–12	0.4–4.5	3–9	1.5	22.5	1	28 nm FDSOI CMOS
[30]	−19–21	4	17–47	1.2	3.5	0.012	65 nm CMOS
This work	**6.7–18**	**0.85–4.3**	**5.5–9.6**	**±1.5**	**5.1**	**0.003**	**0.35 µm BiCMOS**

4. Conclusions

A very compact, low power, low voltage and high bandwidth RF-VGA based on the cascade connection of two CCCII blocks has been presented. The circuit was implemented in a standard low cost SiGe BiCMOS 0.35 µm process. A gain control from 6.7 to 18 dB is obtained varying the bias current of the circuit. The present work achieves, to the authors' knowledge, the lowest area occupation. For a polarization current I_{02} of 50 µA, the circuit achieves a power consumption of 1.7 mA with a ±1.5 V DC supply, an input return loss better than 20 dB from DC up to 10 GHz and a noise figure from 5.5 dB at maximum gain settings to 9.6 dB at minimum gain settings. Finally, the measured P_{1dB} is −20.18 dBm. The RF-VGA achieves a very competitive trade-off between gain, noise figure, input return loss, power consumption, and die footprint, making this architecture suitable for the design of compact wide-band, low-power, and low-noise variable gain amplifiers.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

BW	bandwidth
CCII	second-generation current conveyor
CCCII	second-generation controlled current conveyor
ISM	industrial, scientific and medical
LNA	low noise amplifier
MICS	medical implant communication system
RF-VGA	radio frequency variable gain amplifier
SDR	software design radio
VGA	variable gain amplifier

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