Voltage Mode Driver for Low Power Transmission of High Speed Serial AER Links

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***Abstract*—This paper presents a voltage-mode high speed driver to transmit serial AER data in scalable multi-chip AER systems. To take advantage of the asynchronous nature of AER (Address Event Representation) streams, this implementation allows an energy efficient burst-mode operation. This is achieved by switching on/off the driver in data pauses to reduce static power consumption. Impedance matching is calibrated continuously to track temperature variations, obtaining an optimal performance without degrading the data rate. Power management techniques for switching drivers are discussed and an internally compensated high speed regulator is presented. The system has been designed in a 0.35μm CMOS technology to transmit data rates up to 500Mbps using Manchester enconding. Layout extracted simulation results are presented, which include all interconnect parasitics. Estimated peak rate is 15Meps for 32 bit events. Simulated power consumption of transmitter and receiver at peak rate is 33.2mW, while below 100 Keps is 1.3mW.**

I. Introduction

Building complex event-driven processing systems will require several tens to hundreds of individual AER (Address Event Representation) processing chips on a single PCB [1]. This enforces the use of serial AER links to reduce interconnect complexity. Commercial serial links need to be kept transmitting all the time to maintain transmitter and receiver synchronized. In multi-layered processing systems, event rate tends to reduce as information processing progresses. Thus, the sustained event rate of AER links is well below their peak rate. If serial links, which consume several mWs per link, can be turned on/off quickly, overall power consumption could be reduced by several orders of magnitude depending on event traffic. Let's call switchable "driver" a serial driver that can be turned on/off quickly.

In the past, we proposed a serializer/deserializer for serial AER links, capable of stopping and starting data transmission using only two bits of overhead [2]. However, it uses a conventional current-mode LVDS non-switchable driver. Manchester coding was used to embed the transmission clock in the AER data flow. The receiver was able to extract synchronization information on the fly even when there were long pauses in the transmission. This way, no synchronization commas had to be transmitted during event pauses.

For non-switchable links, static current consumption is constant because bias sources are always active. If this power consumption is integrated during a ΔT time window and driver current is I_{on}, power is $V_{dd} I_{on} \Delta T$. For a switchable driver, current consumption is not constant and depends on event rate. In this case, power consumption is:

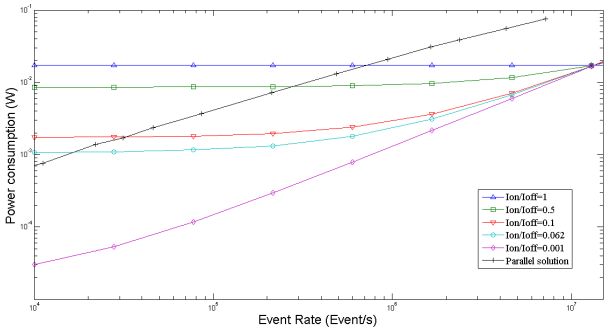

Fig. 1. Driver power consumption vs output data rate.

$$P_{off} = (Ev T_f I_{on} + I_{off} - Ev T_f I_{off})\, \Delta T V_{dd} \qquad (1)$$

where Ev is the event rate, I_{off} is the idle state current and T_f is the time needed to transmit a single event.

Fig. 1 shows a comparison between power consumption in switchable and non-switchable ($I_{on}/I_{off} = 1$) driver implementations. Different curves were plotted depending on I_{on}/I_{off} ($I_{on} = 5.2mA$, $T_f = 75ns$). For comparison, Fig. 1 also includes the power consumption of a fully parallel 32-bit AER part (based on data from [3]). The curve $I_{on}/I_{off} = 0.062$ corresponds to the driver presented in this paper. Minimizing current consumption in pauses improves AER link energy efficiency and improves reliability of multi-chip systems. In this paper we present a switchable voltage mode driver for this purpose.

II. Comparison Between Current-Mode and Voltage-Mode Drivers

Current mode drivers switch a constant current source of several mA to produce an output differential voltage over a termination resistor. Implementing a switching mechanism to disable these large currents requires dedicated circuit techniques [4] that complicate hardware and increase power consumption. On the other hand, voltage mode drivers switch a constant voltage through a termination resistor. As impedance of the switch can be easily controlled by an efficient pre-driver,

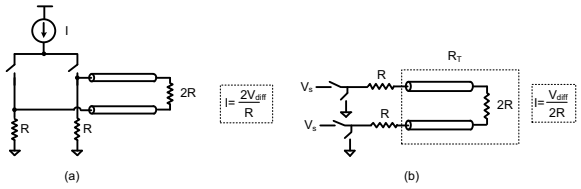

Fig. 2. Comparison between current-mode (a) and voltage-mode (b) termination schemes.

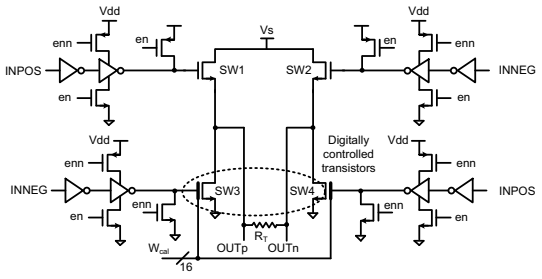

Fig. 3. Voltage-Mode driver and pre-driver circuits.

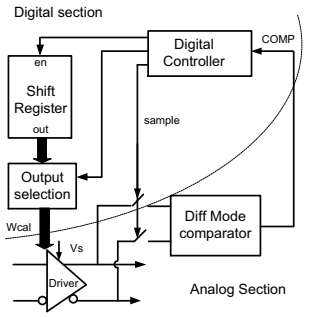

Fig. 4. Calibration circuit system level description.

voltage-mode drivers are very suitable to implement energy efficient burst mode serial transmitters.

Furthermore, an ideal voltage-mode driver with differential receiver termination enables a potential reduction in driver power. Fig. 2 shows how the termination scheme used in this kind of circuits requires four times less current flowing through the driver for a desired differential output amplitude. On the other hand, lower supply voltages can be used for voltage-mode drivers due to their low common mode and low swing requirements. However, real power consumption is also influenced by output impedance control or pre-driver power.

Power saving advantages are achieved at the cost of reducing maximum transmission rate. Using AC coupling and a matched channel, current-mode approaches can transmit data over several meters of cable lengths. Voltage-mode drivers are intended to be used in short-haul chip to chip interconnect while dissipating low power [5]. The present driver is targeted for use in multi-chip architectures, where units are located on the same board at a centimeter distance along with a system requirement to integrate many such units.

While impedance matching is easy in current-mode drivers, it is an important issue in voltage-mode circuits. In these solutions, switch resistance is used to match the termination resistor. As this parameter is severely affected by temperature and process variations, some kind of calibration is required to keep reflections and differential output amplitude within the desired target values. Some published solutions use an additional control loop to tune the driver characteristic [5]-[6]. However, this extra loop requires significant high static power. Our approach is based on [7], where impedance of the switch is digitally tuned. This method stores the information in digital registers and allows the designer to reduce static power consumption associated with impedance.

III. Voltage-Mode Link Description

A. Driver Circuit

Fig. 3 shows a schematic of a low swing voltage mode driver that only uses NMOS switches SW1-SW4. Desired differential output amplitude of 500mV is generated at $R_T = 100\Omega$ by setting $V_s = 1V$. R_T in Fig. 3 accounts for the off-chip resistive components (transmission line and receiver impedance termination). The two R resistors in Fig. 2-(b) account for the on-chip switches SW_i resistance. Impedance matching is digitally controlled by adjusting the width of SW3-SW4. Upper switches SW1-SW2 are fixed-width transistors. This asymmetric control makes calibration loop simple, but output common mode is not tuned. This implementation uses a 16 bit thermometric control for the impedance, sufficient to limit the output differential amplitude error within 5%.

A tri-state pre-driver is used to switch off the driver during pauses. During regular operation, pre-driver inverters are not at high impedance and driver transistor gates are forced to proper values. During pauses, these inverters are tri-stated, with SW3-SW4 open and SW1-SW2 closed. In this situation, no static current flows through the termination resistor as output terminals are both tied to V_s.

Fig. 4 shows a system level description of the calibration circuit. Analog section is a comparator that senses and compares the differential output signal to an internal reference. A digital controller analyzes this information to act over a bi-directional shift register that stores the impedance control thermometric code. Output selection is used to select the proper calibration word that is applied to the driver. Calibration algorithm has two parts: an initial calibration when the system is turned on and a calibration refresh to track temperature variations.

Fig. 5 is a schematic of the proposed differential mode comparator. Two source degenerated differential pairs are used to compare differential amplitudes in the order of 500mV. A resistor divider is used to generate precise internal references. All static power consumption is eliminated when the driver is not being calibrated. A dedicated sampling circuit is used to sense output signals with minimum link idle time. When it receives a calibration pulse, the circuit waits until the last AER event finishes its transmission. As the link is stopped

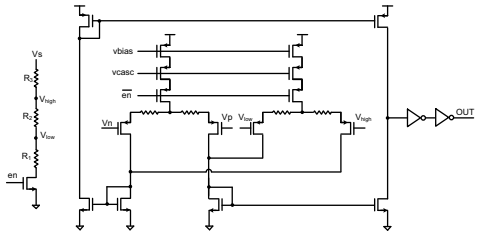

Fig. 5. Differential mode comparator circuit.

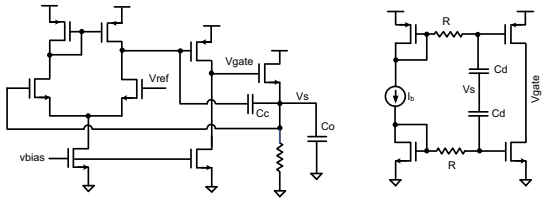

Fig. 6. Regulator circuit with internal and transient compensation.

while sampling, a short pulse is generated in order to optimize link throughput. Finally, output analog values are stored in capacitors and the comparator can process them.

B. Power management for switching drivers

The driver requires around 5mA to generate a 500mV differential amplitude, but this current drops to nA range during pauses. Furthermore, instantaneous current pulses supplied by V_s must be very sharp for a high speed switching operation. Typical voltage regulators using a low frequency dominant pole for loop stability lack the agility to react at the speed demanded by instantaneous output current. A large external capacitor is used to compensate the loop and provide these charge packets needed during transients. Even if the load is not demanding current, the regulator power transistor can draw several mA due to the loop dynamics.

Internally compensated regulators do not employ this large output capacitor. Dominant pole is located in an internal node and output capacitor cannot be used to provide instantaneous output current pulses. These kind of regulators require transient response compensation in order to achieve similar specifications as externally compensated regulators. However, they allow the pass transistor current to change at the same speed as the output current. Fig. 6 shows the regulator schematic used in this work to generate V_s.

We have used several design techniques to combine internal compensation with good transient response. Stability is achieved using a two stage amplifier with a Miller capacitor C_c. This capacitor splits the amplifier internal pole (the dominant one) and the output pole, improving the system phase margin. The pass element is built with a source follower as no low drop-out is required. If output voltage increases, NMOS overdrive is reduced and output current is lowered. In the other case, the loop acts in the opposite way, increasing the output current. Using an NMOS transistor as pass element

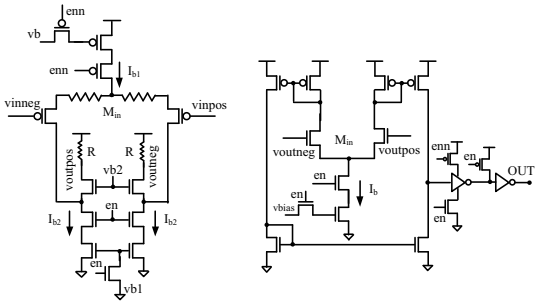

Fig. 7. Two stage receiver circuit.

helps stability because V_s is a low impedance node and output pole is pushed to high frequencies.

However, the gate voltage is not affected by changes in the output node. A fast path between this output node and pass transistor gate is implemented to reinforce the transient compensation. A class AB differentiator derivates the output voltage and generates an output current proportional to this voltage peak. This current is injected or subtracted from the pass transistor gate when a negative or positive output voltage slope is detected. This extra loop impacts the stability by dropping the output pole to lower frequencies, degrading the phase margin.

C. Receiver design for low common mode

The common mode generated by the calibration circuit is not well controlled as only one branch is implemented as a digitally controllable transistor. Moreover, the reference voltage is low (around 1V), leading to a low output common mode. For this reason, the receiver front-end must be implemented with PMOS transistors and input common-mode range must be optimized. This must be combined with techniques to turn off the bias currents for power savings.

Fig. 7 shows the receiver circuit schematics. A pre-amplifier provides a first gain stage that is able to process a very low common-mode. DC voltages at the PMOS differential pair output are set low enough to enlarge input common mode range. This is done by using a folded cascode output stage that shifts up the output common mode. A rail-to-rail version of the serial signal is obtained by using a high gain amplifier.

IV. Simulation results

The presented voltage mode link has been implemented in $0.35\mu m$ CMOS. The driver takes a layout area of 500x386μm (55870μm^2 for the calibration circuitry), while the receiver needs 290x250μm. The Serializer/Deserializer is described in [2] and takes a 1500x700μm area. Target data rate is chosen as 500 Mbps using Manchester coding. Reference voltage is chosen as 1V to generate a differential amplitude around 500mV. Fig. 8 shows the calibration step curves obtained across process and temperature corners. A montecarlo simulation with process and mismatch variations was performed, resulting in a 3σ error of 6% after calibration for the specified differential amplitude.

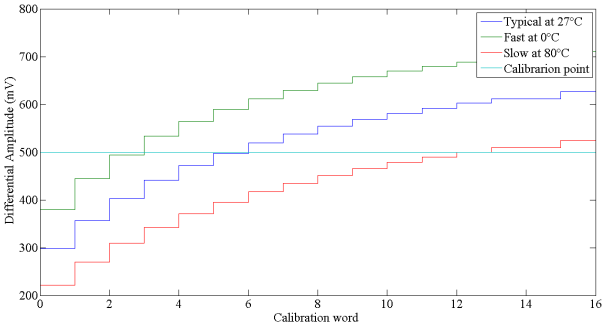

Fig. 8. Calibration curves in technology corners.

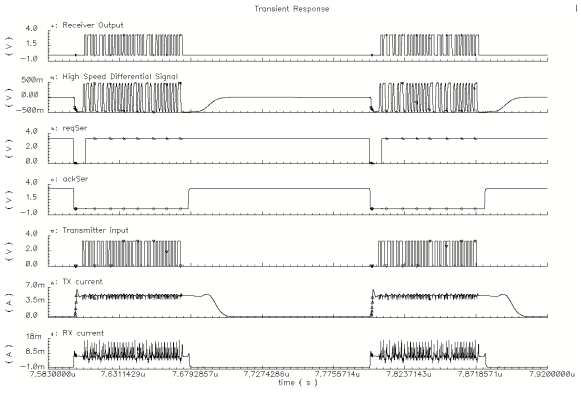

Fig. 9. Full link transient simulation.

However, calibration is very sensitive to temperature variations. Simulation results indicate that a temperature variation from 0ºC to 80ºC causes a 16% error in impedance matching. This result justifies the need of a calibration refresh. Rate of calibration refresh must be carefully chosen to track temperature variations and keep the driver always calibrated.

Fig. 9 shows a post-layout transient simulation of the full link transmitting. This was modelled by a transmission line for the PCB trace and lumped elements for pads and bonding wires. If a new event needs to be transmitted, the serializer activates *reqSer* and sends it to the receiver. This action switches on the driver and receiver. If the receiver can handle a new event, *ackSer* is activated low while data are being transmitted. This way, the link has a temporal reference ($reqSer$ and $ackSer$) to switch on/off its bias currents. Driver and receiver power consumption is also represented in Fig. 9. The driver demands $311\mu A$ during pauses and $5mA$ in transmission. The receiver requires $69\mu A$ in idle status and $7mA$ in operation. The link power consumption for 5 Meps rate (32-bits event) was 20mW in simulation, while the mathematical model (eq. 1) predicted 15.5mW without including dynamic power consumption. Power consumption is 33.2mW at peak rate of 15Meps and 1.3mW at minimum event rate.

Fig. 10 is a regulator transient simulation, where V_s and the output current are shown. When the driver is switched on, the output current swings the whole range. A 150mV drop is detected in this situation. However, the regulator control loop

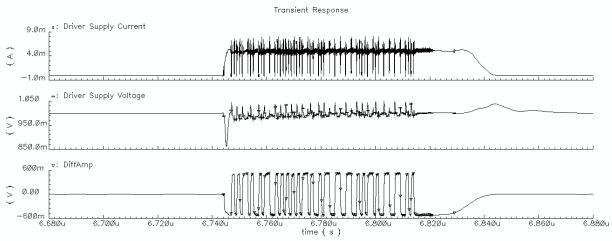

Fig. 10. Regulator transient simulation.

reacts within a few hundred of ps. Note that this is the time the driver needs to switch from the pause mode to the active mode. Regulator stability has also been intensively simulated under all load conditions. Worst case for stability occurs at the minimum load condition, resulting in 64º phase margin. Open loop gain is 75dB and unity gain frequency was set to 6.3MHz.

V. Conclusions

A voltage-mode driver capable of transmitting a 500 Mbps serial AER stream is presented. Techniques to achieve accurate impedance matching through calibration and real burst mode operation capability were discussed. Furthermore, power management techniques for switching drivers were analyzed. A high speed internally compensated regulator was presented as proof of concept. Intensive post-layout simulations were performed in order to check the robustness of the approach.

Acknowledgment

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