

A Precise CMOS Mismatch Model for Analog Design from Weak to Strong Inversion

Teresa Serrano-Gotarredona, Bernabé Linares-Barranco, and Jesús Velarde-Ramírez

Abstract

A five parameter mismatch model continuous from weak to strong inversion is presented. The model is an extension of a previously reported one valid in the strong inversion region [1]. A mismatch characterization of NMOS and PMOS transistors for 30 different geometries has been done with this continuous model. The model is able to predict current mismatch with a mean relative error of 13.5% in the weak inversion region and 5% in strong inversion. This is verified for 12 different curves, sweeping V_G , V_{DS} and V_S . Since data is available for 30 different sizes, the mismatch model can be expressed as function of transistor width W and L , independently. The proposed model, with explicit W and L dependency has been implemented in the Spectre simulator. Simulations reveal that such precise modeling of mismatch (with explicit W and L dependency) can improve analog circuit performance without penalty on power and area consumption: just by splitting transistors into the optimum number of segments.

1. Introduction

Characterization of transistor mismatch is crucial for precision analog design. Using very reduced transistor geometries produces large deviations in the transistor electrical parameters. This may render the analog circuit useless due to unexpected large variations of the circuit specifications. On the contrary, if too conservative transistor geometries are used, the consequence is a waste of area, that also produces an increase in circuit capacitances. This may degrade the speed specifications and increase the circuit power consumption. Thus, a precise mismatch characterization as a function of transistor area is necessary for optimizing area-speed-power-noise-precision consumption in analog design.

Some works on statistical characterization have been previously published in the literature [1]-[3]. These works do statistical characterization in the ohmic and/or saturation for the strong inversion region of operation. However, as low-power and low-voltage are becoming increasingly important specifications in analog design, the analog design is moving towards the moderate and weak inversion regions of the transistor operation. Recently, a mismatch model valid for all regions of operation has been published [4]. However, relative errors in the weak inversion region of the order of 100% are reported. In the present work, we report a continuous 5-parameter mismatch model valid for all regions of operation. The model predicts the current mismatch with a mean relative error of 13.5% in weak inversion and 5% in the strong inversion region. The maximum prediction

error of our model is less than 50% for all the operation regions, for all 12 curves. NMOS and PMOS transistors of 30 different geometries have been characterized. The model is an extension of a previously reported 5-parameters mismatch model [1] to the weak inversion region.

2. Mismatch Model

To generate a unique mismatch model valid in all regions of operation, a transistor model continuous from weak to strong inversion is necessary [5]-[6]. The present mismatch model is based on the ACM transistor model which is continuous for all regions of operations and is physically based, so that it has a reduced number of physically meaningful parameters [6]. This makes this model especially suitable for transistor mismatch characterization. We have verified that very similar results are obtained if the EKV model [5] is used.

In the ACM model, the current through the transistor I_{DS} is expressed as,

$$\begin{aligned} I_{DS} &= I_s(i_f(V_p - V_S) - i_r(V_p - V_D)) \\ V_p - V_{S(D)} &= \phi_t(\sqrt{1 + i_{f(r)}} - 2 + \ln(\sqrt{1 + i_{f(r)}} - 1)) \\ V_p &= \frac{V_G - V_{TO}}{n} \\ n &= 1 + \frac{\gamma}{2(\sqrt{V_G - V_{TO} + 2\phi_F + \gamma\sqrt{2\phi_F + 1/4\gamma^2 - 1/2\gamma}})} \\ I_S &= I_s' n = \mu n C_{ox} W / L \phi_t^2 / 2 \end{aligned} \quad (1)$$

where V_G , V_S and V_D are, respectively, the gate, source and drain voltages referred to the bulk. Parameter ϕ_t is the thermal voltage; γ is the body factor; ϕ_F is Fermi potential; μ is mobility; C_{ox} is density of oxide capacitance and W and L are the transistor width and length, respectively.

The complete transistor model taking into account some second order effects relevant for mismatch and small transistor geometries, is [7]

$$I_{DS} = \frac{I_S(i_f - i_r)(1 + \lambda(V_D - V_S))}{(1 + \theta_o[V_p - V_S]^+)(1 + \theta_e V_{DS_{eff}})}, \quad (2)$$

where,

$$\begin{aligned} V_{DS_{eff}} &= V_{DS} \text{ in ohmic region} \\ V_{DS_{eff}} &= [V_p - V_S]^+ \text{ in saturation} \end{aligned}$$

Parameter λ models the channel pinchoff, and parameters θ_e and θ_o model mobility degradation, velocity saturation and, drain and source series resistances [1]. The operator $[]^+$ in equation (2) is a smoothed rectification function as shown in Fig. 1. The

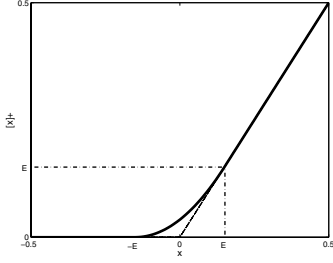


Fig. 1. Smoothed rectification operator

function in Fig. 1 is continuous and has continuous derivative. It is defined as,

$$[x]^+ = \begin{cases} 0 & \text{if } x < -E \\ \frac{(x+E)^2}{4E} & \text{if } -E < x < E \\ x & \text{if } x > E \end{cases} \quad (3)$$

However, in equation (2), a discontinuity in the derivative still exists in the definition of $V_{DS_{eff}}$. This problem can be easily solved by expressing $V_{DS_{eff}}$ as the combination of two smoothed rectification operators,

$$V_{DS_{eff}} = [V_p - V_S]^+ - [V_p - V_D]^+ \quad (4)$$

The extension of the smoothed region has been empirically chosen to be a fraction of V_{DS} , namely, $E = 0.3V_{DS}$.

Our five parameter mismatch model, expresses the current mismatch $\Delta I_{DS}/I_{DS}$ as a first order Taylor series expansion of 5 mismatch parameters,

$$\frac{\Delta I_{DS}}{I_{DS}} = \frac{\Delta I_S'}{I_S'} + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial \gamma} \Delta \gamma + \frac{1}{I_{DS}} \frac{\partial I_{DS}}{\partial V_{TO}} \Delta V_{TO} - \frac{[V_p - V_S]^+}{1 + \theta_o [V_p - V_S]^+} \Delta \theta_o - \frac{V_{DS_{eff}}}{1 + \theta_e V_{DS_{eff}}} \Delta \theta_e \quad (5)$$

where the set of 5 mismatch parameters $\{\Delta I_S'/I_S', \Delta \gamma, \Delta V_{TO}, \Delta \theta_e, \Delta \theta_o\}$ characterizes transistor mismatch for any bias point.

3. Mismatch Characterization Results

To characterize the mismatch, arrays of 36 NMOS transistors of 30 different geometries and arrays of 36 PMOS transistors of 30 different geometries were measured accessing to a reduced number of pins [1]. A cell containing 30 different sized NMOS transistors and 30 different sized PMOS transistors is arranged in a 6×6 matrix. This characterization chip was fabricated in a standard $0.35\mu m$ CMOS technology. The 30 geometries correspond to 6 different widths and 5 different transistor lengths.

The transistor widths are: $40\mu m$, $20\mu m$, $10\mu m$, $5\mu m$, $2\mu m$ and $0.8\mu m$.

The transistor lengths are: $10\mu m$, $5\mu m$, $2\mu m$, $0.8\mu m$ and $0.35\mu m$.

For each transistor in the array, we measured 12 different curves. In each curve, we swept voltage V_G while keeping the other voltages constant. The 12 different measured curves correspond to a two dimensional sweep of four V_S values and three different V_{DS} voltages. Each curve is measured with 101 data points for $V_G \in [0, 3.3V]$ and varied in $0.033V$ steps. The 12 measured curves correspond to

$V_S = \{0V, 0.5V, 1V, 1.5V\}$ and $V_{DS} = \{0.1V, 0.7V, 1.3V\}$. V_G and V_S voltages are referred to the local substrate.

To extract the mismatch parameters, first the large signal parameters $\{I_S', \gamma, \phi_F, V_{TO}, \theta_e, \theta_o, \lambda\}$ have to be extracted in order to compute the partial derivatives of equation (5). The large signal parameter extraction is done using nonlinear curve fitting techniques.

To extract the mismatch parameters we compute the current difference ΔI between two consecutive transistors in the array. This way, we transform the 6×6 array of transistors into a 5×6 array of transistor pairs. For each transistor pair, we fit the measured $\Delta I/I$ data for 9 of the curves ($V_S = \{0V, 0.5V, 1V\}$ and $V_{DS} = \{0.1V, 0.7V, 1.3V\}$) to equation (5). From this fitting, we extract a unique set of 5 mismatch parameters $\{\Delta I_S'/I_S', \Delta \gamma, \Delta V_{TO}, \Delta \theta_e, \Delta \theta_o\}$ for each transistor pair. Note that we have not used the 3 curves with $V_S = 1.5V$ during the extraction of the mismatch parameters. We have left these curves only for evaluation purposes.

For each transistor type (NMOS or PMOS) and for each transistor size, we compute the five standard deviations $\{\Delta I_S'/I_S', \Delta \gamma, \Delta V_{TO}, \Delta \theta_e, \Delta \theta_o\}$ and the 10 corresponding correlation terms.

The current mismatch can be predicted using the mismatch parameters, through the theoretical equation,

$$\sigma^2\left(\frac{\Delta I}{I}\right) = \sigma^2\left(\frac{\Delta I_S'}{I_S'}\right) + \left(\frac{1}{I} \frac{\partial I}{\partial \gamma}\right)^2 \sigma^2(\Delta \gamma) + \left(\frac{1}{I} \frac{\partial I}{\partial V_{TO}}\right)^2 \sigma^2(\Delta V_{TO}) + \left(\frac{1}{I} \frac{\partial I}{\partial \theta_o}\right)^2 \sigma^2(\Delta \theta_o) + \left(\frac{1}{I} \frac{\partial I}{\partial \theta_e}\right)^2 \sigma^2(\Delta \theta_e) + \text{correlation terms} \quad (6)$$

Fig. 2 shows a comparison, for the 30 geometries of NMOS transistors, between the measured current mismatch (circles) and the current standard deviation computed using the extracted mismatch parameters and equation (6) (solid lines). Fig. 2 corresponds to the random current standard deviations measured and computed for $V_S = 0.5V$, $V_{DS} = 1.3V$ while sweeping the gate voltage V_G . Fig. 2 depicts 6 subfigures, one for each transistor width. Each subfigure

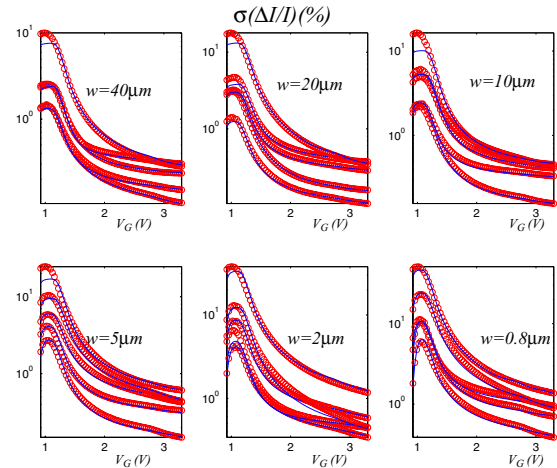


Fig. 2. Comparison between the measured and computed current random standard deviation for the 30 different sizes of NMOS transistors. (a) Curve $V_S = 0.5V$, $V_{DS} = 0.1V$, and (b) curve $V_S = 0.5V$, $V_{DS} = 1.3V$

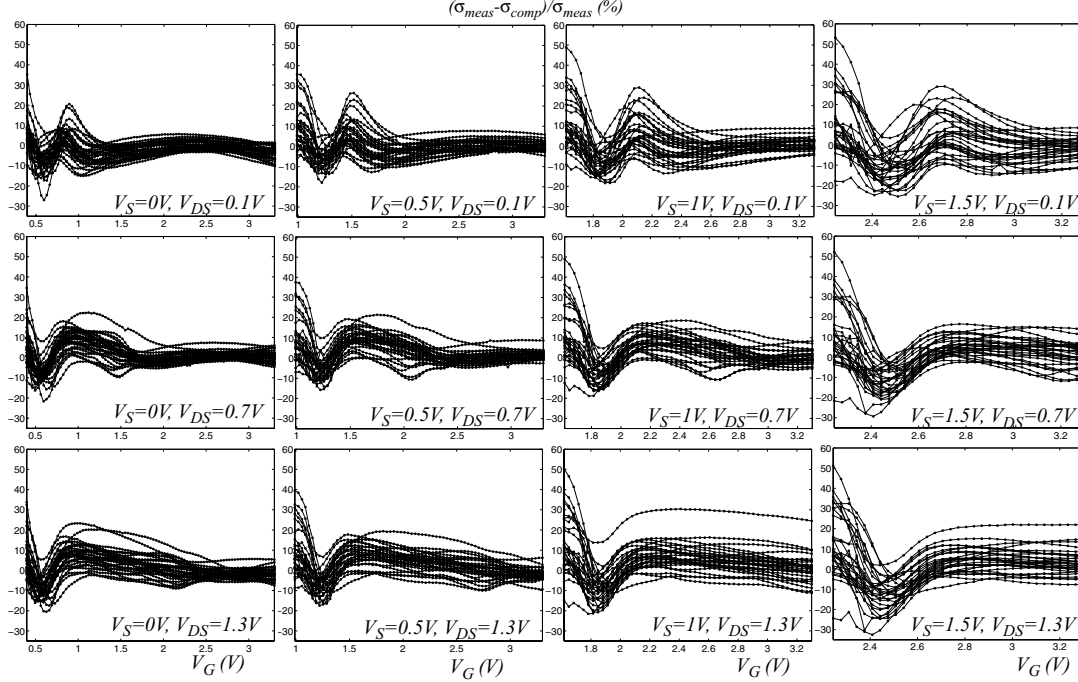


Fig. 3. Errors (in %) between the measured and computed current random standard deviation for the 30 geometries of NMOS transistors. Each subfigure corresponds to one of the 12 curves $V_S = \{0V, 0.5V, 1V, 1.5V\}$ and $V_{DS} = \{0.1V, 0.7V, 1.3V\}$.

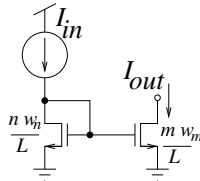


Fig. 5: Simple NMOS current mirror

plots 5 curves, each one corresponding to a different transistor length.

In Fig. 3, we show the error between measured and predicted values (in %) for all 12 curves for NMOS transistors. In each subfigure, the errors are superimposed for all sizes. The mean relative error is 8% in the weak inversion region and 4% in strong inversion.

Similar figures are obtained for the 30 PMOS transistor geometries. The mean relative error, in this case, is 13.5% in the weak inversion region and 5% in strong inversion. The maximum prediction error of the current mismatch is less than 40% in the weak inversion region and below 20% in the strong inversion region.

The current mismatch is computed using the five standard deviations $\{\Delta I_S'/I_s', \Delta\gamma, \Delta V_{T0}, \Delta\theta_e, \Delta\theta_o\}$ and the 10 possible correlation terms. However, only the three correlations $r(\Delta I_S'/I_s', \Delta\theta_e)$, $r(\Delta I_S'/I_s', \Delta\theta_o)$ and $r(\Delta\theta_e, \Delta\theta_o)$ are relevant for the NMOS transistor mismatch. For the PMOS transistors we find correlation $r(\Delta\gamma, \Delta V_{T0})$ is also important. Fig. 4 depicts the mismatch parameters $\{\Delta I_S'/I_s', \Delta\gamma, \Delta V_{T0}, \Delta\theta_e, \Delta\theta_o\}$ obtained for the NMOS transistors of the 30 different geometries.

4. Implications for Analog Design

Precise modeling of mismatch in analog circuit design can be crucial for minimizing area and current consumption.

In the previous Sections we have shown a mismatch model that allows precise prediction from weak to strong inversion. This has been verified for a large number of transistor sizes (30) and each for 12 different biasing curves. Consequently, this allows to predict mismatch reasonably well for any other size by properly interpolating between the data of available sizes [1]. We have implemented in Spectre some alternative nmos and pmos subcircuit cells that use Spectre-AHDL

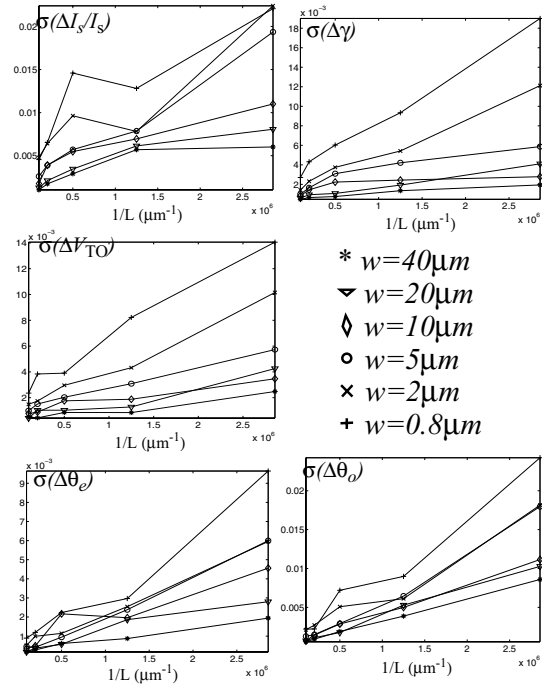


Fig. 4. Mismatch parameters for all the geometries of NMOS transistors

descriptions to predict mismatch for any transistor size and bias condition from weak to strong inversion. Using this framework, we can illustrate now the convenience of having a precise mismatch modeling from weak to strong inversion and dependent on transistor width W and length L (not just area).

Consider the example in Fig. 5 to illustrate this. It is a simple nmos unity gain current mirror with input and output transistors of equal width W and length L . Mismatch simulations were performed for different currents and by splitting the transistors into different number of segments n , but preserving the total width $W = nw_n = 20\mu m$. In Fig. 6 we show the mismatch results for a high precision application which requires high biasing currents. In this case we used a mirror input current of $10\mu A$, while setting transistor length $L = 10\mu m$ and width $W = nw_n = 20\mu m$. Five different values of n were considered: splitting a transistor into $n=25$ segments each of width $w_n = 0.8\mu m$, into $n=10$ segments each of $w_n = 2\mu m$, into $n=4$ each of $w_n = 5\mu m$, into $n=2$ segments of $w_n = 10\mu m$, or not splitting ($n=1$) and preserving $w_n = 20\mu m$. Fig. 6 shows three different curves, with the x-axis being n (log scale) and the y-axis the mirror precision in per cent. The curve with ‘o’ corresponds to splitting the mirror output transistor into different segments while keeping unsplit the input transistor. The curve with ‘*’ corresponds to splitting the input

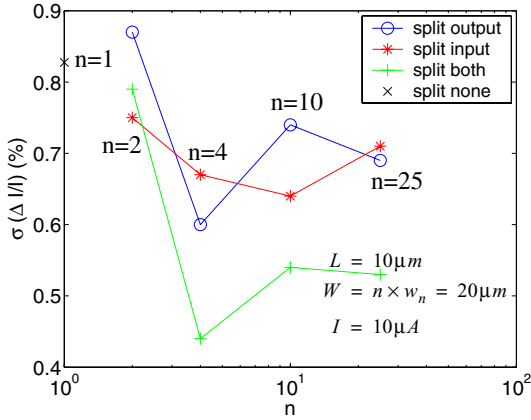


Fig. 6: Different splitting cases for constant current

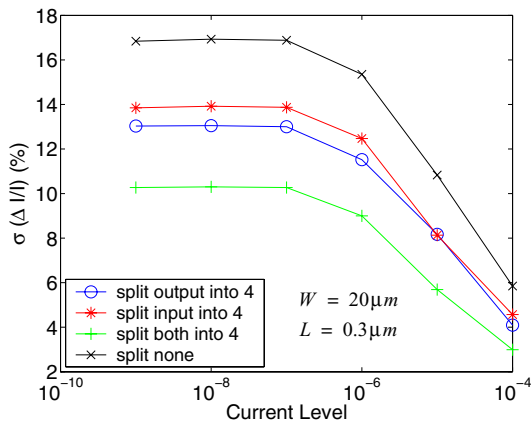


Fig. 7: Different splitting cases covering a wide current range

transistor, while not splitting the output one. The curve with ‘+’ corresponds to splitting both input and output transistors. Also shown with an ‘x’ is the case where no transistor is split ($\sigma = 0.83\%$). As can be seen, we can have up to almost a factor of 2 improvement in mismatch by splitting both transistors into 4 segments. Traditionally, a designer would multiply transistor area by 4 in order to achieve a factor 2 improvement in mismatch [2]. Also note that optimum mismatch is obtained for non-square segments. This contradicts the common belief that a square transistor produces the minimum mismatch. In Fig. 6 the square transistor case ($n=2$) does not improve much the original mismatch of non-split transistors.

Fig. 7 shows simulations for $n=4$ only, for transistors of minimum length $L = 0.3\mu m$ and total width $W = nw_n = 20\mu m$, and while sweeping operating currents from $1nA$ to $100\mu A$ (5 decades). Again, ‘o’ are for splitting output transistor only, ‘*’ for splitting input transistor only, ‘+’ for splitting both and ‘x’ for splitting none. For very low currents and splitting both, the improvement goes up to a factor 1.7, while for high currents it is about 2.

5. Conclusions

This paper presents a 5 parameter mismatch model valid for all regions of operation. The model is based on a transistor model continuous from weak to strong inversion [5]-[6] and a previously reported mismatch model for the strong inversion region. This is, to our knowledge, the first mismatch model published in literature able to predict the current mismatch with mean error less than 13.5% in all the transistor operation regions, and for such a wide range of transistor curves and geometries. It is shown how precise W and L dependent mismatch modeling can be used advantageously for analog design.

6. Acknowledgements

This work was partially supported by spanish grants TIC1999-0446-C02-02, TIC2000-0406-P4-05 (Victor), FIT-07000/2002/921 (Arquimedes), TIC2002-10878-E, TIC-2003-08164-C03-01 (Samanta), and EU grant IST-2001-34124 (Caviar).

7. References

- [1] T. Serrano-Gotarredona and B. Linares-Barranco, “Systematic Width-and Length Dependent CMOS Transistor Mismatch Characterization and Simulation,” *Analog Integrated Circuits and Signal Processing*, vol. 21, pp. 271-296, Kluwer Academic Publishers, 1999.
- [2] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, “Matching Properties of MOS Transistors,” *IEEE Journal of Solid State Circuits*, vol. 24, No. 5, pp. 1433-1440, 1989.
- [3] J. Bastos, *Characterization of MOS Transistor Mismatch for Analog Design*, Ph. D. Dissertation, Katholieke Universiteit Leuven, 1998.
- [4] J. Croon, M. Rosmeulen, S. Decoutere, and W. Sansen, “An Easy-to-Use Mismatch Model for the MOS Transistor,” *IEEE Journal of Solid State Circuits*, vol. 37, No. 8, pp. 1056-1064, August, 2002.
- [5] C. C. Enz, F. Krummneracher and E. A. Vittoz, “An Analytical MOS Transistor Model Valid for All Regions of Operation and Dedicated to Low-Voltage Low-Current Applications,” *Analog Integrated Circuits and Signal Processing Journal*, vol. 8, pp 83-114, July 1995.
- [6] C. Galup-Montoro, M. C. Schneider and A. I. A. Cunha, “A Current-Based MOSFET Model for Integrated Circuit Design”, Chapter 2 in *Low-Voltage/Low-Power Integrated Circuits and Systems*, edited by E. Sanchez-Sinencio and A. G. Andreou, IEEE Press, August 1998.
- [7] T. Serrano-Gotarredona and B. Linares-Barranco, “CMOS Transistor Mismatch Model valid from Weak to Strong Inversion,” *Proc. 2003 European Solid-State Circuits Conference, ESSCIRC’03*, September 2003.