A Mismatch Calibrated Bipolar Spatial Contrast AER Retina with Adjustable Contrast Threshold

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Abstract

Address Event Representation (AER) is an emergent technology for assembling modular multi-blocks bio-inspired sensory and processing systems. Visual sensors (retinae) are among the first AER modules to be reported since the introduction of the technology. Spatial contrast AER retinae are of special interest since they provide highly compressed data flow without reducing the relevant information required for performing recognition. Reported AER contrast retinae perform a contrast computation based on the ratio between a pixel's local light intensity and a spatially weighted average of its neighbourhood. This resulted in compact circuits, but with the penalty of all pixels generating output signals even if they sensed no contrast. In this paper we present a spatial contrast retina with bipolar output: contrast is computed as the relative difference between a pixel's local light and its weighted spatial average. As a result, contrast includes a sign and the output will be zero if there is no contrast. Furthermore, an adjustable thresholding mechanism has been included, such that pixels remain silent until they sense an absolute contrast above the adjustable threshold. The pixel contrast computation circuit is based on Boahen's Biharmonic operator contrast circuit, which has been improved to include mismatch calibration and adaptive current based biasing. As a result, the contrast computation circuit shows much less mismatch, is almost insensitive to ambient light illumination, and biasing is much less critical than in the original voltage biasing scheme. A full AER retina version has been submitted for fabrication. In the present paper we provide simulation results.

I. Introduction

AER is a spike based representation hardware technique for communicating spikes between layers of neurons in different chips. AER was first proposed in 1991 in one of the Caltech research labs [1], and has been used since then by a wide community of neuromorphic hardware engineers. Spatial contrast AER retina sensors are of special interest. Computing contrast on the focal plane reduces data flow significantly, although relevant information for shape and object recognition is conserved. In a conventional luminance sensor (a commercial camera) all pixels are sampled with a fixed period and its light intensity (integrated over this period) is communicated out of the sensor to the next stage. In an AER sensor pixels are not sampled. On the contrary, the pixels are who initiate an asynchronous communication cycle, called "event", when a given condition is satisfied. For example, a spatial contrast retina pixel would send an event whenever the computed local contrast exceeds a given threshold. As a consequence, AER systems are frame-less: there is no sequence of still frames as in conventional video. Rather, the information flows in a continuous manner between AER modules as events are generated at the pixel levels, either in the sensors or at later processing stages.

Previously reported spatial contrast retinae [2],[3] compute contrast as the ratio between a pixel's locally sensed light intensity $I_{ph}(x, y)$ and a spatially weighted average of its surrounding neighborhood $I_{avg}(x, y)$ computed with some kind of diffusive network

$$I_{cont}(x, y) = I_{ref}\frac{I_{ph}(x, y)}{I_{avg}(x, y)} \quad (1)$$

Since this is always positive, let us call it "unipolar" contrast computation. This yielded circuits where no subtraction operation was required. This was crucial to maintain mismatch (and precision) at reasonable levels. Note that for computing I_{avg} and I_{cont} circuits have to handle directly photo currents, which can be as low as pico-amperes or less. Performing a simple mirroring operation introduces mismatches with errors in the order of 100% [4]. This can be overcome by increasing transistor area, but then leakage currents may become comparable to the available photo currents. Consequently. while handling photo currents, it is desirable to keep complexity at a minimum. Therefore, from a circuit point of view, the way of computing contrast as in eq. (1) was very convenient. However, this presents an important drawback: when there is no contrast ($I_{avg} = I_{ph}$) then $I_{cont} \neq 0$. In an AER circuit this means that a pixel sensing no contrast will be sending out information (events) and consuming communication bandwidth on the AER channels. This is contrary to the advantages of AER (where it is expected that only information relevant events will be transmitted) and contrary to the advantages of computing contrast at the focal plane (so that only contrast relevant pixels need to send information). In prior work [3], although spatial contrast was computed by eq. (1) in the retina, a post-processing with AER (convolution) modules was added to effectively compute the contrast as the signed (or bipolar) quantity

$$I_{cont}(x, y) = I_{ref}\left(\frac{I_{ph}(x, y)}{I_{avg}(x, y)} - 1\right) \quad (2)$$

This reduced significantly the data flow (from about 400keps[1] to about 10keps), but also at the expense of reducing the speed response of a pixel by a factor of about 10.

In the present paper we present a new spatial contrast retina design, where the contrast computation follows eq. (2). The design is based on the original contrast computation circuit by Boahen [2], which has been

1. keps stands for "kilo events per second".

improved to overcome its inherent limitations on mismatch, ambient light dependence, and critical controllability. Section II summarizes a prior AER mismatch-calibrated contrast retina pixel that followed eq. (1), Section III summarizes briefly Boahen's spatial contrast computation circuit, Section IV summarizes a more compact calibration circuit than the one used in [3] and which has been used in the present design, and Section V introduces the new pixel design. Finally, Section VI provides simulation results.

II. Prior AER Mismatch-Calibrated Unipolar Spatial Contrast AER Retina

Fig. 1 shows the basic schematic of the contrast computation circuit used in a previous unipolar spatial contrast retina [3]. A p+/nwell photo diode sensed current $I_{ph}(x, y)$ is replicated twice using a sub-pico-ampere current mirror [5]. The first replica is used in a cascoded diffusive network [6], which implements the discrete approximation of the 2D Laplacian equation

$$I_{ph}(x, y) = \left(1 - \lambda_x \frac{\partial^2}{\partial x^2} - \lambda_y \frac{\partial^2}{\partial y^2}\right) I_{avg}(x, y) \qquad (3)$$

This equation provides a good spatial average of I_{ph} over neighboring pixels, such that closer pixels contribute more to this average than distant pixels. The second replica of the photo current is fed together with $I_{avg}(x, y)$ to a translinear circuit computing the ratio between both, scaled by reference current I_{ref}. The resulting current $I_{cont}(x, y)$ is thus proportional to a unipolar contrast (as in eq. (1)) and is fed to an integrate-and-fire neuron generating periodic spikes with a frequency proportional to $I_{cont}(x, y)$. Scaling current I_{ref} is made locally trimmable for each pixel in order to compensate for all mismatch contributions from the photo diode, current mirror, diffusive network, translinear circuit, and integrate-and-fire neuron. As a result, inter-pixel mismatch contrast computation could be reduced from about $\sigma \approx 60\%$ to $\sigma \approx 6\%$ using 5-bit pixel registers to control $I_{ref}(x, y)$. Pixel complexity was kept relatively simple (104 transistors + 1 capacitor) thanks to the unipolar nature of the contrast computation, and the whole pixel could be fit into an area of $58\mu m \times 56\mu m$ in a $0.35\mu m$ CMOS process. The main drawback is that pixels with no contrast would generate output events at a constant rate proportional to I_{ref}. To overcome this, the 4-AER-module system shown in Fig. 2 was assembled to compute effectively a bipolar contrast as in eq. (2). A uniform image AER flow with negative sign bit was merged with the retina AER flow and fed to an AER convolution chip [7] configured to operate as an array of signed (bipolar) integrators. As a result, the background

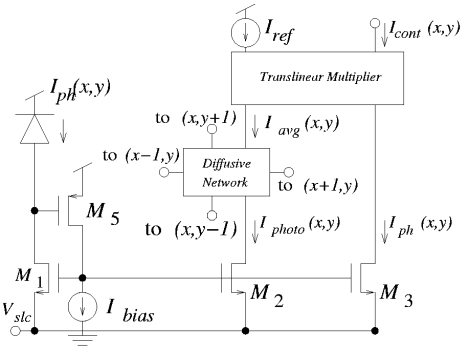

Fig. 1: Block diagram of pixel in prior unipolar contrast retina

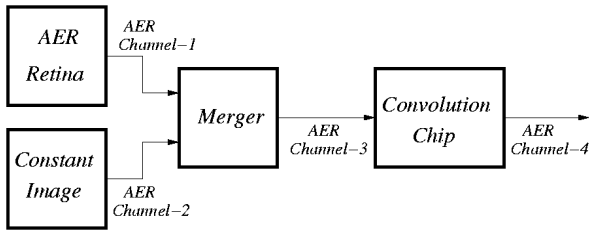

Fig. 2: Setup used to convert the unsigned AER retina output with DC level to a signed AER stream with no DC level

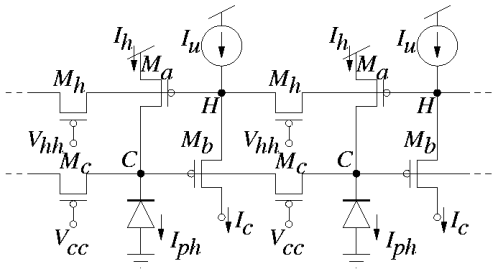

Fig. 3: Boahen original contrast computation circuit

DC component in eq. (1) was removed, yielding a computation equivalent to that in eq. (2). However, as a backside effect, the effective firing rate of a pixel at the output channel was reduced by a factor of around 10, thus diminishing its speed response. In the design presented in this paper, this is solved by performing all the bipolar contrast computation at the sensor chip using an improved version of Boahen's original biharmonic contrast computation circuit.

III. Boahen's Biharmonic Contrast Circuit

A trivial solution to subtract the DC component of the circuit in Fig. 1 is to subtract another DC current $I_{ref2}(x, y)$ from $I_{cont}(x, y)$. However, this second DC current also needs to be trimmable to compensate for its own mismatch. Note that the available trimming current $I_{ref}(x, y)$ will not compensate it together with the rest of mismatch sources [3].

However, the same result can be achieved by using Boahen's compact biharmonic spatial contrast computation circuit [2]. Thus, by using a slightly more complex diffuser network, we will not require any more the sub-pico-ampere current mirror nor the translinear circuit. The original circuit, in its all-PMOS version, is shown in Fig. 3. The schematic only shows two neighboring pixels of a 1-D retina version. In practice, the horizontal transistors form a 2D mesh. The continuous approximation of this circuit solves approximately the following equations [6]

$$\begin{aligned} I_h(x, y) &= I_{ph}(x, y) + a\nabla^2 I_c(x, y) \\ I_c(x, y) &= I_u - b\nabla^2 I_h(x, y) \end{aligned} \qquad (4)$$

Solving for I_h results in the biharmonic equation used in computer vision to find an optimally smooth interpolating function of the stimulus I_{ph}. Consequently, the output $I_c(x, y)$ is the second order spatial derivative of the interpolation I_h according to the bottom eq. (4). Since the interpolation is a spatially integrated version of the stimulus, I_c can be interpreted as a version of a first order derivative of the stimulus, therefore, spatial contrast.This can also be understood with the help of Fig. 4. The top trace shows a step stimulus I_{ph} and its spatial average

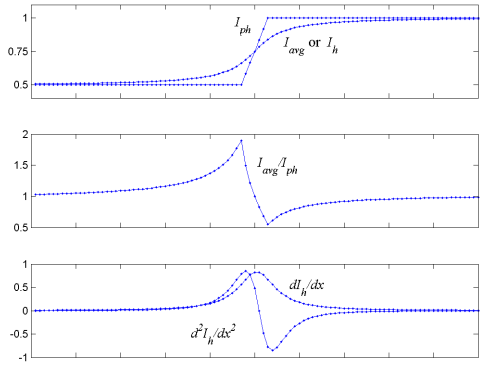

Fig. 4: Interpretation of spatial contrast computations

(I_{avg} or I_h). The center trace shows the contrast computation as I_{avg}/I_{ph}, and the bottom trace shows the contrast computation as the second order spatial derivative of I_h. Both are equivalent. According to the bottom eq. (4), I_c includes a DC term I_u. The original circuit implementation of this model suffered from a series of drawbacks. First, mismatch was comparable to output signal. Second, output signal would degrade for the same contrast stimulus when changing lighting conditions. Third, bias voltages V_{cc} and V_{hh} in Fig. 3 had very narrow and critical tuning range. All three drawbacks have been improved with the present implementation.

IV. New Compact Calibration Circuit

We reduce mismatch by introducing calibration. One dominant source of mismatch is the DC component in the bottom of eq. (4). Since this current is set constant, independent of lighting conditions, we can directly subtract it with a trimmable current source. The output current will thus be directly the bipolar contrast current we were looking for. To implement the trimmable current source, we follow the recently reported very compact circuit based on series transistors association [8]. Fig. 5 shows the basic principle behind this circuit. Each switched MOS operates as a segment of an effective longer MOS whose length is controlled digitally by switching individual segments from ohmic to saturation, and vice versa. The key consists in making each segment to contribute approximately as a power of 2^n to the total length. As a result, the effective length is digitally controlled as in a digital-to-analog conversion. Fig. 6 shows the circuitry used to subtract the DC component of the contrast current. Transistors to the left of the dashed line are shared by all pixels, while those to the right are replicated for each pixel. Transistors M_{1-4} form a translinear loop [6], thus $I_{un} = = I_1 I_2 / I_{3n}$. I_{3n} is a mirrored version of I_3 by transistors M_{ta} and M_{tb}. M_{tb} is made of the digitally controlled length mos of Fig. 5. consequently, I_{un} is proportional to this length. I_{cal} is added to the base bias current I_{ub}, thus compensating mismatch originated at I_{ub} and in the pixel.

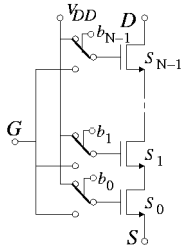

Fig. 5: Digitally controlled length MOS used for calibration

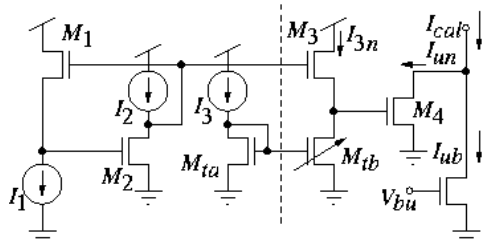

Fig. 6: Translinear tuning circuit

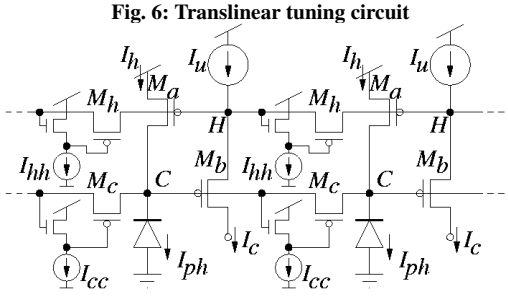

Fig. 7: Boahen improved circuit with current biasing

V. The improved spatial bipolar contrast pixel

Fig. 7 shows how the pixel has been modified to include a current biasing scheme for controlling the original voltages V_{cc} and V_{hh} in Fig. 3. This way, gate voltages V_{cc} and V_{hh} tend to follow voltage excursions at nodes 'C' and 'H'. The first advantage of this is that biasing will adapt to ambient light conditions. For example, if all photodiode currents are scaled up/down by the same factor, the voltage at all nodes 'H' will follow it logarithmically. Also, since I_u is constant, the voltage at node 'C' will also tend to follow the same shift. Since bias currents I_{hh} and I_{cc} are kept constant, the gate voltages of transistors M_h and M_c will thus follow also this same global voltage shift, adapting to the global light change. Another beneficial effect of this current biasing scheme is that it attenuates mismatch. After doing careful mismatch analysis and identifying the main sources of mismatch for this circuit, one can find out that transistor M_a and current I_u are the dominant sources of mismatch. The effect of I_u will be compensated by calibration, and the effect of M_a will be attenuated by the current biasing scheme. Note that mismatch in all M_a transistors will introduce random voltage variations at nodes 'H' and 'C'. These variations will be transformed into random lateral currents through transistors M_h and M_c. The random currents through M_h will be collected by output current I_c and can be compensated by calibration. However, random currents through M_c transistors operate as if they were generated by the photodiodes. Thanks to the current biasing scheme, an increase in 'C' will increase the gate voltage of the new bottom NMOS transistor, increasing its source voltage, thus increasing the gate voltage of M_c, which will reduce the lateral random current. A similar effect will be happening for transistors M_h. Finally, the third advantage is a more robust means for biasing the lateral transistors. In the original scheme, voltages V_{cc} and V_{hh} suffered from a very narrow and critical tuning range (about 100mV or less). Now, bias currents I_{cc} and I_{hh} can be tuned over several decades, while still perceiving their effect.

Another modification introduced is thresholding. This is done at the integrate-and-fire neuron, as is shown in Fig. 8. Since contrast current I_{cont} can now be positive or negative we need two comparators to detect whether the net

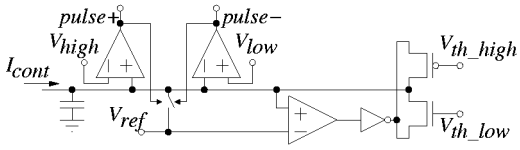

Fig. 8: intergate and fire bipolar neuron with thresholding

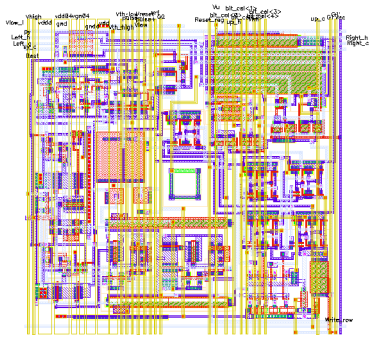

Fig. 9: Layout of 80x80um^2 bipolar spatial contrast pixel

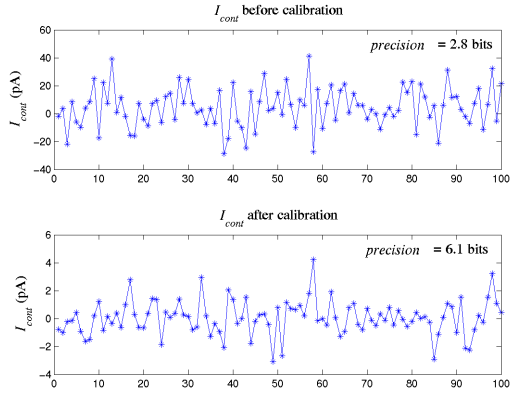

Fig. 10: Output contrast current under uniform stimulus. Top trace is before calibration. Bottom trace is after calibration.

contrast integration has reached an upper threshold V_{high} (generating a positive event at *pulse+*) or a lower one V_{low} (generating a negative event at *pulse-*). In either case, the capacitor will be reset to a central voltage V_{ref}. For introducing thresholding a third comparator detects whether capacitor voltage is above or below V_{ref} and turns on either a positive or negative threshold current, which I_{cont} needs to exceed for producing an event. The thresholding transistors in Fig. 8 use large area (2/30) to redude mismatch impact.

VI. Simulation Results

A full 32 x32 pixel AER bipolar spatial contrast retina has been designed and submitted for fabrication in a 0.35µm CMOS process. Fig. 9 shows the layout of its $80 \times 80 \mu m^2$ pixel. To verify the expected performance of the pixel, Monte Carlo simulations have been performed on a one dimensional array of 100 pixels. The top trace of Fig. 10 shows the output contrast current I_{cont} obtained when applying a uniform optical stimulus (no contrast) before performing calibration. The output contrast current range is $\pm I_u = \pm 250\,pA$. Before calibration $\Delta I_{cont} = I_{cont}^{max} - I_{cont}^{min} = 70\,pA$. This is equivalent to a precision of 2.8 bits. The bottom trace shows the same, but after calibration, with $\Delta I_{cont} = 7.3\,pA$. This is equivalent to a precision of 6.1 bits.

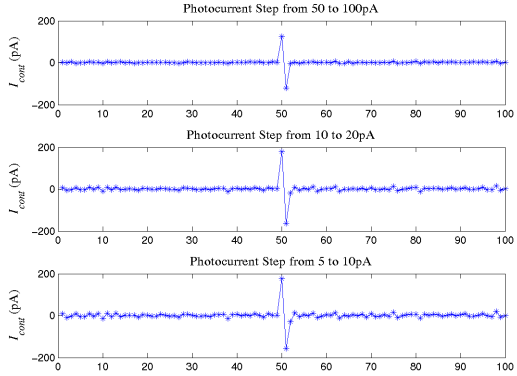

Fig. 11: Spatial contrast computation after calibration for a factor 2 step photo current stimulus at different values.

After calibration at uniform 50pA photo current, we apply a factor 2 step stimulus at the photo detectors for different values: from 50 to 100pA, from 10 to 20pA, and from 5 to 10pA, while bias current I_u was always set to 250pA. The response of the contrast computation circuit is shown in Fig. 11. As can be seen, although photo current changes by a factor of 10, output response remains at the same level.

VII. Conclusions

A new AER bipolar contrast retina has been presented. It uses an improved and calibrated version of Boahen's contrast circuit. Simulation results are provided.

VIII. Acknowledgements

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IX. References

[1] M. Sivilotti, *Wiring Considerations in Analog VLSI Systems with Application to Field-Programmable Networks*, Ph.D. Thesis, California Institute of Technology, Pasadena CA, 1991.

[2] K. Boahen and A. Andreou, "A contrast-sensitive retina with reciprocal synapses," in J. E. Moody (Ed.), *Advances in neural information processing,* vol. 4, pp. 764--772, San Mateo CA, 1992. Morgan Kaufman.

[3] J. Costas-Santos, T. Serrano-Gotarredona, R. Serrano-Gotarredona and B. Linares-Barranco, "A Spatial Contrast Retina with On-chip Calibration for Neuromorphic Spike-Based AER Vision Systems," *IEEE Trans. Circuits and Systems, Part-I: Regular Papers*, vol. 54, No. 7, pp. 1444-1458, July 2007.

[4] T. Serrano-Gotarredona and B. Linares-Barranco, "CMOS Mismatch Model valid from Weak to Strong Inversion", *Proc. of the 2003 European Solid State Circuits Conference*, (ESSCIRC'03), pp. 627-630, September 2003.

[5] B. Linares-Barranco and T. Serrano-Gotarredona , "On the Design and Characterization of Femtoampere Current-Mode Circuits," *IEEE Journal of Solid-State Circuits*, vol. 38, No. 8, pp. 1353-1363, August 2003.

[6] A. G. Andreou and K. Boahen, "Translinear Circuits in Subthreshold CMOS," *Analog Integrated Circuits and Signal Processing*, Kluwer, no. 9, pp. 141–166, Apr. 1996.

[7] R. Serrano-Gotarredona, T. Serrano-Gotarredona, A. Acosta-Jiménez, and B. Linares-Barranco, "A Neuromorphic Cortical Layer Microchip for Spike Based Event Processing Vision Systems," *IEEE Trans. on Circuits and Systems, Part-I*, vol. 53, No. 12, pp. 2548-2566, Dec. 2006.

[8] J. A. Leñero-Bardallo, T. Serrano-Gotarredona, and B. Linares-Barranco, "A Calibration Technique for Very Low Current and Compact Tunable Neuromorphic Cells. Application to 5-bit 20nA DACs," *IEEE Trans. Circuits and Systems, Part-II: Brief Papers*, vol. 55, No. 6, pp. 522-526, June 2008.