# A General Subthreshold MOS Translinear Theorem

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## Abstract

**This paper outlines the conditions under which the Translinear Principle can be fully exploited for MOS transistors operating in subthreshold. Due to the exponential nature of subthreshold MOS transistors the Translinear principle applies immediately as long as the *Source-to-Bulk* voltages are made equal to zero (or constant). This paper addresses the conditions under which subthreshold MOS transistors still satisfy a Translinear principle but without imposing this constraint. It is found that the Translinear principle results in a more general formulation than the original for BJTs since now multiple Translinear loops can be involved. The constraint of even number of transistors is no longer necessary.**

## I. Introduction

The translinear principle, introduced by Barry Gilbert in 1975 [1], is one of the most important circuit theory contributions in the electronics era. In its original formulation, the translinear principle provides a simple and efficient way to analyze and synthesize nonlinear circuits based on bipolar junction transistors (BJTs). Due to their exponential characteristics, the translinear principle can be extended to MOS transistors operating in weak inversion [2], [3] without and with floating-gate devices [4]. For MOS transistors operating above threshold there has also been found a similar way to analyze and synthesize nonlinear circuits [5].

For bipolar transistors one practical problem that may require some attention when applying the translinear principle is the nonzero base current [6]. In contrast, the translinear principle holds for MOS subthreshold transistors in an exact manner if source and bulk are short-circuited. However, it has been found that the principle holds as well in an exact manner under different circumstances [2]-[3], although a general subthreshold MOS translinear theorem has not been devised until now. In this paper we provide this general theorem and outline the conditions under which subthreshold MOS transistors, viewed as four terminal devices, satisfy a general translinear principle.

The operation of a subthreshold MOS can be described by the following equation [2], [7]-[9]

$$I_{DS} = I_o S e^{\kappa (V_{GS}/V_{th})} e^{(1-\kappa)(V_{BS}/V_{th})} (1 - e^{-V_{DS}/V_{th}}) \quad , \qquad (1)$$

where $V_{th} = KT/q$ is thermal voltage, $I_o$ is a positive constant current, $S$ is the transistor size factor ($S = W/L$, where $W$ is transistor width and $L$ is its length), and $\kappa$ is a technology dependent positive parameter. This equation holds true as long as

$$\frac{1}{2}\phi_{FB} \le V_{GS} \le \phi_{FB} \qquad (2)$$

where $\phi_{FB}$ is the device's flat band voltage [10]. Voltage $V_{BS}$ can take either positive or negative values as long as the parallel PN diode junction is biased below its forward conduction threshold voltage. Parameter $\kappa$ is known to have a slight dependency on voltage $V_{BS}$ [2]. However, in this paper we will assume $\kappa$ to be constant, which is a reasonable assumption if care is taken to make the $V_{BS}$ voltages similar for all transistors.

For operation in saturation eq. (1) can be simplified to (if $V_{DS} \gg V_{th}$)

$$I = \frac{I_{DS}}{S} = I_o e^{\kappa (V_{GS}/V_{th})} e^{(1-\kappa)(V_{BS}/V_{th})} \qquad (3)$$

and be rewritten as

$$I = I_o i_G^{\kappa} i_B^{(1-\kappa)} \qquad (4)$$

where $I$ (a "*normalized current*") is transistor current normalized with respect to transistor size factor $S = W/L$, and $i_G$, $i_B$ are dimensionless numbers called *pseudo-currents* and equal to

$$i_G = e^{V_{GS}/V_{th}} \qquad i_B = e^{V_{BS}/V_{th}} \qquad (5)$$

Let us use the symbol in Fig. 1 to represent a weak-inversion MOS in saturation. Let us call the path that goes from the gate terminal $G$ to the source terminal $S$ the $G-branch$ (or *Gate-branch*), and the path that goes from the bulk terminal $B$ to terminal $S$ the $B-branch$ (or *Bulk-branch*). We are using a diode-like symbol to represent the exponential relationship between the voltage of the branch and the current flowing out of the device and a capacitive-like termination to each diode symbol to represent the capacitive coupling nature of the *Gate* and *Bulk* terminals. If $V_{BS} = 0$ (or constant) there is an exact exponential relationship between $V_{GS}$ and $I_{DS}$ (see eq. (3)) and the original BJT translinear formulation can be directly and exactly applied.

## II. Generalized Translinear Theorem for Subthreshold MOS Transistors

In this section we will consider the conditions under which translinear principles can be applied to circuits

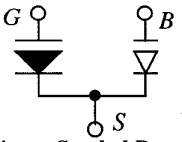


**Fig. 1: Translinear Symbol Representation for Subthreshold MOS Transistor in Saturation**

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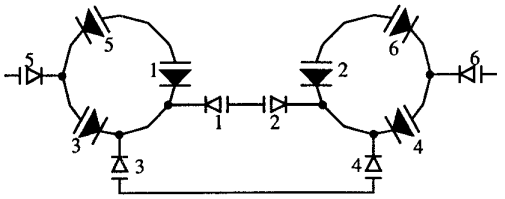

**Fig. 2: Example of Coupled *G-loops* using translinear symbol representation**

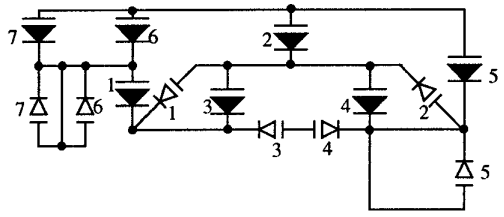

**Fig. 3: Illustration of the *G-order* concept. Devices '1-2-3-6' form a *G-loop* which is coupled to *G-loop* formed by devices '2-4-5', because devices '1-2-3-4' form a *B-loop*. Devices '1-2-3-4-5-6' form a *Closed Translinear Set*, and so do devices 6 and 7. Device 2 has a *G-order* of $n_{G2} = 2$ because its *G-branch* belongs to two *G-loops* of the same *Closed Translinear Set*. All other devices have *G-order* one.**

with subthreshold MOS transistors but without imposing the constraint of making $V_{BS} = 0$. We will introduce first some preliminary theorems and definitions, and then state and proof the generalized translinear theorem for subthreshold MOS devices.

The first concepts to be introduced are *G-loop* and *B-loop*. A *G-loop* (or *Gate-loop*) is a closed loop of *G-branches*, and a *B-loop* (or *Bulk-loop*) is a closed loop of *B-branches*. For these loops we can state translinear theorems for their *pseudo-currents*, whose proof is identical as for the original BJT Translinear Theorem.

**Theorem:** In a *G-loop* containing an **arbitrary** number of *G-branches*, the product of *pseudo-currents* $i_G$ of branches connected in the Clock-Wise (CW) direction is equal to the corresponding product for branches connected in the Counter-Clock-Wise (CCW) direction.

Note that since *pseudo-currents* are dimensionless entities we can have an arbitrary number of branches oriented CW and another arbitrary number of branches oriented CCW (as opposed to the case of eq. (7)). A completely equivalent theorem holds directly for *B-loops*.

Up to now things are similar to classical translinear loops, except that an arbitrary number of branches are allowed. However, the presence of two exponential branch voltages in eq. (3) is what makes subthreshold MOS translinear loops more general and complicated than the classical ones. A first consequence of this fact is the following concept of *coupled loops*:

**Definition:** Two *G-loops* are said to be coupled if at least one MOS device of the first *G-loop* and at least one other different device of the second *G-loop* share their respective *B-branches* in a common *B-loop*.

This is illustrated in Fig. 3. Devices '1-3-5' form a *G-loop* and devices '2-4-6' form another *G-loop*. However, devices '1-2-3-4' form a *B-loop*, thus making the previous two *G-loops* to be coupled through the *B-branches* of devices 1, 2, 3 and 4.

An equivalent definition applies for *coupled B-loops*. Note that two loops may have a common branch without being necessarily *coupled loops*.

In the example of Fig. 3, we can write for the two *G-loops*

$$\begin{aligned}\frac{I_3 I_5}{I_1} &= I_o\left(\frac{i_{G3} i_{G5}}{i_{G1}}\right)^{\kappa}\left(\frac{i_{B3} i_{B5}}{i_{B1}}\right)^{1-\kappa} = \\ &= I_o e^{(V_{BS3}+V_{BS5}-V_{BS1})\frac{1-\kappa}{V_{th}}} \\ \frac{I_4 I_6}{I_2} &= I_o\left(\frac{i_{G4} i_{G6}}{i_{G2}}\right)^{\kappa}\left(\frac{i_{B4} i_{B6}}{i_{B2}}\right)^{1-\kappa} = \\ &= I_o e^{(V_{BS4}+V_{BS6}-V_{BS2})\frac{1-\kappa}{V_{th}}}\end{aligned} \tag{6}$$

where all *pseudo-currents* $i_G$ have cancelled out by applying the above Theorem. However, due to *B-loop* '1-2-3-4',

$$V_{BS1} + V_{BS4} = V_{BS2} + V_{BS3} \tag{7}$$

which introduces a coupling between the two equations in (11), and makes *G-loops* '1-3-5' and '2-4-6' to be *coupled loops*.

When devices form multiple touching loops it is not clear which ones to choose or how many to choose. For example, in Fig. 4 one can choose *G-loops* '1-2-3-6', '6-7', and '2-4-5'. But why not consider '1-3-4-5-6', '6-7', and '2-4-5', or '1-3-4-5-7' and '1-2-3-6'. One can try all possible options as long as one chooses a set of *Non-Redundant* (NR) loops:

**Definition:** A set of loops is said to be *Non-Redundant* (NR) if the sum of branch voltages of any loop cannot be expressed as a linear combination of the sum of branch voltages of other loops in the set.

For example, in Fig. 4, for *G-loops* '1-2-3-6', '2-4-5', and '1-3-4-5-6' their respective sum of branch voltages is,

$$\begin{aligned} V_{GS6} + V_{GS1} &= V_{GS2} + V_{GS3} \\ V_{GS2} + V_{GS4} &= V_{GS5} \\ V_{GS6} + V_{GS1} + V_{GS4} &= V_{GS3} + V_{GS5} \end{aligned} \tag{8}$$

Any of these three equations can be expressed as a linear combination of the other two. Thus the three *G-loops* do not form a *Non-Redundant set of G-loops*. However, any two of these three *G-loops* do form a *Non-Redundant set of G-loops*.

The fact that subthreshold MOS transistors can form *coupled loops* yields naturally to the following concept of *Closed Translinear Set*,

**Definition:** Given a set of MOS devices, and once a *Non-Redundant* set of loops has been chosen, a *Closed Translinear Set* (CTS) is a set of devices such that all loops they form are only coupled among them, but not to loops

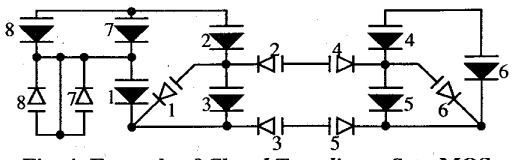

**Fig. 4: Example of *Closed Translinear Sets*. MOS Devices 7 and 8 form a *Closed Translinear Set*, and so do MOS Devices 1-7.**

where branches of other devices (not belonging to the CTS) are present.

This is illustrated in Fig. 5. Let us select the NR set of *G-loops* '1-2-3-7', '4-5-6', and '7-8', and the NR set of *B-loops* '1-2-3-4-5-6', '7', and '8'. *G-loops* '1-2-3-7' and '4-5-6' are coupled because there is are *B-branches* of devices of both *G-loops* that are shared in the common *B-loop* '1-2-3-4-5-6'. The two *G-loops* '1-2-3-7' and '4-5-6', and the two *B-loops* '1-2-3-4-5-6' and '7' are not coupled to other loops (either *G-loop* '7-8' nor *B-loop* '8'), thus (for the chosen NR set of loops) devices '1-2-3-4-5-6-7' form a *Closed Translinear Set*. On the other hand, *G-loop* '7-8' is not coupled to any other loop, nor are *B-loops* '7' and '8'. Therefore, devices '7-8' form another *Closed Translinear Set*.

When working with multiple *G-loops* and *B-loops*, with some of them being coupled, it is not very convenient to classify each branch as being CW or CCW oriented, as will become apparent later. Let us instead classify all branches into two orientation groups, the α-*wise* oriented branches and the β-*wise* oriented branches. Two branches are classified into the same group (either the α-*wise* or the β-*wise*) if they appear in the same loop with the same orientation. On the contrary, two branches are classified each into a different group (one into the α-*wise*, the other into the β-*wise*) if they appear in the same loop with opposite orientation. Note that now a CW branch in one loop and a CCW branch in another loop can be classified into the same α-*wise* or β-*wise* group. If a branch is short-circuited, it forms a one branch loop and can be classified as either α-*wise* or β-*wise*.

Another concept that is useful for stating the generalized translinear subthreshold MOS theorem is that of *G-order* and *B-order* of a MOS device in a *Closed Translinear Set*:

**Definition 4:** Once a NR set of loops has been chosen, a subthreshold MOS transistor which is part of a *Closed Translinear Set* is said to have a *G-order* of value $\mathbf{n}_G$, if its *G-branch* belongs to $\mathbf{n}_G$ *G-loops* of the given *Closed Translinear Set*.

An equivalent definition of *B-order* can be stated for *B-loops*. The concept is illustrated in Fig. 4. Let us choose the NR set of *G-loops* '1-2-3-6', '2-4-5', and '6-7' and of *B-loops* '1-2-3-4', '5', '6', and '7'. *G-loops* '1-2-3-6' and '2-4-5' are coupled because devices '1-2-3-4' form a *B-loop*. There are no other couplings among the chosen loops. Consequently, devices '1-2-3-4-5-6' form a *Closed Translinear Set* which consists of *G-loops* '1-2-3-6' and '2-4-5' and *B-loops* '1-2-3-4', '5', and '6'. Devices 6 and 7 form one *G-loop* ('6-7') and two *B-loops* ('6' and '7') which are not coupled to any other loop. Therefore devices 6 and 7 form another *Closed Translinear Set*. MOS device 2 has *G-order* $\mathbf{n}_{G2} = 2$ because its *G-branch* appears in two *G-loops* of the same *Closed Translinear Set*. MOS device 6 does not have *G-order* 2 because, although its *G-branch* belongs to two different *G-loops*, these two loops do not belong to the same *Closed Translinear Set*. All MOS devices have *B-order* one because their *B-branches* appear only in one *B-loop*.

When a *G-branch* has *G-order* greater than one it belongs to more than one *G-loop* of the same *Closed Translinear Set*. In such cases it is possible that the branch be classified as α-*wise* in some *G-loops* and as β-*wise* in other *G-loops*. Under these circumstances it is convenient to divide its *G-order* into two parts

$$\mathbf{n}_G = \mathbf{n}_{\alpha,G} + \mathbf{n}_{\beta,G} \tag{9}$$

where $\mathbf{n}_{\alpha,G}$ (let us call it *G-α-order*) denotes the times this *G-branch* is classified as α-*wise* in a CTS, and $\mathbf{n}_{\beta,G}$ (let us call it *G-β-order*) denotes the times it is classified as β-*wise* in CTS. Similarly, for *B-branches*, the *B-order* can be separated into the *B-α-order* ($\mathbf{n}_{\alpha,B}$) and the *B-β-order* ($\mathbf{n}_{\beta,B}$).

Using the concepts and preliminary theorems introduced until now, it is possible to state and proof the generalized translinear theorem for subthreshold MOS transistors[1]:

**Theorem:** Given a set of subthreshold MOS devices and choosing for them a set of *Non-Redundant G-loops* and *B-loops*, for each *Closed Translinear Set* the following can be stated:

If it is possible to find an α- and β-*wise* classification of their *G-loops and B-loops* such that

a) the sum of *G-α-orders* equals the sum of *G-β-orders*

$$\sum_{j \in \{\alpha\text{-}wise\}} \mathbf{n}_{\alpha,Gj} = \sum_{l \in \{\beta\text{-}wise\}} \mathbf{n}_{\beta,Gl} \tag{10}$$

b) and, every time a device's *G-branch* is classified as α-*wise* in a *G-loop* its *B-branch* can be classified as α-*wise* in some *B-loop*, and every time a device's *G-branch* is classified as β-*wise* in a *G-loop* its *B-branch* can be classified as β-*wise* in some *B-loop*,

then the product of normalized currents raised to the power of their *G-α-order* of all transistors in the CTS whose *G-branches* have been classified α-*wise* equals the product of normalized currents raised to the power of their *G-β-order* of all transistors whose *G-branches* have been classified β-*wise*.

*Proof*:

For each *G-loop* in the *Closed Translinear Set* the following holds:

$$1 = \frac{\prod_{j \in \{\alpha\text{-}wise\}} i_{Gj}}{\prod_{l \in \{\beta\text{-}wise\}} i_{Gl}} \tag{11}$$

1. The theorem will be stated using *G-branches* as primary branches and making *B-branches* to depend on them. However, because of the symmetry between *G-branches* and *B-branches* (due to the symmetry between $V_{GS}$ and $V_{BS}$ voltages in eq. (3)), the theorem can be stated as well by interchanging *G-branches* and *B-branches*.

Since this is true for every single *G-loop* we can multiply these equations for the chosen set of *Non-Redundant G-loops* and their product will still be equal to unity,

$$1 = \left( \frac{\prod_{j \in \{\alpha-wise\}} i_{Gj}}{\prod_{l \in \{\beta-wise\}} i_{Gl}} \right|_{G-loop_1} \times \ldots \times \left( \frac{\prod_{j \in \{\alpha-wise\}} i_{Gj}}{\prod_{l \in \{\beta-wise\}} i_{Gl}} \right|_{G-loop_P} = \frac{\prod_{j \in \{\alpha-wise\}} (i_{Gj})^{n_{\alpha,Gj}}}{\prod_{l \in \{\beta-wise\}} (i_{Gl})^{n_{\beta,Gl}}} \tag{12}$$

Furthermore, we can raise it to the power of $\kappa$, and it still be equal to unity,

$$1 = \left( \frac{\prod_{j \in \{\alpha-wise\}} (i_{Gj})^{n_{\alpha,Gj}}}{\prod_{l \in \{\beta-wise\}} (i_{Gl})^{n_{\beta,Gl}}} \right)^{\kappa} \tag{13}$$

Note that, since the devices form a CTS, all branches will be present and no branch of another CTS appears. Consequently, eq. (18) includes all *G-branches* of the CTS and only the branches of this CTS. Equivalently, the same can be stated for all *B-loops*,

$$1 = \frac{\prod_{j \in \{\alpha-wise\}} (i_{Bj})^{n_{\alpha,Bj}}}{\prod_{l \in \{\beta-wise\}} (i_{Bl})^{n_{\beta,Bl}}} = \left( \frac{\prod_{j \in \{\alpha-wise\}} (i_{Bj})^{n_{\alpha,Bj}}}{\prod_{l \in \{\beta-wise\}} (i_{Bl})^{n_{\beta,Bl}}} \right)^{1-\kappa} \tag{14}$$

but raising now to the power of $1 - \kappa$, for convenience. Note that, due to statement b) in Theorem 3, every time a device has its *pseudo-current* $i_{Gj}$ in the numerator of eq. (18), its *pseudo-current* $i_{Bj}$ will also appear in the numerator of eq. (19), and both will appear $\mathbf{n}_{\alpha,Gj}$ times. And the same holds for *pseudo-currents* in the denominators of eqs. (18) and (19). Therefore, let us define $\mathbf{n}_{\alpha,j}$ and $\mathbf{n}_{\beta,l}$ such that

$$\begin{aligned} \mathbf{n}_{\alpha,Gj} &= \mathbf{n}_{\alpha,Bj} = \mathbf{n}_{\alpha,j} \\ \mathbf{n}_{\beta,Gl} &= \mathbf{n}_{\beta,Bl} = \mathbf{n}_{\beta,l} \end{aligned} \tag{15}$$

Also, since the devices form a *Closed Translinear Set*, eq. (18) includes all devices of the CTS, and so does eq. (19). Consequently, we can multiply eqs. (18) and (19) and index the $i_G$ and $i_B$ *pseudo-currents* of the same device with the same subscript and use this subscript to index the MOS device,

$$1 = \left( \frac{\prod_{j \in \{\alpha-wise\}} (i_{Gj})^{n_{\alpha,Gj}}}{\prod_{l \in \{\beta-wise\}} (i_{Gl})^{n_{\beta,Gl}}} \right)^{\kappa} \left( \frac{\prod_{j \in \{\alpha-wise\}} (i_{Bj})^{n_{\alpha,Bj}}}{\prod_{l \in \{\beta-wise\}} (i_{Bl})^{n_{\beta,Bl}}} \right)^{1-\kappa} = \frac{\prod_{j \in \{\alpha-wise\}} \left( i_{Gj}^{\kappa} i_{Bj}^{1-\kappa} \right)^{n_{\alpha,j}}}{\prod_{l \in \{\beta-wise\}} \left( i_{Gl}^{\kappa} i_{Bl}^{1-\kappa} \right)^{n_{\beta,l}}} \tag{16}$$

On the other hand, due to statement a) in the theorem the following is satisfied

$$1 = I_o^{\left[ \sum_{j \in \{\alpha-wise\}} n_{\alpha,j} - \sum_{l \in \{\beta-wise\}} n_{\beta,l} \right]} = \frac{\prod_{j \in \{\alpha-wise\}} (I_o)^{n_{\alpha,j}}}{\prod_{l \in \{\beta-wise\}} (I_o)^{n_{\beta,l}}} \tag{17}$$

By multiplying eqs. (21) and (22), and using eq. (4) we obtain

$$1 = \frac{\prod_{j \in \{\alpha-wise\}} (I_o)^{n_{\alpha,j}}}{\prod_{l \in \{\beta-wise\}} (I_o)^{n_{\beta,l}}} \frac{\prod_{j \in \{\alpha-wise\}} \left( i_{Gj}^{\kappa} i_{Bj}^{1-\kappa} \right)^{n_{\alpha,j}}}{\prod_{l \in \{\beta-wise\}} \left( i_{Gl}^{\kappa} i_{Bl}^{1-\kappa} \right)^{n_{\beta,l}}} = \frac{\prod_{j \in \{\alpha-wise\}} (I_j)^{n_{\alpha,j}}}{\prod_{l \in \{\beta-wise\}} (I_l)^{n_{\beta,l}}} \tag{18}$$

which concludes the proof of the *Generalized Subthreshold MOS Translinear Theorem.* ❑

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