A 1.5 ns OFF/ON Switching-Time Voltage-Mode LVDS Driver/Receiver Pair for Asynchronous AER Bit-Serial Chip Grid Links With Up to 40 Times Event-Rate Dependent Power Savings

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***Abstract*—This paper presents a low power fast ON/OFF switchable voltage mode implementation of a driver/receiver pair intended to be used in high speed bit-serial Low Voltage Differential Signaling (LVDS) Address Event Representation (AER) chip grids, where short (like 32-bit) sparse data packages are transmitted. Voltage-Mode drivers require intrinsically half the power of their Current-Mode counterparts and do not require Common-Mode Voltage Control. However, for fast ON/OFF switching a special high-speed voltage regulator is required which needs to be kept ON during data pauses, and hence its power consumption must be minimized, resulting in tight design constraints. A proof-of-concept chip test prototype has been designed and fabricated in low-cost standard 0.35 μm CMOS. At $\pm$500 mV voltage swing with 500 Mbps serial bit rate and 32 bit events, current consumption scales from 15.9 mA (7.7 mA for the driver and 8.2 mA for the receiver) at 10 Mevent/s rate to 406μ A (343μ A for the driver and 62.5 μA for the receiver) for an event rate below 10 Kevent/s, therefore achieving a rate dependent power saving of up to 40 times, while keeping switching times at 1.5 ns. Maximum achievable event rate was 13.7 Meps at 638 Mbps serial bit rate. Additionally, differential voltage swing is tunable, thus allowing further power reductions.**

***Index Terms*—Address event representation (AER), asynchronous circuits, asynchronous communications, event-driven processing, low voltage differential signaling (LVDS), LVDS drivers, Manchester encoding, neuromorphic circuits and systems, serial AER, serial interchip communication.**

I. Introduction

ADDRESS Event Representation (AER) is a powerful technology for developing very fast, low power, highly efficient, but sophisticated bio-inspired sensory-processing systems. One challenge for AER event-driven processing systems is to provide a means of interconnecting a high number of processing modules capable of interchanging and processing asynchronous events, while retaining short latencies and low power. Some researchers have already faced the need of assembling a small number of AER chips for providing a given sensory-processing functionality [1]–[7], and some have proposed possible schemes towards providing a framework for scalable multi-chip AER systems [8]–[11]. Recent proposals rely on distributing AER event-driven modules over a 2D grid, where each module interchanges asynchronous and sparse events with its neighbors exploiting locally programmed routers. This makes it possible to map any topological processing architecture onto the 2D grid [12]–[14]. For low pin-count low cost and low power grid chip arrangements it is a good choice to use low voltage differential signal (LVDS) bit-serial AER links, so that each AER module in the 2D grid communicates with each of its four neighbors through two LVDS links, one for transmitting and one for receiving events. More details on how these multi-module AER grids can be used is explained elsewhere [14].

Conventional LVDS links with embedded clock need to transmit continuously to keep the link sender and receiver synchronized. However, in AER systems events are asynchronous and sparse. Consequently, considerable extra power savings can be achieved if the links are turned OFF during inter-event pauses, and quickly back ON when a new event needs to be transmitted. Recently, a Manchester-encoding Serializer/Deserializer scheme has been demonstrated which turns the link OFF and back ON with zero-bit acquisition time [15], but the link was demonstrated using a conventional LVDS driver [16] that was not meant to be turned ON/OFF quickly. Conventional drivers [16], [17] consume several mWs per link even when no data is transmitted. Power down modes on such drivers' large current sources can be very slow, thus losing the benefits of burst-mode AER SerDes [15] links. We previously reported a Current-Mode high-speed ON/OFF switchable LVDS driver for AER bit serial communications [18]. That driver required common-mode voltage control and was designed for fixed differential amplitude of $\pm$300 mV. At 10 mega events per second (Meps) driver and receiver consumed 17.1 mA, while below 100 keps current consumption settled to 0.84 mA. For the present design, fabricated in the same technology, at 10 Meps

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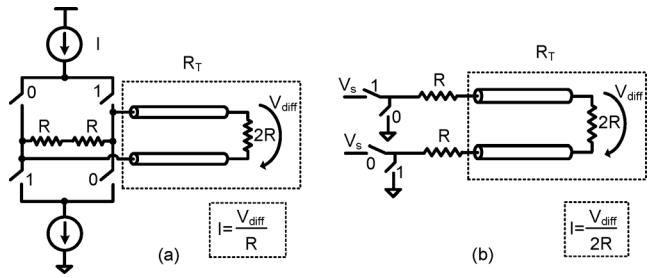

Fig. 1. (a) Comparison between current-mode and (b) voltage-mode termination schemes. $V_{\rm diff}$ is the differential output amplitude and I is the bias current needed to achieve this amplitude.

driver and receiver consume consume 15.9 mA while below 100 keps the current consumption settles to 0.40 mA. Although Voltage-Mode drivers intrinsically consume half the power, as illustrated in Fig. 1, they require extra high consumption circuitry, such as calibration circuits and a high-speed voltage regulator. On the other hand, the voltage regulator allows to easily adjust the differential amplitude, thus allowing for extra power savings. In this paper we provide the experimental demonstration of a switchable voltage-mode LVDS driver with switching times as low as 1.5 ns, whose concept was proposed earlier [19].

In Section II the transistor level design is presented with techniques to quickly switch OFF the driver and receiver, match the line impedance and manage the driver current consumption. Section III provides experimental results of a proof of concept prototype fabricated in 0.35 μm CMOS.

II. Serial Link Voltage-Mode Implementation

Fig. 2(a) shows the block diagram of the complete bit-serial AER LVDS link. Bit-serial high-speed data is transmitted through a PCB differential microstrip using the LVDS driver, while handshaking signals *reqSER* and *ackSER* are lower speed and use conventional single-ended rail-to-rail digital pads. Conventional AER circuits are designed normally using a parallel bundled data bus with asynchronous four-phase handshaking. Reported single chip AER systems normally use 16 bits or less for each event. Events of 16 bits are usually enough to address all neurons in a single chip. Typical event communication rates vary from about 1 Meps to about 30 Meps per parallel link. However, for large multi-chip AER systems more bits are required to address all pixels or neurons in all modules. Here we are using 32-bit addressing. This allows to address up to about 2×10^9 neurons. However, to date the largest systems do not go beyond millions. Nonetheless, the circuits presented here are not restricted to 32-bit event encoding, and even the serializer/deserializer circuits used [15] are easily modifiable to use different number of bits per event.

In Fig. 2(a), the transmitter reads the 32-bit parallel input AER data and implements a 4-phase handshaking protocol with *reqIN* and *ackIN* signals. It then generates *reqSER* for the receiver when the event data is latched and ready to be transmitted. When *ackSER* acknowledges this previous request, the address is serialized into a pair of wires and two bits of preamble are added. This data flow is encoded in a Manchester format with

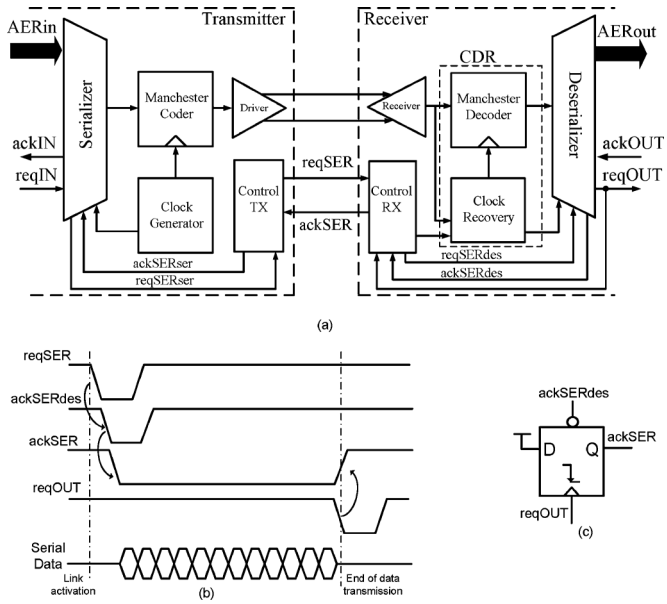

Fig. 2. (a) Block Diagram of the bit serial AER LVDS link. (b) Timing of signals. (c) Circuit to generate signal *ackSER*, which remains active during serial bit stream transmission.

the time reference given by a master clock. The deserializer is able to decode the input stream and put it into a parallel format, ready to be processed by the destination parallel-AER block. The output interface is again implemented with the 4-phase handshaking protocol, using signals *reqOUT* and *ackOUT*. Fig. 2(b) shows the timing of signals.

The transmitter turns OFF the driver during data pauses. The receiver generates *ackSER* using the simple circuit shown in Fig. 2(c). The deserializer generates a pulse in *ackSERdes* when it detects that *reqSER* is at low level requesting an event transmission. This pulse generates a reset for the falling edge triggered flip-flop shown in Fig. 2(c) and causes the activation of *ackSER*. This signal remains at low level until a falling edge at *reqOUT* is detected. At this point, the flip-flop is triggered and captures its input which is tied to the voltage supply. This makes *ackSER* return to high level and the link is turned OFF.

A. Driver Circuitry

Fig. 3 shows a top level description of the proposed switchable voltage mode driver. Signals *INPOS* and *INNEG* are provided by the serializer circuit and contain the event information that must be transmitted. These rail to rail digital signals are processed by a two stage pre-driver designed to drive the high capacitive load at the driver input, while presenting a low input capacitance. This block also performs the task of switching OFF the transmitter operation when there is no data to be transmitted. Signal *en* enables the pre-driver operation when *reqSER* or *ackSER* signals are at low level, indicating an event transmission.

The matching of the transmission line impedance at the transmitter side is essential to ensure good signal integrity. In voltage mode implementations, the output differential voltage is created by switching a constant voltage across the termination resistor. In this paper, the switching transistors are also used to match the

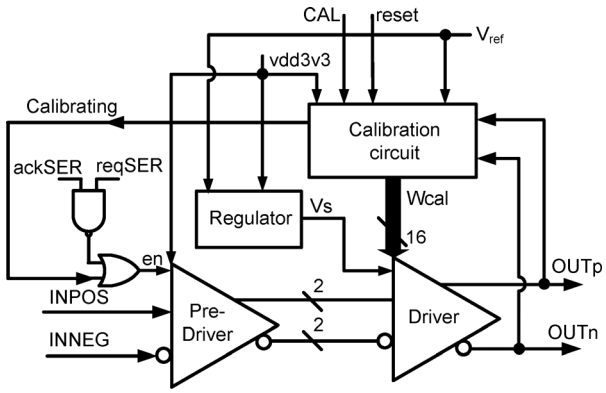

Fig. 3. Top level description of proposed switchable voltage mode driver.

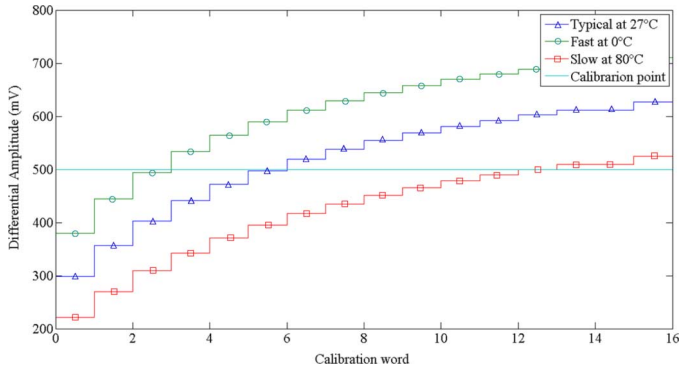

Fig. 5. Post Layout Worst-Case Corner Analysis Simulations to verify the size of the Thermometric Code for Calibration.

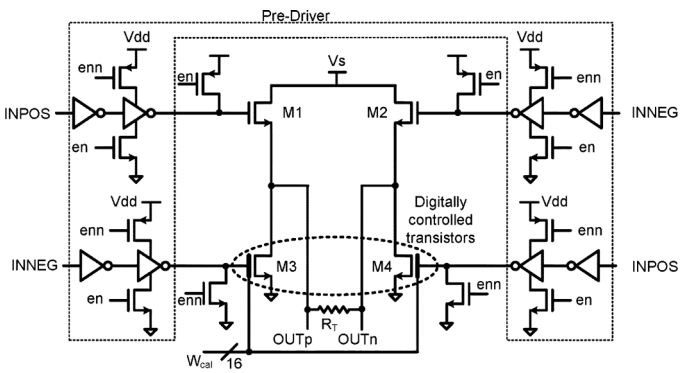

Fig. 4. Proposed Voltage-Mode driver and Pre-Driver circuits.

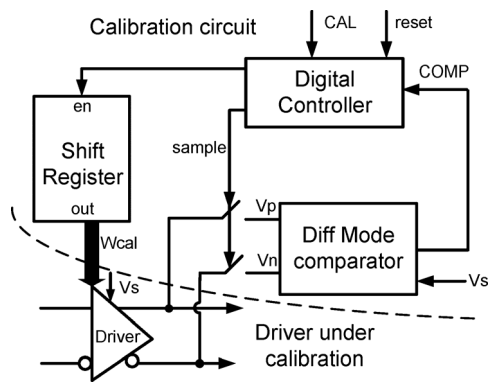

Fig. 6. Calibration circuit system level description.

line impedance. After analyzing the circuit in Fig. 1(b), it can be stated that the impedance matching condition is achieved when the serial resistance of the switches used to create the output swing is equal to the receiver termination resistor. If this condition is satisfied, the differential amplitude is $V_s/2$, where V_s is the driver supply voltage. A dedicated calibration circuit to compensate the process variations is included to tune the driver termination impedance by measuring the output differential amplitude. V_s is generated by an internally compensated regulator which sets a constant value for this voltage and allows a very sharp switching of the supply current without compromising the regulated voltage transient response.

Fig. 4 shows the schematics of a low swing voltage mode pre-driver/driver using only NMOS transistors M1–M4 for line termination purposes. The desired differential output amplitude V_{diff} is generated at R_T by setting $V_s = 2V_{\text{diff}}$. R_T in Fig. 4 accounts for the off-chip resistive components (transmission line and receiver impedance termination). The two R resistors in Fig. 1(b) account for the on-chip termination resistance provided by transistors M_i. Impedance matching is digitally controlled by adjusting the width of M3–M4, using unitary transistors of $(4.5/0.35)$ μm activated by $(4.5/0.35)$ μm switches. Upper termination transistors M1–M2 are fixed-width transistors with $(80/0.35)$ μm aspect ratio. This asymmetric control makes the calibration loop simple, but the output common mode is not tuned. This implementation uses a 16 bit thermometric control for the impedance. Fig. 5 shows post-layout worst-case corner analysis simulations indicating that this number of bits is sufficient. Besides this, extensive post-layout Montecarlo simulations with mismatch and process variations were performed to make sure that this number of bits were satisfactory to limit the output differential amplitude error to within 7% of 3-σ error. Additionally, Monte-Carlo analysis around this calibration point revealed 3-σ error of 25% from the nominal value of 600 mV for the output common mode.

A tri-state pre-driver is used to switch OFF the driver during pauses. During pauses, pre-driver inverters are tri-stated, with M3–M4 open and M1–M2 closed. In this situation, no static current flows through the termination resistor as the output terminals are both tied to V_s. Hence, the driver consumption is reduced to the pA range, corresponding to auxiliary digital circuit leakage currents. The regulator consumes about 340 μA in the OFF-state, which is the total driver and regulator standby power.

Fig. 6 shows a system level description of the calibration circuit used to achieve impedance matching. The serializer used [15] sets the differential lines to logic value '0' when no data is transmitted. When the calibration circuit is activated, data communication is momentarily inhibited, the driver is forced to be enabled (through signal *Calibrating* in Fig. 3), and the serializer sets value '0'. Then an analog differential difference comparator senses the differential line voltage and compares it to an internal reference $(V_s/2)$. A digital controller analyzes this information to act on a shift register which stores the impedance control thermometric code. This code activates a number of fingers in

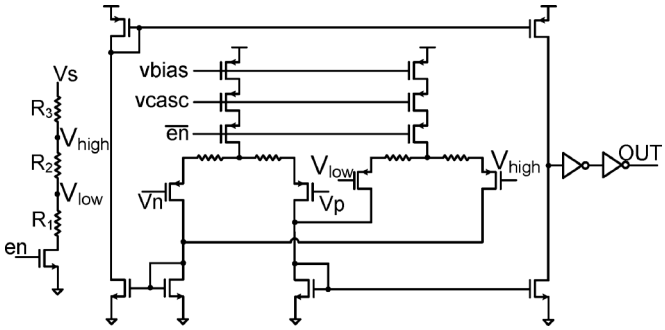

Fig. 7. Differential mode comparator circuit.

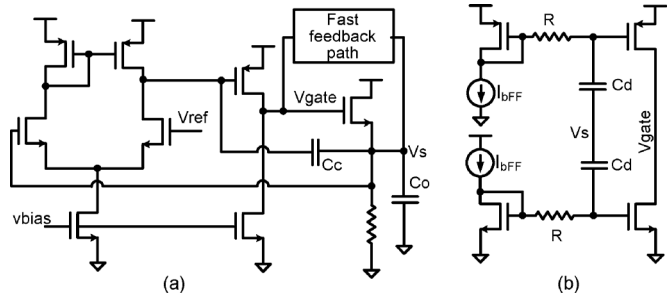

Fig. 8. (a) Regulator circuit with internal compensation and NMOS pass transistor. (b) Fast feedback path used for transient response compensation.

the digitally programmable transistors to control the output differential amplitude. The calibration algorithm starts by setting the calibration word to the minimum switch resistance situation (all the fingers disabled). At every calibration step, the differential amplitude is compared with the reference and the calibration word shifted if the amplitude is lower than the target. The process stops when the programmed differential amplitude is detected to be higher than the target and this is considered as the optimum calibration word. Calibration is quite robust against V_{dd} variations and initial calibration compensates well against process variations. However, it is wise to recalibrate in case of strong temperature variations. For this purpose, calibration controller input signal CAL (see Figs. 3 and 6) can be activated when recalibration is required.[1] Initial calibration requires about 20 controller clock cycles and recalibration about less than five. Controller clock is 10 MHz. This clock frequency has to be slow enough to allow differential amplitude to settle before the digital controller takes a reliable reading. This way, stability of the thermometric control algorithm is guaranteed. During the design phase we verified by post-layout simulation with real delays for gates and interconnections that a controller clock period of 100 ns was safe enough, which was then verified experimentally.

Fig. 7 shows the schematics of the proposed differential mode comparator. Two source degenerated differential pairs are used to compare differential amplitudes which may be in the order of 500 mV. Amplitudes in this range need to be processed by a highly linear differential pair to generate currents proportional to the target differential amplitude without saturation. The currents generated by the input stage are combined through current mirrors in order to produce an output current proportional to the difference between a reference differential amplitude and the programmed amplitude. A resistor divider is used to generate precise internal references. All static power consumption is eliminated when the driver is not being calibrated using an enable switch.

B. Power Management for Switching Drivers

The driver requires the output current to switch from the mA range during regular transmission to the nA range during pauses. Furthermore, instantaneous current pulses supplied by V_s must be very sharp for a high speed switching operation. Typical voltage regulators using a low frequency dominant pole for loop stability are not able to react at the speed demanded by the required instantaneous output current. A large external capacitor is used to compensate the loop and provide the needed charge packets during transients. Even if the load is not demanding current, the regulator power transistor can draw several mA due to the loop dynamics.

Internally compensated regulators do not employ this large output capacitor. The dominant pole is located in an internal node and the relatively small output capacitor cannot be efficiently used to provide instantaneous output current pulses. These kinds of regulators require internal transient response compensation in order to achieve similar specifications as externally compensated regulators. However, they allow the pass transistor current to change at the same speed as the output current. Fig. 8(a) shows the regulator schematics used in this work to generate the driver voltage supply V_s.

Several design techniques have been used to combine internal compensation with good transient response. Stability is achieved using a two stage amplifier with a Miller compensation capacitor C_c. This capacitor splits the dominant amplifier internal pole and the output pole, improving the system phase margin. The pass element is built with a source follower because no low drop-out is required as $V_s < 1$ V is well below $V_{dd} = 3.3$ V. If output voltage increases, NMOS overdrive is reduced and output current is lowered. Otherwise, the loop acts in the opposite way, increasing the output current. Using an NMOS transistor as pass element helps stability because V_s is a low impedance node and the output pole is pushed to high frequencies.

A fast feedback path between the output node and the pass transistor gate is implemented to reinforce the transient compensation and improve the regulator slew rate. The compensation circuit is based on differentiating the output voltage V_s and generating a current that is injected or subtracted from the pass transistor gate node $V_{\rm gate}$. If a positive voltage variation at V_s is detected, then the current drawn by the pass transistor is excessive for the current load conditions and its gate voltage must be decreased by subtracting current from $V_{\rm gate}$; that current is instantaneously provided by the N-type transistor of the fast feedback path. A negative slope in V_s means that the load is demanding current that the regulator cannot provide. Thus, the fast feedback path injects current in $V_{\rm gate}$ to increase the pass transistor driving capabilities and improve the response time to the change in the load conditions.

[1]In this prototype we did not include any temperature tracking circuit to trigger signal CAL. Signal CAL is activated periodically by an external circuit every 10 seconds.

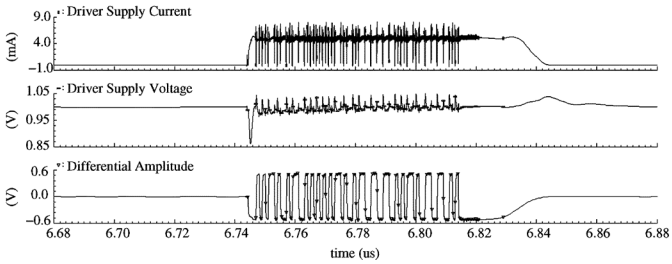

Fig. 9. Transient simulation of regulator voltage V_s during an event data burst.

This extra loop may impact stability by pushing the output pole to lower frequencies, degrading the phase margin. The transient compensation has therefore been carefully designed, since there is a trade-off between stability and transient response to variations in the load conditions. Montecarlo simulations with process and mismatch variations for the worst case scenario for stability (no load) reveal a 62° mean phase margin with 1.2° of 1-σ variation, demonstrating the robustness of the employed design procedure. Fig. 9 shows a post-layout simulation of the transient response of the regulator supplied voltage V_s during an event with OFF-to-ON switching before the transmission and ON-to-OFF switching afterwards. As can be seen, voltage V_s suffers a slight decrease from 1 V to 0.85 V during the OFF-to-ON transient that lasts for about 150 ps. Such short transient does not affect the event data integrity.

C. Receiver Circuitry

The common mode generated by the calibration circuit is not well controlled as only one branch is implemented as a digitally controllable transistor. Moreover, the reference voltage V_s is around 1 V, leading to a low output common mode for a 3.3 V voltage supply. The receiver front-end must therefore be implemented with PMOS transistors and input common mode range must be optimized. This must be combined with techniques for quickly turning the bias currents ON/OFF.

The receiver circuit is shown in Fig. 10. A pre-amplifier provides a first gain stage capable of processing a very low common mode. DC voltages at the PMOS differential pair output are set low enough to enlarge input common mode range. This is done by using a folded cascode output stage that shifts up the output common mode. The load resistances to the output stages determine the gain, output common mode and bandwidth of the amplifier. However, as the comparator can be designed with lower aspect ratio devices thanks to its preamplifier stage, the load capacitance can be minimized. This pushes the output pole to higher frequencies, improving the frequency response of the receiving chain. A rail-to-rail version of the serial signal is obtained using a continuous time comparator.

Receiver power consumption is mainly due to preamplifier and comparator bias currents. However, these two circuits are not needed during pauses if the comparator output is forced to have a constant value (zero in this design). Their bias currents can therefore be disabled during pauses. Signal *ackSER* is used to switch the receiver ON/OFF. The switches marked with dashed lines in Fig. 10 are used to turn OFF the bias currents in the OFF state. These switches have been designed to enable

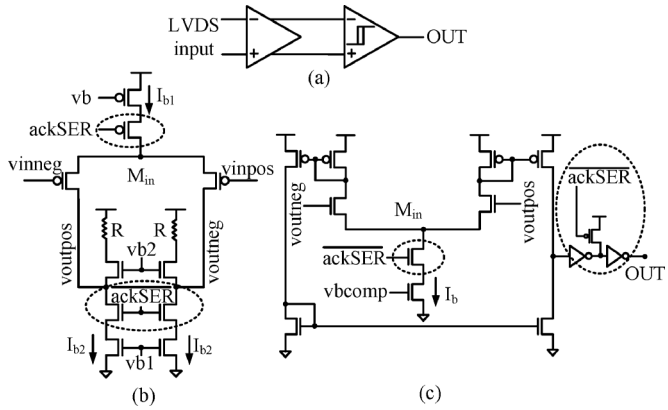

Fig. 10. (a) Receiver architecture. (b) Preamplifier. (c) Continuous time comparator.

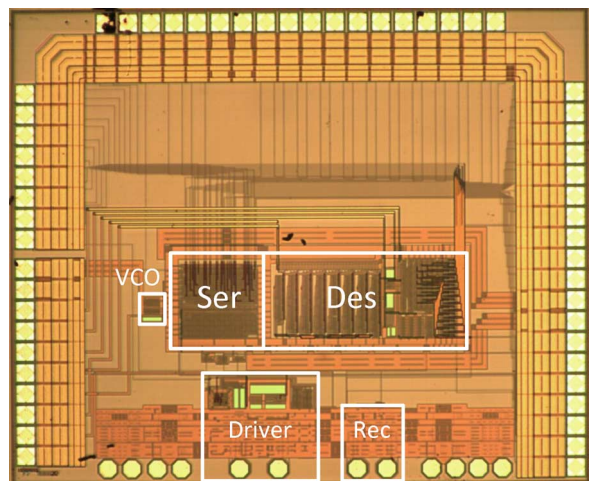

Fig. 11. Microphotograph of the test chip.

very fast transitions and to have a low ON resistance. A large current passes through these transistors when the receiver is enabled and any voltage drop through the switches may affect the tail current source saturation.

III. Experimental Results

A test prototype for the switchable I/O circuits was fabricated in 3.3 V 0.35 μm CMOS. All the components described in this paper were integrated as custom-made pads with ESD protections, along with ground and supply voltage decoupling capacitors and a circuit providing the analog biases. The voltage mode driver needed a 530×490 μm^2 area, while the receiver took 270×341 μm^2. Fig. 11 shows a microphotograph of the fabricated chip, the main parts of which have been highlighted. The serial AER Manchester-encoding SerDes circuit [15] handles the parallel AER flow and creates the proper signals for the driver/receiver pair. The transmission channel consists of a pair of PCB traces forming a 100 Ω differential microstrip line 5 cm in length.

Fig. 12 shows a snapshot of the test set-up used in the experiments. Two 16-bit USB-AER boards [25], configured as senders, receive events from a PC through USB connections. These events are sent through parallel connectors to the test board using the parallel-AER protocol. Each USB-AER board

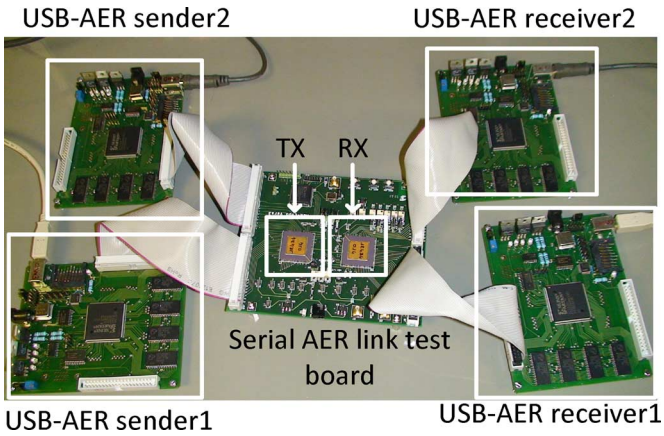

Fig. 12. Test set-up to generate a 32 bit AER pattern.

provides a 16-bit AER bus, but a 32-bit version is needed for the serial transmitter. For this reason, streams coming from the two different boards must be synchronized to form a 32-bit AER bus. A CPLD implements a C-element to generate the input request for the chip that acts as the serializer. This way, both 16-bit parallel input streams are merged into a single 32-bit stream which is serially transmitted. At the receiver side, the output flow must be split into two AER streams, each of which can be captured by a single 16-bit parallel USB-AER board, configured as a receiver. The CPLD performs this task in the same way as on the transmitter side but the acknowledge is generated using the handshaking signals provided by the receiving USB-AER boards. Each output USB-AER board is able to transmit captured events to the PC through its USB connection.

Fig. 13 shows how the AER protocol signals flow through the voltage mode serial link for a 500 Mbps bit rate. The delay between *reqIN* and *ackIN* at the input parallel AER interface is 15 ns and the serialization process duration is 68 ns. The serial handshaking protocol introduces a delay of 4.6 ns between the *reqSER* and *ackSER* and the acknowledge stays activated for 81 ns. The output handshaking protocol with the USB-AER test boards introduces a delay of 23 ns. For a 500 Mbps bit rate, an input to output request latency of 89 ns is measured, leading to a maximum event rate of 11.2 Mevent/s.

Fig. 14 shows the differential mode of the high speed bit stream at the receiver input. Waveforms were acquired with the Agilent DSO81304 B Infinium oscilloscope with 5 GHz bandwidth probes. The bit rate is set to 500 Mbps and a 5 Mevent/s 32 bit event rate stream is generated with the USB-AER boards. The differential amplitude measured after calibration is 520 mV, which represents a 4% error with respect to the target amplitude of 500 mV ($V_s = 1$ V). ON/OFF switching transients are the times taken for the differential signal to change from 0 to V_s and viceversa (see Fig. 14). Switching ON time is 1.5 ns, while the switching OFF time is 7 ns. The latter was made longer to minimize the voltage drop observed in the regulator when the output current is switched from maximum to minimum values. Fig. 15 shows the eye diagram measured at the receiver input. A 40 ps of rms jitter was obtained for this implementation, very similar to the value reported previously [15] with the conventional non-switchable LVDS driver [16]. Note that, since our

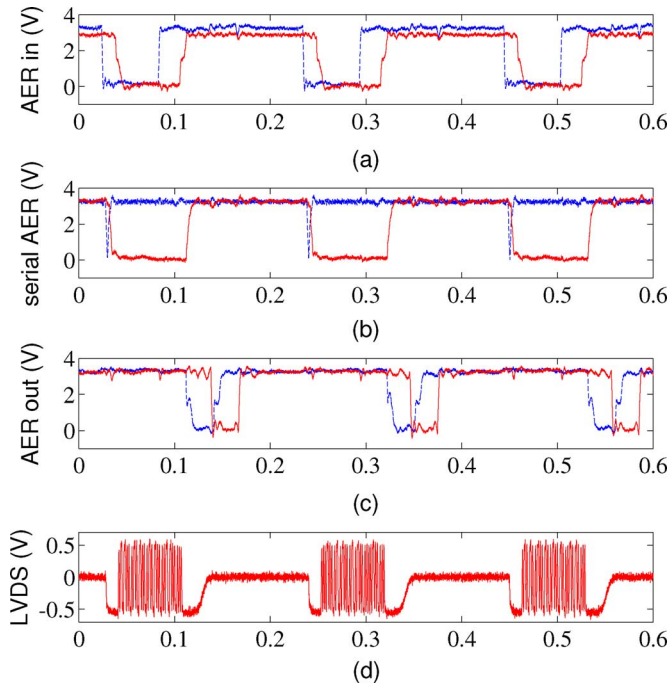

Fig. 13. AER protocol management at (a) *reqIN* (dotted line) and *ackIN* (continuous line) signals, (b) *reqSER* (dotted line) and *ackSER* (continuous line) signals, (c) *reqOUT* (dotted line) and *ackOUT* (continuous line) signals, and (d) differential mode of the LVDS signal. Time scale is μs.

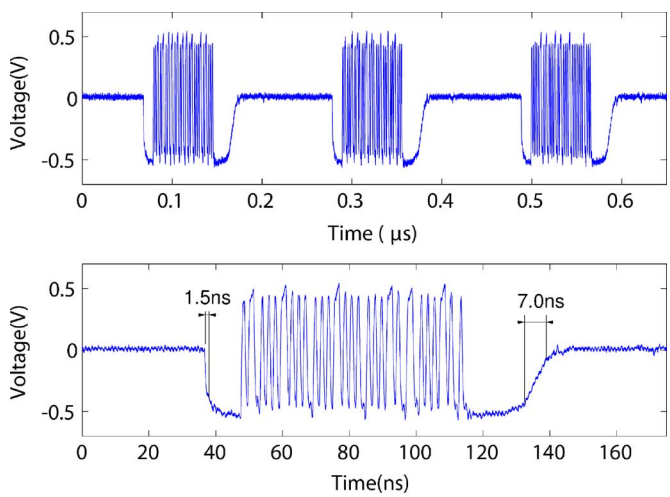

Fig. 14. Measured high speed serial signal at receiver input for the voltage mode driver.

bit serial data streams are Manchester encoded, there is always a transition in the middle of a bit transmission, which makes the eye diagram look different than when transmitting conventional non-Manchester-encoded random bits.

Transmission frequency was varied by tuning the on-chip high frequency Voltage Controlled Oscillator (VCO) to achieve the maximum event rate. In this case, the link worked correctly at a maximum bit rate of 638 Mbps, with an input to output request latency of 73 ns. This reveals that the maximum achievable event rate combining the burst mode SerDes architecture proposed previously [15] with the switchable I/O circuitry presented in this paper is 13.7 Mevent/s with 32-bit events.

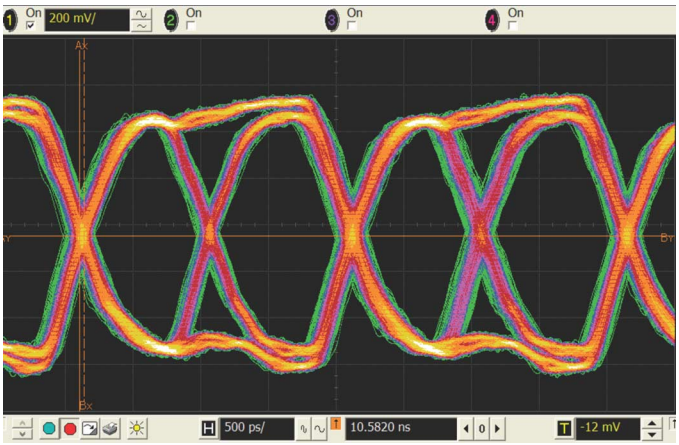

Fig. 15. Eye diagram for the voltage mode driver at receiver input.

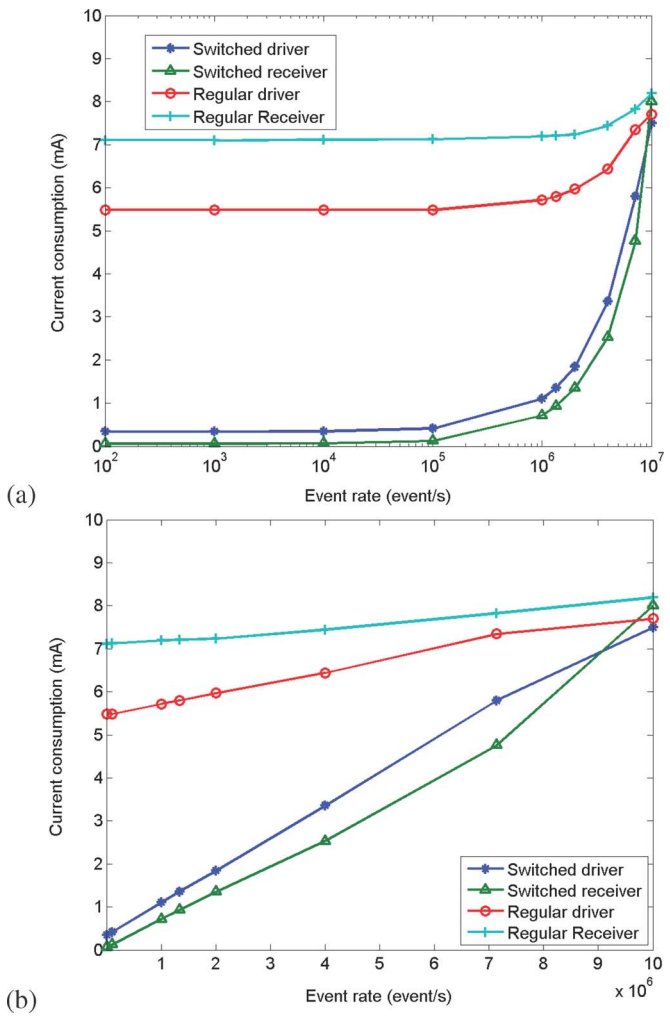

Fig. 16. Voltage-mode switchable driver and receiver current consumption versus event rate. (a) Event rate in log scale. (b) In linear scale.

Fig. 16 shows the current consumption dependence with the event rate for the case $V_s = 1$ V. Current consumption scales down with the event rate, reaching a minimum of 406 μA (343 μA for the driver and 62.5 μA for the receiver) when the link operates below 10 Kevent/s. The test chip has a control

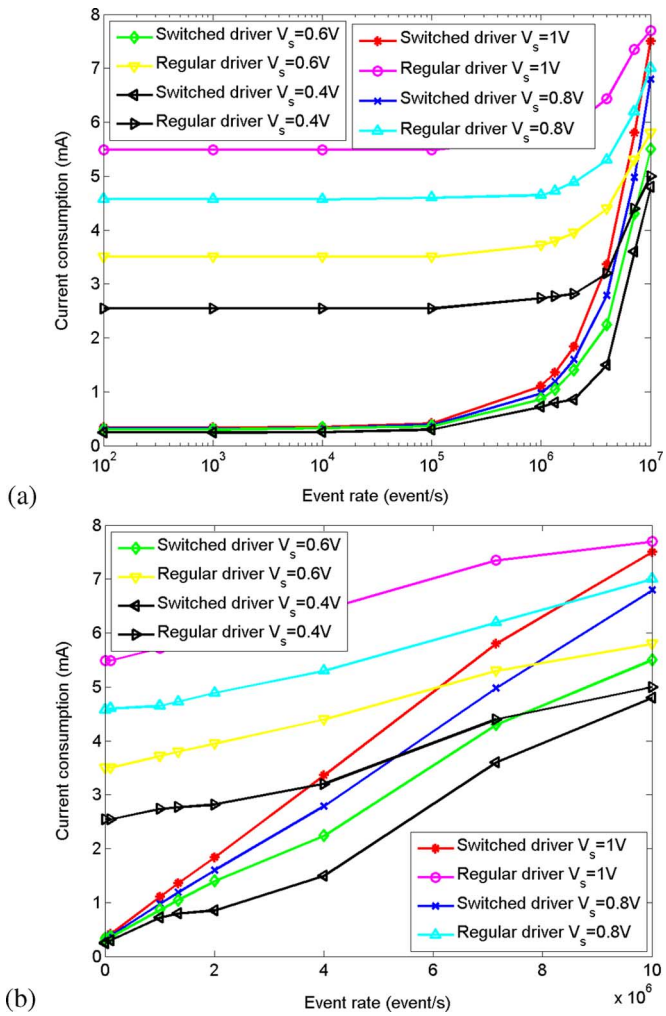

Fig. 17. Voltage-mode switchable driver current consumption versus event rate for different V_s voltages. (a) Event rate in log scale. (b) In linear scale.

bit which disables the switching mechanism resulting in a conventional voltage mode link. If the circuits are configured to not switch OFF during pauses, current consumption for the minimum event rate is 12.6 mA (5.5 mA and 7.1 mA for the driver and receiver, respectively). In the maximum event rate situation, driver and receiver stay turned ON most of the time and current consumption is the same for the switching and non-switching implementations. This maximum current consumption is 15.9 mA (7.7 mA for the driver and 8.2 mA for the receiver), which is 40 times the consumption at 10 Kevent/s.

The lower current consumption is due to the regulator quiescent current. Decreasing this current leads to a larger gap in the pass transistor gate voltage for ON and OFF situations. This trades off with the regulator transient response because compensation circuits have to be faster in charging/discharging the pass transistor gate node. However, this problem can be alleviated in more advanced technologies which enable a faster regulator step response without compromising stability.

Differential amplitude is controllable through an off-chip analog bias voltage. Power consumption while transmitting events is proportional to the differential amplitude defined by V_s. The amplitude control calibration loop selects the optimum

TABLE I
PERFORMANCE COMPARISON WITH OTHER VOLTAGE MODE DRIVERS

	[20]	[21][2]	[22][3]		[23][4]	[24][4]	This work
Technology	90 nm	0.18 μm	0.18μm		65 nm	90 nm	0.35 μm
f_t(GHz)	180	120	120		250	180	15
Power Supply (V)	1	1.8	1.8		1 (pre-driver) 1.5 (driver)	1.2	3.3
V_{amp}: Diff Amplitude(mV)	150	125	450	88	500	600	200-500
BR: Bit Rate(Gbps)	6.25	3.6	3.5	3	8.5	8	1.28
Bit Rate / f_t	0.035	0.03	0.029	0.025	0.034	0.044	0.085
Area (mm^2)	0.15	0.198	0.044	0.024	0.065	0.138	0.26
Area/λ^2	74	24	5	3	61	68	8.5
P_{max} (mW)	2.26	7.86	22.1	9.0	96	101	15.8-25.4
P_{min} (mW)	2.26	7.86	22.1	9.0	96	101	1
Impedance Matching	Pre-Driver Supply Voltage	Pre-Driver Supply Voltage	Number of fingers		Source series termination	Pass Transistor	Number of fingers
FoM1=BR/P_{max} (Gb/J)	2780	460	160	330	89	80	81-51
FoM2=FoM1/f_t	15	3.8	1.3	2.8	0.35	0.44	$5.4-3.4$

[2]w/o internal regulator and single ended output
[3]w/o internal regulator
[4]power consumption of one whole TX chip

calibration word to achieve the required driver switches resistance and have a $V_s/2$ amplitude. Fig. 17 shows how the selected differential amplitude affects driver current consumption. Current consumption for higher event rates can be reduced by setting a lower amplitude, but it remains roughly constant for very low event rates. In this situation, current consumption is not given by the current delivered to the load, but by the regulator quiescent current.

Table I compares between voltage mode implementations of high speed drivers reported in literature. Two figures of merit are provided. The first one is $FoM1 = BR/P_{\max}$ (max bit rate over max power), which is a standard figure of merit giving an absolute measure of the final performance, but strongly dependent on technology. In order to provide an additional figure of merit to evaluate the intrinsic benefit of the design technique, we also provide a second figure of merit which is $FoM1$ normalized with respect to the technology transition frequency f_t. The higher $FoM2$ is, the more efficient one can consider the design. This work is the only solution that scales down link power consumption with event rate. The driver design is comparable to other state of the art solutions in terms of area, supply voltage and differential amplitude. Bit rate and area data are also shown normalized by the corresponding technology transition frequency[2] f_t and λ to allow a fair comparison between designs. The physical bit rate for this work is 1.28 Gbps which corresponds to twice the Manchester encoded transmitted data bit rate of 0.64 Gbps.

IV. CONCLUSION

This paper describes the design and testing of a low power switchable driver/receiver pair intended to be used in large scale event-driven neural networks hardware implementations. As AER streams are inherently asynchronous, the link only transmits packets when there is relevant information that must be communicated. Arbitrarily long pauses can occur and they can be used to switch off the driver and receiver currents to save power. However, this switching mechanism must be fast enough to avoid a reduction in the maximum event rate achievable by the link. This imposes the design constraints addressed in this paper, regarding the impedance matching mechanism, the power management of the high speed driver and the low common mode of the received signal. Experimental results are provided for a 3.3 V 0.35 μm CMOS prototype which achieves a current consumption reduction factor between the maximum and minimum event rate situations of 22 for the driver and 130 for the receiver at 500 Mbps.

[2]References in Table I do not provide their technology f_t, but this number has been estimated from other similar technologies.

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