Real-time phase correlation based integrated system for seizure detection

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ABSTRACT

This paper reports a low area, low power, integer-based digital processor for the calculation of phase synchronization between two neural signals. The processor calculates the phase-frequency content of a signal by identifying the specific time periods associated with two consecutive minima. The simplicity of this phase-frequency content identifier allows for the digital processor to utilize only basic digital blocks, such as registers, counters, adders and subtractors, without incorporating any complex multiplication and or division algorithms. In fact, the processor, fabricated in a 0.18μm CMOS process, only occupies an area of 0.0625μm^2 and consumes 12.5nW from a 1.2V supply voltage when operated at 128kHz. These low-area, low-power features make the proposed processor a valuable computing element in closed loop neural prosthesis for the treatment of neural diseases, such as epilepsy, or for extracting functional connectivity maps between different recording sites in the brain.

Keywords: Seizure detection, Phase synchronization, Low power CMOS VLSI

1. INTRODUCTION

Epilepsy[1,2] is the second most common neurological disorder after strokes affecting over 1% of the worlds population.[3] In about 65% of patients with epilepsy, seizures are well-controlled with currently available anti-epileptic drugs.[4,5] Another 5% could benefit from resective therapy, i.e., from surgically removing a circumscribed region of the brain that generates seizures. In these cases, there is a 60-70% chance of gaining long-term remission.[6] Unfortunately, even with maximal available therapy, 30% of patients with epilepsy continue to have uncontrolled seizures, resulting in impaired quality of life and increased risk of injury, disability, and death. Thus, other therapeutic options for refractory epilepsy are needed.

Recently neural prostheses have been introduced as an alternative method for treating epilepsy.[7] These prostheses, generically represented in Fig. 1, take the form of a closed loop feedback systems which detect specific bio-markers in neural signals during the pre-ictal or ictal stages of seizures. Following detection, these feedback systems stimulate zones of the brain, with the goal of disrupting the excitability of the neurons around specific regions and, hence, preventing the spreading of seizures.[8] Different bio-markers have been explored in order to try to predict seizures before they happen. They include neural spiking,[9] correlation[10] and the most tantalizing, phase synchronization,[11] in which this paper focuses.

As described in Ref. 11, a large decrease in synchronization between two neural signals can be seen for a given period during the pre-ictal stage. This decrease in synchronization is believed to be a significant bio-marker which could hold the key to prediction and prevention of epileptic seizures via neural prosthesis. To detect such bio-marker, Application-Specific Integrated Circuit (ASIC) processors such as in Ref. 8 have been designed. However, they utilize complex algorithms to extract the instantaneous phase of the signals and demand bulky and power-hungry computations.[12] This makes multichannel extension difficult as scalability is reduced.

The Discrete Distance Approximation (DDA) processor proposed in this paper uses a combination of signal filtering, minima detection and error accumulation in order to calculate the phase-frequency differences between

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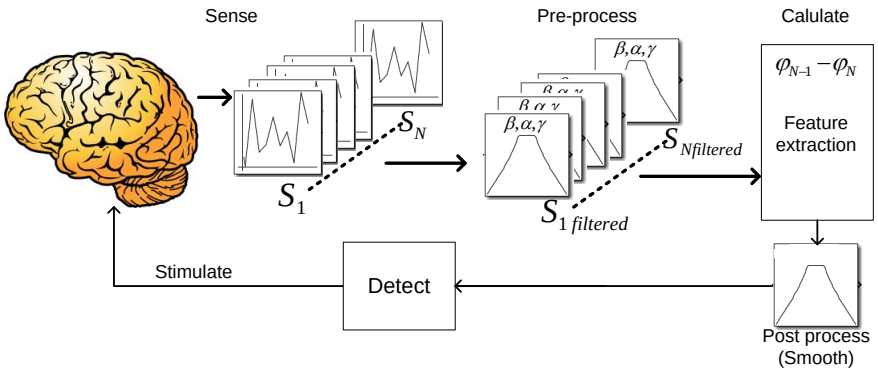

Figure 1. Scheme of a closed-loop neural prosthesis.

two neural signals. The processor is integer-based and incorporates only power of two divisions and multiplications. This processor has an accuracy comparable to that of more complex algorithms and, in terms of logic, the DDA processor can reduce the amount of hardware needed to detect pre-ictal events by as much as 96.8% which could be exploited for multichannel calculations. Indeed, the processor, fabricated in a 0.18μm CMOS technology, consumes 12.5nW under full load and only occupies 0.0625μm^2.

The paper is organized as follows. Sec. 2 reviews some of the methods most commonly used for quantifying the phase synchronization between signals and introduces the proposed algorithm. Then, Sec. 3 presents the structure and operation of the developed processor for DDA computation and describes the methods followed for testing the processor and the achieved performance. Sec. 4 presents experimental results obtained with neural recordings available in epilepsy databases and, finally, Sec. 5 gives some concluding remarks.

2. ALGORITHMS FOR MEASURING SYNCHRONIZATION

Synchronization is usually expressed by the *phase locking* condition $n \cdot \varphi_{s1} - m \cdot \varphi_{s2} = const.$, where n and m are integers, and φ_{s1} and φ_{s2} denote the phase variables of the oscillating signals $s_1(t)$ and $s_2(t)$. However, in the presence of noise, this condition is relaxed to the weaker constraint $|n \cdot \varphi_{s1} - m \cdot \varphi_{s2}| < const.$ or to the *frequency entrainment* condition, $n \cdot \langle \omega_{s1} \rangle - m \cdot \langle \omega_{s2} \rangle = 0$, where ω_{s1} and ω_{s2} denote the angular frequencies of $s_1(t)$ and $s_2(t)$, respectively, and $\langle \cdot \rangle$ denotes averaging over time.[13] In practical situations, the estimation of phase synchronizations between neural signals is preceded by a pre-filtering stage and, therefore, signals $s_1(t)$ and $s_2(t)$ are band-limited in specific frequency bands. For instance, in the case of signals obtained by EEG or ECoG methods, these bands range from almost zero to 100Hz and can be further separated in to the conventional neuro-physiological bands: δ∼0.1-3Hz, θ∼4-7Hz, α∼8-12Hz, β∼12-30Hz or γ∼30-100Hz.[14] Accordingly, it is more likely to encounter synchronization for phase locking values $n = m = 1$.

The algorithms for measuring the synchronization between two signals $s_1(t)$ and $s_2(t)$ over time encompass two main steps.[15,16] First, the phase angles φ_{s1} and φ_{s2} are estimated. This is often done by extracting the instantaneous phase at each signal sample.[13] Once the phase angles are derived, their difference (relative phase or relative error), $\triangle\varphi = \varphi_{s1} - \varphi_{s2}$, is obtained. The second step consists in quantifying the amount of synchronization over a given period of time. This period is usually defined by a sliding window of N samples and, hence, the quantification inherently carries out a data reduction process. The synchronization measures thus obtained often contain rapid fluctuations. Hence, an additional smoothing process can provide a more useful baseline for changes in synchronization and lead to more accurate detection of events.

Before presenting in subsection 2.2 the proposed technique for the computation of phase angles and the associated calculation of the synchronization measure, the next subsection will briefly reviewed more conventionally approaches, which are regarded as benchmarks. This will help to further highlight the simplicity of the proposed algorithm.

2.1 Conventional approaches

Two main approaches have been proposed for the estimation of phase angles. One is based on the Hilbert Transform and the other on the Wavelet Transform.

The Hilbert transform (HT) creates a projection of the original signal on to the imaginary plane, creating a 90° phase shifted version, $\tilde{s}(t)$, of the original signal, $s(t)$. Analytically, the Hilbert transform can be interpreted as the convolution of $s(t)$ with the function $h(t) = 1/(t)$ and is given by:[16]

$$\tilde{s}(t) = \frac{1}{\pi} \int_{-\infty}^{+\infty} \frac{s(\tau)}{t-\tau} \cdot d\tau, \tag{1}$$

where the integral is taken in the sense of Cauchy principal value. This is equivalent to passing $s(t)$ through a linear filter with a transfer function $-jsgn(f)$. From (1), the instantaneous phase can be extracted as

$$\varphi_s(t) = \arctan \frac{\tilde{s}(t)}{s(t)}, \tag{2}$$

A similar approach for estimating phase angles[17] uses a definition based on the Wavelet Transform (WT). Here, the phase variable is defined as,

$$\varphi_s(t) = \arctan \frac{imag(W(t))}{real(W(t))}, \tag{3}$$

where $W(t)$ is the convolution of the band-limited signal $s(t)$ with a complex Gabor wavelet $\psi(t)$,

$$\begin{aligned} W(t) &= \int_{-\infty}^{+\infty} \psi(t-\tau) s(\tau) \cdot d\tau, \\ \psi(t) &= \exp\left(\frac{-t^2}{2\sigma^2}\right) \cdot \exp\left(j\omega_0 t\right) \end{aligned} \tag{4}$$

where σ is the decay rate of the wavelet and ω_0 is the center frequency of the signal band.

The Phase Locking Value, PLV, or mean phase coherence usually accompanies the HT or WT methods as an index for quantifying the amount of synchronization between two signals. It is defined as,

$$PLV = \left|\frac{1}{N} \sum_{k=0}^{N-1} \exp(j\triangle\varphi_k)\right| = \frac{1}{N} \cdot \sqrt{[\sum_{k=0}^{N-1} \cos(\triangle\varphi_k)]^2 + [\sum_{k=0}^{N-1} \sin(\triangle\varphi_k)]^2}, \tag{5}$$

The PLV converts instances of the relative phase $\varphi_{s1} - \varphi_{s2}$ into unit vectors on the complex plane. If N of said vectors all have the same instantaneous phase (i.e the same vector direction) then the PLV will average out to 1 which equates to fully coupled oscillations for that period. However, in the case that the relative phase angles are very different the PLV will result in a value close to 0.

Other measures of phase synchronization are based on conditional probability or on Shanon entropy.[11] In both cases, the synchronization measures are confined to the interval [0, 1] where high values indicate a high degree of phase synchronization and low values correspond to unsynchronized signals.

The above methods can be easily programmed in computers, however, they break down when dealing with silicon integration as they occupy large area and consume a lot of power. For instance, in a recent implementation of the HT approach with PLV synchronization computation, trigonometric functions were implemented using the CORDIC algorithm and the gate count was as much as 41,366, occupying 0.178mm^2 and dissipating 70.4μW from a 1.2V supply.[8]

2.2 Discrete Distance Approximation (DDA) and Synchronization Index (SI)

The proposed method is based on the estimation of the instantaneous phase of a band-limited signal through the identification of distinct marker events in its waveform. Without loss of generality, it will be assumed that such events correspond to the signal minima $t_n, n = 1, 2, \ldots$. The time interval between two consecutive minima correspond to one complete cycle and, therefore, the phase increment during this period is exactly 2π. Hence, the signal phase can be approximated for any arbitrary time instant $t_n < t < t_{n+1}$ as,

$$\varphi_s(t) \approx 2\pi \frac{t - t_n}{t_{n+1} - t_n} + 2\pi n, \tag{6}$$

where the term $2\pi n$ unwraps the phase angle and $T_n = t_{n+1} - t_n$ is defined as the transition period between the minima. Note that this approximation notably simplifies phase estimation as the problem basically reduces to measure time intervals. For this reason, the algorithm has been called Discrete Distance Approximation (DDA).

Another important consideration taken into account in the DDA algorithm is the fact that the computation of the synchronization measure ultimately relies on the evaluation of relative phases over a time interval (see eq. 5). Accordingly, in DDA, the focus is not put on the calculation of individual phases for their ulterior subtraction, but on the direct estimation of $\triangle\varphi$. Following eq. 6, the target will be thus the evaluation of the differences $\triangle T_n = T_n^1 - T_n^2$, where $T_n^x = t_{n+1}^x - t_n^x$ denotes the transition period between two consecutive minima in signal x, with $x = 1$ for signal 1 and $x = 2$ for signal 2.

Regarding the synchronization measure, instead of using the PLV function in eq. 5, the proposed approach avoids the use of trigonometric functions by linearly approximating the exponential for small $\triangle\varphi$ values as $PLV \simeq |1 + j\sum_{k=0}^{N-1} \triangle\varphi_k/N|$. After some further simplifications, the following synchronization index, SI, can be defined,

$$SI = 1 - \sum_{n=0}^{K-1} \frac{|\triangle T_n|}{K \cdot \triangle T_{max}}, \tag{7}$$

where $\triangle T_{max}$ is the maximum possible difference between transition periods which occurs for frequencies at the opposite corners of the signal band limits. Additionally, K represents the number of complete $\triangle T_n$ considered in the averaging sliding window. Similar to the PLV, the synchronization index provides an approximate 0 indicating close to no coupling and an approximate 1 for perfect coupling. As long as the duration of $\triangle T_n$ may vary in the course of time, the update rate of the synchronization index SI, although synchronous with the sampling rate of the neural signals, will not be uniform. Differently, the PLV value in eq. 5 updates every N signal samples.

Fig. 2 shows the results obtained from both the Hilbert transform (utilizing a $N = 100$ sample window) and the DDA approaches, for a 22Hz static sine wave and a chirp from 12Hz to 32 Hz. From these results we can note that the DDA accomplishes the detection of the fully synchronized signals at 22 Hz by producing a value 1. Either side of the 22Hz center frequency the DDA index value falls away at a steady rate. The two approaches are comparable, with the DDA producing a piecewise linear approximate of the Hilbert transform and eliminating the side lobes.

3. DIGITAL IMPLEMENTATION

3.1 Block Diagram

Fig. 3 shows the block diagram of the proposed VLSI implementation of the DDA algorithm. Initially both signals are pre-processed by a bandpass filter to select the desired range of frequencies for the estimation of phase synchronization. Additionally, a low pass filter is used to further attenuate high frequency components. Afterwards, the filtered signals are respectively passed through corresponding marker detectors for identifying the time instances leading to the calculation of the transition periods. As already mentioned, signal minima will be considered as marker events in this work. Each detector simply consists of a digital comparator driven by the current and previous samples of the signal, $s_x(i)$ and $s_x(i-1)$, a shift register which stores the M most

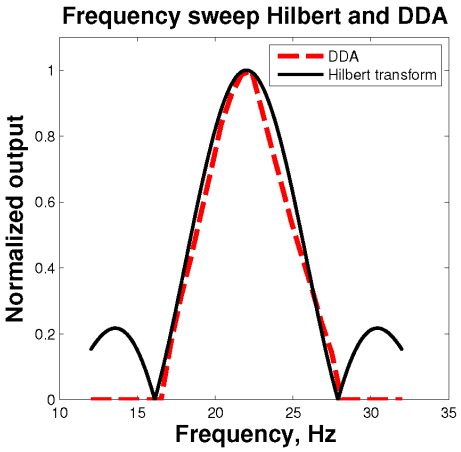

Figure 2. Results from DDA and Hilbert transform approaches, using a static sine wave of 22Hz and a frequency sweep from 12 to 32 Hz.

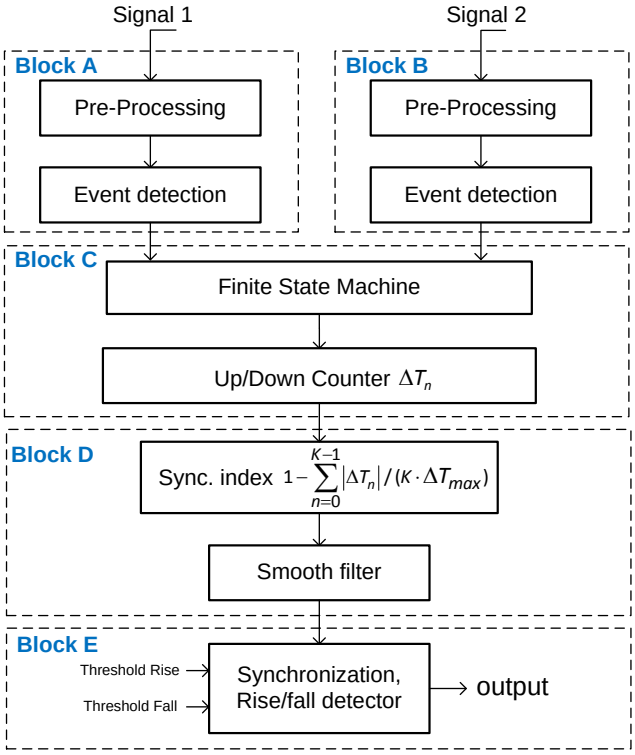

Figure 3. Algorithm Flow Diagram

recent results of the pair-wise comparison, and a combinational block which, based on the sequence gathered in the register, decides if a minimum is present. This latter block allows for a finite number Q of potential outliers in the up and down transitions of the signal which may result from noise perturbations. In the proposed implementation $M = 10$ and $Q = 2$.

Based on the detected markers, an up/down counter controlled by a finite state machine calculates the differences between transition periods, $\triangle T_n$. Fig. 4 shows the algorithm implemented by the finite state machine. In short, the machine defines the state of the counter according to the counter previous state and the signal that generated the last marker. Using the obtained $\triangle T_n$ values, an accumulator generates the synchronization

```
Reset {counter to zero; MSx = 0, x = 1, 2}
Detect first Event(s) and identify the signal source
Increment by 1 the Event count variable per signal, MSx = MSx + 1, for x = 1, 2
If simultaneous Event(s) in both signals, keep counter frozen, otherwise, count up.

While on
        Detect new Event(s) and identify the signal source
        Increment by 1 the Event count variable per signal, MSx = MSx + 1, for x = 1, 2

        If MS1 > 1 && MS2 > 1
                Save unsigned counter value  → DeltaT
                Counter to zero; MSx = 0 or 1, x = 1, 2, according to last Event(s)
                Define counter state according to the last Event(s) – see next
                Continue

        % Define counter state
        if simultaneous Event(s) in both signals, counter frozen
        if Event detected on the same signal of last Event,
                if the counter state was frozen, it starts counting up, …
                … otherwise, keep the same state in counter
        otherwise
                if the counter state was frozen, it starts counting down, …
                … otherwise, the counter is frozen

        if counter overload
                Save unsigned counter value  → DeltaT_max
                Counter to zero; MSx = 0, x = 1, 2
end
```

Figure 4. Finite state machine algorithm.

index, as defined in eq. 7. The number of iterations K performed by the accumulator and the value of $\triangle T_{max}$, which can be estimated a priori from the signal' bandwidth, are chosen so that the scaling factor $K \cdot \triangle T_{max}$ can be closely approximated by a power of two. The synchronization index thus obtained is smoothed by a lowpass filter for removing fast fluctuations. In order to reduce the hardware burden, a simple exponential filter defined by the recursive equation:

$$y(m) = (1 - \alpha) \cdot y(m - 1) + \alpha \cdot SI(m), \tag{8}$$

where α is comprised between 0 and 1. In practice, this parameter is chosen as a negative power of two, so that multiplications reduce to simple shifting operations in a register.

The last element in the diagram of Fig. 3 is an alarm block which detects if the synchronization index has dropped below a certain threshold, T_{fall}, for a set number of cycles or whether it has risen above a certain threshold, T_{rise}, for a set number of cycles. The former operation can be used to potentially predict upcoming seizures, while the latter can be used to gather useful information on seizure activity of a given patient (i.e number of seizures, severity of seizures). Comparators and counters constitute the basic elements of the alarm block.

3.2 Test chip

Fig. 5 shows the test board (left) and layout (right) of a test-chip implementing the DDA algorithm. The chip has been fabricated in a 0.18μm CMOS process and occupies an active area of 0.0625μm^2 including, in addition to the main processor core, two series-to-parallel input signal ports, one parallel-to-series output port and some buffers for testing intermediate nodes. The total number of integrated gates is 6,053.

An Agilent 16823A logic analyzer was used for the evaluation of the chip. Input signal waveforms were uploaded to the analyzer for driving the chip. The synchronization index output was collected through a data pod

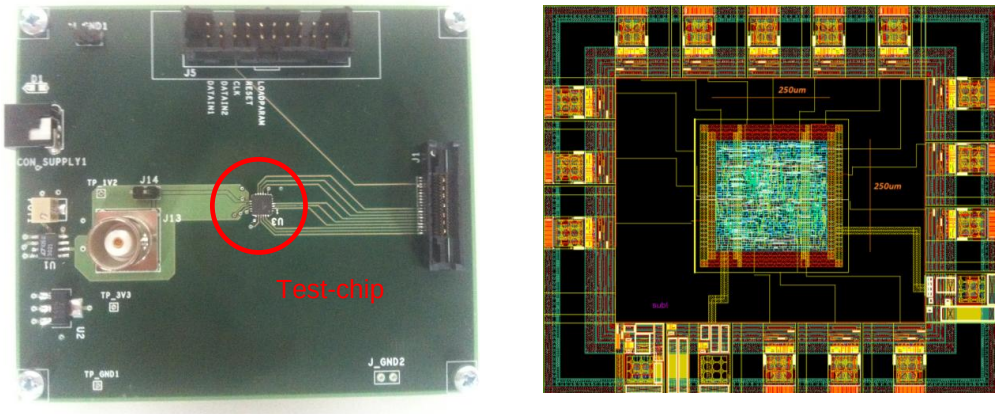

Figure 5. AMS-0.18-micro chip

connector and transferred to a laptop for further analysis. Both input and output signals have 10-b resolution. The chip operates from a single master clock at 128kHz. The test platform features a voltage regulator for externally adjusting the biasing voltage of the chip to 1.2V and level shifters for interfacing with the 3.3V used by the analyzer.

The power consumption of the chip and its performance largely depends on the sampling frequency of the input signals. The slower the sampling rate, the lower the number of operations per second carried out by the chip and, hence, the lower its power consumption. However, the accuracy achievable on the calculation of the transition periods decreases and the overall performance of the DDA algorithm degrades. On the other hand, for high sampling rates, the performance improves at the cost of higher dissipation. This is illustrated in Fig. 6 which shows the power consumption of the chip in terms of the sampling frequency, assuming that both input signals are band-limited in the β band. In the same plot, the correlation between the measured synchronization index and the PLV value (calculated off-chip for the same input signals) is represented as an accuracy measure of the DDA approach. It is worth noting that beyond a given sampling rate of about 120-160S/s, no further improvement can be observed in the chip performance as the correlation states around 85%. Hence, a sampling rate of 128S/s is chosen for which the power consumption of the chip core is 12.5nW from 1.2V supply voltage. Similar trade-offs can be observed for other EEG frequency bands.

4. EXPERIMENTAL RESULTS

The processor has been exhaustively tested using neural recording data available in the European Epilepsy database (http://epilepsy-database.eu/). This database contains recordings of over 275 patients including 225 scalp recordings, 50 intracranial recordings and over 100 annotated sets using both intracranial and surface electrodes which were organized into a standard 10-20 format. For the purpose of illustrating the performance of the proposed processor, three blocks of EEG data were used for testing.

- Set 1: Patient FR_1084, block 0161. A 48 year old female over a net 6 hours recorded at 1024S/s. During this block, three low β wave seizures were annotated.
- Set 2: Patient FR_565, block 0016. A 13 year old male over a net 1 hour recorded at 256S/s. During this block, one θ wave seizure was annotated.
- Set 3: Patient FR_1096, block 0072. A 32 year old female over a net 1 hours recorded at 1024S/s. During this block, one low β wave seizure was annotated.

For each block, signals were first pre-filtered with Matlab (using bandpass fourth-order Butterworth filters) into the frequency bands in which the seizures were annotated. Afterwards, signals were downsampled to 128S/s and converted to binary words of 10 bits for transferring to the logic analyzer. For each experiment, the

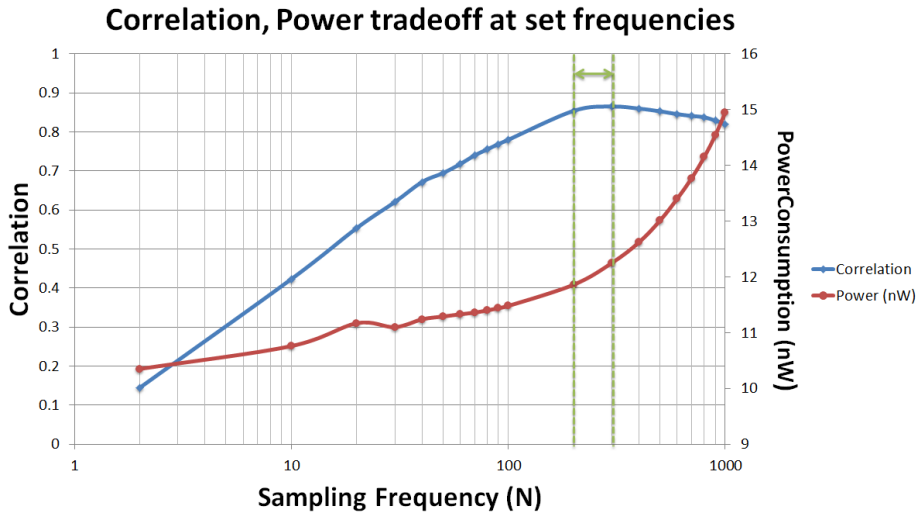

Figure 6. Power consumption and accuracy performance (correlation with HT approach) results at different input signal sampling rates

synchronization index generated by the processor was transferred to a laptop and plotted alongside with the theoretical PLV value obtained through the Hilbert Transform method.

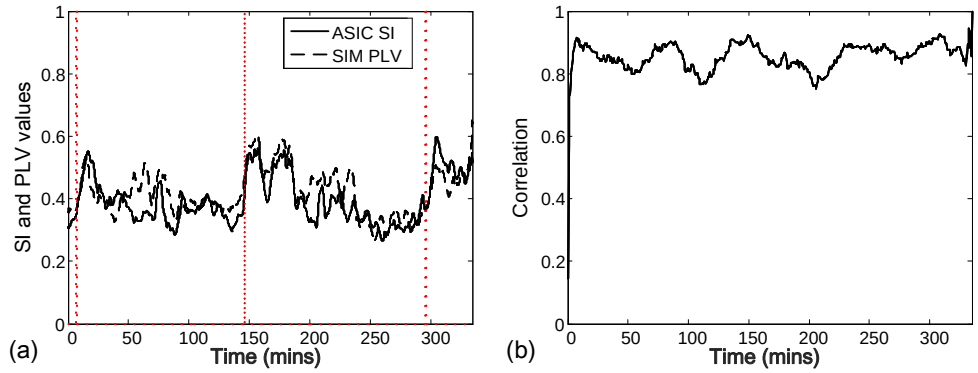

Figure 7. Results for patient FR_1084 Block 0161, electrode position M5.

Fig. 7 and Fig. 8 show, respectively, the results obtained for patient FR_1084 at two recording electrodes, namely, M5 and GA2. For each figure, the plots on the left show the experimental Synchronization index and the calculated PLV value, while the plots on the right represent the correlation between both measures. The plots on the left also indicate the occurrence of seizures, which coincide with noticeable increments on the synchronization measures.The DDA algorithm detects these large changes and indeed follows a similar trend to that of the more complex phase extraction algorithms. This is verified by the high correlation results of approximately 0.9 on average.

Fig. 9 shows results for patient FR_565. Note that there is an increase in synchronization just after the annotated seizure, however the large increase in synchronization at approximately 55 minutes was identified as a false positive which was identified by both the ASIC processor and the Hilbert transform plus PLV approach.

Fig. 10 shows results for FR_1096. Again the results show a large spike in synchronization just after the seizure start time. The correlation is high and no false positives were detected.

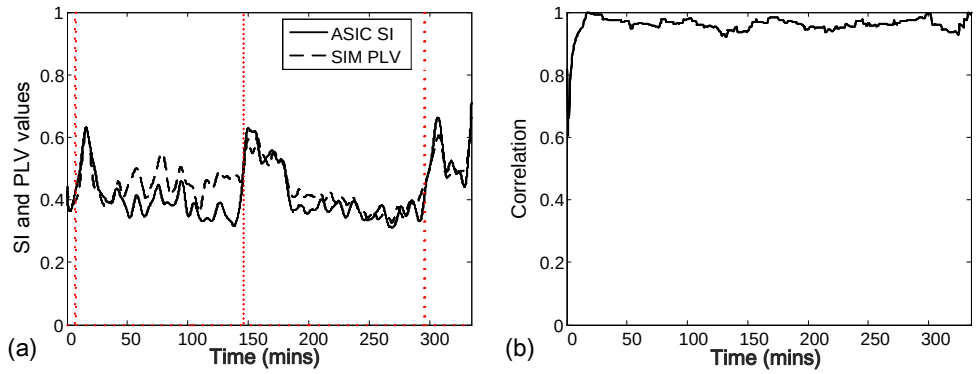

Figure 8. Results for patient FR_1084, Block 0161, electrode position GA2.

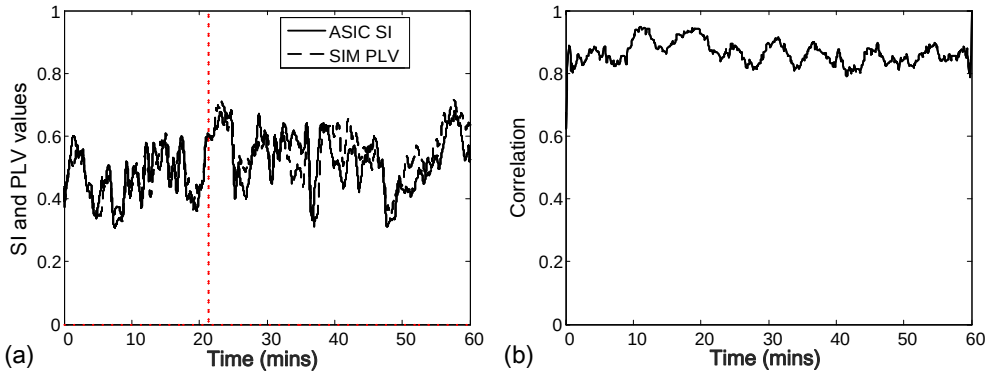

Figure 9. Results for patient FR_565, Block 0016, electrode position GA2

5. CONCLUSION

A dedicated processor, fabricated in a 0.18μm CMOS process, has been proposed for the estimation of the phase synchronization between neural signals. It obtains similar results as those achievable with more computationally demanding algorithms. The design exhibits low-voltage, low power features and it is highly scalable which allows for embedded multichannel phase calculations.

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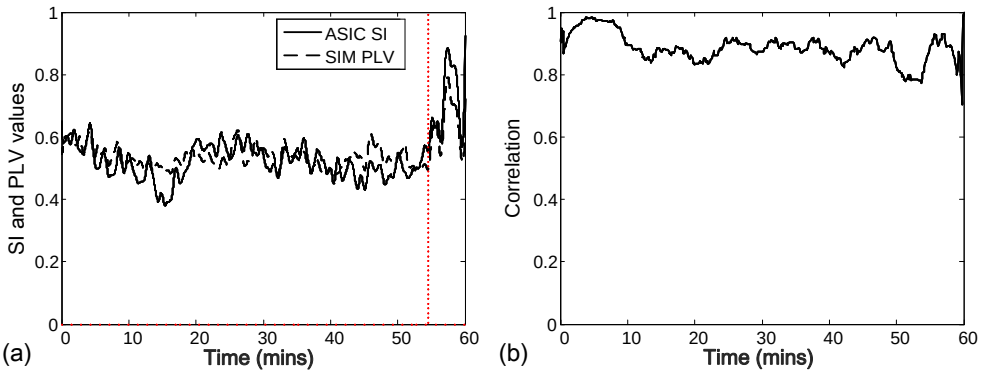

Figure 10. Results for patient FR_1096, Block 072, electrode positions MHL2

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