# Modular Design of Adaptive Analog CMOS Fuzzy Controller Chips

Angel Rodríguez-Vázquez * and Fernando Vidal **

*Dept. of Analog and Mixed-Signal Circuit Design
Centro Nacional de Microelectrónica-Universidad de Sevilla
Edificio CICA, C/Tarfia s/n, 41012-Sevilla, SPAIN
FAX:: 34 5 4624506; Phone:: 34 5 3623811
email: angel@cnm.us.es

**Dto. de Arquitectura y Tecnología de Computadores y Electrónica
Universidad de Málaga
Pza. El Ejido s/n, Málaga, SPAIN
FAX: 34 5 2131413; Phone: 34 5 2131390
email: vidal@tecma1.ctima.uma.es

**ABSTRACT:** Analog circuits are natural candidates to design fuzzy chips with optimum speed/power figures for precision up to about 1%. This paper presents a methodology and circuit blocks to realize fuzzy controllers in the form of analog CMOS chips. These chips can be made to adapt their function through electrical control. The proposed design methodology emphasizes modularity and simplicity at the circuit level -- prerequisites to increasing processor complexity and operation speed. The paper include measurements from a silicon prototype of a fuzzy controller chip in CMOS 1.5μm single-poly technology.

## 1. INTRODUCTION

Fuzzy inference enables predicting the behavior of systems whose mathematical description is unknown, or ill-defined, based on *insights* about *local* features of their behavior [1]. For instance, to stabilize an inverted pole on a moving cart based on statements such as "if the pole is falling rapidly to the left then the cart must move rapidly to the left", with no need for exact formulation of the dynamics -- similar to a human operator. Fuzzy technology has also proven viable for incorporation into new products within a short development time and with low development cost [2] which, together with its functionality potential, render it very well suited to build marketable intelligent systems. In many of these systems, inference can be realized by *software* on conventional processors; to attain up to 1Kflip inference speed with 8 to 16 bits of resolution. However, those requiring either high-speed inference, reduced power consumption, or smaller dimensions have prompted the development of dedicated *hardware*.

Fuzzy inference ASICs can be designed using either *digital* or *analog* circuits. Digital provides larger *accuracy*, while analog features larger *speed efficiency* (measured as the power consumption and area needed for a given speed) for medium to low accuracy. Consequently, the latter are better suited where major design issues relate to power consumption or system dimensions, or operation speed, while accuracy remains secondary. This is actually the case in most applications, where *accuracy* requirements range from 10% to 1% [3] -- affordable with even the cheapest VLSI technologies [4]. Another obvious advantage of analog fuzzy circuits is their simpler interfacing to physical sensors and actuators, requiring no data converters.

Previous approaches to the use of analog circuits for fuzzy controllers did not actually present methodologies for monolithic design, but rather focused on the realization of different fuzzy subsystems using different technologies [4][5][6]. Also, they covered mainly the case

where the input-output function of the controller remains *fixed* -- not appropriate for most practical applications, where the exact function is unknown a priori or must adapt to specific environmental characteristics [2]. This paper presents an architecture for *adaptive* fuzzy controllers and circuit blocks for their realization in the form of CMOS chips. Major emphasis is placed on full exploitation of the functional features of the MOS transistors and on *modularity* of the circuits used for adaptability. This circuit methodology runs parallel to the development of hardware-compatible *learning* algorithms that enable the chips to be trained in-situ through examples and, thus, compensate second-order hardware non-linearities [7].

## 2. CHIP ARCHITECTURE

Fuzzy inference is a tool for modeling multidimensional nonlinear systems. For instance, a fuzzy washing machine sets the level of water as a function of the clothes' mass, the impurity of water, and the time differential of impurity [2]. This is equivalent to capturing the input-output behavior of the system as a *surface response*,

$$y = f(\mathbf{x}) \qquad \mathbf{x} = \{x_1, x_2, \ldots x_M\}^T \tag{1}$$

where $y$ is the output and the vector $\mathbf{x}$ the input. Distinctive features of fuzzy inference are:

- The surface response, which is a *global* model of the system behavior, is obtained as a composition of functions which capture *local* features of this behavior.
- These local features represent *insights* about the system operation, and are described through inference *rules* of the type,

  **IF** $x_1$ is $A_{i1}$ **AND** $x_2$ is $A_{i2}$ **AND** ... $x_M$ is $A_{iM}$ **THEN** *Consequent* Action

  where $A_{ij}$ are called *fuzzy labels*, and the consequent assign values to $y$ depending on the outcome of the combination of statements involved in the antecedent clause.
- The matching between input variables and fuzzy labels in the statements "if $x_j$ is $A_{ij}$" is graded continuously from 0 (no matching) to 1 (maximum matching).

Since the statements involved in the fuzzy inference rules are in natural language, for instance "if the temperature is low", this technique is very well suited to capture human expertise. Also, the locality of the pieces of knowledge, the basis on which the global surface response is built, enables simpler model updating for changes that affect only limited regions of the input space.

Out from the different algorithms reported in literature [1] our approach follows a particularization of Takagi-Sugeno´s inference where the consequent of each rule is a constant value -- a *singleton*.This is advantageous for hardware implementation and programming [3], and obtains the surface response as a linear combination of weighted *normalized basis* functions,

$$y = f(\mathbf{x}) = \sum_{i=1.N} y_i^* w_i^*(\mathbf{x}) \tag{2}$$

where each normalized basis function $w_i^*(\mathbf{x})$ corresponds to a fuzzy rule and its weight $y_i^*$ is the singleton associated to it. This maps onto the parallel chip architecture of Fig.1(a), which contains three *layers*: *input* layer, where the non-normalized basis functions $w_i(\mathbf{x})$ are evaluated; *normalization* layer; and *output* layer, where each normalized function is multiplied by the singleton associated to it in the corresponding fuzzy rule.

Fig.1(b) shows a more detailed block diagram of the input layer. For each input variable, a set of membership functions $s_{ij}(\mathbf{x})$ are evaluated to obtain the matching degrees among this input and the fuzzy labels associated to it. Then the outputs of these membership functions are combined through minimum operators to obtain the basis functions $w_i(\mathbf{x})$.

## 3. CMOS CIRCUIT BLOCKS

Our proposed circuits realizes all the internal operations of Fig.1 in current mode, to obtain full advantage of the functional features of MOS transistors and, thus, produce simplest and fastest possible circuits. The inputs are voltages for easier interface to conventional equipment. The *v-i* interface is realized by the membership function circuitry, which combines this function with the realization of the membership function itself, through exploitation of the large signal characteristics of a MOS differential pair. Fig.2(a) shows the basic circuit used for membership functions, where the rectangles represent transistors. Fig.2(b) and (c) show the circuits for the minimum operator and for normalization, respectively; both with O($n$) complexity and optimum speed. Since the outputs of the normalization circuit are currents, the operation of singleton weighting is realized directly through current mirrors and the output current obtained by routing the outputs of all these current mirrors to a common node.

The feature of adaptation requires that the shape and location of the membership functions, and the singletons values, are controlled electrically. In our approach this is realized by using either of the compound MOS transistors of Fig.3 in the signal path of membership function and singleton circuits. They feature electrical control of the transconductance with voltage $B$ while keeping the circuit function unchanged. Thus, the same circuitry is used for fixed and for adaptive chips. The difference is that the latter use simple transistors while the former use composite transistors. Our studies demonstrate that the range provided by these devices enable to cover most practical applications. On the other hand, the non-linearities observed in the control function makes not a problem since they are absorbed by the learning mechanism [7].

## 4. EXPERIMENTAL RESULTS

Fig.4 is a microphotograph of a prototype of a 3-input 4-rule controller which was fabricated in 1.5μm CMOS single-poly technology. Actual circuits in this chip incorporated circuit strategies not displayed explicitly in Figs.2 and 3 to keep the accuracy about 1% (such as cascode transistors, optimum design for random variations of technological parameters, etc.). Fig.5 illustrates the operation of the compound transistors. Measurements correspond to singleton current mirror with the series transistors. The floating control voltage is generated on/chip from an external grounded voltage. Fig.6(a) shows the transfer characteristics measured when the controller is used to interpolate a sine wave, and Fig.6(b) shows a bi-dimensional surface map measured for a particular setting of the singleton values. Operation speed of the prototype is about 5MFlips with ±2.5v and 15μA tail current.

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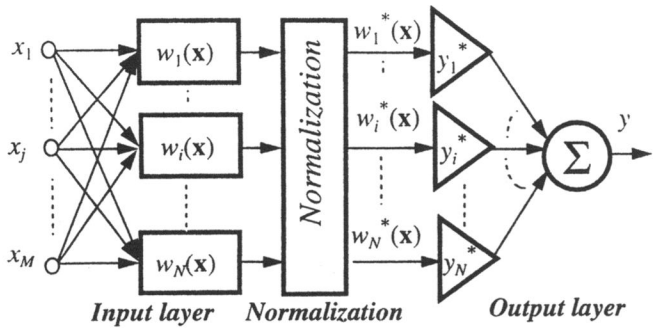



Figure 1(a)

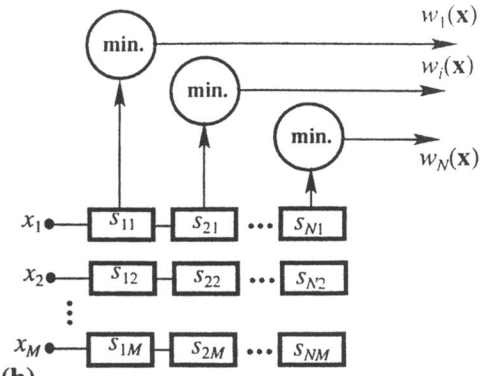



Figure 1(b)

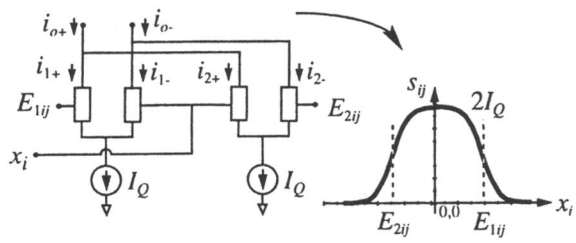
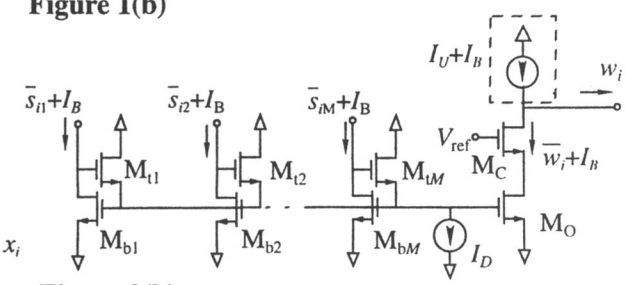



Figure 2(a)

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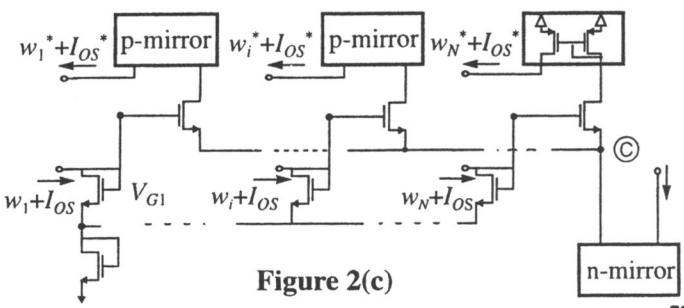


Figure 2(c)

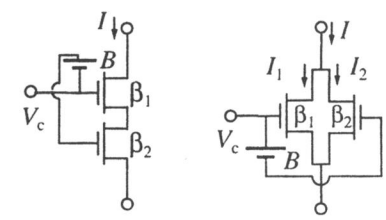


Figure 3

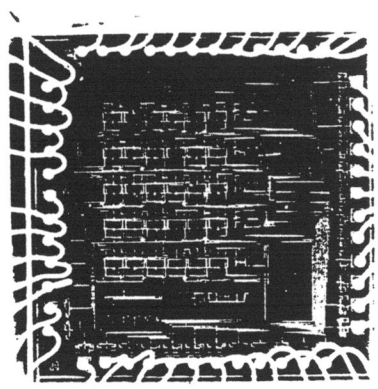

Figure 4

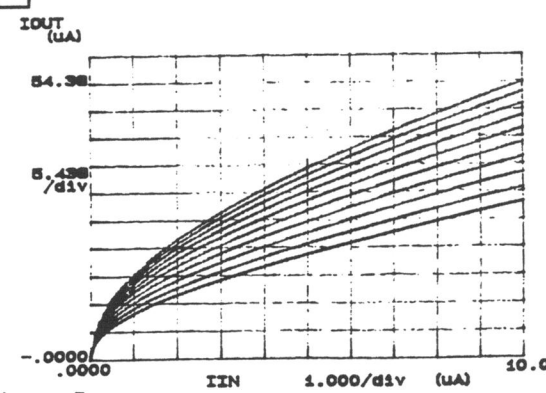


Figure 5

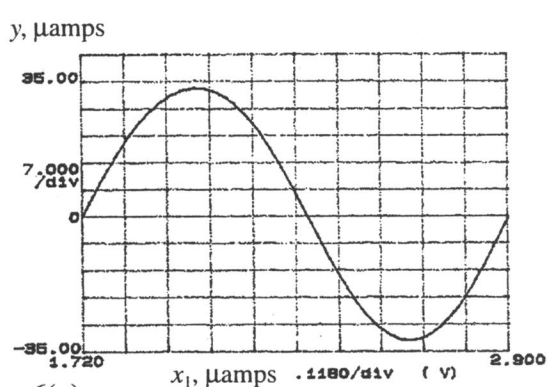


Figure 6(a)

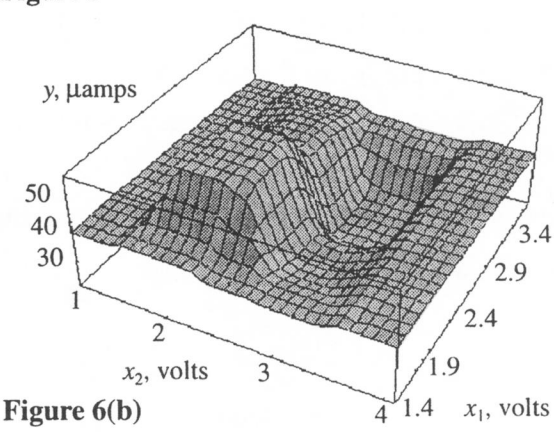


Figure 6(b)