A Mismatch-Insensitive High-Accuracy High-Speed Continuous-Time Current Comparator in Low Voltage CMOS

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Abstract

This paper presents a CMOS current comparator which employs nonlinear feedback to obtain high-accuracy (down to 1.5pA) and high-speed for low input currents (8ns@50nA). This structure is much faster for low currents (below 10μA) than other previous nonlinear feedback comparators [1], [2], [3], [4]. Particularly, when compared to the fastest current comparator reported up to now [4], the new one goes more that 100 times faster for 1nA current, with smaller area occupation and similar power consumption. In addition, the new comparator is virtually insensitive to mismatch and capable to operate with supply voltages as low as 1V.

1. Introduction

Analog current-mode techniques are drawing strong attention today due to their potential application in the design of high-speed mixed-signal processing circuits in low voltage standard VLSI CMOS technologies [5]. Also current-mode circuits are natural candidates for image sensory information processing where current sensing and comparison is necessary. Current comparators are basic building blocks for nonlinear current-mode signal processing and analog to digital converters. The availability of large current ranges is an appealing feature for both fields. Also, efficient small current level detection is fundamental for high accuracy and high speed applications.

Low level, high speed current detection is also required in different light and radiation sensing applications: i.e. γ-detectors using wide band gap semiconductors [6], or controllability and reconfigurability issues in E-beam testing of integrated circuits [7]. For instance, in the latter the need arises to detect current levels as low as 1nA in a few μs. Subthreshold CMOS current mode massive computation architectures [8] also require efficient detection of low current levels for fast discriminating function evaluation. To highlight another application, current detection is also required in IDDQ VLSI testing approaches [9].

In recent years, many current comparator circuits have been proposed [1], [2], [3], [4], [10], [11], [12]. A possible classification of them is to distinguish between the ones where the input current is first sensed at a low impedance node (resistive input) and them amplified using a voltage gain mechanism, and the ones where the input current is sensed at a high impedance node (capacitive input). The firsts provide high speed for high current levels but are somewhat inaccurate; the seconds obtain enlarged resolution at the cost of increasing voltage excursions at the input node and consequently decreasing the operation speed [12].

Another possible classification is to distinguish between the structures that use autozeroing techniques to attenuate offset or to reduce propagation delays by adding clock signal generation circuitry and the ones that work on asynchronous mode.

In this paper we propose an asynchronous mode current comparator that uses nonlinear feedback to combine the advantages of capacitive-input and resistive-input architectures. Because the proposed circuit is offset insensitive by construction it does not require autozero for offset attenuation. We include also a comparative study with the operation of the current comparator which is claimed the fastest among all

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those reported to now [4].

2. Circuit behaviour

Fig.1 shows the schematic of the so-called Current Switch Comparator, whose advantages for low input currents have been demonstrated in [12]. The operation of this circuit involves two different regions.

If a positive current flows towards the input node, and assuming null initial conditions ($V_{in} = V_o = E$) transistors M_n and M_p are *OFF*, therefore the equivalent impedance at the input node is capacitive and consequently the circuit exhibits a very high resolution (only limited by the leakage currents), the input current is integrated in the parasitic input capacitor (C_{in}) producing a continuous increase of the input voltage. The amplifier causes V_o to decrease faster than V_{in} and so that *Mp* turn *ON* draining the input current and closing a negative feedback loop around the amplifier. It obtains a virtual ground at the amplifier input, thus fixing the voltage at the input node. A similar situation occurs for negative input current where M_n becomes *ON*.

The transient evolution is dominated by the first operation mode (the capacitive input behaviour), and if we consider a single pole model for the amplifiers with a gain-bandwidth product (*GB*) and linear capacitors for their input and output nodes one obtains

$$\begin{aligned} \Delta V_{in} &= \frac{I_{in}}{C_{in}} t \\ \Delta V_o &\cong -\frac{GB}{2}\frac{I_{in}}{C_{in}} t^2 \end{aligned} \qquad (1)$$

However, due to the parasitic capacitors between input and output nodes (C_M) the transient response is slowed down even for an ideal amplifier; this behaviour is similar to the slew rate phenomena in Miller operational amplifiers. In the comparator of Fig.1 the coupling capacitor is formed by the C_{gs} capacitors of

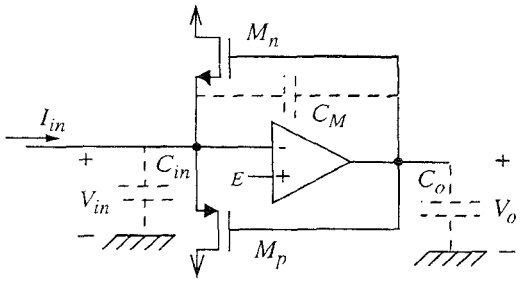

Fig. 1 Current Switch Comparator Schematic.

M_n and M_p, and eventually the intrinsical coupling capacitor of the amplifier. Due to C_M, input and output nodes of the comparator are coupled, so that the transient response evolution follows a linear characteristic instead a quadratic law

$$\begin{aligned} \Delta V_{in} &= \frac{(C_o + C_M)}{C^2} I_{in} t \\ \Delta V_o &\cong -\frac{C_M}{C^2} I_{in} t \end{aligned} \qquad (2)$$

where $C^2 = C_{in}C_o + C_{in}C_M + C_oC_M$.

Note that in (1) the output voltage is directly proportional to the amplifier *GB*, and hence the faster the amplifier is the faster the current comparator solves. However in (2) this dependence is vanished.

The response time can be calculated from (1) and (2) by making $\Delta V_o(T_D) = E_{OH}$, where E_{OH} denotes the logic noise margin.

$$\begin{aligned} T_D &= \frac{C^2}{C_M}\frac{E_{OH}}{I_{in}} \quad ; (C_M \neq 0) \\ T_D &= \sqrt{\frac{2C_{in}}{GB}\frac{E_{OH}}{I_{in}}} \quad ; (C_M = 0) \end{aligned} \qquad (3)$$

According to this formula, Fig.2 shows a comparison of the response time for the current switch comparator of Fig.1 with and without the coupling capacitor. We are assuming E_{OH}=1*V*, typical capacitances values of C_{in}=C_o=50*fF* and g_m=100μ*A*/*v*^{2} for the amplifier.

For low current levels, it is seen that the comparator behaviour becomes severely degraded due to the coupling capacitor, even for low values of this capac-

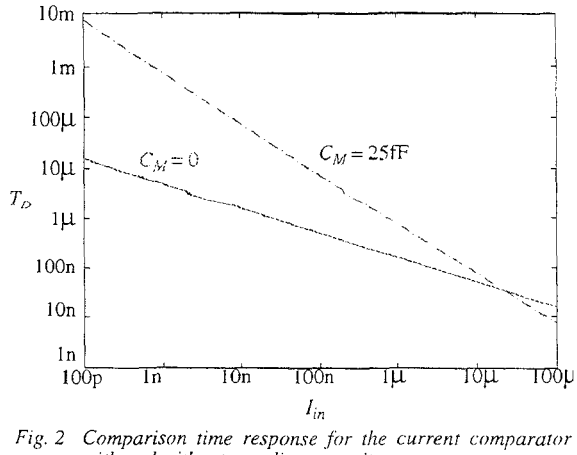

Fig. 2 Comparison time response for the current comparator with and without coupling capacitor.

itor. On the other hand, for large currents (in the order of tens of μAs) smaller times response are obtained in the coupled current comparator. For these high current levels a simple inverter features fast operation speed, with no feedback needed.

To improve transient response of the current switch comparator for low input currents, circuit strategies are required to uncouple input and output nodes of the amplifier and hence, reducing the coupling capacitance.

In order to achieve faster response times simple CMOS inverters are usually used as amplifiers. To avoid the overlap capacitors influence cascode transistors could be used in the amplifier output node. Also, the feedback mechanism used to obtain the non-linear driving-point characteristic should be modified to avoid M_p and M_n C_{gs} influence, so that using a source follower in the feedback loop must be avoided.

The new comparator schematic is shown in Fig.3. The circuit has two operation zones. If a positive current flows towards the input node, and assuming that the initial conditions are:

$$V_{in} = V_o = E \qquad V_n \leq E + V_{tn} \qquad V_p \geq E - |V_{tp}| \quad (4)$$

transistors M_n and M_p are *OFF*, so that the equivalent impedance at the input node is capacitive (i.e., very large in DC) and consequently the circuits exhibits a very high resolution (only limited by the leakage currents), the input current is integrated in the input capacitor (C_{in}) and produce a continuous increase of the input voltage. The amplifier causes V_o to decrease faster than V_{in} increasing V_{gs} for the transistor M_n and decreasing V_{sg} for M_p, so that M_n is driven into the *ON* state and a negative feedback loop is created around the amplifier. It obtains virtual ground at the amplifier input, fixing the voltage at the input node. A similar situation occurs for negative currents, where M_p becomes *ON*.

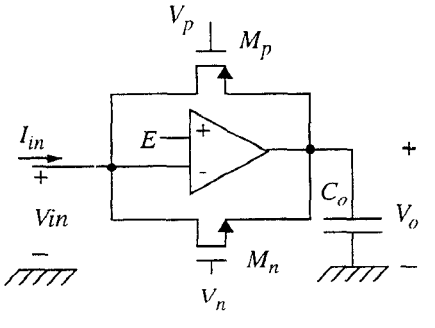

Fig. 3 Current Steering Comparator Schematic.

This structure reduces response times of the Fig.1 comparator. An improved around two orders of magnitude is observed with the comparator in [4] if we compare the worst cases (negative input currents).

We can also obtain a symbolic expression for the response time parameter by transient analysis. If we consider an input current step at t=0 from a negative overdrive level -J up to a positive overdrive level +J, the response time can be written as follows:

$$T_D \cong \sqrt{\frac{2C_{in}}{GB}\frac{(V_p - V_n + V_{tn} + |V_{tp}|)}{J}} \quad (5)$$

Fig.4 shows the final schematic for the new current steering comparator. As it can be seen the amplifier that appears in Fig.3 has been implemented by a CMOS inverter with two cascode transistors which avoid the capacitors between input and output nodes, so that the transient evolution presents a quadratic time dependence instead of a linear dependence, as occurs for the comparator in [4].

The response times simulation measures of the two comparators for a range of input currents are shown in Fig.5. We have considered the worst case,

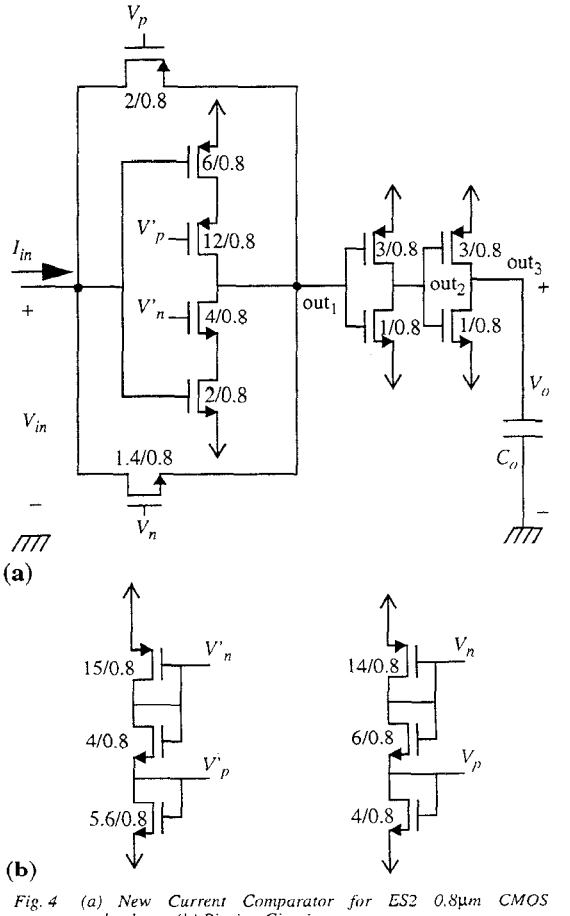

Fig. 4 (a) New Current Comparator for ES2 0.8μm CMOS technology., (b) Biasing Circuitry

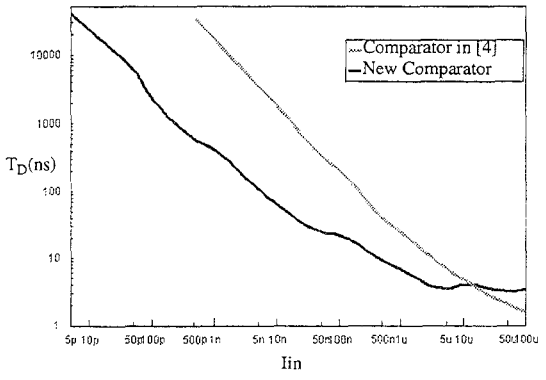

Fig. 5 Speed of the New and [4] Comparators.

i.e. a step input current from a positive overdrive level +J to a negative overdrive level -J. The results show that the greatest speed improvement occurs for low input currents, and for less than 10μA the new comparator remains faster than the one in [4]. The quadratic time law predicted in (2) can be observed in Fig.6. It can be seen how this approach is suitable in order to describe the main transient evolution. It contrasts with the behaviour observed in Fig.7 where the slew-rate phenomena governs the temporal response. The circuit which provides the wave-form in Fig.7 is the same as in Fig.4 but using the feedback scheme that appears in Fig.1.

A possible technique to improve comparison times is to reduce the voltage excursions at the amplifier output node. This approach was applied by the authors in [4] to the circuit in Fig.1. However it presents a very high sensitivity to mistmatch effects. In order to avoid the mistmatch influence the excursions on the output voltage must be larger than the expected maximum fluctuations due to mistmatch.

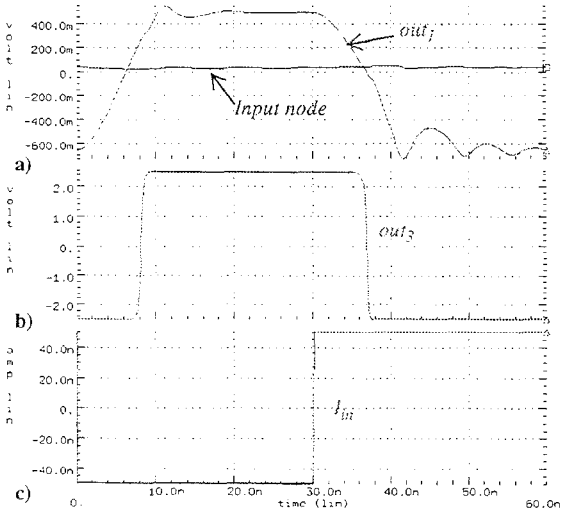

Fig. 6 Response of the comparator in Fig.4 for a 50nA input pulse.

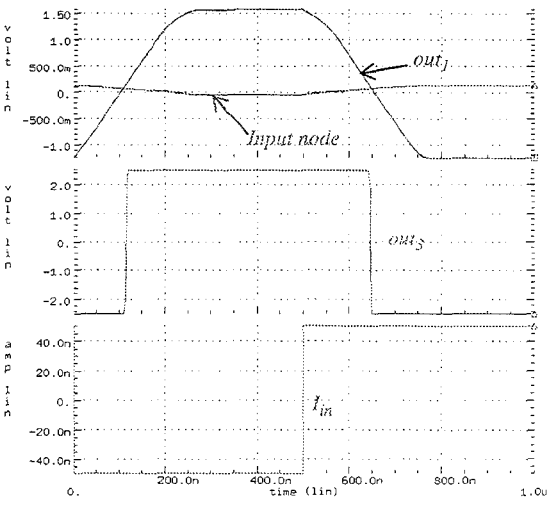

Fig. 7 Response of the current switch comparator in Fig.1 for a 50nA input pulse.

Fig.8 shows a comparative study by Monte Carlo analysis of the new and [4] comparators designed in the same technology (ES2 1.5μm). It is shown how the percentage of successful comparisons for [4] decreases as input current level becomes lower. However, for the new comparator this percentage becomes 100% as soon as the input current reaches the maximum offset level (<1.5pA).

In order to obtain the maximum improvements the comparator has finally been designed using ES2 0.8μm technology. Fig.9 illustrates the layout for the comparator and the biasing circuitry.

The main characteristics of the new comparator are:

- 5V power supply.
- Input Current Offset lower than 1.2pA.
- Maximum resolution in the order of few pA.
- Maximum delay for a 50nA step input current 8ns.
- Maximum delay for a 1μA step input current 2ns.

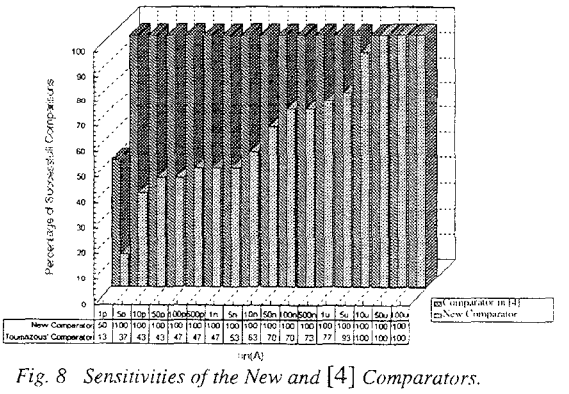

Fig. 8 Sensitivities of the New and [4] Comparators.

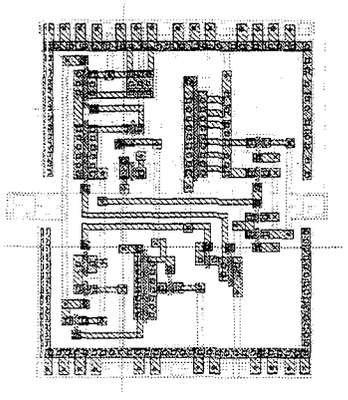

Fig. 9 Layout of the comparator and the biasing circuitry.

- Area consumption without bounding pads $0.005 mm^2$.
- Power consumption 2.5mW.

Fig.10 shows a comparison between schematic and extracted response times. It can be observed how the extracted response times are twice slower than schematic times due to the parasitic effects. A careful layout must be developed in order to minimize the parasitic capacitor effects.

Another important feature of this new structure is its capability for working at low voltage supplies. As it can be seen in Fig.4 the biasing circuitry requires

$$V_{DD} > 2V_{tn} + |V_{tp}| \tag{6}$$

whereas the CMOS amplifier need

$$V_{DD} > V_{tn} + |V_{tp}| + 2V_{dsat} \tag{7}$$

It allows proper operation with a power supply below 3V. If a lower power supply is needed the biasing circuitry should be modified, in this case (7) provides the minimum V_{DD} value (lower than 2V). This comparator can operate even below this limit if the

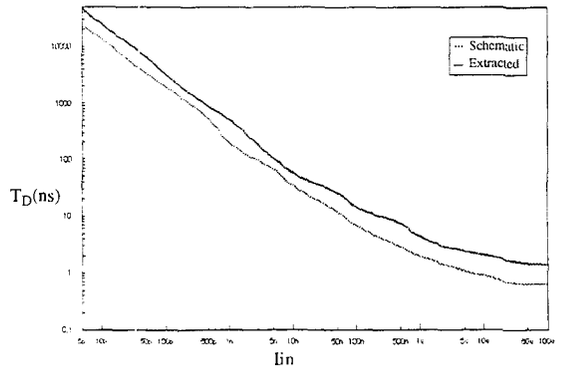

Fig. 10 Comparison Between Schematic and Extracted Delays.

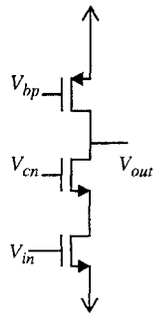

Fig. 11 Low voltage amplifier

amplifier in Fig.11 is used. In this case the new limit becomes around 1V.

$$V_{DD} > \begin{cases} V_{tn} \\ |V_{tp}| \\ 3V_{dsat} \end{cases} \tag{8}$$

Fig.12 shows the response times of the comparator in Fig.4 for two different rail-to-rail voltages. It can be observed how for low input current levels the maximum speed is obtained using a 3.3V rail-to-rail voltage. It is due to lower voltage excursions at the output node of the amplifier.

3. Conclusions

An analysis of the transient evolution of nonlinear feedback current comparators demonstrates that its response time degrades significantly at low currents due to the influence of a Miller coupling capacitor. This can be partially overcome by reducing the voltage excursions, the price to be paid for this is a reduction of the circuit tolerance to mismatches, specially significant at low-voltage supplies. The comparator presented in this paper uses another strategy to obtain large operation speed without degrading the comparator resolution and keeping the comparator operation virtually mismatch-insensitive, even for voltage supplies as low as 1V.

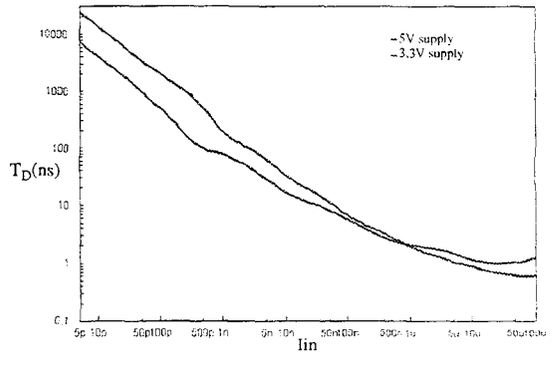

Fig. 12 Delay Times for Different rail-to-rail Voltages

4. References

[1] R. Domínguez Castro, A. Rodríguez Vázquez and J.L. Huertas: "Sobre el Diseño de Comparadores de Intensidad". *Diseño de Circuitos Integrados 91*, ISBN 84-87412-61-0, pp 61-66, Universidad de Cantabria 1991.

[2] R. Domínguez-Castro, A. Rodríguez-Vázquez, F. Medeiro and J.L. Huertas: "High-Resolution CMOS Current Comparators". *1992 European Solid-State Circuits Conf*, ISBN 87-984232-0-7, pp. 242-245, Kandrup 1992.

[3] H. Traff: "Novel Approach to High Speed CMOS Current Comparators". *Electronics Letters*, Vol.28, No.3, pp. 310-312, 1992.

[4] A.T.K.Tang, C.Toumazou: "High Performance CMOS Current Comparator". *Electronics Letters*, Vol.30, No.1, pp. 5-6, Jan. 1994.

[5] C. Toumazou, F. J. Lidgey and D. G. Haigh: "*Analogue IC Design: The Current Mode Approach*". *IEE Circuits and Systems*, series 2, 1990.

[6] P. Olmos et al: "Computer Simulations of the Behavior of the Partial Charge Collection Model in Thick HgI2 γ-detectors". *Nuclear Inst. and Methods in Physics Research*, A302, pp 91-104, 1991.

[7] J. Madrenas and J. Cabestany: "E-Beam Detector Devices for IC Controllability". *Microelectronics Engineering* 16, pp465-472, 1992.

[8] A.G. Andreou et al: "Current-Mode Subthreshold MOS Circuits for Analog VLSI Neural Systems". *IEEE Trans. on Neural Networks*, Vol. 2, pp 205-213, March 1991.

[9] J. Rius and J. Figueras: "Proportional BIC Sensor for Current Testing". *Journal of Electronic Testing*, Vol. 3, pp 387-396, Dec. 1992.

[10]G.Palmisano, G. Palumbo, S. Pennisi: "A High-Accuracy High-Speed CMOS Current Comparator". *Proc. ISCAS'94*, June 1994.

[11]J.P.A. Carreira, J.E. Franca: "High Speed CMOS Current Comparator".*Proc. ISCAS'94*, June 1994.

[12]A. Rodríguez-Vázquez, R. Domínguez-Castro, F. Medeiro, M. Delgado-Restituto: "High Resolution CMOS Current Comparators: Design and Applications to Current-Mode Function Generation". *Analog Integrated Circuits and Signal Processing*, 7, pp. 149-165, 1995.