A Self-Calibration Circuit for a Neural Spike Recording Channel

Alberto Rodríguez-Pérez[1], Jesús Ruiz-Amaya[1], Manuel Delgado-Restituto[1],
Mohamad Sawan[2] and Ángel Rodríguez-Vázquez[1]

[1]Institute of Microelectronics of Seville
and University of Seville
Tlf.: +34 954 466 667 Fax: +34 954 466 600
{alberto, ruiz, mandel}@imse-cnm.csic.es

[2]Polystim Neurotechnologies Laboratory
Dept. of Electrical Engineering,
École Polytechnique de Montréal
mohamad.sawan@polymtl.ca

***Abstract* - This paper presents a self-calibration circuit for a neural spike recording channel. The proposed design tunes the bandwidth of the signal acquisition Band-Pass Filter (BPF), which suffers from process variations corners. It also performs the adjustment of the Programmable Gain Amplifier (PGA) gain to maximize the input voltage range of the analog-to-digital conversion. The circuit, which consists on a frequency-controlled signal generator and a digital processor, operates in foreground, is completely autonomous and integrable in an estimated area of 0.026mm^2, with a power consumption around 450nW. The calibration procedure takes less than 250ms to select the configuration whose performance is closest to the required one.**

I. Introduction

Implantable neural sensors provide relevant information for neuroscientists to understand brain´s operation and are hence key tools for the prevention and treatment of neural diseases. The combination of these sensors with wireless technologies has enabled the development of efficient Brain Machine Interfaces (BMI) for both animals and humans and has paved the way for the treatment of neural diseases like epilepsy and the like. These interfaces consist of MultiElectrode Arrays (MEAs) implanted in the cortex, together with low-power mixed-signal and RF circuits for signal digitalization and wireless transmission [1-8].

Because these interfaces deal with extremely weak signals, careful filtering and amplification are needed for correct operation [9]. Actually, programmability of both the amplifier gain and the bandpass filter poles is required to achieve correct adaptation of the front-end response to the input stimuli. The rationale for gain programmability is that the amplitude of the signal depends on the position of the electrode with respect to the sensed neuron. Regarding filter programmability, it is needed to compensate for electrical process parameters deviations – intrinsic to any IC implementation [10]. Different works have confronted these issues by incorporating programmability at circuit level [4-8]. However, programming is made in most cases in open loop and, to the best of our knowledge, there is no integrated solution yet addressing self-calibration for this sort of interfaces.

In this work we present a calibration mechanism for the neural sensor channel previously presented in [11]; this neural channel has proven in silicon through a 130nm CMOS chip – not yet published. The system first calibrates the bandpass filter to set its bandwidth at 200Hz-7kHz and then calibrates the Programmable Gain Amplifier (PGA) gain to maximize the voltage amplitude at the input of the Analogue-to-Digital Converter (ADC). Both calibrations are completed as foreground process. The calibration circuitry is completely autonomous and can be embedded together with the rest of the neural sensor interface circuitry within the available neural channel area defined by the electrode pitch. The combination of these two components hence results into a self-calibrated neural recording channel.

The calibration algorithm and the associated circuitry are described in Section II. Section III shows the simulation results to illustrate the performance of the proposed circuit. Section IV ends with the conclusions of the work.

II. Calibration of the Channel

Fig.1 shows the architecture of the proposed neural spike channel. It consists of a Band-Pass Low-Noise Amplifier (BP-LNA), which conditions the signal from the electrode, followed by a PGA and an ADC [11].

Since each channel is affected by different process variations parameters and owing to the fact that the sensed neural signal levels depend on the position of the electrodes with respect to the neurons, the calibration process has to be carried-out separately for each channel.

The calibration process is split in three steps, according the flow diagram shown in Fig.2. First, the input of the system is connected to a frequency-controlled signal generator to calibrate the low-pass and high-pass frequencies of the BP-

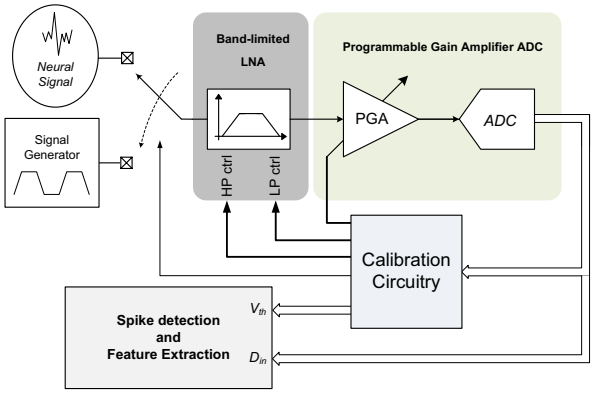


Fig. 1: Neural sensor channel architecture

LNA. After that, the input of the system is switched to the electrode and the PGA is calibrated to maximize the dynamic range of the ADC. Once the system is calibrated, it is configured to detect and transmit the information about the spikes positions and features. To that purpose an algorithm to determine the neural spike threshold voltage is ran as a background process similar to that in [12]. The BP-filter and PGA calibrations are explained in detail in the following subsections.

A. BP-filter calibration

As it has been stated, the BP-LNA bandwidth is subject to changes due to process variations. To compensate for these changes, two bit-programmability is introduced to control both the position of the high-pass ($HPctrl$<1:0>) and low-pass ($LPctrl$<1:0>) poles. The former controls the value of the pseudo-resistor whereas the latter controls the value of the load capacitance [11].

The objective of the calibration flow is to adjust these control bits to set the BP-band from 200Hz to 7kHz. For that purpose, three main circuits are involved during the BP-filter calibration procedure (see Fig. 1): 1) a frequency-controlled signal generator, which provides input waveforms to the LNA; 2) a digital circuit, which controls the calibration flow and determines the bits-configurability; and 3) a PGA and ADC to extend to full-range and monitor the output signal from the LNA. The PGA and the ADC were previously reported in [11]. Herein, the two first circuits will be detailed.

A.1 Frequency-controlled signal generator.

Fig. 3(a) shows the block diagram of the signal-generator. This circuit provides pseudo-sinusoidal waveforms with very low amplitude (around 2mV) at the frequency of the input clock signal (clk). It consists of: 1) a charge pump, which generates a truncated triangular waveform at the input clock frequency; 2) a band-pass filter, which attenuates by a factor 4 and filters high-order harmonics of the output signal from the charge pump; and 3) an attenuator, which reduces the signal amplitude to the required levels for the LNA and filters thermal noise. Detailed schematics of these circuits are illustrated in Fig. 3(b), (c) and (d), respectively. Three clock frequencies are used along the calibration procedure (obtained from the division of the 800kHz system clock), which are 195.3125Hz, 1.5625kHz and 6.25kHz. Depending on the selected frequency, the charge pump is reconfigured by means of two control bits ($b_1 - b_2$) which modify the slope of the triangular waveform and guarantee that the high and low values are not reached more than a 15% of the period of the input clock. This reduces the high order harmonics of the triangular waveform signal. In the same way, the band-pass filter is reconfigured to set the low pass frequency such that the high order harmonics are attenuated. The worst-case total power consumption of the frequency-controlled signal generator is around 370nW and the estimated silicon area is 0.02mm^2.

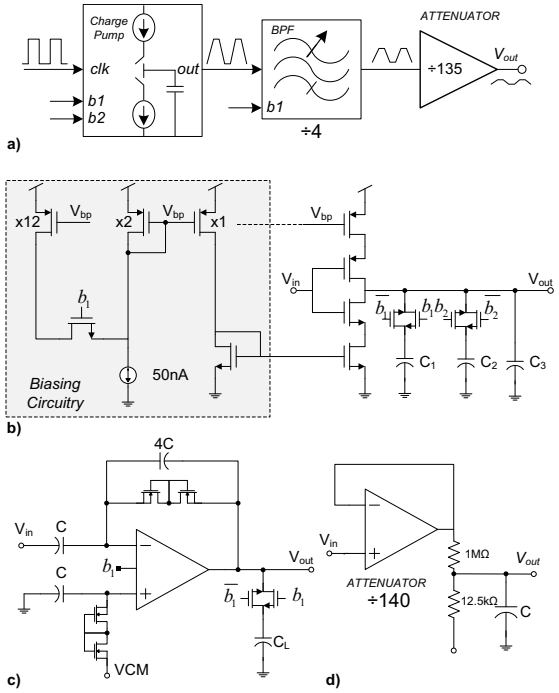


Fig. 3: Frequency-controlled signal generator: (a) block diagram, (b) charge-pump, (c) BP-filter and (d) attenuator.

A.2 Digital calibration circuit.

The process flow of the BP-filter calibration is shown in Fig.4. First, the signal generator is programmed to work at the band-pass frequency (1.5625kHz). Setting the BP-filter to the widest band, the PGA is calibrated to maximize the input dynamic range of the ADC. Once it is finished, the system stores the maximum value of the output signal under this configura-

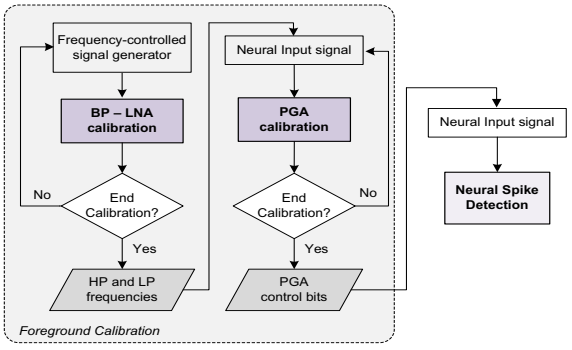


Fig. 2: Global calibration process

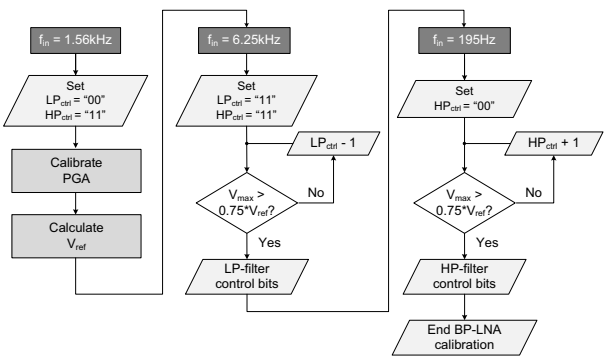


Fig. 4: BP-filter calibration flow

tion, that is, the *reference amplitude*.

The next step is the calibration of the LP-frequency. The signal generator is configured to create a 6.25-kHz signal and the controls bits of the LP-filter are configured to set the lowest frequency. The ADC is configured to sample the input signal at 80kHz. The calibration is performed by comparing the maximum output value of the system for a 6.25kHz input with the stored BP-band reference. If the drop of the first is equivalent or lower than 3dB (75%), the LP-frequency is corrected and the calibration ends. In other case, the LP-frequency is risen to the next step and the comparison is performed again. This routine is repeated until either the drop voltage is lower than 3dB with respect to the stored BP-band amplitude reference or the LP-frequency is configured at its widest value.

The same procedure is followed to complete the calibration of the HP-frequency. First, the frequency controlled signal generator is configured to compose a 195.32Hz signal, that will be used as the input of the system. The HP-pole is set to its highest value at the beginning, and the ADC samples the input signal at 20kHz, which is compared with the stored reference value to determine if the calibration ends (if it is higher), or continue with the next HP-pole position.

It is worth mentioning that the proposed procedure could be successfully applied for an arbitrary number of calibration bits as long as the drop voltage between the different configurations was higher than the resolution of the signal at the output LNA. In this design, the effective resolution (ENOB) of the LNA output signal is around 5 bits for an output swing of 480mV. This implies that the minimum change of amplitude which could be distinguished would be:

$$\Delta = \frac{\text{Output swing}}{2^{ENOB}-1} = \frac{480\text{mV}}{2^5-1} \approx 15.5\text{mV} \qquad (1)$$

B. PGA calibration

The calibration of the PGA starts by switching the signal from the electrode directly to the input of the calibrated BP-LNA of the recording system. Then, the system follows a calibration flow in which the gain of the PGA is adjusted using a successive approximation algorithm similar to that of the SAR ADCs, in which the 3-bits are successively set starting with the most significant one and continuing with the rest until the least significant.

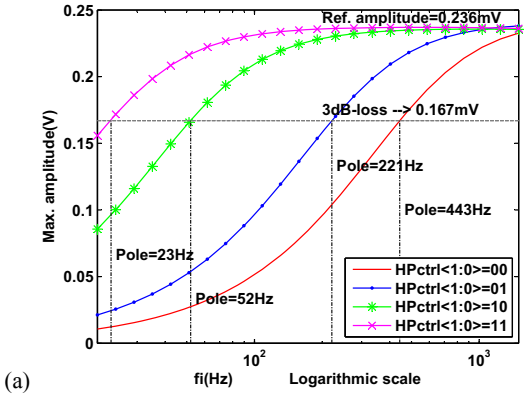
In this case, the system sets the MSB of the PGA gain control bits to '1', while the others remain to '0'. Then, the output of the recording channel is analysed during a certain time in order to detect if the signal is saturated (it exceeds the 95% of the full-scale) or not. In the first case, the MSB is switched to '0'; otherwise, it is kept to '1'. The next iteration starts switching the next bit to '1' and, hereinafter, the same analysis is performed. The calibration ends repeating the explained algorithm for the third bit.

III. Simulation Results

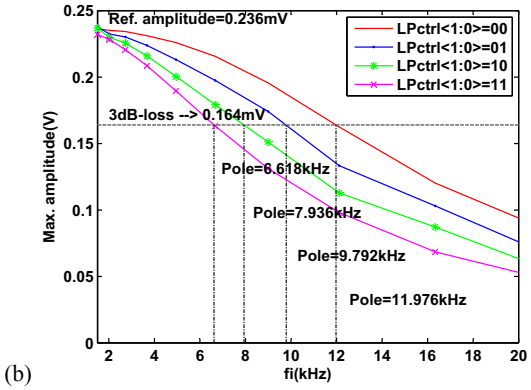
The bandwidth of the LNA presented in [11] is tuned from 200 Hz to 7 kHz by following the proposed calibration procedure. Before that, the LNA has been simulated on typical conditions in order to extract the bandwidth for the different configurations. The results for the high-pass and low-pass filtering are shown in Fig.5 (a) and (b), respectively,

According to these results, it can be easily inferred that the configuration $HPctrl\langle 1{:}0\rangle = "01"$ and $LPctrl\langle 1{:}0\rangle = "11"$ should be selected by the calibration procedure, since it provides the closest bandwidth to the required one.

Fig. 6 shows the chronogram of the calibration procedure. It starts by waiting around 30ms until the circuits reach their stationary response. After that, the ADC is enabled and the PGA calibration is carried out. A detailed view is shown in Fig. 6(a), where the frequency-controlled signal generator provides a pseudo-sinusoidal wave at 1.5625kHz while the ADC samples the LNA output at 20kS/s. Since the LNA output swing is around 500mVpp, a gain equal to 2 ($PGA\langle 2{:}0\rangle="001"$) is selected to not exceed the 95% of the full-scale range. Once the PGA gain has been set, the calibration procedure stores the maximum amplitude of the ADC output. Next, it begins the calibration of the low frequency pole. At this point, the signal generator is reconfigured to provide an input tone at 6.25kHz and the ADC sampling rate is increased to 80kS/s. As shown in Fig. 6(b), the procedure starts using the configuration bits with lower bandwidth ($LPctrl\langle 1{:}0\rangle = "11"$) and looks for the setting whose attenuation is closer to the required one (75%). Finally, the procedure is repeated for the high frequency pole, with the signal generator providing a 195.3125Hz input tone and the ADC sam-



(a)



(b)

Fig. 5: LNA amplitude attenuation versus the input frequency for the different configurations in the: (a) high-pass and (b) low-pass filtering.

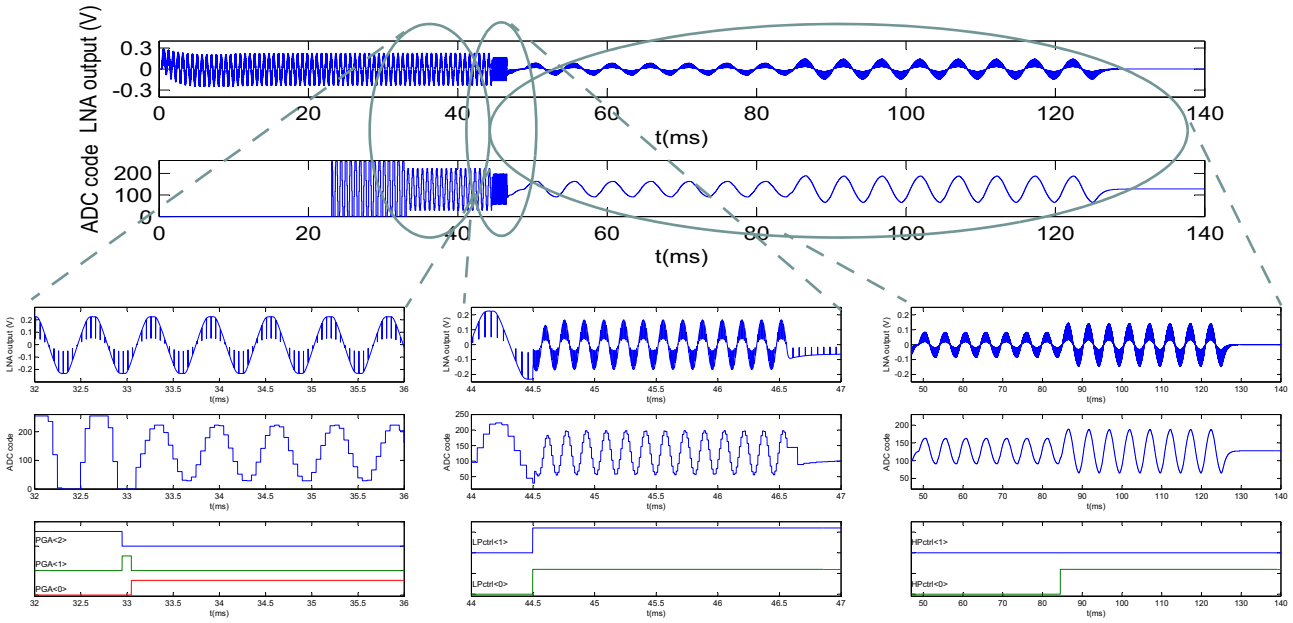


Fig. 6: Chronogram of the digital calibration procedure on the typical corner: (a) ADC and LNA output, detailed views of the (a) PGA, (b) low-frequency pole and (c) high-frequency pole calibrations.

pling at 20kS/s. A detailed view is shown in Fig. 6(c). As it can be checked, the selected configuration is the required one ($LPctrl<1:0> = "11", HPctrl<1:0> = "01"$).

A similar procedure has been carried out in several technological and environmental corners. In all cases, the control bits has been successfully selected.

IV. Conclusions

A calibration procedure to tune the bandwidth of a LNA and the gain of a PGA for a neural spike recording channel have been presented. The procedure only requires a frequency-controlled signal generator and digital circuitry to perform the calibration, while the rest of the needed blocks (ADC and biasing), are reused from the recording channel. The proposed calibration is performed as a foreground process and takes less than 250ms.

The estimated area and power consumption of the dedicated blocks are around 0.026mm^2 and 450nW, respectively. The procedure has successfully selected the configuration closest to the required specifications in all considered corners.

Acknowledgments

This work has been supported by the Spanish Ministry of Science & Innovation under grant TEC2009-08447, the Junta de Andalucía under grant TIC-02818 and the 2007-2013 FEDER Programme.

References

[1] R. R. Harrison *et al.*, "A Low-Power Integrated Circuit for a Wireless 100-Electrode Neural Recording System," *IEEE J. Solid-State Circ.,* vol. 42(1), pp. 123-133, Jan. 2007.

[2] M.S. Chae *et al.*, "A 128-Channel 6mW Wireless Neural Recording IC With Spike Feature Extraction and UWB Transmitter," *IEEE T. on Neural Systems and Rehabilitation Eng.,* vol. 17(4), pp. 312-321, Aug. 2009.

[3] B. Gosselin *et al.*, "A Mixed-Signal Multichip Neural Recording Interface with Bandwidth Reduction," *IEEE T. Biomed. Circ. Sys.,* vol. 3(3), pp. 129-141. June 2009.

[4] A. M. Sodagar *et al.*, "An Implantable 64-Channel Wireless Microsystem for Single-Unit Neural Recording," *IEEE J. Solid-State Circ.*, vol. 44(9), pp. 2591-2604, Sept. 2009.

[5] F. Shahrokhi *et al.*, "The 128-Channel Fully Differential Digital Integrated Neural Recording and Stimulation Interface," in *IEEE Trans. on Biomedical Circuits and Systems*, vol. 4(3), pp. 149-161, June 2010.

[6] S. B. Lee *et al.*, "An Inductively Powered Scalable 32-Channel Wireless Neural Recording System-on-a-Chip for Neuroscience Applications," in *IEEE ISSCC 2010*, pp. 120-123. Feb. 2010.

[7] S. Rai *et al.*, "A 500uW Neural Tag with 2uVrms AFE and Frequency-Multipying MICS/ISM FSK Transmitter," in *IEEE ISSCC 2009,* pp. 212-214. Feb. 2009.

[8] X. Zou *et al.*, "A 1-V 450-nW Fully Integrated Programmable Biomedical Sensor Interface Chip," in *IEEE J. on Solid-State Circuits*, vol. 44(4), pp. 1067-1077, April 2009.

[9] R. R. Harrison and C. Charles, "A low-power low-noise CMOS amplifier for neural recording applications", *IEEE J. Solid-State Circ.*, vol. 38, no. 3, pp. 958-965, June 2003.

[10] J. Ruiz-Amaya *et al.*, "A comparative study of low-noise amplifiers for neural applications," in *Int. Conf. on Microelectronics (ICM 2010),* pp. 327-330, Dec. 2010.

[11] A. Rodríguez-Pérez *et al.*, "A Power Efficient Neural Spike Recording Channel with Data Bandwitdh Reduction," in *IEEE ISCAS 2011,* pp. 1704-1707, May 2011.

[12] A. M. Kamboh and A. J. Mason, "On-chip Feature Extraction for Spike Sorting in High Density Implantable Neural Recording Systems," in *IEEE BIOCAS 2010)*, pp. 13-16. Nov. 2010.