Enhancement of dielectric barrier layer properties by Sol-Gel and PECVD stacks

Carmen López-López,[1] Mari-Fe Menendez,[2] Luis Andres Menendez,[2] Armando Menendez,[2] Pascal Sánchez,[2] Maria D. Alba,[3] Emilio Sánchez-Cortezon,[1] Jose-Maria Delgado-Sanchez[1]*

[1] Abengoa, Campus Palmas Altas, C/ Energía Solar 1, 41014 Sevilla, Spain
[2] Photonic Group – ITMA Materials Technology, Calafates 11, 33417 Avilés, Spain
[3] ICMS (CSIC-US), Americo Vespuccio 49, 41092 Sevilla, Spain

Corresponding Author

*Carmen López-López

E-mail: maria.lopez@abengoa.com

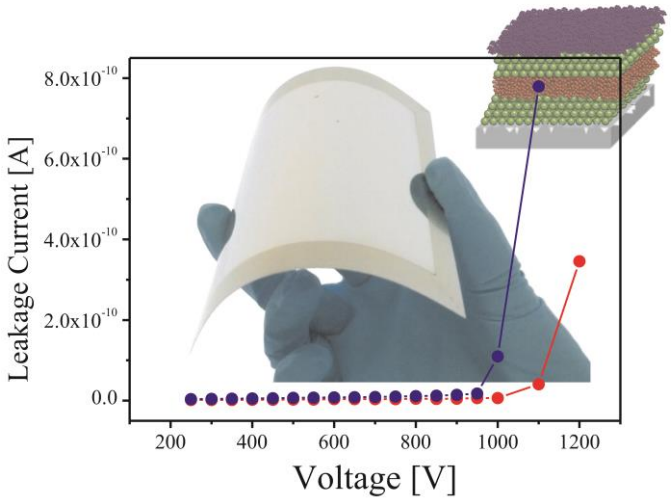
Address: Abengoa, Campus Palmas Altas, C/ Energía Solar 1, 41013 Sevilla, Spain

ABSTRACT

Thin-film PV modules grown on flexible, light weight, thermally stable and low cost substrates such as stainless steel foil, are an attractive product for solar market applications. When metal foils are used as substrate, it is essential to deposit a dielectric barrier layer to isolate electrically and chemically the thin-film solar cells front the substrate. In this work, SiOx stacks deposited on 'rough' stainless steel by a combination of a new sol-gel formulation and a Plasma Enhanced Chemical Vapor Deposition (PECVD) deposition step are reported as a suitable dielectric barrier layer candidate. Using these SiOx multilayers, a smooth and homogeneous film was achieved. X-ray diffraction (XRD) analysis showed that back contact of the solar cell (based on Molybdenum) is not affected by the presence of the barrier layer. Moreover,

according to X-ray photoelectron spectroscopy (XPS) and Secondary Ion Mass Spectrometry (SIMS) measurements, this approach led to excellent barrier layer properties against the diffusion of impurities from the stainless steel. A complete electrical characterization of these dielectric barrier layers was also carried out showing good electrical insulation.

GRAPHICAL ABSTRACT



RESEARCH HIGHLIGHTS

- Dielectric barrier layer for flexible metallic substrates has been developed.
- SiO_x based on Sol-Gel process showed a novel chemical formulation.
- The dielectric barrier layer exhibits a dielectric breakdown voltage about 1000 V for a 4 microns thick stack.
- Dielectric barrier layer was capable to reduce the surface roughness by 40-50%.
- This research opens new challenges for low cost thin-film manufacturing.

ABBREVIATIONS

PECVD, Plasma Enhanced Chemical Vapor Deposition; CTE, coefficient thermal expansion; R_t, surface roughness; TOF-SIMS, SEM, Scanning Electron Microscopy; Secondary Ion Mass Spectrometry; XRD, X-ray diffraction; XPS, X-ray photoelectron spectroscopy.

KEYWORDS: SiOx barrier layer, dielectric, stainless steel, breakdown voltage, flexible, thin- films solar cell

1. INTRODUCTION

One of the challenges for photovoltaic (PV) market applications is to be able to manufacture efficient low cost optoelectronic devices based on suitable low cost materials and processes. Therefore, there is an industrial interest to transfer conventional manufacturing process from thin film PV technologies (CIGS and CZTS) based on glass to alternative low cost materials.[1-7] Furthermore, new substrates for thin-film PV devices will open new market opportunities and features such as flexibility, low weight, low cost, roll-to-roll manufacturing, etc. It is believed that these PV modules are the ideal candidates for PV markets such as Building Integrated Photovoltaic Applications (BIPV) and distributed generation in rooftops. Stainless steel is often identified as one of the best alternative candidate to rigid glass substrates traditionally used for thin-film PV modules.[8,9] However, an extra layer must be added to the stainless steel, named dielectric barrier layer, to make it compatible with the thin-film PV modules, guaranteeing their performance and their electrical interconnection through the so-called monolithic integration process.

The dielectric barrier layer and its application on the metallic substrate must be designed with the following functions: (i) inhibit diffusion of transition metallic elements (Fe, Cr, Ni) from the stainless steel substrate to the semiconductor structure of the solar cell; (ii) reduce the surface roughness of the substrate as much as possible in order to ensure low cost and to minimize the pinholes creation; (iii) mechanically stable to avoid failures during the subsequent thermal annealing like delamination or presence of cracks. This is achieved by designing the layer with a coefficient of thermal expansion (CTE) similar to those materials in contact with it; (iv) provide electrical insulation between the metallic substrate and the back contact of the solar cell. This feature is critical in order to monolithically integrate the neighboring solar cells to build

the thin-film PV module.[3] Numerous examples consisting of Al_2O_3, ZnO, SiO_2 or enameled layer, deposited by sputtering, sol-gel, PECVD or spray techniques have been previously investigated.[10-14] Nevertheless, few of them report on the electrical properties of these layers and the effect of surface roughness on the dielectric function.

The aim of this work was to develop and integrate dielectric barrier layers on commercially available stainless steel foils with high surface roughness and low cost. In the present work, the feasibility of dielectric barrier layers based on SiO_x stacks has been studied. These SiOx stacks were grown by a combination of sol-gel and Plasma Enhanced Chemical Vapor Deposition (PECVD). It is well documented that one of the most common failures in this barrier layer is the mechanical stability, during and after the post-thermal annealing which is the process responsible for the formation of the CIGS or CZTS semiconductor.[8] Moreover it is demonstrated that, these mechanical failures can be solved by the insertion of SiO_x multilayers between the back contact film (Molybdenum) and the stainless steel substrates. The processed samples were 100x100 mm^2, which shows the scalability of the proposed process technology.

2. EXPERIMENTAL

2.1. Material selection

In the recent years, several related works have shown that flexible metals such a have Al,[15] Ti,[16] and steel [10,9] can yield performances close to soda lime glass (SLG). Steel is a competitive material against Ti or Al in terms of both cost and physical properties (mechanical, thermal and coefficient thermal expansion). Moreover, steel meets requirements of a PV substrate since it is very good barrier to oxygen and water, and robustness against external shocks thanks to its good weight/stiffness ratio. Table 1

presents some technical data for potential candidates to substitute glass, such as density, CTE and maximum surface roughness [2].

Table 1. Density, coefficient of thermal expansion (CTE), and surface roughness (Rt) of soda lime glass (SLG) and alternative foils.

	SLG	Ti	Kapton	Stainless Steel
Density [g/cm3]	4.5	4.5	8.2	7.7
Tmax [ºC]	600	> 600	< 500	> 600
CTE [10-6 K-1]	9	8.6	17	10 – 11
R_t [nm]	10 - 15	1400	540	1600

To replace soda lime glass ensuring similar CTE and low cost, the selected substrate was stainless steel AISI430, 0.2 mm thickness and 100x100mm^2 active area (average roughness (Ra=0.23±0.04μm) and peak-to-valley roughness (Rt=1.51±0.33μm)).

The material proposed in this work as dielectric barrier multilayer is SiO_x, which CTE (1-9·10^{-6} K^{-1}) is similar to the AISI430 stainless steel substrate (10-11·10^{-6} K^{-1}) and Mo back contact (5-6·10-6 K^{-1}) of the solar cell. [2] Moreover, the SiO_x, due to its strong ionic interatomic bonding, allows the impurity blocking. Finally, its dielectric character provides suitable electrical insulation between the stainless steel substrate and the electrode of the solar cells.

2.2. Processing

In order to analyze the barrier layer properties of the SiO_x stacks, two alternative structures based on PECVD and sol-gel have been deposited on the AISI430 stainless steel substrate, shown in Figure 1: a SiO_x bilayer structure [Steel/PECVD/sol-gel] [BL-

01] (Figure 1A), and a three-layer SiO_x structure [Steel /sol-gel/PECVD/sol-gel] [BL-02] (Figure 1B). A full description of the sample preparation is presented below. Afterwards the Mo layer to serve as the solar cell back contact was deposited by DC-sputtering on both structures. This Mo layer is needed to evaluate the electrical insulation provided by the dielectric barrier layer.

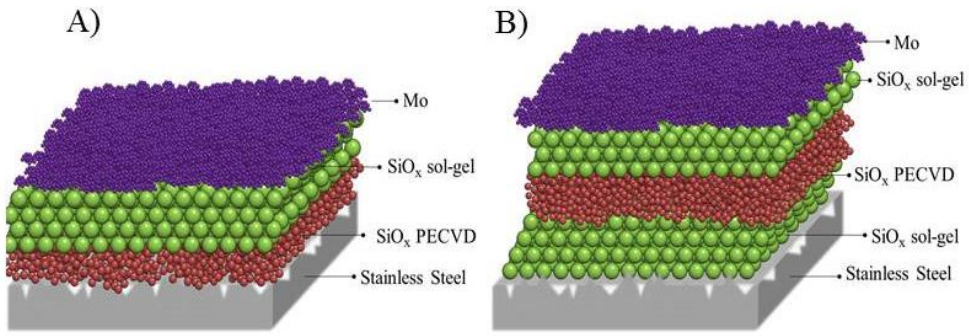


Figure 1. Barrier multilayer scheme integrated in thin-film solar cell structure. A) BL-01: Steel/PECVD/sol-gel, B) BL-02: Steel/sol-gel/PECVD/sol-gel.

Before film deposition, the stainless steel surface was cleaned with soapy water, acetone and dryed with nitrogen to remove any grease contamination which may have hindered the SiO_x adhesion.

A novel SiO_x sol-gel process [17] based on acid catalysis was formulated to reduce the appearance of cracks during high temperature (ca. 550 ºC) thermal annealing. The coating sols were prepared from a 2 mL of tetraethylorthosilicate (TEOS), 8 mL of Methyltriethoxysilane (MTES) and 3 mL of 2,4,N,N'-Dimethylformamide (2,4,N,N'-DMF) which were mixed at room temperature under vigorous stirring during 15 min. After, 5 mL of polyethylene glycol 400 (PEG), 2mL of deionized water and 250 µL of H_3PO_4 were added in different steps waiting 15 min between each one. The so-obtained solution was finally aged for 1 h before its use. After the addition of H_3PO_4, the

temperature of the solution increased about 5 to 8 ºC and became transparent. To achieve the suitable solution for being spin-coated, the molar ratios were adjusted as follows: 4.9 MTES/TEOS, 2.4 DI H2O/(MTES+TEOS), 0.8 N,N'-DMF/(MTES+TEOS) and 0.3 PEG-400/(MTES+TEOS). The resulting sol-gel precursor had a pH between 5.0 and 5.5 and a viscosity of 14 and 18 cP (22 ºC).

Then, 2 mL of precursor solution was deposited on the steel substrate by spin-coating (Spin coater SUS Microtec Delta 6RCTT) working at 1750 rpm for 20 seconds. A dense SiO_x film was formed by sintering the sol-gel film in a hot plate (Titan 5P) following this thermal profile: 60 ºC for 15 minutes in order to remove the solvents, 150 ºC for 60 minutes, 300 ºC for 30 minutes and 550 ºC for 30 minutes, finally the coated substrates were taken out form the hot plate after cooling at room temperature.

The PECVD SiO_x layer was deposited by radiofrequency (13.56 MHz) in a cluster tool from Elettrorava (model V0714) with a ratio of SiH_4 to N_2O of 6:80. The applied power density was 20.8 mW/cm^2 at 500 mTorr pressure and substrate temperature was 480 ºC, which resulted in a deposition rate of 6.25 Å/s.

The final thicknesses of the SiO_x stacks for both BL-01 and BL-02 were 3 and 5 μm ca, respectively. Previous experiments showed that thinner SiO_x stacks presented a higher probability for pinhole formation whereas thicker SiO_x stacks leaded to mechanical failures such as delamination or cracks formation.[2,18,19]

To measure the dielectric properties and the impurity diffusion through the SiO_x stack a Molybdenum bilayer structure, suggested by Scofield et al, [20] was deposited by magnetron sputtering, with a total thickness of 800 nm to ensure good mechanical and electrical properties of the back contact.

2.3. Characterization

Surface roughness of all samples was characterized with a mechanical profilometer (model Ambios XP1, Ambios Technology), following the ISO 4287 protocol. Scotch adhesion tests were performed based on ISO 2409 protocol. Depth profiling of the barrier layers and potential diffusion of metallic elements from the metallic substrate was performed by Secondary Ion Mass Spectrometry (TOF-SIMS) from a CAMECA system, using 5 keV primary Ar^+ ions. Cross sections and top surface of the barrier layers were studied with a Scanning Electron Microscope (SEM), from Hitachi S4800.

The film structure was analysed by X-ray diffraction (XRD) using a Philips Panalytical X'Pert X-ray diffractometer. X-ray photoelectron spectroscopy (XPS) is an ideal technique for analyzing the surface composition and the diffusion process of stainless steel elements such as Fe, Ni or Cr. XPS equipment used in this work was a VG ESCALAB210 with a monochromatic X-ray source Aluminum K_α line with 1486.6 eV. Depth profiles analyses were obtained by sputtering the surface with an Ar^+ ion source. Electrical properties of the SiO_x stacks were measured using an Agilent 34401A source meter coupled to a DC power supply. [21]

3. RESULTS AND DISCUSSIONS

3.1. Adhesion, morphology and microstructure

The BL-01 and BL-02 SiO_x stacks were initially kept at 85 ºC during 1000 h, and then submitted to periodic thermal cycles from -25 ºC to 85 ºC during 300 hours in order to stress them thermally and mechanically. After these thermal cycles, no evidence of cracks was found in any of the stacks. Furthermore, these layers showed a pencil hardness of 6HB, and the Scotch test was successfully conducted.[22] These results

showed that the combination of this novel sol-gel formulation and the PECVD process, were a promising dielectric layer candidate since it passed all mechanical tests. Previous works with similar stack structure could not withstand a thermal treatment, which lead to mechanical failures. [10,23]

The SEM images of the samples showed dense, compact, continuous and uniform layers without any cracks in any of the proposed structures (Figure S1). Cross-section SEM images indicated that no tubular microstructure was present in any stack. Low density tubular growth is expected in magnetron sputtering processes and leads to various types of electrical failures such as pinholes or chemical contamination of the semiconductor due to an easy diffusion with metallic impurities from the substrate.

Batchelor et al [24] reported that the photovoltaic performance of solar cells is strongly dependent on the surface roughness of the substrate. In order to avoid pinholes and shunts and to promote a uniform deposition of the subsequent layers, the native roughness of the substrate should be reduced by the barrier layer. [25] The evolution of the surface roughness average (Ra) value was studied (Figure 2) by mechanical profilometry, examples of roughness profiles before and after barrier layer deposition are displayed in Figure S2. It can be observed that both BL-01 and BL-02 stacks are able to reduce the initial substrate roughness over 40% and 50% ca, respectively. Regarding the roughness evolution during the different deposition steps, the novel sol-gel formulation is the key to improve the surface levelling since it reduces the roughness. Nevertheless, the application of the SiO_x layer by PECVD technique is also crucial since it leads to a dense SiO_x layer that filled up the possible defects forming during the sol-gel annealing stage, such as scratches or small grooves. The SiO_x layer deposited by PECVD is also needed to obtain the optimum barrier layer thickness for

electrical insulation without structural damage. A PECVD layer is therefore sandwiched in between two sol-gel layers, ensuring adhesion between them.

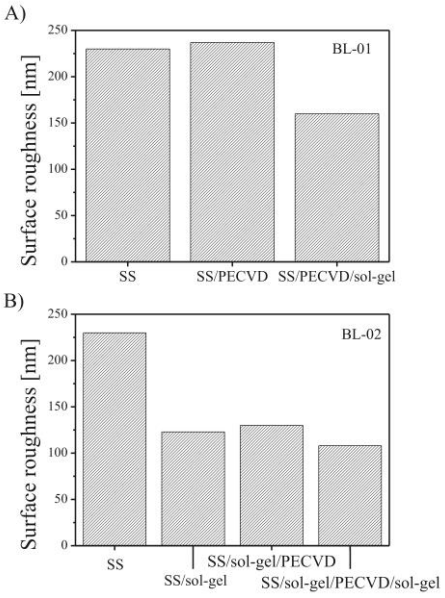


Figure 2. Average surface roughness A) BL-01: Steel/PECVD/sol-gel and B) BL-02: Steel/sol-gel/PECVD/sol-gel.

It is known that the substrate surface properties affect the microstructure of the subsequent thin film layer, such as Mo layer grown on the SiOx stacks. XRD was used to verify that the barrier layer did not affect significantly the microstructure of the upper layer. In Figure S3, the XRD pattern of a Mo layer deposited on BL-01 and BL-02 stacks was compared with that of a Mo layer stacked on a standard glass substrate. It shows, additional peaks corresponding to reflections from the SiO_x structure in BL-01 and BL-02. However, Mo presented the same reflections in all the samples, showing a well-defined Mo microstructure with a strong (110) orientation, which has been reported as the preferential orientation for the back contact used in world record efficiency thin film photovoltaic technologies.[20] It was concluded that the crystalline structure and quality of the solar cell should not be influenced by the proposed barrier

stacks presented in this work, since there were no significant changes in the Mo growth compared to soda-lime glass.

3.2. Barrier against impurities from steel substrate

Recent publications [5,10] have reported that the diffusion of transition metallic elements (such as Fe, Ni or Cr) from the metallic substrate in the semiconductor structure may cause the failure of the solar cell, mainly due to a reduction of the fill factor. In order to evaluate the ability of the SiO_x structures to block the diffusion of undesired atoms such as Fe, Mn, Cr and Ni from the stainless steel, XPS measurements as well as SIMS analysis were carried out. Since element diffusion is favored at high temperatures, these studies were performed on the samples before and after a thermal annealing at 550˚C (simulating the conventional annealing treatment needed to create CIGS or CZTS absorber layers).

The XPS spectra of the Mo surface on BL-01 and BL-02 is shown in Figure 3A. Survey spectra show that all samples have the same composition on the surface after thermal annealing. Two contributions from different Mo oxidation states (Mo and MoO_6) can be distinguished. On the other hand, no signal from transition metals was detected. However, this lack of any impurities on the Molydenum surface did not imply that the SiO_x stacks blocked completely the element diffusion. SIMS was used to assess the quality of the SiO_x stacks as blocking layers. Figure 3B and 3C show the chemical depth profile of these samples. Note that the low signal from metallic atoms (Fe, Cr and Ni) along the back contact layer cannot be distinguished from the background noise signal of the instrument. Other important feature includes the double peak in the Mo signal, corresponding to Mo bilayer followed by the Si signal from the barrier layer.

Therefore, it was concluded that the BL-01 and BL-02 SiOx stacks fulfilled the metallic impurities barrier requirement.

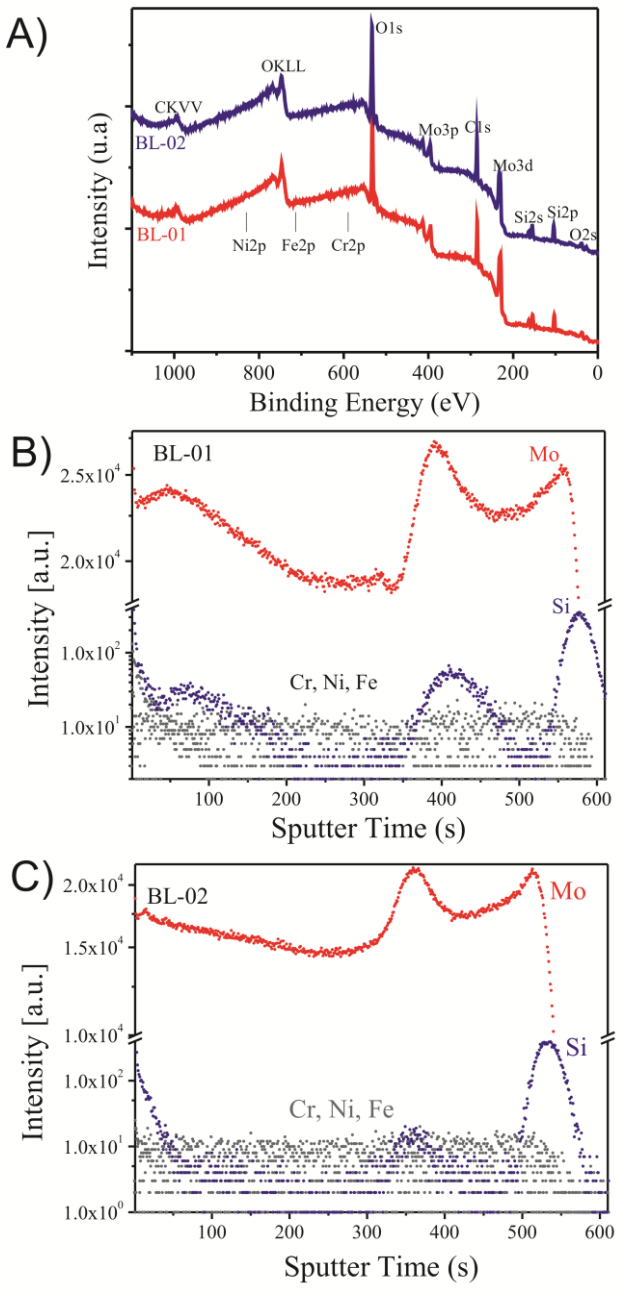


Figure 3. A) XPS patterns; B) and C) SIMS depth profile for BL-01/Mo and BL-02/Mo, respectively.

3.3. Dielectric performance of the barrier layer

Since a high voltage can be generated when several solar cells are interconnected in series onto the dielectric barrier layer, it is critical to determine the breakdown voltage. Both proposed SiO_x stacks exhibited the electrical response of a capacitor when a clock-voltage signal was applied to them. During the periods when the external electric field was applied, both SiO_x stacks responded with a shift in the interfacial polarization (Figure 4) and with a charge imbalance because of the dielectric material's insulating properties. The interface was charged accordingly to the external voltage applied, and a very low leakage current was always observed as it was expected in a good insulating material. Dielectric Absorption Ratio (DAR) was measured on both samples for 60 s, and both stacks resulted in values higher than 1.45 which is the condition for an adequate electrical insulation.[26]

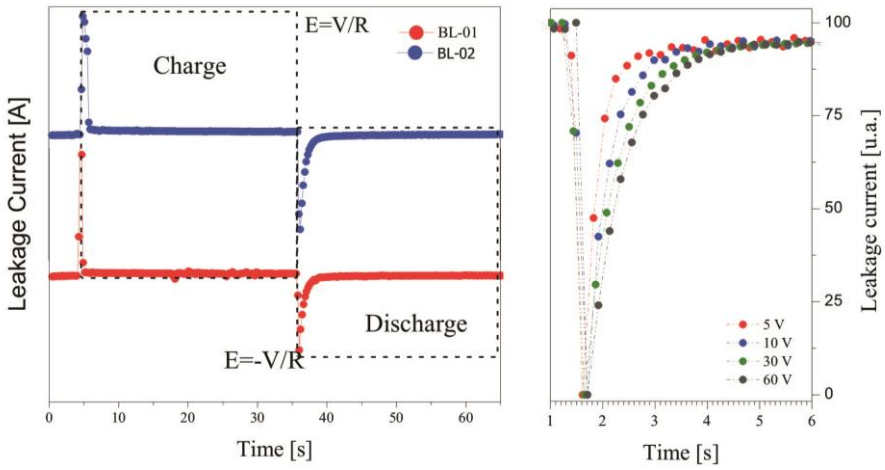


Figure 4. Polarization transient states during charge/discharge of the barrier layer when external electric field is applied.

The leakage current was measured at different DC-voltage levels, keeping 60 s between two consecutive values, and the breakdown voltage was estimated as the voltage at

which the current increased abruptly (Figure 5 left). As expected the breakdown voltage increased from 943V to 1169V when the most sophisticated and thicker barrier structure (BL-02) was employed (Figure 5 right). However, since both structures had similar breakdown voltage values, the bilayer structure (BL-01) supported a higher electric field across the barrier layer because some of the charge carriers that are forced through the barrier layer were trapped in impurities or interfaces defects. [27] Neither of these electrical insulation levels was achieved when rough stainless steel was covered only with a single SiO_x layer deposited by PECVD or sol-gel.

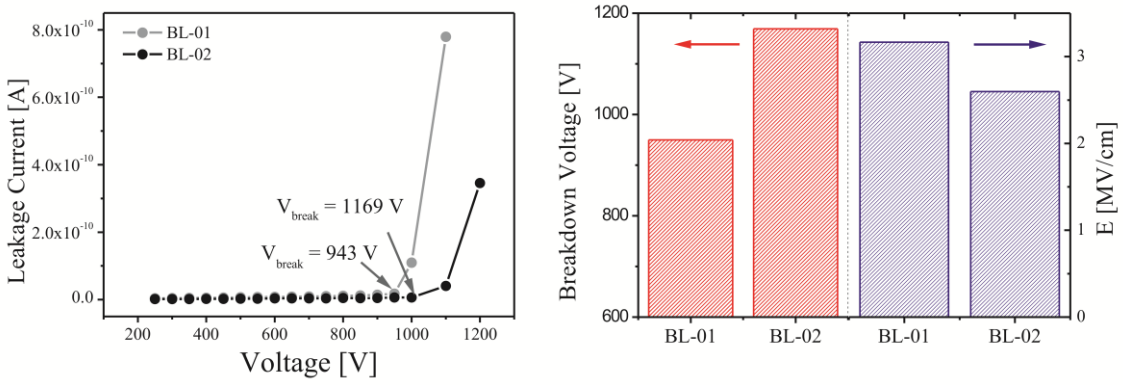


Figure 5. Breakdown voltage determination and maximum electric field through barrier layers proposed.

Additionally, the performance of both barrier layer structures was tested after mechanical stress.[28,29] BL-01 and BL-02 were subjected to a bending test using the method discussed in the supporting information (Figure S4). The breakdown voltage was measured as a function of the bending radius (Figure S4.C). Negligible variation on the breakdown voltage of the samples is observed when they were strained. The samples were also examined by optical microscopy and no evidence of cracks or surface deformation after the mechanical stress test was observed. Moreover, a cyclic fatigue

test was also carried out at the minimum bending radius showing no change in the breakdown voltage of the samples after 500 cycles at maximum curvature radius.

Finally, we can conclude that BL-01 is the most suitable barrier layer structure for thin-film PV technology. Both stacks exhibited a similar morphology and dielectric properties but the fabrication process of the BL-01 stack involves two steps instead of three, which means a significant manufacturing cost reduction.

4. CONCLUSIONS

Dielectric barrier stacks based on a hybrid process (sol-gel/PECVD) have been manufactured on low cost 'rough' AISI430 stainless steel substrates, using a novel sol-gel formulation process. It has been demonstrated that these barrier stacks fulfilled the functionalities for thin-film photovoltaic on metallic substrate substrates: a significant reduction of the surface roughness, no impact on the back contact microstructure, no diffusion of transition metals (Fe, Ni, Cr) into the semiconductor stack, and electrical insulation between the back contact solar cell electrode and the metallic substrate. Whereas these features cannot be achieved by employing a single barrier layer deposited by PECVD or sol-gel. Moreover, both processes have the characteristic to be easy to transfer to the industrial scale. The novel barrier layer and processes proposed in this work open new opportunities to transfer thin-film photovoltaic technology from glass to flexible, lower weight and cost substrates. The results demonstrated that barrier layer proposed is compatible with conventional thin-film technology as CIGS, but also with emerging thin-film technologies such as CZTS.

Corresponding Author

*Carmen López-López

Abengoa, Campus Palmas Altas, C/ Energía Solar 1, 41013 Sevilla, Spain

AKNOWLEDGEMENTS

The research leading to these results has received funding from the European Union's Research Fund for Coal and Steel (RFCS) research program under grant agreement nº RFSR-CT-2014-00014

5. REFERENCES

[1] Contreras, M.A.; Egaas, B.; Ramanathan, K.; Hiltner, J.; Swartzlander, A.; Hasoon, F.; Noufi, R., Progress toward 20% efficiency in Cu[In,Ga]Se_2 polycrystalline thin-film solar cells. Prog. Photovolt: Res. Appl., **1999**, 7, 311–316.

[2] Kessler, F.; Rudmann, D.; Technological aspects of flexible CIGS solar cells and modules. Solar Energy, **2004**, 77, 685-695.

[3] Kessler, F.; Herrmann, D.; Powalla, M.; Approaches to flexible CIGS thin-film solar cells. Thin Solid Films, **2005**, 480-481, 491-498.

[4] Khelifi, S.; Belghachi, A.; Lauwert, J.; Decock, K.; Wienke, J.; Caballero, R.; Kaufmann, C.A.; Burgelman, M.; Characterization of flexible thin film CIGSe solar cells grown on different metallic substrates. E-MRS Spring Meeting **2009**, Energy procedia, 2010, 2, 109-117.

[5] Wuerz, R.; Eicke, A.; Frankenfeld, M.; Kessler, F.; Powalla, M.; Rogin, P.; Yazdani-Assl, O.; CIGS thin film solar cells on steel substrates. Thin Solid Films, **2009**, 517, 2415-2418.

[6] Ishizuka, S.; Yoshiyama, T.;M izukoshi, K.; Yamada, A.; Niki, S.; Monolithically integrated flexible Cu[In,Ga]Se_2 solar cell submodules. Solar Energy Materials & Solar Cells, **2010**, 92, 2052.

[7] Tian, Q.; Xu, X.; Han, L.; Tang, M.; Zou, R.; Chen, Z.; Yu, M.; Yang, J.; Hu, J.; Hydrophilic Cu_2ZnSnS_4 nanocrystals for printing flexible, low-cost and environmentally friendly solar cells. CrysEngComm, **2012**, 11, 3847-3850.

[8] Herz, K.; Kessler, F.; Wächter, R.; Powalla, M.; Schulz, A.; Schumacher, U.; Dielectric barriers for flexible CIGS solar modules. Thin Solid Films, **2002**, 403/404, 384.

[9] Blosch, P.; Chirila, A.; Pianezzi, F.; Seyrling, S.; Rossbach, P.; Buecheler, S.; Nishiwaki, S.; Tiwari, AN.;, Comparative study of different back contact designs for high efficiency CIGS solar cells on stainless steel foils. IEEE Journal of photovoltaics, **2011**, 2, 194-199.

[10] Shi, C.Y.; Sun, Y.; He, Q.; Li, F.Y.; Zhao, J.C.; Cu[In, Ga]Se_2 solar cells on stainless-steel substrates covered with ZnO diffusion barriers. Solar Energy Materials & Solar Cells, **2009**, 93, 654-656.

[11] Gledhill, S.; Zykov, A.; Allsop, N.; Rissom, T.; Schniebs, J.; Kaufmann, C.A.; Lux-Steiner, M.; Fisher, CH.; Spray pyrolysis of barrier layers for flexible thin film solar cells on steel. Solar Energy Materials & Solar Cells, **2011**, 95, 504-509.

[12] Wuerz, R.; Eicke, A.; Kessler, F.; Paetel, S.; Efimenko, S.; Schegel, C.; CIGS thin-film solar cells and modules on enamelled steel substrates. Solar Energy Materials & Solar Cells, **2012**, 100, 132-137.

[13] Moriwaki, K.; Nomoto, M.; Yuuya, S.; Murakami, N.; Ohgoh, T.; Yamane, K.; Ishizuka, S.; S. Niki, Monolithically integrated flexible Cu[In,Ga]Se_2 solar cells and submodules using newly developed structure metal foil substrate with a dielectric layer. Solar Energy Materials and Solar Cells, **2013**, 112, 106-111.

[14] Thongkam, W.; Pankiew, A.; Yoodee, K.; Chatraphorn, S.; Enhancing efficiency of Cu[In,Ga]Se_2 solar cells on flexible stainless steel foils using NaF co-evaporation. Solar Energy, **2013**, 92, 189-195.

[15] Bremaud, D.; Rudmann, D.; Kaelin, M.; Emits, K.; Bilger, G.; Dobeli, N.; Zogg, H.; Tiwari, A.N.; Flexible Cu[In,Ga]Se_2 on Al foil and the effects of Al during chemical bath deposition. Thin solid films, **2007**, 515, 5857–5861.

[16] Yagioka, T.; Nakada, T.; Cd-free flexible Cu[In,Ga]Se_2 thin film solar cells with ZnS[O,OH] buffer layers on Ti foils. Applied Physics Express, **2009**, 2, 072201-1–072201-3.

[17] Andrés Menendez, L.J.; Fernández Suárez, M.F.; Menéndez Estrada, A.; Sancho Martínez, D.; Gómez Plaza, D.; Sánchez, P.; Sánchez Cortezón, E.; Delgado Sánchez, J.M.; "Procedimiento para la preparación de una capa barrera dieléctrica de óxido de silicio [SiOx] y capa así preparada". World Intellectual Property Org. [WIPO], PCT/ES2014/000150, September **2014**.

[18] Chung, Y.D.; Cho, D.H.; Han, W.S.; Park, N.M.; Lee, K.S.; Oh, S.Y.; Kim, J.; The thickness effect of SiO_x layer in CIGS thin-film solar cells fabricated on stainless-steel substrate. Photovoltaic Specialists Conference [PVSC], **2010,** 35th IEEE, 003401-003402.

[19] Green, M.A.; Thin-film solar cells: review of materials, technologies and commercial status. Journal Material Science: Material Electron, **2007**, 18, S15-S19.

[20] Scofield, J.H.; Duda, A.; Albin, D.; Ballard, B.L.; Predecki, P.K.; Sputtered molybdenum bilayer back contact for copper indium diselenide-based polycrystalline thin-film solar cells. Thin Solid Film, **1995**, 260, 26-31.

[21] Amouzou, D.; Guaino, P.; Dumont, J.; Fourdrinier, L.; Richir, J.B.; Sporken, R.; Maseri, F.; Novel high thermal layers for flexible CIGS solar cells on stainless steel substrates. Photovoltaic Specialists Conference [PVSC], **2011**, 37th IEEE, 001229 – 001234.

[22]Shapiro, L.; Marx, S.; Mandler, D.; Preparation and characterization of ultra-thin sol-gel films. Thin Solid Films, **2007**, 515, 4624-4628.

[23] Amouzou, D.; Dumont, J.; Fourdrinier, L.; Richir, J.B.; Maseri, F.; Sporken, R.; Adhesion resistivity and structural, optical properties of molybdenum on steel sheet coated with barrier layer done by sol-gel for CIGS solar cells. Thin Solid Films, **2013**, 531, 535-540.

[24] Batchelor, W.K.; Repins, I.L.; Schaefer, J.; Beck, M.E.; Impact of substrate roughness on $CuIn_xGa_1$-xSe_2 device properties. Solar Energy Materials & Solar Cells, **2004**, 83, 67-80.

[25] Delgado-Sánchez, J.M.; Guilera, N.; Francesch, L.; Alba, M.D.; López, L.; Sánchez, E.; Ceramic Barrier Layers for Flexible Thin Film Solar Cells on Metallic Substrates: A Laboratory Scale Study for Process optimization and Barrier Layer Properties. Applied Materials & Interfaces, **2014**, 6, 18543-18549.

[26] ANSI/NETA ATS, "Standard for Acceptance Testing Specifications for Electrical Power Equipment and Systems", **2013.**

[27] Allers, K.H.; Prediction of dielectric reliability from I–V characteristics: Poole–Frenkel conduction mechanism leading to E model for silicon nitride MIM capacitor, Microelectronic Reliability, **2004**, 44, 411-423.

[28] Lee, S; Yeo, J.S; Ji, Y.; Cho, C.; Kim, D.Y.; Na, S.I.; Lee, B.H.; Lee, T.; Flexible organic solar cells composed of P3HT:PCBM using chemically doped graphene electrodes, Nanotechnology, **2012**, 23, 344013-344019.

[29] Rathmell, A.R.; Bergin, S.M.; Hua, Y.L.; Li, Z.Y.; Wiley, B.J.; The growth mechanism of Copper nanowires and their properties in flexible, transparent conducting films, Advanced Materials, **2010**, 22, 3558-3563.

Supporting Information

Enhancement of dielectric barrier layer properties by Sol-Gel and PECVD stacks

Carmen López-López,[1] Mari-Fe Menendez,[2] Luis Andres Menendez,[2] Armando Menendez,[2] Pascal Sánchez,[2] Maria D. Alba,[3] Emilio Sánchez-Cortezon,[1] Jose-Maria Delgado-Sanchez[1]*

RESULTS AND DISCUSSIONS

1. Adhesion, morphology and microstructure

SEM cross sectional images of BL-01 [Steel/PECVD/sol-gel] and BL-02 [Steel /sol-gel/PECVD/sol-gel] were performed to check the layered structure of both SiO_x stacks. It can be seen in figure S1, the thickness of both structures was ca. 3 and 5 µm, respectively which fulfill the thickness requirements of the barrier layer.

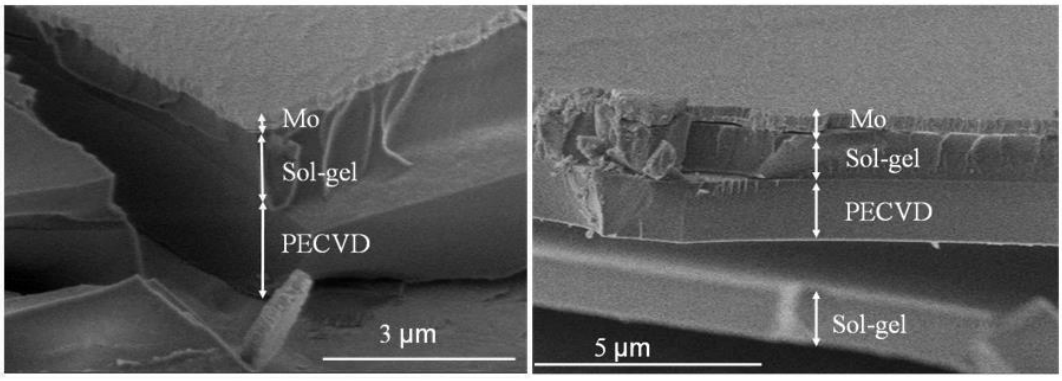


Figure S1. Cross section of barrier layers processed observed by SEM. BL-01 (right) and BL-02 (left).

The surface topography of the stainless steel before and after barrier layer deposition was studied and it is displayed in Figure S2. One can observe the presence of streaks on the uncoated steel surface (Figure S2.A) due to the rolling process. Such surface topography was drastically smothered when the steel was coated with the SiOx stack (Figure S2.B).

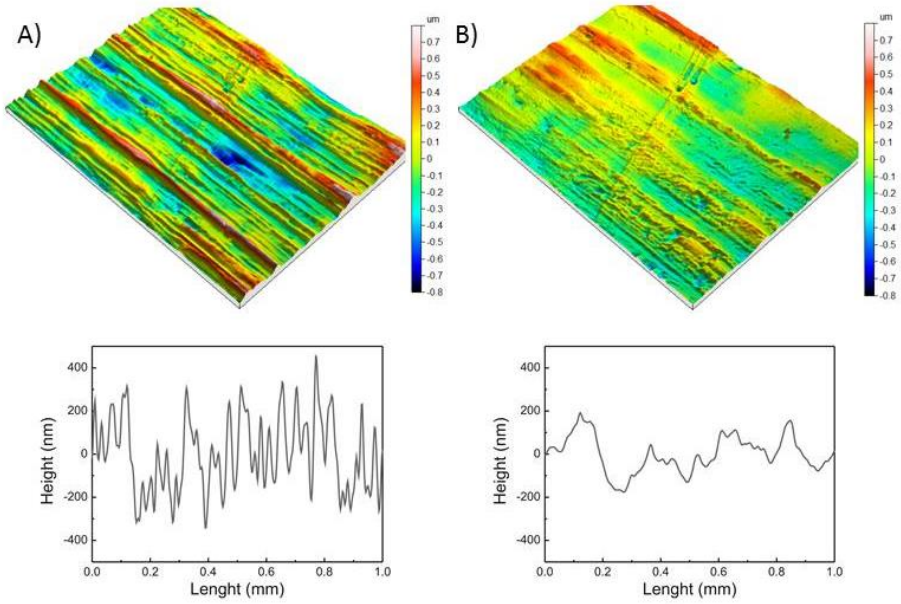


Figure S2. 3D surface topography images and surface profiles of Steel A) before coated and B) after barrier layer deposition.

Figure S3 shows XRD patterns of the Mo layer deposited on glass and steel coated with BL-02 structure. From these XRD it is clear that the insertion of the barrier layer did not influence the deposition of the Mo layer, since the pattern of Mo grown on the BL-02 structure had the same diffraction peaks as those of the Mo on the glass.

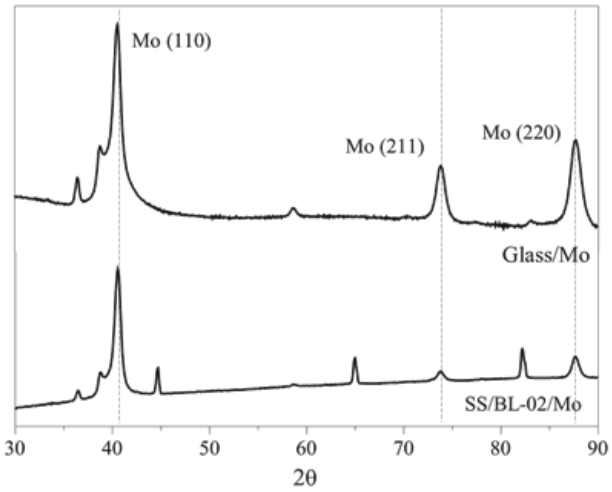


Figure S3. XRD patterns of Glass/Mo (top) and Steel/BL-02/Mo (bottom)

2. Dielectric performance of the barrier layer

To assess the impact of mechanical stress on the sample quality, selected samples were subjected to both manual compression and tensile bending (Figure S4.A). Each sample was placed surface down to induce compressive strain and surface up to apply tensile strain (Figure S4.B). Figure S4.C shows the breakdown voltage measured for BL-01 and BL-02 samples after applying different bending radii. Although the bending strain was increased, the breakdown voltage of both structures remained almost unchanged. The optical microscopy results showed no evidence of cracks or surface deformation after the stress test was found. This characterization was also performance after 500 cycles at the minimum bending radius leading to the same conclusion: this process did not provoke any observable change in the electrical properties of the barrier layers.

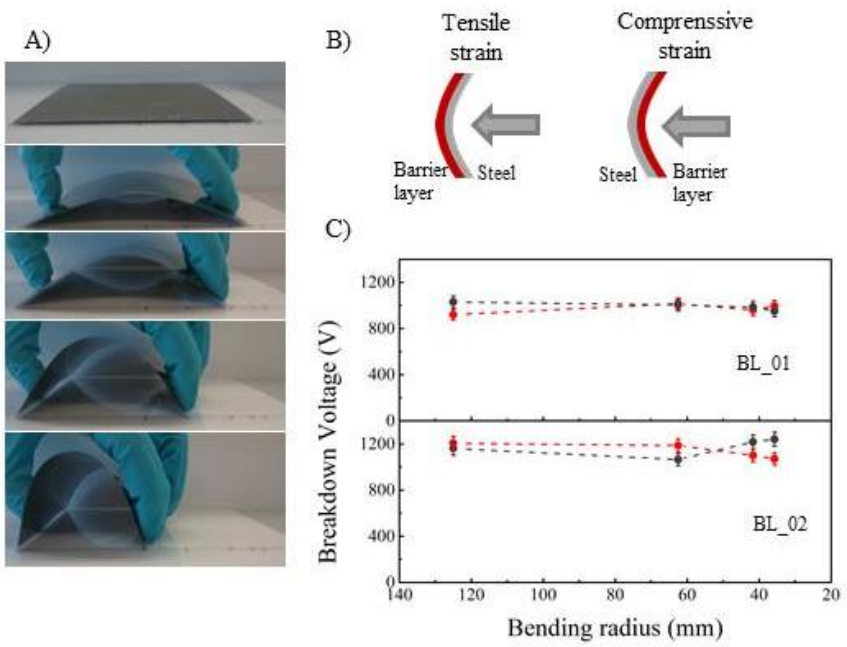


Figure S4. A) Images illustrating application of bending force for different bending radius. B) Schematic illustration of the measurement configuration for the bending test. C) Effect of the applied bending radius on the Breakdown voltage under tensile (Grey dots) and compressive (red dots) strain conditions.