# A LOW-PASS FILTER WITH AUTOMATIC FREQUENCY TUNING FOR A BLUETOOTH RECEIVER

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## ABSTRACT

A third-order Gm-C Chebyshev low-pass filter with high linearity and automatic frequency programmability has been designed. The filter is intended to be used as a channel-select filter for a zero-IF Bluetooth receiver. The frequency tuning scheme is simpler and has more relaxed specifications than conventional ones. The filter bandwidth is 0.5 MHz and the overall scheme dissipates 1.1 mA from a 1.8-V supply. The third-order intermodulation (IM3) distortion of the filter for a 1Vpp two-tone signal centered at 350 kHz is −67dB.

***Index Terms***— analog CMOS circuits, Gm-C filters, linear transconductors, frequency tuning, direct-conversion receivers.

## 1. INTRODUCTION

The great demand for wireless communications systems has created new challenges for circuit designers from receiver architecture to cell level. Different requirement tradeoffs must be overcome related to complexity, power dissipation, bandwidth, linearity, integration level, noise and offset. The trend to implement fully integrated receivers with low power consumption has led the research about Gm-C filter strives to yield more efficient solutions than conventional active RC topologies. The stringent requirements for the analog channel filter of the receiver dominate the performance of the overall chain.

The targeted application for the low-pass filter presented in this paper is the zero-IF filtering section of a Bluetooth receiver with an on-chip automatic tuning circuit required due to process tolerances [1]-[2]. The design meets the selectivity and linearity requirements of Bluetooth while consuming low power. Low-IF and zero-IF architectures seem to be more suitable for a Bluetooth receiver. The direct conversion receiver avoids the requirement for image rejection but the flicker noise and dc offset can degrade the signal to noise ratio.

## 2. TRANSCONDUCTOR TOPOLOGY

The design has to be concerned with power efficiency but stringent linearity and noise performances are required as well. The need of a tunable transconductor with high linearity requirements [3]-[4] led us to the use of the MOS transistor in its triode region as linear voltage to current conversion since this allows a direct control on the MOS's transconductance value through its $V_{DS}$. The first-order expression for the large-signal drain current of an n-MOS transistor operating in strong inversion and the triode region is given by:

$$I_D = \mu C_{ox} \frac{W}{L}(V_{GS} - V_{TN} - \frac{V_{DS}}{2}) \cdot V_{DS} \quad (1)$$

and the linear dependence of the transconductance on $V_{DS}$ is

$$G_M = \frac{\partial I_D}{\partial V_{GS}} = \mu C_{ox} \frac{W}{L} V_{DS} \quad (2)$$

where all parameters have their usual meaning. According to the above equations, a triode transistor achieves ideally perfect linearity between the output current and the input voltage. This linear characteristic can be assumed for long channel MOS transistors.

The transconductance cell is shown in Fig. 1. Both input transistors $M_1$ and $M_2$ are in the triode region and cascode transistors $M_3$ and $M_4$ are used to fix the drain voltage. Linearity is highly dependant on $V_{DS}$ of $M_1$-$M_2$ transistors because the large signal transconductance of $M_{1,2}$ is directly proportional to their $V_{DS}$. Regulated-cascode transistors must ensure that $M_{1,2}$ drain voltage remains practically constant despite large input current variations. The feedback loop formed by transistors $M_5$ and $M_6$ and the bias current $I_B$ guarantees a very low variation of $V_{DS1,2}$ around their quiescent value.

Transistors $M_6$ and $M_7$ implement a very low impedance node at the common source of $M_5$ and $M_6$ that sets the dc voltage at drain of input transistors $M_1$ and $M_2$ to a value equal to the tuning voltage $V_{prog}$. The small signal impedance at the source of $M_6$ is given by $r_x=1/(g_{m6} \cdot g_{m7} \cdot r_6)$ where $g_{m6}$, $g_{m7}$ are

the small-signal transconductance gains of $M_6$ and $M_7$, respectively, and $r_6$ is the small-signal output resistance of $M_6$. The solution to control the transconductance ensures power efficiency and simplicity. The feedback loop boosts the transconductor output impedance and maintains the output nodes isolated from the low impedance drain of the input transistor. The boosted output resistance at the drain of $M_3$ is approximately: $r_{out} \cong g_{m3} \cdot g_{m5} \cdot r_{o1} \cdot r_{o3} \cdot r_{o5}$, where the feedback loop gain is given by $g_{m5}r_{o5}$. $I_o$ is a voltage-controlled cascode current source that ensures high output impedance.

The programmability of the transconductor requires an adaptive-bias circuit (common-mode feedforward, CMFF) to set the common-mode output current. This circuit has been implemented with a replica of a branch of the transconductance cell. A conventional common-mode feedback circuit (CMFB) fixes the common-mode output voltage. Both CMFF and CMFB control the current source $I_o$, stabilizing the common-mode output over the tuning range which is required for low supply voltage and high linearity, and further increase the CMRR of the pseudo-differential topology.

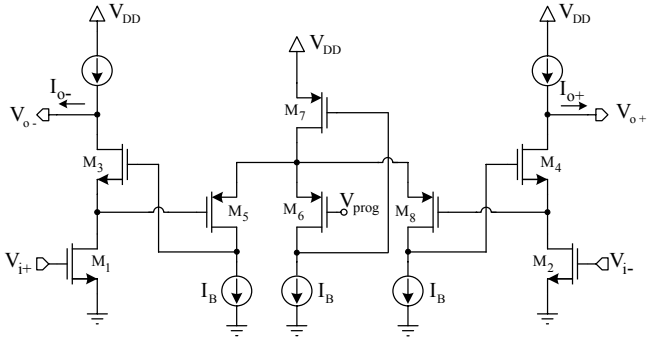


Fig. 1. Used transconductance cell.

*Design considerations:* The tuning voltage $V_{prog}$ of the circuit can be set to near ground. This fact allows to achieve a large tuning range while maintaining a low level of distortion in the output current for a given input voltage range, and requiring a low supply voltage for this kind of transconductor based on input transistors operating in triode region. The upper limit for the tuning voltage $V_{prog}$ must ensure that $M_1$ is kept in the triode region, and the condition $V_{prog} < V_{i,CM}-(V_{id}/2)-V_{TN}$ must be satisfied for the entire range of the input signal. It is necessary that $M_5$ remains in saturation region for the complete range of *Vi* and the maximum value of $V_{prog}$. To fulfill that $V_{SD5} > V_{SG5}-V_{TH}$, the size of $M_3$, $M_5$ ($M_6$) and the bias current $I_B$, must be carefully adjusted.

The transconductor was sized according the design parameters of a 0.5 µm n-well CMOS process with nMOS and pMOS threshold voltages of $V_{TN}$ = 0.67 V and $V_{TP}$ = –0.96 V, respectively. The following transistor sizes (in micrometers) were used: $M_1$-$M_2$: 20/3, $M_3$-$M_4$: 100/0.6, $M_5$, $M_6$, $M_8$: 10/2, $M_7$: 30/1.2 and the current bias $I_B$ = 10 µA. The circuit was simulated with a single supply $V_{DD}$ = 1.8 V and the common-mode input (output) voltage $V_{i,CM}$ ($V_{o,CM}$) was set to 1.3 V.

Fig. 2 shows the simulated transconductance range of approximately one decade between 15 to 165 µA/V for a tuning interval from $V_{prog}$ = 25 mV to 250 mV. It can be seen that a linear behavior is obtained for a large differential input voltage. For the nominal transconductance ($V_{prog}$ = *125 mV*), the unity-gain frequency is 22 MHz, the quiescent input current is $I_{D1}$= 43 µA, and the total power consumption about 360 µW. The post-layout simulated output spectrum for a 1-MHz input signal of amplitude of 1 $V_{pp}$, featuring −74 dB of THD for the nominal transconductance.

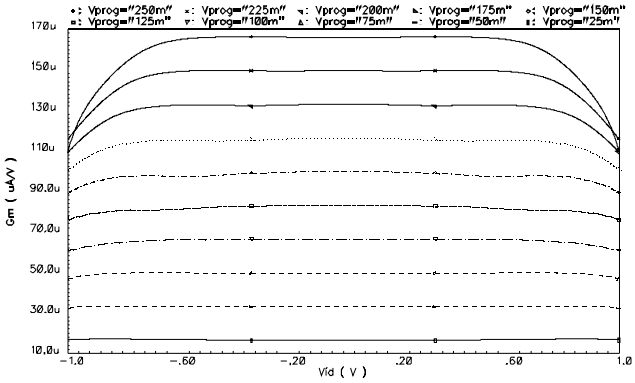


Fig. 2. Simulated transconductor behavior. Transconductance versus differential input voltage

## 3. FILTER DESCRIPTION

In order to use the properties of the transconductor, a continuous-time filter with severe linearity requirements and power efficiency for a zero-IF Bluetooth receiver has been designed. The filter specifications are given in Table I.

TABLE I. CHANNEL FILTER SPECIFICATIONS

| | |
|---|---|
| Type | Chebyshev |
| Order | 3th |
| Topology | Low Pass |
| Passband ripple | 0.5 dB |
| Cutoff frequency | 0.5 MHz |
| DC gain | 10 dB |
| THD | > 60dB |

For the third-order Chebyshev low-pass filter a Gm-C topology has been chosen as shown in Fig. 3.

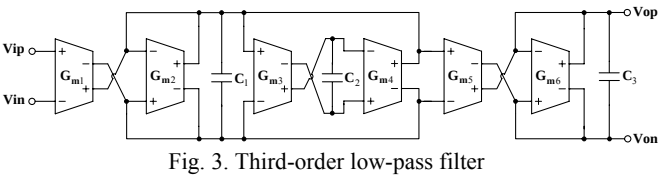


Fig. 3. Third-order low-pass filter

The implementation uses differential transconductors and poly-poly floating capacitors. The filter transfer function is given by:

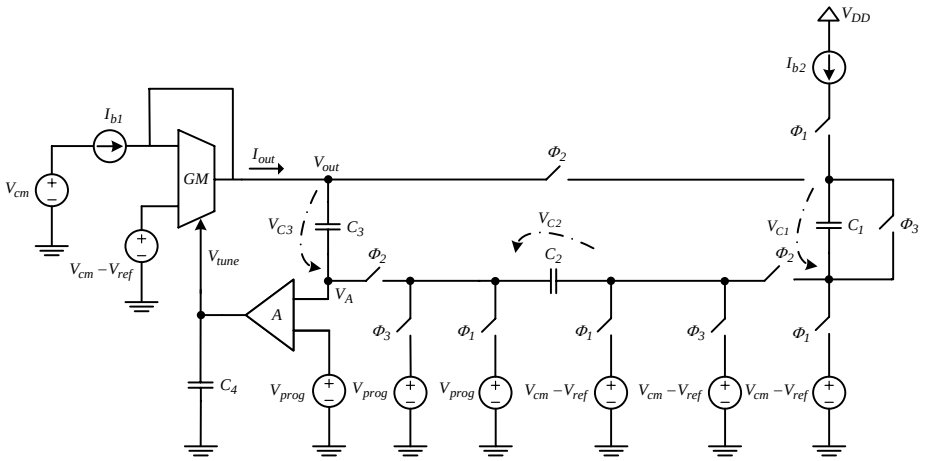


Fig. 4. Frequency tuning circuit for the filter.

$$H(s)=\frac{G_{m1}G_{m3}/C_1C_2}{s^2+(G_{m2}/C_1)\cdot s+G_{m3}G_{m4}/C_1C_2}\cdot\frac{G_{m5}/C_3}{s+G_{m6}/C_3} \quad (3)$$

The required voltage gain of ≈ 10 dB is achieved by adding three $G_{m1}$ transconductors in parallel. For the practical design all transconductance values are set to $G_m$= 64 μA/V ($V_{prog}$ = 100 mV) giving the capacitor values $C_1 = C_3$ = 16.26 pF and $C_2$ = 5.58 pF. The common-mode control has been implemented using a minimum number of adaptive-bias and CMFB circuits decreasing the area and the power consumption. The adaptive-bias circuit has been generated only once and mirrored to all transconductors. Furthermore, a CMFB circuit by filter node has been employed, leading to a more compact filter topology.

*Frequency tuning scheme*

Fig. 4 show the automatic frequency tuning circuit of the low pass filter used to compensate for process variations. The frequency tuning scheme uses the Gm/C tuning technique. This method basically uses an extra transconductor in the tuning circuit to generate the control signal for all the transconductors of the filter. Although the use of this technique requires a good matching between the extra transconductor and the filter's transconductors, its simplicity allows very low power consumption and small silicon area.

The frequency tuning circuit is based on a switched capacitor circuit controlled by three non-overlapping clock signals ($\Phi_1$, $\Phi_2$ and $\Phi_3$) and consists of only three capacitors, some switches and a replica transconductor to adjust the pole frequency of the filter.

The operation of the tuning circuit is described as follows: During the clock phase $\Phi_1$, capacitors $C_1$ and $C_2$ are charged to the following values:

$$V_{C1}=\frac{T_1\cdot I_{b2}}{C_1} \quad (4)$$

$$V_{C2}=V_{prog}-(V_{cm}-V_{ref}) \quad (5)$$

where $T_1$ is the period of time in which $\Phi_1$ is active, $V_{cm}$ is the common-mode input voltage of the transconductor, $V_{ref}$ is a reference voltage and $V_{prog}$ is the theoretical control voltage of the transconductor. In phase $\Phi_2$, capacitors $C_1$ and $C_2$ are connected in series and both in parallel with capacitor $C_3$, so a charge transfer takes place between these three capacitors. Finally, the purpose of clock phase $\Phi_3$ is to reset the capacitor $C_1$ in order to start in a correct value the next clock phase.

In quiescent conditions:

$$V_{out}-V_A=\frac{T_1\cdot I_{b2}}{C_1}+(V_{cm}-V_{ref})-V_{prog} \quad (6)$$

$$I_{b1}=Gm\cdot\left[V_{out}-(V_{cm}-V_{ref})\right] \quad (7)$$

$$V_{tune}=A\cdot(V_A-V_{prog}) \quad (8)$$

Using the expressions shown above:

$$Gm=\frac{I_{b1}}{\frac{I_{b2}\cdot T_1}{C_1}+\frac{V_{tune}}{A}}\approx\frac{I_{b1}}{I_{b2}}\frac{C_1}{T_1} \quad (9)$$

As it can be noticed from expression (9) the transconductance value is proportional to the value of capacitor $C_1$ that will be affected by process variations in the same way the capacitors of the filter. The term given by $V_{tune}/A$ is just an error that can be negligible if the amplifier gain is high enough. In our case an amplifier gain of only 20 dB is needed, so that a very simple architecture has been used. The main advantage of the tuning circuit is that the operational amplifier has more relaxed specifications of gain and bandwidth, and no need an extra low-pass filter at the output to stabilize the tuning voltage of the filter as conventional solutions. The frequency tuning topology gives a good tradeoff between simplicity and performance.

## 4. SIMULATION RESULTS

The filter and the frequency tuning have been designed in a 1.8-V, 0.5 μm CMOS technology. The filter area is 0.52 $mm^2$, and the tuning circuit area is 0.16 $mm^2$. The circuit operates from a single 1.8-V and draws 1.1 mA. The simulated frequency response is shown in Fig. 5. The automatic tuning loop ensures that the cut-off frequency of the filter remains constant for process variations. The accuracy in the tuning system shows that a ±20% variations on the capacitor sizes results in a tuning error of only a ±1% in the cut-off frequency. Fig. 6 shows the post-layout simulated output spectrum for a 100-kHz signal of peak-to-peak amplitude of 1 V, featuring −72 dB of THD. Distortion is mainly of third order owing to the balanced topology. Fig. 7 illustrates the simulated third-order intermodulation distortion of the filter for a 1-Vpp two-tone signal centered at 350 kHz is –67 dB. Table II summarizes the performance parameters of the filter.

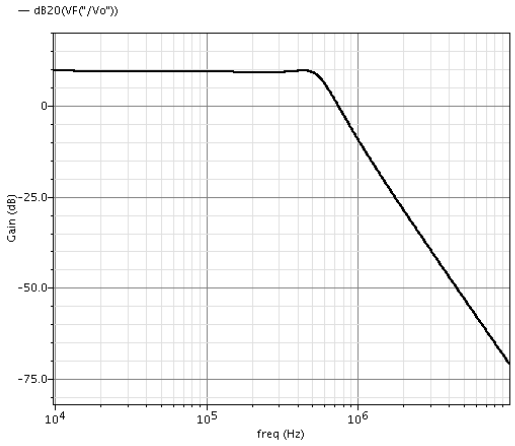


Fig. 5. Frequency response.

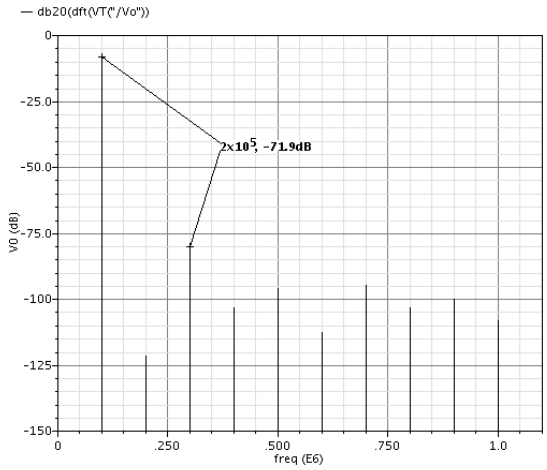


Fig. 6. Output power spectrum for 100 kHz, 1 Vpp signal.

## 5. CONCLUSIONS

A Gm-C filter for zero-IF Bluetooth receiver has been presented. The design uses a pseudo-differential transconductor suitable to operate in low voltage environment with a good tradeoff between performance and compactness. An automatic frequency tuning circuit with more relaxed specifications and simplicity those conventional solutions has been used. The filter achieves a distortion of −72 dB for a 100 kHz, 1 Vpp input voltage at a 1.8 V supply voltage.

TABLE II. FILTER PERFORMANCE PARAMETERS

| Parameter | Value |
|---|---|
| Technology | 0.5 μm CMOS |
| Threshold voltage | $V_{TP}$ = –0.96V, $V_{TN}$ = 0.67V |
| Supply voltage | 1.8 V |
| Cut-off frequency | 500 kHz |
| THD@100kHz, 1Vpp | −72 dB |
| IM3@350kHz, 1Vpp | −67 dB |
| Current consumption | 1.1 mA |
| Silicon area | 0.68 $mm^2$ |


Fig. 7. Simulated IM3. The intermodulation component is at −67dB for a 1Vpp. Input tones are at 300 kHz and 400 kHz.

## ACKNOWLEDGMENTS

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