# Delay degradation effect in submicronic CMOS inverters

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## Abstract.

This communication presents the evidence of a degradation effect causing important reductions in the delay of a CMOS inverter when consecutive input transition are close in time. Complete understanding of the effect is demonstrated, providing a quantifying model. Fully characterization as a function of design variables and external conditions is carried out, making the model suitable for using in library characterization as well as simulation at a transistor level. Comparison with HSPICE level 6 simulations shows satisfactory accuracy for timing evaluation.

## 1. Introduction

Timing simulation of digital integrated circuits is a traditional source of doubt for the designer when he has to choose between accuracy of results and simulation time. Event-driven logic simulators provide high speed, and their main disadvantage lies in their lack of precision due to the fact that they usually incorporate an excessively simple propagation delay model. To improve the precision of the simulation results in logic simulators, other effects must be considered: *input signal transition time* [1, 2, 3, 4]; *input to output coupling capacitance* and *short-circuit currents* [3, 4]; *reduction of serial connected MOSFETs* [5, 6] and *input collisions* [5, 7].

This paper focuses on glitch type input collisions. As the circuit frequencies goes higher, input transitions begin to happen closer in time, forming narrow pulses. This may cause important delay reductions, as will be shown in this paper. We have called this effect *delay degradation* or simply *degradation effect*. Two needs arise: for the IC

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designer, the need to know which timing conditions this effect take place in, and for the logic simulator programmer and the cell library characterizer, the need of delay models taking account of this effect. In this paper we present a model to calculate the propagation delay of an inverter under glitch input conditions. It will be shown that significant delay reductions are obtained as the input pulse widths become comparable to a few times the normal propagation delay of the gate. This way, the classical approach establishing a sharp limit between normal propagation delay and pulse filtering is no longer valid and its use can drive to important inaccuracies. The proposed model is fully characterized in terms of inverter size, load capacitance, input transition time and power supply, which make it suitable for cell library characterization and transistor level logic simulation.

In sec. 2 we describe the nature of degradation effect and a model for its characterization. In sec. 3, some examples are presented showing the importance of degradation effect and the timing range in which it may occurs. In sec. 4, a complete analysis of degradation parameters in terms of design and external parameters is developed. Simulation results validating the model are included in sec. 5, to finish with some conclusions in sec. 6.

## 2. Degradation effect modelling.

Degradation effect takes place when an input transition arise and the gate has not yet fully switched since the previous transition was propagated. A parameter that reflects the state of the gate when a new transition happens can be simply the elapsed time since the last output transition (T, shown in Fig. 1), where a transition means any signal crossing the 50% of the supply rail ($V_{DD}/2$).

At an electrical level, different cases can be considered. In Fig. 2, in thin line, different input transitions are shown, with the corresponding output transitions in thicker line. Three cases can be observed (a, b and c) corresponding to three different values of T: Case a) if T is large enough ($T=T_0$), the output signal has completely switched when a new input transition occurs and so this will propagate with a delay independent on T (i.e. with normal delay) (Fig. 2a). Case b) if T is small enough ($T=T_1$), the output starts

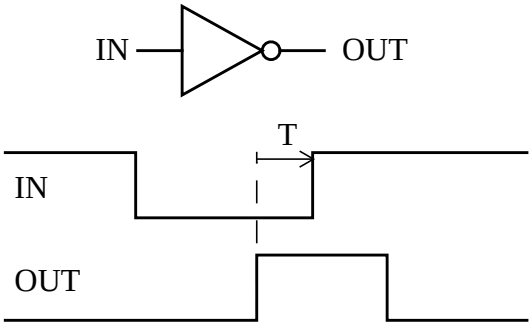


Fig. 1: T parameter

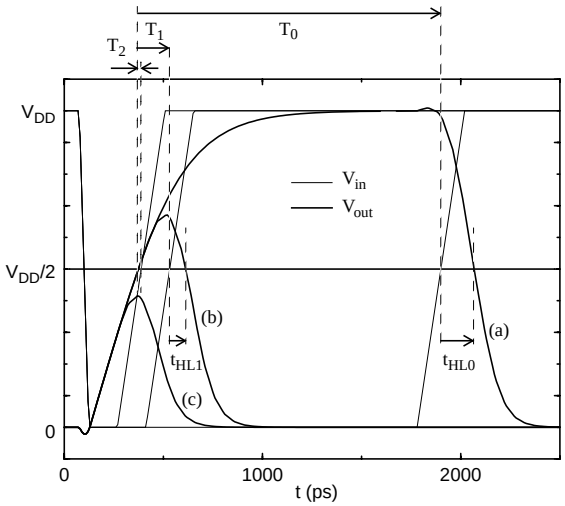


Fig. 2: Different behavior depending on T. a) Normal propagation, b) Degradation effect, c) Filtering

to propagate a transition in the opposite direction when is still switching the previous one (Fig. 2b). This yields a reduced propagation delay compared to the normal one ($t_{HL1}<t_{HL0}$). This is the case of *degradation effect*. Case c) for even smaller values of T ($T=T_2$), it is possible that output comes back to the low level before it crosses the logical threshold (Fig. 2c), hence, in this case, and in a logical sense, neither the current, nor the previous transition take place. This behavior is referred as *pulse filtering*.

This behavior provides a continuous reduction in propagation delay as T decreases, giving curves as the one shown in Fig. 3, with three qualitatively different zones: one corresponding to normal propagation, one with different levels of degradation effect and a pulse filtering zone.

These curves can be fitted to the following exponential expression:

$$t_{HL} = t_{HL0}\left(1 - e^{-\frac{T - T_{HL}}{\tau_{HL}}}\right) \qquad (1)$$

where $t_{HL0}$ is the normal propagation delay and $\tau_{HL}$ and $T_{HL}$ are the parameters describing the degradation effect that will be referred as *degradation parameters*.

The degradation parameters $\tau_{HL}$ and $T_{HL}$ have a clear physical meaning. To understand this meaning let us consider the input pulse causing degradation effect plotted in Fig. 4, and let us assume that an *effective gate's activation threshold voltage* exists ($V_{TL}$) denoting the minimum input voltage needed for a high-to-low output transition to start

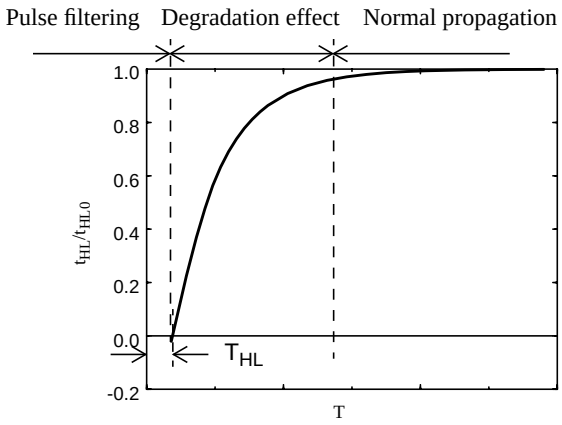


Fig. 3: $t_{HL}$ vs. T curve showing regions with different behavior

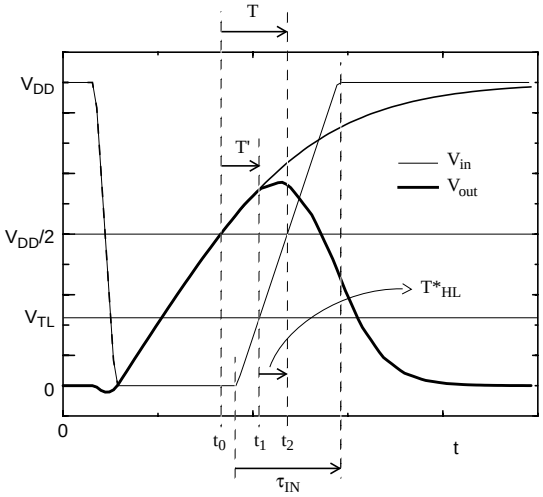


Fig. 4: Electrical behavior causing degradation effect.

swinging. This threshold is related to the NMOS threshold voltage ($V_{TN}$) extracted from the inverter I-V characteristic, but is also affected by the complementary transistor (PMOS) since at the beginning of an output switching, both transistors may drive some current at the same time. In these conditions and after the output transition at instant $t_0$, degradation effect will take place or not depending on T', i.e. the state of the output when the gate is activated. With respect to delay evaluation, we can say that if T' is larger than a given value, say T*, the delay will be essentially equal to the normal propagation delay (e.g. greater than $0.95t_{HL0}$). Additionally, if we can express T' as a function of T:

$$T' = T - T^*_{HL} \tag{2}$$

where $T^*_{HL}$ represents the elapsed time since $V_{in}$ crosses $V_{TL}$ to it crosses $V_{DD}/2$ ($t_2$-$t_1$). Thus we obtain:

$$\begin{aligned} T - T^*_{HL} < T^* &\Rightarrow t_{HL} < 0.95 t_{HL0} \\ T - T^*_{HL} > T^* &\Rightarrow t_{HL} > 0.95 t_{HL0} \end{aligned} \tag{3}$$

On the other hand, from (1) we derive that:

$$\begin{aligned} T - T_{HL} < 3\tau_{HL} &\Rightarrow t_{HL} < 0.95 t_{HL0} \\ T - T_{HL} > 3\tau_{HL} &\Rightarrow t_{HL} > 0.95 t_{HL0} \end{aligned} \tag{4}$$

so the following correspondence between (3) and (4) can be established:

$$\begin{aligned} T_{HL} &\equiv T^*_{HL} \\ 3\tau_{HL} &\equiv T^* \end{aligned} \tag{5}$$

yielding the following definitions for the degradation parameters:

- $\tau_{HL}$: A measure of the time required by the gate's output after a logical transition to achieve a steady state. A gate's activation after a time greater than $3\tau_{HL}$ since the last logical transition will generate a propagation delay that can be considered normal ($t_{HL} > 0.95t_{HL0}$).
- $T_{HL}$: the elapsed time since $V_{in}$ crosses $V_{TL}$ to it crosses $V_{DD}/2$. A simple analysis based on Fig. 4 gives:

$$T_{HL} = \left(\frac{1}{2} - \frac{V_{TL}}{V_{DD}}\right)\tau_{in} \tag{6}$$

where $\tau_{in}$ is the linearized input transition time.

## 3. Evaluating degradation effect importance.

In this section we show how to quantify the input timing producing significant degradation effect (middle zone in Fig. 3). For quantification purposes it is convenient to define the *degradation limit* (DL) as (for a high-low transition):

$$DL_{HL} = T_{HL} + 3\tau_{HL} \tag{7}$$

This is an appropriate limit between degradation and normal propagation regions, as long as

$$T > DL_{HL} \Rightarrow t_{HL} > 0.95t_{HL0} \tag{8}$$

This way, DL is the time to wait after an output transition for a new input transition to propagate with an essentially normal propagation delay. The importance of degradation effect can then be evaluated by the value of DL related to the normal propagation delay. In Table 1 we show fitted degradation parameters as well as the DL to $t_{HL0}$ ratio for two minimum length CMOS inverter examples, under different input slope conditions. In this table, k is the internal configuration ratio ($W_P/W_N$), $C_L$ the output loading capacitance, $C_{IN}$ the inverter's equivalent input capacitance, $T_{HLS}$ the step response delay [4] and $\tau_{in}$ the linearized input transition time. Here, k, $C_{IN}$ and $T_{HLS}$ are used as convenient normalizing parameters.

From these data, an important fact arises: degradation effect is not a marginal effect

Example 1: **k=1**

| $\tau_{IN}/2T_{HLS}$ | $t_{HL0}$ (ps) | $\tau_{HL}$ (ps) | $T_{HL}$ (ps) | DL(ps) | $DL/t_{HL0}$ |
|---|---|---|---|---|---|
| 0.1 | 121 | 189 | -5.86 | 561 | 4.6 |
| 2 | 162 | 139 | 79.4 | 496 | 3.1 |
| 5 | 187 | 140 | 217 | 637 | 3.4 |

Example 2: **k=2**

| $\tau_{IN}/2T_{HLS}$ | $t_{HL0}$ (ps) | $\tau_{HL}$ (ps) | $T_{HL}$ (ps) | DL(ps) | $DL/t_{HL0}$ |
|---|---|---|---|---|---|
| 0.1 | 183 | 137 | -0.16 | 411 | 2.2 |
| 2 | 250 | 117 | 76 | 427 | 1.7 |
| 3 | 278 | 108 | 135 | 459 | 1.7 |

Table 1: DL to $t_{HL0}$ ratio for several inverter configurations. $W_N$=4μm, $C_L$=4$C_{IN}$, $V_{DD}$=5V

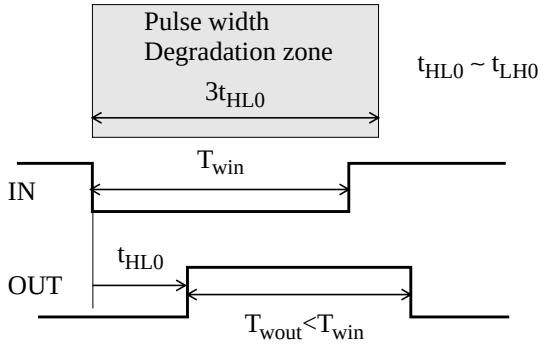


Fig. 5: Pulse narrowing due to degradation effect on its second transition

since an input transition will propagate with a delay sensibly smaller than the normal propagation delay even if the elapsed time since the last output transition is as large as 2-3 times the normal propagation delay.

In order to see this situation from the point of view of a single input pulse entering an inverter, let us assume for the sake of clarity that both $t_{HL0}$ and $t_{LH0}$ are equal and that $DL/t_{HL0}$ is equal to 2. In this case, Fig. 5 shows how the second transition of an input pulse of width $T_{win} < 3t_{HL0}$ will suffer degradation effect and a corresponding width shortening: $T_{wout} < T_{win}$. This behavior is in clear disagreement with the classical approach in which the only condition for a pulse to propagate with normal delay was $T_{win} > t_{HL0}$ while pulses with $T_{win} < t_{HL0}$ were eliminated from the output (filtered), yielding to an erroneous discontinuous behavior of the propagation delay. In fact there is a continuous variation as expressed in (1) and plotted in Fig. 3 that extends along a timing region of significant width.

## 4. Design oriented characterization of degradation parameters.

From now on, we will consider minimum length transistors.

Regarding equation (1), the parameters to be characterized are the normal propagation delay ($t_{HL0}$) and the degradation parameters ($\tau_{HL}$ and $T_{HL}$). $t_{HL0}$ characterization has been a main issue in delay modelling for years and the case of the inverter has been widely studied in the bibliography [3, 4, 5, 8]. In particular, the model proposed by

Daga et. al. includes complete dependence with design parameters for a wide range of values in a submicronic technology, achieving a high accuracy degree. Thus, the present paper will concentrate in the characterization of $\tau_{HL}$ and $T_{HL}$. Once it is done, the term:

$$\left(1 - e^{-\frac{T - T_{HL}}{\tau_{HL}}}\right) \tag{9}$$

might be applied to any previously developed model for $t_{HL0}$ in order to achieve degradation effect correction (1).

Basing on the definitions for $\tau_{HL}$ given in sec. 2, we propose the following expression for $\tau_{HL}$:

$$\tau_{HL} V_{DD} = A_f + B_f \frac{C_L}{W_P} \tag{10}$$

where $A_f$ and $B_f$ are fitting constants characteristic for a given technology. It has been assumed that the product $\tau_{HL} V_{DD}$ does not depend on changes in supply voltage. This hypothesis will be validated in sec. 5.

Regarding $T_{HL}$, we have seen in sec. 2 that it can be modelled as:

$$T_{HL} = \left(\frac{1}{2} - v_{TL}\right)\tau_{in} \tag{11}$$

where $v_{TL}$ is the *reduced effective gate's activation threshold voltage* defined as $v_{TL} = V_{TL}/V_{DD}$, which is closely related to the active transistor threshold voltage (NMOS in this case) as we will see in next section.

## 5. Simulation results.

Validation of the proposed model has been done through HSPICE [9] level 6 simulations for a 0.7μm CMOS process. As mentioned above, all MOSFETs are of minimum length. Several simulations have been performed for typical value ranges of $C_L$, $\tau_{in}$, $V_{DD}$, $W_N$ and $W_P$ .

Curves like the one on Fig. 6 can be obtained measuring the propagation delay (e.g. $t_{HL}$) for different values of T. On the other hand, a simple transformation of (1) gives:

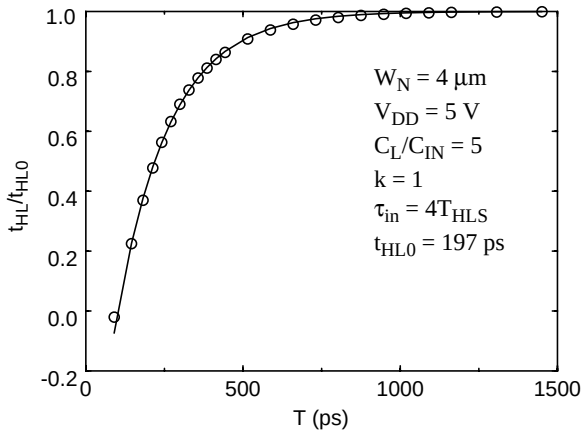


Fig. 6: $t_{HL}$ vs. T simulation data for a sample inverter

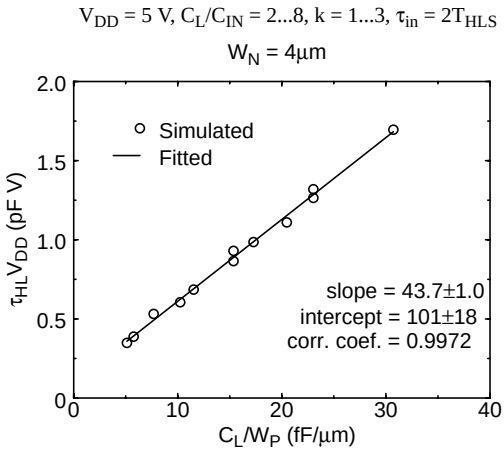


Fig. 7: $\tau_{HL}V_{DD}$ vs. $C_L/W_P$ curve.

$$T = T_{HL} + \tau_{HL}\left[-\ln\left(1 - \frac{t_{HL}}{t_{HL0}}\right)\right] \tag{12}$$

which allow us to obtain $T_{HL}$ and $\tau_{HL}$ by linear regression. The corresponding fitting is the solid line in Fig. 6. All the studied cases give similar good fittings which validates the proposed equation. This process is done repeatedly for different design and external parameter values to check the validity of (10) and (11).

## $\tau_{HL}$ characterization.

In Fig. 7 we plot $\tau_{HL}V_{DD}$ vs. the ratio $C_L/W_P$ for $W_N$=4μm, $V_{DD}$=5V and $\tau_{in}$=2$T_{HLS}$. Wide ranges of load capacitances and inverter configuration ratios are involved. The linearity obtained in Fig. 7 validates (10) and allow us to calculate the technology characteristic parameters $A_f$ and $B_f$ for the ES2 CMOS 0.7μm process:

$$A_f = (96.5 \pm 17)\ \text{ps} \times \text{V} \qquad B_f = (43.2 \pm 1.0)\ \frac{\text{ps} \times \text{V} \times \mu\,\text{m}}{\text{fF}} \tag{13}$$

$$\text{corr. coef.} = 0.9973$$

Similar results has been obtained for $W_N$=8μm, $V_{DD}$=3V and $\tau_{in}$ up to 10$T_{HLS}$ with maximum discrepancies of 5% for $B_f$ and 2% for $A_f$. Thus the product $\tau_{HL}V_{DD}$ can be considered independent of the mentioned parameters in the range of interest, in agreement with (10).

| k | $/2 - v_{TL}$ | $v_{TL}$ | $v_{TL}/v_{TN}$ |
|---|---|---|---|
| 1 | 0.239 | 0.261 | 1.05 |
| 2 | 0.160 | 0.339 | 1.35 |
| 3 | 0.130 | 0.370 | 1.48 |

Table 2: Dependence of $v_{TL}$ on *k* for $V_{DD}$=5V and $W_N$=4μm. $V_{TN}$=1.25V for the current technology [4].

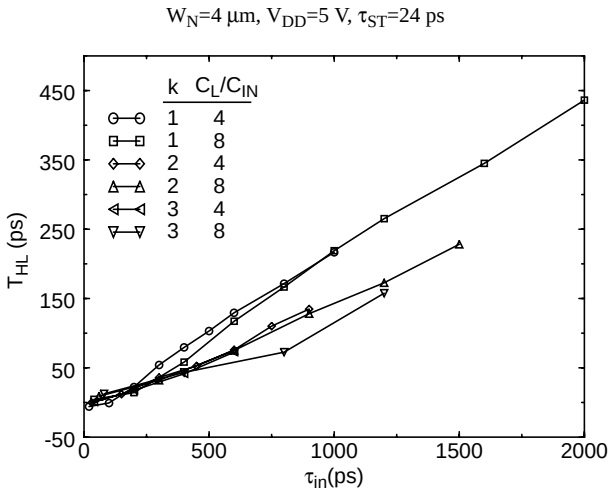


Fig. 8: $T_{HL}$ vs. $\tau_{in}$ curves for different output loads and configuration ratios.

## $T_{HL}$ characterization

Eq. (11) gives the model for the second degradation parameter, $T_{HL}$. This equation predicts a linear dependence of $T_{HL}$ on $\tau_{in}$, which is obtained in Fig. 8 for different inverter configurations and load capacitances. The different curves maintain the same slopes even if we duplicate the output load. However, a significant variation in the slope is observed as the value of k increases. This, in turn, means a variation of $v_{TL}$. This variations are summarized in Table 2, as well as the corresponding values for $v_{TL}$ and the $v_{TL}$ to $v_{TN}$ ratio, being $v_{TN}$ the reduced threshold of the driving transistor ($V_{TN}/V_{DD}$). It can be observed how $v_{TL}$ increases as the driving capability of the PMOS with respect to the NMOS (represented by k) increases, which is due to the fact that for a stronger PMOS, a higher conduction level is needed in the NMOS to makes the output to start switching. This agrees with the fact that for a relatively weak PMOS (k=1) the effective activation threshold tends to the threshold voltage of the NMOS ($v_{TL} \cong v_{TN}$) as shown in Table 2. Further work should be devoted to analyze $v_{TL}$ dependence on k. At this moment two compromise solutions are proposed as long as only a few values of k are typically considered: the first one is to choose a constant trade-off value for $v_{TL}$ in the range of interest. For example, if $k \in [1, 2]$, a compromise value would be $v_{TL\text{comp}}/v_{TN} = 1.2$, which deviation is below 15% in the given range. The second and

more precise approach consists of using a linear interpolation formula for $v_{TL}$ as a function of k in the range of interest. In this case, the maximum deviation is below 6% for data in Table 2 and $k \in [1, 3]$ .

## 6. Conclusions

This communication has presented the evidence of a degradation effect in the delay of a CMOS inverter when consecutive input transition are close in time. Complete understanding of the effect has been offered, providing a model to quantify the effect. The model takes the form of a simple correcting factor which make it suitable to be applied to any previously developed inverter delay model.

The timing regions in which the effect become important are easily derived from the model, showing how input transition forming pulses of width in the order of a few times the propagation delay are likely to suffer the effect, in clear contradiction with classical assumptions.

The primary degradation parameters ($\tau_{HL}$ and $T_{HL}$) have been fully characterized as functions of design variables and external conditions, making the model suitable for using in library characterization as well as simulation at a transistor level.

Validation has been performed through HSPICE simulations, showing satisfactory accuracy for timing evaluation.

## 7. References


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